UNITED STATES DISTRICT COURT
FOR THE EASTERN DISTRICT OF TEXAS
MARSHALL DIVISION

NETLIST, INC., Plaintiff, vs. MICRON TECHNOLOGY, INC., MICRON SEMICONDUCTOR PRODUCTS INC., MICRON TECHNOLOGY TEXAS LLC, Defendants.	Case No. 2:22-CV-203-JRG-RSP JURY TRIAL DEMANDED [redacted]

PLAINTIFF NETLIST, INC.'S REPLY CLAIM CONSTRUCTION BRIEF

TABLE OF CONTENTS

Page

TABLE OF AUTHORITIES

Page(s)

Cases

I. U.S. Patent Nos. 8,787,060 and 9,318,160

A. "electrical communication" ('060, cls. 1, 11, 20, 29; '160 patent, cl. 1)

Micron concedes that "electrical connection" and "electrical communication" are two different concepts, as Netlist has explained. Dkt. 109 at 2; Dkt. 97 at 1-3. Its expert, Dr. Stone, however, testified to precisely the opposite, asserting that, in his view "electrical communication" means "electrical connection." Ex. 24 (Stone Tr.) at 95:10-13 ("What does the word 'electrical communication' mean to you? A. Electrical connection. That's -- I got that from the patent. I can show you where he says that."). Dr. Stone further explains that electrical connection leads to electrical communication because it allows signal or electrical wave transmission between the TSV and the array die(s). *Id.* at 91:16-19, 93:20-94:15, 96:19-97:8. Thus, it appears that Micron is at least trying to preserve the right to argue at trial that its HBM products do not satisfy the "not in electrical communication" limitation because there is "electrical connection" between the die interconnects and all of the array dies in the accused products to allow passing of electrical waves from the TSV into a portion of the die, just as Samsung did in *Samsung I*. *See* Dkt. 97-24 at 1056:24-1057:17; Ex. 25 (DDX4-54).

Under such a view, a TSV would be in communication with an array die if it is connected to a stub on the array die. Ex. 24 (Stone Tr.) at 95:6-8 ("Is it your testimony that the connection between a TSV and a stub is electrical communication? A. Yeah This demonstrates it, because the wave travels on that."). The patent teaches, however, that in cases where "electrical connections leading from the TSV of the array dies that are not configured to be in electrical communication with the die interconnect … may be stubs" that "are not configured to provide electrical communication with the memory cells of the array dies." '060 patent, 8:53-62. Thus, the Court should reject Micron's attempt to equate "electrical communication" with "electrical connection," and adopt Netlist's proposed construction that distinguishes the two different concepts rather than creating confusion. As to whether certain configurations, such as that shown on Samsung's DDX4-54 (Ex. 25), result in

electrical communication, that is a question of fact for the jury to decide.

Micron also misreads the prosecution history. Netlist deleted a "data port" limitation from part of '060 claim 1, but otherwise retained the language requiring "each array die having data ports." Dkt. 109-3 at 10. Micron mistakenly suggests that Netlist disavowed a "data port" requirement by this amendment, citing *Blackbird* in support. Dkt. 109 at 3. In *Blackbird*, the amendment was made, by the applicant's own admission, "to resolve 112 issues." *Blackbird Tech LLC v. ELB Elecs., Inc.*, 895 F. 3d 1374, 1378 (Fed. Cir. 2018) ("Any skilled artisan would understand that if an examiner requires an amendment for § 112 reasons it is an amendment required for patentability."). Here, Micron does not allege that the amendment at issue was required for patentability. Dkt. 109 at 3 (pointing to vague statements that the claim was "amended to better define the inventions"). Nor can it: the only Office Action that issued prior to the amendment concerned an unrelated restriction requirement. Dkt. 109-3 at 5. For Micron to say that data ports are not involved in electrical communication is inconsistent with the claims and the specification. The claims that were amended expressly recite the presence of data ports. The specification teaches that data ports are what is used for electrical communication. '060 patent, 5:41-45. Netlist is not asking for a construction that expressly requires data ports. Whether electrical communication is possible without a data port is a question of fact.

Micron's responsive brief attempts to add another negative limitation—not requiring "responsiveness"—to "electrical communication." Dkt. 109 at 1-2. It is unclear what Micron has in mind, but in *Samsung I*, Netlist treated a die interconnect as being in electrical communication with an array die even when the array die's data port connected to the die interconnect is disabled. There is electrical communication in that case, because signals are still received by the input stage of the receiver, even though the signals are not further transferred to the memory array.

B. Claim 7 of the '060 Patent Is Not Indefinite

Micron insists the term "array die[s] are selected in consideration of a load … so as to reduce

a difference" requires a user to perform a method step. That interpretation has no basis in the intrinsic evidence. The claim language makes no reference to user input. '060 patent, 24:37-47. This is contrast to the claim in *Barkan Wireless IP Holdings, L.P. v. Samsung ElecElectronics Co., Ltd.*, which expressly made reference to an action taken by an "individual or entity." 2019 WL 497902, at *33 (E.D. Tex. Feb. 7, 2019) ("6. The add-on base station of claim 1, wherein the add-on base station expands coverage of a cellular network and ***is owned and installed by an individual or entity*** ....") (emphasis added).

Nor do any of Micron's specification citations provide that a user "selects" the number of array dies in the first/second groups of the claimed memory package. *See* '060 patent, 19:13-14 (referencing unrelated RDIMM embodiment), 18:67-19:1 (referring to "a programmable secondary 1-to-2 rank decoder" of 3DS-DIMM), 22:28 (referring to operational modes of unrelated RDIMM embodiment), 18:67-19:1; 23:33-45 (generic disclosure that "one or more embodiments necessarily include logic for deciding, with or without author input or prompting").

C. "the second driver size being different from the first driver size" ('160 cl. 1)

Micron does not dispute that the plain language of '160 claim 1 does not specify that the difference in "driver size" need be along "physical dimensions." Dr. Stone's testimony illustrates why Micron's proposed construction should be rejected: it could lead to an indefiniteness argument down the road. Dr. Stone testified that the size of a driver with 10 transistors is the space needed to accommodate the 10 transistors if all 10 transistors would be used some of the times, but the same driver would have a size corresponding to two transistors if only two of the ten transistors would ever be required in use. Ex. 24 (Stone Tr.) at 147:8-148:20, 149:9-15. That is, Micron's construction could result in the infringement of an apparatus claim turning impermissibly on usage, rather than the configuration of the accused products. Nor does Micron dispute that its citations to the specification are to non-limiting embodiments.

II. U.S. Patent No. 10,860,506

A. "one or more previous operations" ('506, cls. 1-3, 11, 15, 16)

The Board's final written decision in IPR2022-00236 makes clear that Netlist's argument was directed to whether the write leveling disclosed in the prior art is the same as a memory write operation as understood at the time of the invention. *See* Dkt. 109-7 (FWD) at 29 ("Patent Owner also emphasizes that the terms 'write leveling' and 'write operation' are not synonymous and that the write leveling procedure taught in Tokuhiro is not a write operation."); *see also id.* at 28-33, 43-45. Netlist's statements thus do not amount to disclaiming write leveling operations (let alone all types of leveling operations) from all types memory operations. The Board did not agree with Netlist that write leveling is not a memory operation (*id.* at 33), but rather, found that Micron had failed to show that write leveling is a memory write operation as defined by JEDEC at the time of the invention (*id.* at 43-45).

Micron is also wrong that Netlist broadly disclaimed "leveling operations." Micron cites to statements Netlist made in its sur-reply in IPR2022-00236 regarding "MRS commands," but omits citations to Netlist's response that make clear that Netlist was referring specifically to the **DDR3** standard, JESD 79-3. *Compare* Dkt. 109-5 (Netlist's sur-reply) at 4 ("Netlist expressly argued in its Response that the write leveling procedure that follows any MRS command does not include any 'memory operation' and is not a 'memory operation' in its own right. Resp., 20-29.") *with* Dkt. 97-13 (Netlist's Response) at 22-23 ("For example, ***JESD79-3A*** states that …. During write leveling mode, only NOP or DESELECT commands are allowed, **as well as an MRS command to exit write leveling mode**."'). Netlist's counsel's statements during oral argument were likewise referring to DDR3 write leveling. *See* Ex. 26 (PTAB Hearing Tr.) at 41:15-17 ("If you look at Slide 57, Petitioners don't dispute a number of things. They don't dispute that Tokuhiro discloses only known write leveling procedures outlined in ***JESD 79C***."). Micron's attorney argument in its responsive brief that the disclosures of Tokuhiro and Osanai are not so limited should be disregarded. Micron's brief does not dispute that its own expert in IPR2022-00236 only relied on DDR3 write leveling. Dkt. 109 at 8.

B. "determining" ('506, cl. 14)

Micron contends that the Court should revisit its prior construction of the "determining" step from *Samsung I* because of arguments Netlist made in the '506 IPR. Dkt. 109 at 9. The use of the term "reflected" in association with claim 14 refers to the fact that the portion of the limitation in dispute (strobe delay feature) was included in both claims 1 and 14, and that dispute did not concern whether the steps took place in a previous operation or another step. The IPR argument results from the fact that Samsung offered no separate analysis for claim 14 from claim 1. *See* Dkt. 109-12 (IPR2022-00711, Patent Owner Response) at 32. Indeed, Netlist explained that "[t]he ***Petitioner*** does not advance different arguments for the strobe delay feature of independent claim 14 (see Petition, 64), or suggest there are any material differences between claims 1 and 14." *Id.* at 32, n. 5.

III. U.S. Patent No. 10,949,339

A. The "drive" terms ('339, cls. 1, 11, 19, 27)

Netlist is not seeking to re-litigate the "fork-in-the-road" versus "straight-line" dispute. To the contrary, it is Micron's construction that injects those words into this case. Dkt. 109 at 10.

Micron admits that its true motivation is to exclude interpretations where (1) the "other possible paths" in the Court's prior construction are paths for read data, and (2) the "byte-wise" data paths may be a half-byte (i.e. four bits or a nibble) wide. Dkt. 109 at 12. The intrinsic record contemplates that one of the paths will be a read path. *See, e.g.*, Dkt. 97-8 at 9-10 (prosecution history indicated the claim is about "controlling the data paths between the memory devices and the bus interface so that the data paths are open for a time period to allow data to be driven between the memory devices and the memory controller" without reference to specific read or write path). Likewise, the intrinsic record contemplates that the "byte-wise" data path through the buffer may comprise half-byte (i.e., nibble or four bit) data paths that may be enabled or disabled independently. *See* '339 patent, 13:54-63 (in preferred embodiments Figs. 3B and 4B, a byte-wise section of the N-bit

wide data is transferred over two 4-bit paths), 14:1-14 (data transmission circuit 416 of FIG. 4B "selectively transmits ***data bits 0-3*** to a first memory device … and ***data bits 4-7*** to a second memory device"), 14:15-17 (Fig. 4B shows example of "byte-wise" buffer), 14:15-34 (teaching that, in certain embodiments, "not all the [data] bits are grouped together and not all the bits produce the same behavior (e.g., logic- and/or time-wise)").

Micron's suggestion that Netlist is "regurgitating" previously rejected arguments regarding preferred embodiment depicted in Figs. 3B and 4B is unfounded. Dkt. 109 at 13. Netlist is citing these embodiments as evidence that Micron's ***new*** construction—adding the phrase "byte-wise section of the N-bit wide write data"—would exclude embodiments where a byte-wise section of the N-bit wide data is transferred over two 4-bit (i.e. half-byte or nibble) paths, which the Court's Order did not previously consider. Dkt. 97 at 11. It seems that what Micron ultimately desires is to slip in a construction of "byte-wise." But if it wants a construction of "byte-wise" it should have announced this in the claim construction process so that there could be a full and fair engagement of the issue.

IV. U.S. Patent Nos. 11,016,918 and 11,232,054

A. "pre-regulated input voltage" / "input voltage" ('918, cls. 16-22, 30)

Micron argues that because the claims separately recite "a pre-regulated input voltage" and "an input voltage," the same structure cannot satisfy both terms. As the Court recognized in *Samsung I*, the term "pre-regulated input voltage" simply "gives context to what the buck converters do—that is, receive an input voltage and produce an output voltage." Dkt. 97-8 at 22; '918 patent, 39:60-64, 42:21-26. At the pre-trial conference in *Samsung I*, the Court struck portions of Samsung's expert report that argued "pre-regulated input voltage" and "input voltage" were distinct voltages, finding these sections inconstant with the Court's order. Netlist moved to strike this exact argument, which appeared in Paragraph 366 and 367 of the report. *See Netlist Inc. v. Samsung Elecs. Co., Ltd.,* Case No. 21-cv-463, Dkt. 208 at 3 ("Paragraphs 366-372 of Mr. McAlexander's report cite to the same, non-

limiting portions of the specification as Samsung did in its claim construction briefing to support its argument that "pre-regulated input voltage" should be limited to the embodiments in the specification. *Compare* Ex. 1, ¶¶ 366-372 with Dkt. 84 at 11. The Court rejected that argument (Dkt. 114 at 22), and thus Mr. McAlexander's opinions to the contrary should be stricken."). The Court struck the paragraphs as inconsistent with the Order. Ex. 27, at 81:20-82:9; Ex. 30 (McAlexander Rebuttal Rpt.).

The claim language requires an "input voltage" that is "pre-regulated" to be the input to the conversion circuits, and also describes that the "input voltage" is received from "a first portion of the plurality of edge connections." '918 patent, 39:60-62, 40:7-13. These are two different features of what may be the same voltage. Micron is incorrect that there is no support for a design in which the "pre-regulated input voltage" and "input voltage" can be satisfied by the same structure. Micron does not dispute that the specification teaches that power element 1140 in Fig. 16, which can operate as a source of the "pre-regulated input voltage," is an example of power supply 1080 in Fig. 12. Dkt. 97 at 16-17. Nor does Micron dispute that in the embodiment where power supply 1080 is "tethered" to the module (26:30-35) the "pre-regulated input voltage" is supplied from off of the memory module. *Id.* In this embodiment, the "pre-regulated input voltage" supplied to the converters can be the same as the "input voltage" received from the edge connections, contrary to Micron's assertion.

B. "converter circuit" ('918 patent, all asserted claims)

Micron does not dispute that dictionary definitions of "circuit" connote structure. Micron's expert relies on a nearly identical definition. Ex. 24 (Stone Tr.) at 23:9-17 ("circuit" means "a collection of electrical components connected together in some fashion"). The structure of a circuit is electrical components connected together. Because it is structural, the term is not a nonce word. Micron seeks means-plus-function treatment of this term in order to exclude an LDO from the scope of the claim. But its own expert describes "LDO" circuits as an "LDO converter." *Id.* at 19:19-25, 20:3-18. The fact that he is able to describe an LDO converter as a type of circuit shows that it is not a nonce word.

Micron argues that the Court should ignore Federal Circuit precedent finding "circuit"/"circuitry" are not nonce terms because these cases pre-date *Williamson*. Dkt. 109 at 19. But *Williamson* simply abrogated prior case law that the absence of the word "means" gives rise to a "***strong***" presumption against § 112 treatment. *Williamson v. Citrix Online, LLC*, 792 F.3d 1339, 1349 (Fed. Cir. 2015) (*en banc*). These cases are still good law. *See Dyfan, LLC v. Target Corp.*, 28 F.4th 1360 (Fed. Cir. 2022) (discussing *Apex Inc. v. Raritan Comput., Inc.*, 325 F.3d 1364, 1373 (Fed. Cir. 2003) with approval). Micron also ignores that several of these cases do not mention, let alone rely on, the "strong" presumption against means-plus-function treatment in the absence of the word "means." *See MIT v. Abacus Software*, 462 F.3d 1344, 1355 (Fed. Cir. 2006), *Linear Tech. Corp. v. Impala Linear Corp.*, 379 F.3d 1311, 1320-21 (Fed. Cir. 2004). The term "circuit"/"circuitry" is thus not a "nonce" word, in contrast to the "generic, black-box" nonce term "mechanical control assembly" at issue in *MTD Prods. v. Iancu*, 933 F.3d 1336, 1343 (Fed. Cir. 2019).

The specification makes clear that "converter circuit" is a structural limitation. '918 patent, 29:23-27 ("The sub-blocks may comprise various converter circuits such as buck-converters, boost converters, and buck-boost converter circuits"). Micron's citation to trial testimony from *Samsung I* is unavailing. At trial, Dr. Mangione-Smith mapped the claimed "converter circuit" to an LDO. His explanation that "any circuit that converts a voltage is a converter circuit" is not an admission that the term "converter circuit" lacks sufficiently definite structure, because, as explained above, a POSITA would understand that the term "circuit" on its own connotes structure. *See also* Dkt. 97-19 (defining "circuit" as an "[a]rrangement of conductors and passive and active components forming a path, or paths, for electrical current"); Dkts. 97-20, 97-21 (similar definitions connoting structure). Ex. 28 at 4 ("An electric circuit is an interconnection of electrical elements.").

C. "at least one circuit" ('918, cls. 1-3, 5-7, 9-13, 15, 21)

As explained in Section IV.C., the term "circuit" is not a nonce term. The claim language

specifies the inputs/outputs (a first/second plurality of c/a signals) of the "at least one circuit," and that it is "coupled between a first portion of the plurality of edge connections [of the memory module] and the plurality of SDRAM devices" with further requirements specifying coupling to specific voltages. '918 patent, 38:41-43, 38:47-49. Micron argues that under *MTD Products*, the use of functional language such as "operable to" weighs in favor of application of § 112, ¶ 6 regardless of the structural nature of the "coupled to" limitations. Dkt. 109 at 22. But at the outset, the *MTD Products* Court determined that the term "mechanical control assembly" was itself a nonce term. 933 F.3d at 1341-42. The Federal Circuit has consistently found the term "circuit" is not a nonce word. *See supra* IV.C.

If § 112, ¶ 6 applies, Micron's "compromise corresponding structure" should be rejected as unduly narrow because it omits the "registers" of the RDIMM embodiments depicted in Figs. 15A-C, which are depicted as receiving a plurality of c/a signals from the computer system and outputting a plurality of c/a signals to the SDRAMs. *See, e.g.*, '918 patent, Fig. 15A, 23:41-44. Micron's expert Dr. Stone admitted that the register of a DDR RDIMM—which receives and outputs c/a signals in a similar manner—is a "circuit." Ex. 24 (Stone Tr.) at 28:8-15.

D. "controller" ('918, cls. 12, 18-19, 25-26; '054, cls. 5, 7-13, 16-17, 23-25, 29-30)

The claim language demonstrates that the "controller" limitation recites sufficiently definite structure. For example, claim 12 of the '918 patent provides that "in response to the trigger signal, the controller performs a write operation to the non-volatile memory." '918, 39:31-36. The controller is thus circuitry that can perform a write operation to the non-volatile memory. According to Dr. Stone, "the controller needs to be connected directly or indirectly to the non-volatile memory in order to perform the write operation in the non-volatile memory." Ex. 24 (Stone Tr.), 83:22-84:8. Dr. Stone also agreed that a POSITA would understand that a "controller" designed for memory modules would need to be connected to the devices it is controlling. *Id.*, 39:13-18 ("In the context of controllers that are designed for memory modules, the controller which is controlling components on the memory

module would have to be connected to those components; fair? A. I believe that's – that's fair, yes. I would say that's fair."). Nothing in the specification suggests that the claimed "controller" lacks structure. '918 patent, 23:1-27, 21:46-47 (controller may be a "logic element," such as an FPGA, PLD, ASIC, custom-designed semiconductor device, CPLD); *id.* 29:43-44. Additionally, Dr. Stone admits that such controllers are "circuits." Dkt. 97-9 (Stone Decl.) ¶ 25 (POSITA would have been familiar with "***circuits*** such as ASICs, FPGAs, and CPLDs"). The term "controller" is not a nonce term because the term "circuit" denotes structure. *See supra* IV.B. The term "controller" in the context of the claims provides additional structure: not only is a circuit with control functionality required, but in the claim that circuit, to perform its control functionality, must be connected to certain other elements. *See* Ex. 24 (Stone Tr.), 39:13-18; *see also* Ex. 29 at 1 ("A controller is a comparative device that receives an input signal from a measured process variable, compares this value with that of a predetermined control point value (set point), and determines the appropriate amount of output signal required by the final control element to provide corrective action within a control loop.")

E. "[first/second] operable state" ('054 patent, cls. 4-7, 11-12, 16-17, 23, and 25)

The sole dispute is whether the "operable state" terms should be limited to what Micron says is the sole embodiment in the '054 patent that describes the "[first/second] operable state." *Id.* at 28-29. Micron's argument finds no support in the claim language, which simply refers to the state of the memory module. 38:62-64, 39:12-14, 39:46-47, 42:5-6. Micron also ignores that the specification refers to the "first state" as the state of the module when no trigger condition is present, *e.g.*, the state "after power is restored" following a trigger condition. '054 patent, 27:4-5, 25:58-60. The "second state" is also referred to in relation to a trigger condition such as detecting a voltage abnormality in the input voltage. *See id.* 24:23-34, 25:3-7, 25:54-62, 26:38-43.

Dated: June 30, 2023

Respectfully submitted,

/s/ Jason Sheasby

Samuel F. Baxter
Texas State Bar No. 01938000
sbaxter@mckoolsmith.com
Jennifer L. Truelove
Texas State Bar No. 24012906
jtruelove@mckoolsmith.com
MCKOOL SMITH, P.C.
104 East Houston Street Suite 300
Marshall, TX 75670
Telephone: (903) 923-9000
Facsimile: (903) 923-9099

Jason G. Sheasby (*pro hac vice*)
jsheasby@irell.com
Annita Zhong, PhD (*pro hac vice*)
hzhong@irell.com
Andrew Strabone (*pro hac vice*)
astrabone@irell.com
Thomas C. Werner (*pro hac vice*)
twerner@irell.com
Yanan Zhao (*pro hac vice*)
yzhao@irell.com
Michael W. Tezyan (*pro hac vice*)
mtezyan@irell.com

IRELL & MANELLA LLP
1800 Avenue of the Stars, Suite 900
Los Angeles, CA 90067
Tel. (310) 277-1010
Fax (310) 203-7199
Attorneys for Plaintiff Netlist, Inc.

CERTIFICATE OF SERVICE

I hereby certify that, on June 30, 2023, a copy of the foregoing was served to all counsel of record.

/s/ Michael Tezyan
Michael Tezyan

CERTIFICATE OF AUTHORIZATION TO FILE UNDER SEAL

I hereby certify that the foregoing document and exhibits attached hereto are authorized to be filed under seal pursuant to the Protective Order entered in this Case.

/s/Michael Tezyan
Michael Tezyan