Exhibit A

Exhibit A1: Proposed Constructions for the ’060 and ’160 Patents

Exhibit A2: Proposed Constructions for the ’506 Patent

Exhibit A3: Proposed Constructions for the ’339 Patent

Exhibit A4: Proposed Constructions for the ’918 and ’054 Patents

Exhibit A1: Proposed Constructions for the '060 and '160 Patents

Term (Patent/Claim)	Netlist's Proposed Construction	Micron's Proposed Construction	Court's Construction
"die interconnect[s] in **electrical communication** with the . . . group of array dies and **not in electrical communication** with the . . . group of at least one array die" '060: claims. 1, 11, 20, 29; '160: claim 1	Plain and ordinary meaning, that is, "electrical communication" is different from "electrical connection"	Plain and ordinary meaning, *i.e.*, does not require importing a "data port" or "responsiveness" limitation into the claim to require electrical communications (or lack of electrical communications) between the die interconnect(s) and the data ports of the array die(s)	
"**the second driver size being different from the first driver size**" '160: claim 1	Plain and ordinary meaning, that is, the size of the second driver being different from the size of the first driver	"the physical dimensions of the second driver being different from the physical dimensions of the first driver"	
"**The memory package of claim 1, wherein a first number of array dies in the first group of array dies and a second number of at least one array die in the second group of at least one array die are selected in consideration of a load of the first die interconnect and a load of the second die**	Not indefinite	Indefinite	

Term (Patent/Claim)	Netlist's Proposed Construction	Micron's Proposed Construction	Court's Construction
interconnect so as to reduce a difference between a first load on the first data conduit and a second load on the second data conduit, the first load including a load of the first die interconnect, and a load of the first group of array dies, and the second load including a load of the second die interconnect and a load of the second group of at least one array die." '060: claim 7			
"**array die**" '060 and '160: all asserted claims	[Agreed]	[Agreed]	"array die that is different from a DRAM circuit"
"**chip select conduits**" / "**chip select conduits"** '060: claims 6, 11-14, 16-19, 20-21, 23-28	[Agreed]	[Agreed]	Plain and ordinary meaning
"**A memory package**" '060 and '160: all asserted claims	[Agreed]	[Agreed]	The preamble is limiting

Exhibit A2: Proposed Constructions for the '506 Patent

Term (Patent/Claim)	Netlist's Proposed Construction	Micron's Proposed Construction	Court's Construction
"**one or more previous operations**" '506: claims 1-3, 11, 15, 16	one or more previous memory operations	"one or more previous memory operations" where "memory operations" are different from leveling operations	
"before receiving the input C/A signals corresponding to the memory read operation, **determining the first predetermined amount based at least on signals received by the first data buffer**" '506: claim 14	The step of "determining the first predetermined amount based as least on signals received by the first data buffer" occurs before the earlier recited step of "receiving . . . input C/A signals"	"during one or more previous memory operations, determining the first predetermined amount based at least on signals received by the first data buffer" where "memory operations" are different from leveling operations	
"**A memory module operable in a computer system to communicate with a memory controller of the computer system via a memory bus including control and address (C/A) signal lines and a data bus, the memory module comprising**" '506: claim 1	[Agreed]	[Agreed]	The preamble is limiting

Exhibit A3: Proposed Constructions for the '339 Patent

Term (Patent/Claim)	Netlist's Proposed Construction	Micron's Proposed Construction	Court's Construction
"**to actively drive a respective byte-wise section of the N-bit wide write data**" '339: claim 1[1]	to "drive" means "enabling only one of the data paths while the other possible paths are disabled" (i.e., no further construction necessary)	Adopts and applies the Court's adoption of the "fork-in-the- road" configuration and rejection of the "straight-line" configuration to construe "drive" to mean "enabling only one of the data paths while the other possible paths are disabled," *i.e.*, "to enable only one of the data paths for the respective byte-wise section of the N-bit wide write data while the other possible data paths for the same respective byte-wise section of the N-bit wide write data are disabled"	
"**to actively drive a respective section of the N-bit wide write data**" '339: claim 11	to "drive" means "enabling only one of the data paths while the other possible paths are disabled" (i.e., no further construction necessary)	Adopts and applies the Court's adoption of the "fork-in-the- road" configuration and rejection of the "straight-line" configuration to construe "drive" to mean "enabling only one of the data paths while the other possible paths are disabled," *i.e.*, "to enable only one of the data paths for the respective section of the N-bit wide write data while the other possible data paths for the same respective	

[1] The parties' proposed constructions for the "drive" terms in '339 claims 11, 19 and 27 mirror the proposed constructions for '339 claim 1. *See* Dkt. 69-1 at 16-20 (Netlist's proposed constructions), Dkt. 69-2 at 6-22 (Micron's proposed constructions).

Term (Patent/Claim)	Netlist's Proposed Construction	Micron's Proposed Construction	Court's Construction
		section of the N-bit wide write data are disabled"	
"**actively drive a respective section of the [first/second] N-bit wide data**" '339: claim 19	to "drive" means "enabling only one of the data paths while the other possible paths are disabled" (i.e., no further construction necessary)	Adopts and applies the Court's adoption of the "fork-in-the-road" configuration and rejection of the "straight-line" configuration to construe "drive" to mean "enabling only one of the data paths while the other possible paths are disabled," *i.e.*, "enable only one of the data paths for a respective section of the [first/second] N-bit wide data while the other possible data paths for the same respective section of the [first/second] N-bit wide data are disabled"	
"**drive the respective n-bit section of the write data**" '339: claim 27	to "drive" means "enabling only one of the data paths while the other possible paths are disabled" (i.e., no further construction necessary)	Adopts and applies the Court's adoption of the "fork-in-the-road" configuration and rejection of the "straight-line" configuration to construe "drive" to mean "enabling only one of the data paths while the other possible paths are disabled," *i.e.*, "enable only one of the data paths for a respective n-bit section of the write data while the other possible data paths for the same respective n-bit section of the write data are disabled"	
"**drive the respective n-bit section of the read data**"	to "drive" means "enabling only one of the data paths while the other possible paths are	Adopts and applies the Court's adoption of the "fork-in-the-road" configuration and rejection of the "straight-line" configuration to construe "drive" to	

Term (Patent/Claim)	Netlist's Proposed Construction	Micron's Proposed Construction	Court's Construction
'339: claim 27	disabled" (i.e., no further construction necessary)	mean "enabling only one of the data paths while the other possible paths are disabled," *i.e.*, "enable only one of the data paths for a respective n-bit section of the read data while the other possible data paths for the same respective n-bit section of the read data are disabled"	
"**N-bit wide write data**" '339: claims 1-3, 11, 14	[Agreed]	[Agreed]	"write data that is N bits in width"
"**in accordance with a latency parameter**" '339: claims 1, 11, 34, 35	[Agreed]	[Agreed]	"a time period wherein the start of the time period depends on at least a latency parameter"
"**A N-bit-wide memory module mountable in a memory socket of a computer system and configurable to communicate with a memory controller of the computer system via address and control signal lines and N-bit wide data signal lines, the N-bit wide data signal lines including a plurality of sets of data signal lines, each set of data signal**	[Agreed]	[Agreed]	The preamble is limiting.

Term (Patent/Claim)	Netlist's Proposed Construction	Micron's Proposed Construction	Court's Construction
lines is a byte wide, the memory module comprising" '339: claim 1			
"**A N-bit-wide memory module mountable in a memory socket of a computer system and configured to communicate with a memory controller of the computer system via address and control signal lines and N-bit wide data signal lines, the N-bit wide data signal lines including a plurality of sets of data signal lines, the memory module comprising**" '339: claims 11, 19	[Agreed]	[Agreed]	The preamble is limiting

Term (Patent/Claim)	Netlist's Proposed Construction	Micron's Proposed Construction	Court's Construction
"**A memory module mountable in a memory socket of a computer system and configurable to communicate with a memory controller of the computer system via address and control signal lines and data signal lines, the data signal lines including a plurality of sets of data signal lines, each set of data signal lines is n bit wide, the memory module comprising**" '339: claim 27	[Agreed]	[Agreed]	The preamble is limiting

Exhibit A4: Proposed Constructions for the '918 and '054 Patents

Term (Patent/Claim)	Netlist's Proposed Construction	Micron's Proposed Construction	Court's Construction
"**first**" / "**second**" / "**third**" / "**fourth**" "**regulated voltages**" '918: all claims	plain and ordinary meaning (i.e., no further construction necessary beyond the Court's construction in *Samsung I*)	"first regulated voltage that is distinct from the second, third, and fourth regulated voltages" / "second regulated voltage that is distinct from the first, third, and fourth regulated voltages" / "third regulated voltage that is distinct from the first, second, and fourth regulated voltages" / "fourth regulated voltage that is distinct from the first, second, and third regulated voltages"	
"**first**" / "**second**" / "**third**" / "**fourth**" "**voltage amplitude**" '918: all claims	plain and ordinary meaning (i.e., no further construction necessary beyond the Court's construction in *Samsung I*)	"first voltage amplitude that is distinct from the second, third, and fourth voltage amplitudes" / "second voltage amplitude that is distinct from the first, third, and fourth voltage amplitudes" / "third voltage amplitude that is distinct from the first, second, and fourth voltage amplitude" / "fourth voltage amplitude that is distinct from the first, second, and third voltage amplitude"	
"**at least three regulated voltages**" '054: claims 1-15	plain and ordinary meaning (i.e., no further construction necessary beyond the Court's construction in *Samsung I*)	"at least three distinct regulated voltages"	
"**plurality of regulated voltages**" '054: claims 16, 24	plain and ordinary meaning (i.e., no further construction necessary beyond the	"plurality of distinct regulated voltages"	

Term (Patent/Claim)	Netlist's Proposed Construction	Micron's Proposed Construction	Court's Construction
	Court's construction in *Samsung I*)		
"**a second plurality of address and control signals**" '918: claims 1-3, 4-7, 9-13, 15, 21	plain and ordinary meaning (i.e., no further construction necessary beyond the Court's construction in *Samsung I*)	"a second plurality of address and control signals that are distinct from a first plurality of address and control signals"	
"**dual buck converter**" / "**dual-buck converter**" '918: claims 2, 17, 28 '054: claim 15	"a buck converter with two regulated voltage outputs" (i.e., no further construction necessary beyond the Court's construction in *Samsung I*)	"buck converter with two outputs outputting two distinct regulated voltages"	

Term (Patent/Claim)	Netlist's Proposed Construction	Micron's Proposed Construction	Court's Construction
"**pre-regulated input voltage**" / **"input voltage"** '918: claims 16-22, 30	plain and ordinary meaning (i.e., no further construction necessary beyond the Court's construction in *Samsung I*) (this claim construction issue was raised in *Samsung I*, with the Court rejecting the construction Micron now proposes, *see*, Dkt. 110-05 at 81:20-82:9)	plain and ordinary meaning, where "a pre-regulated input voltage" is different from "an input voltage" (this is a new claim construction issue that was not raised or decided in *Samsung I*, *see* Dkt. 109 at 14-15)	
"A **memory module**" '918 and '054: all claims	The preamble is limiting	The preamble is non-limiting	
"**converter circuit**" '918: all claims	Not subject to § 112, ¶ 6; plain and ordinary meaning, i.e., a circuit for voltage conversion	This is a means-plus-function limitation. <u>Function (claim dependent)</u> (i) "provid[ing] a fourth regulated voltage having a fourth voltage amplitude"; (ii) "reduc[ing] the pre-regulated input voltage to provide a fourth regulated voltage"; (iii) "provid[ing] the fourth regulated voltage"; (iv) "reduc[ing] the pre-regulated voltage input to provide the fourth regulated voltage"	

Term (Patent/Claim)	Netlist's Proposed Construction	Micron's Proposed Construction	Court's Construction
		The corresponding structure that is "configured to" perform the recited functions is a "converter circuit," as described in the '918 patent at 29:18–64.	
"**first circuit**" '054: claims 1-13, 15	plain and ordinary meaning	"a circuit that is different from a memory module controller"	
"**at least one circuit**" '918: claims 1-3, 5-7, 9-13, 15, 21	Not subject to § 112(6); plain and ordinary meaning. If subject to §112(6), then: Function: (i) receive a first plurality of address and control signals via [the first/a second] portion of the plurality of edge connections, and (ii) output a second plurality of address and control signals to the plurality of SDRAM devices. Structures: As described in 21:14-23, 23:27-31, 23:41-	This is a means-plus-function limitation. <u>Function (claim dependent)</u> (i) "receiv[ing] a first plurality of address and control signals via the first portion of the plurality of edge connections"; (ii) "output[ting] a second plurality of address and control signals to the plurality of SDRAM devices"; (iii) "receiv[ing] a first plurality of address and control signals via a second portion of the plurality of edge connections"; (iv) "output a second plurality of address and control signals to the plurality of SDRAM devices" The corresponding structure that is "operable to" perform the recited functions is a "circuit that is different from a memory module controller," as described in the '918 patent at 21:14–26:65, 29:33–54.	

Term (Patent/Claim)	Netlist's Proposed Construction	Micron's Proposed Construction	Court's Construction
	24:8 or equivalents thereof.		
"**controller**" '918: claims 12, 18-19, 25-26 '054: claims 5, 7-13, 16-17, 23-25, 29-30	Not subject to § 112(6) and not indefinite; plain and ordinary meaning. To the extent that "controller" is a § 112(6) term, the function and corresponding structure vary for each claim, contrary to Micron's attempt to aggregate all functions into the term. Structures: ASIC, PLD, CPLD, FPGA, custom-designed semiconductor device as described in 23:1-27, 24:35-37, 25:8-31, 29:33-54, 32:49-51 or equivalents thereof.	This is a means-plus-function limitation. <u>Function in '918 Patent (claim dependent)</u> (i) "receiv[ing] the trigger signal, wherein, in response to the trigger signal, the controller performs a write operation to the non-volatile memory"; (ii) "receiv[ing] the signal, wherein the controller executes a write operation in response to the signal"; (iii) "receiv[ing] the signal, wherein, in response to the signal, the controller executes a write operation" <u>Function in '054 Patent (claim dependent)</u> (i) "perform[ing] one or more operations including a write operation to transfer data to non-volatile memory" "in response to the trigger signal"; (ii) "perform[ing] one or more operations in response to the voltage monitor circuit detecting an amplitude change in the input voltage, and wherein the one or more operations include a write operation to transfer data into non-volatile memory" <u>Corresponding Structure in '918 Patent</u> The corresponding structure that is "configured to" perform the recited functions is a "controller that is different from the at least one circuit and the voltage	

Term (Patent/Claim)	Netlist's Proposed Construction	Micron's Proposed Construction	Court's Construction
		monitor circuit and the one or more registers," as described in the '918 patent at 21:14–26:65, 29:33–54. <u>Corresponding Structure in '054 Patent</u> The corresponding structure that is "configured to" perform the recited functions is a "controller that is different from the first circuit and the voltage monitor circuit," as described in the '054 patent at 21:14–26:65, 29:33–54.	
"**first operable state**" '054: claims 4-7, 11-12, 16-17, 23, 25-26	"first operable state" is a "state in which the memory module is operated before transition"; not indefinite	"state in which a controller and a non-volatile memory subsystem are operatively decoupled (e.g., isolated) from a volatile memory subsystem by at least one circuit" In the alternative, indefinite	
"**second operable state**" '054: claims 4-7, 11-12, 16-17, 23, 25-26	"second operable state" is a "state in which the memory module is operated after transition"; not indefinite	"state in which the volatile memory subsystem is operatively coupled to the controller to allow data to be communicated between the volatile memory subsystem and the nonvolatile memory subsystem via the controller" In the alternative, indefinite	