EXHIBIT D

US006233010B1

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Roberts et al.

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(45) Date of Patent: ***May 15, 2001**

(54) **ELECTRONIC STILL VIDEO CAMERA WITH DIRECT PERSONAL COMPUTER (PC) COMPATIBLE DIGITAL FORMAT OUTPUT**

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(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U S C 154(b) by 0 days

This patent is subject to a terminal disclaimer

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(22) Filed: Feb. 19, 1999

Related U.S. Application Data

(63) Continuation of application No 08/712,493, filed on Sep 11, 1996, which is a continuation of application No. 08/098,787, filed on Jul 29, 1993, now Pat No. 5,576,757, which is a continuation of application No 07/878,603, filed on May 5, 1992, now abandoned, which is a continuation of application No 07/615,848, filed on Nov 20, 1990, now Pat No 5,138,459

(51) Int. Cl.[7] H04N 5/225

(52) U.S. Cl. 348/220; 348/207

(58) Field of Search 348/207, 220, 348/221, 222, 230, 232, 233, 239; 358/909, 906 1; H04N 5/225

(56) References Cited

U S PATENT DOCUMENTS

4,758,883	*	7/1988	Kawahara et al	348/231
5,016,107	*	5/1991	Sassonet et al	348/231
5,034,804	*	7/1991	Sasaki et al	348/231
5,153,730	*	10/1992	Nagasaki et al	348/231

FOREIGN PATENT DOCUMENTS

63-284987	5/1987	(JP)
2-125572	11/1988	(JP)
1-114286	5/1989	(JP)
1-248785	10/1989	(JP)
2-146874	6/1990	(JP)
2-202782	8/1990	(JP)
2-208779	8/1990	(JP)
2-222385	9/1990	(JP)
2-257780	10/1990	(JP)

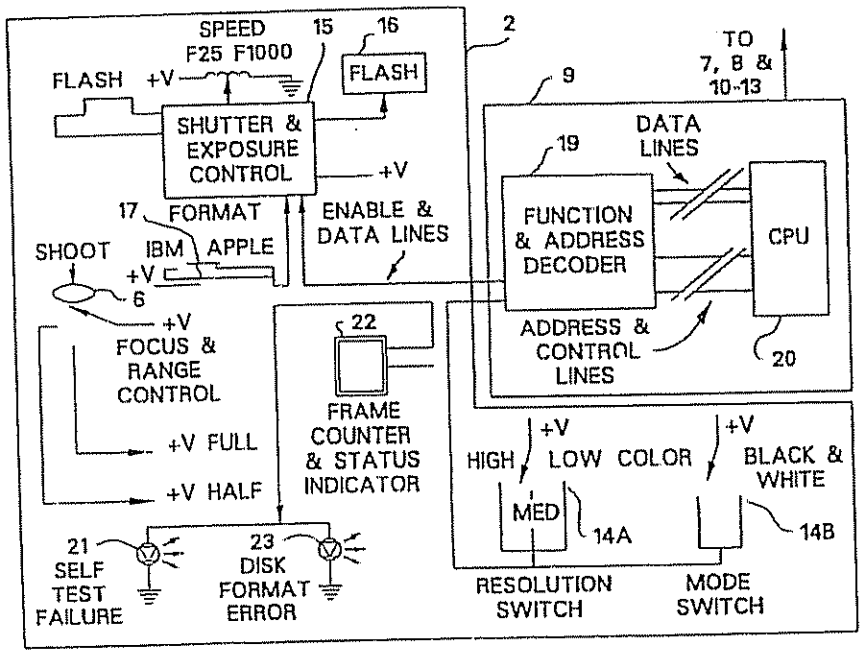
* cited by examiner

Primary Examiner—Tuan Ho
(74) *Attorney, Agent, or Firm*—Harness, Dickey & Pierce, P.L.C

(57) ABSTRACT

A digital camera includes a digital memory system having a control unit for checking for proper format initialization of a removable digital memory element and for performing format initialization of the memory element when necessary

1 Claim, 11 Drawing Sheets



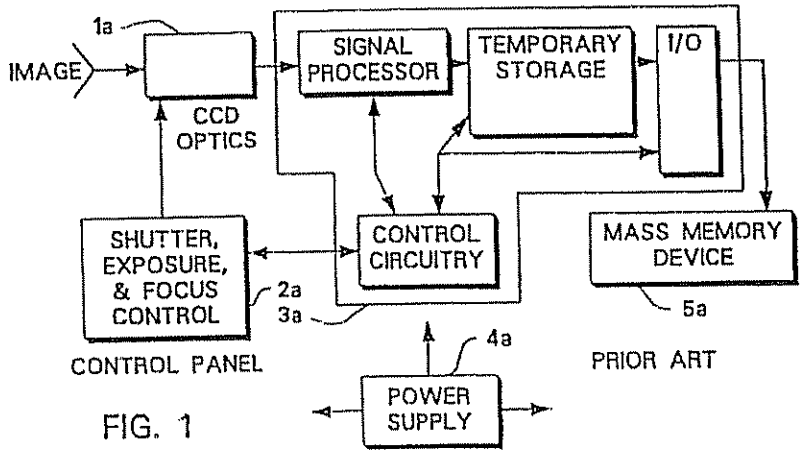

1a
IMAGE
CCD OPTICS
SIGNAL PROCESSOR
TEMPORARY STORAGE
I/O
SHUTTER, EXPOSURE, & FOCUS CONTROL
2a
3a
CONTROL CIRCUITRY
MASS MEMORY DEVICE
5a
CONTROL PANEL
4a
POWER SUPPLY
PRIOR ART

FIG. 1

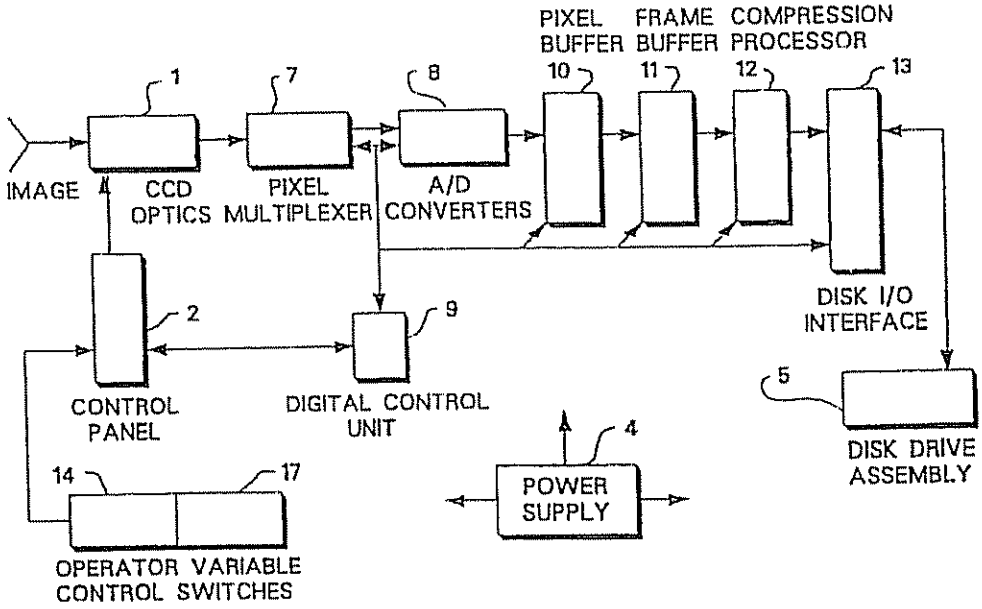

PIXEL BUFFER
FRAME BUFFER
COMPRESSION PROCESSOR
1
7
8
10
11
12
13
IMAGE
CCD OPTICS
PIXEL MULTIPLEXER
A/D CONVERTERS
DISK I/O INTERFACE
2
9
5
CONTROL PANEL
DIGITAL CONTROL UNIT
DISK DRIVE ASSEMBLY
4
14
17
POWER SUPPLY
OPERATOR VARIABLE CONTROL SWITCHES

FIG. 2

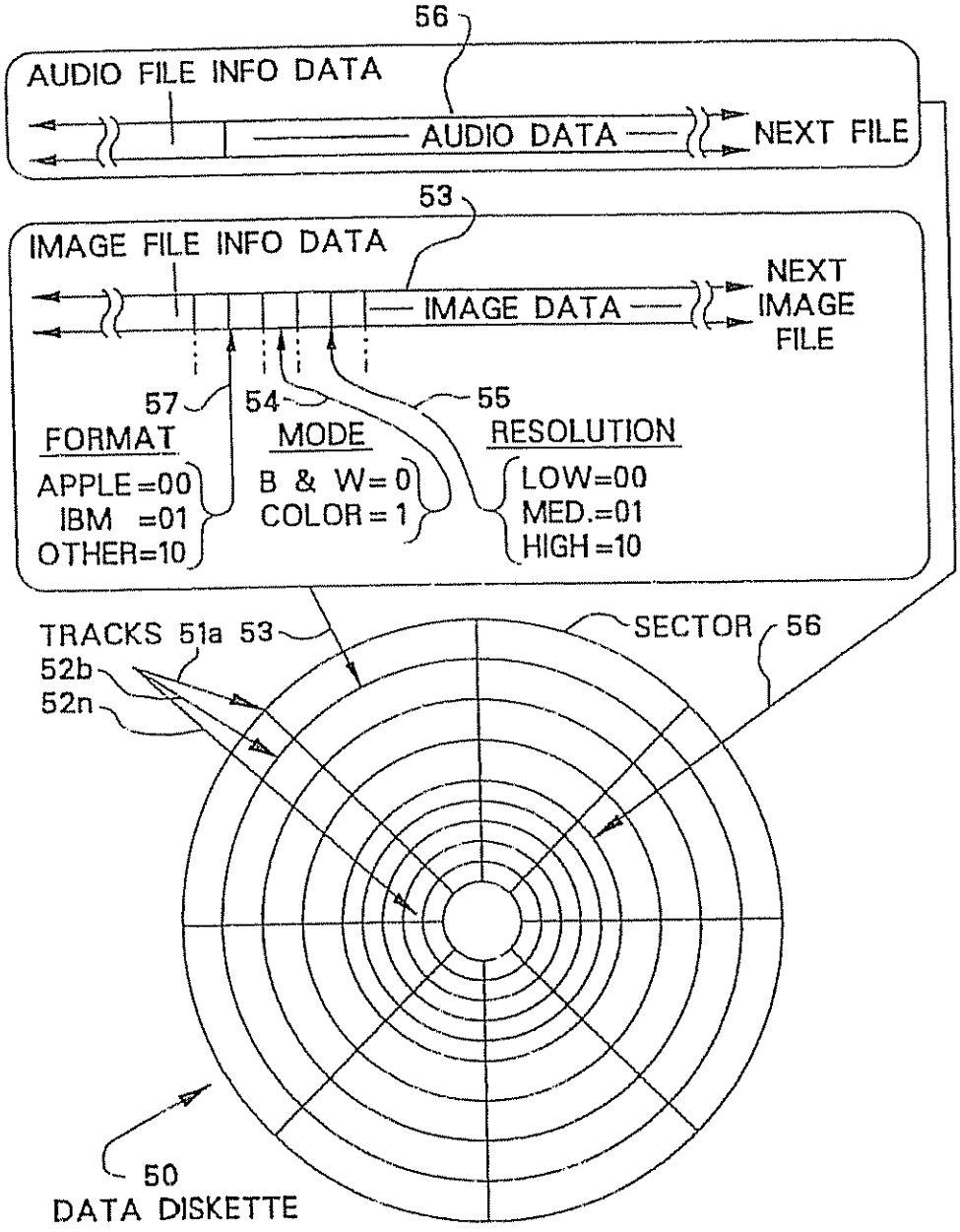

56
AUDIO FILE INFO DATA
AUDIO DATA
NEXT FILE
53
IMAGE FILE INFO DATA
IMAGE DATA
NEXT IMAGE FILE
57
54
55
FORMAT
APPLE=00
IBM =01
OTHER=10
MODE
B & W=0
COLOR=1
RESOLUTION
LOW=00
MED.=01
HIGH=10
TRACKS 51a
53
52b
52n
SECTOR
56
50
DATA DISKETTE

FIG. 2A

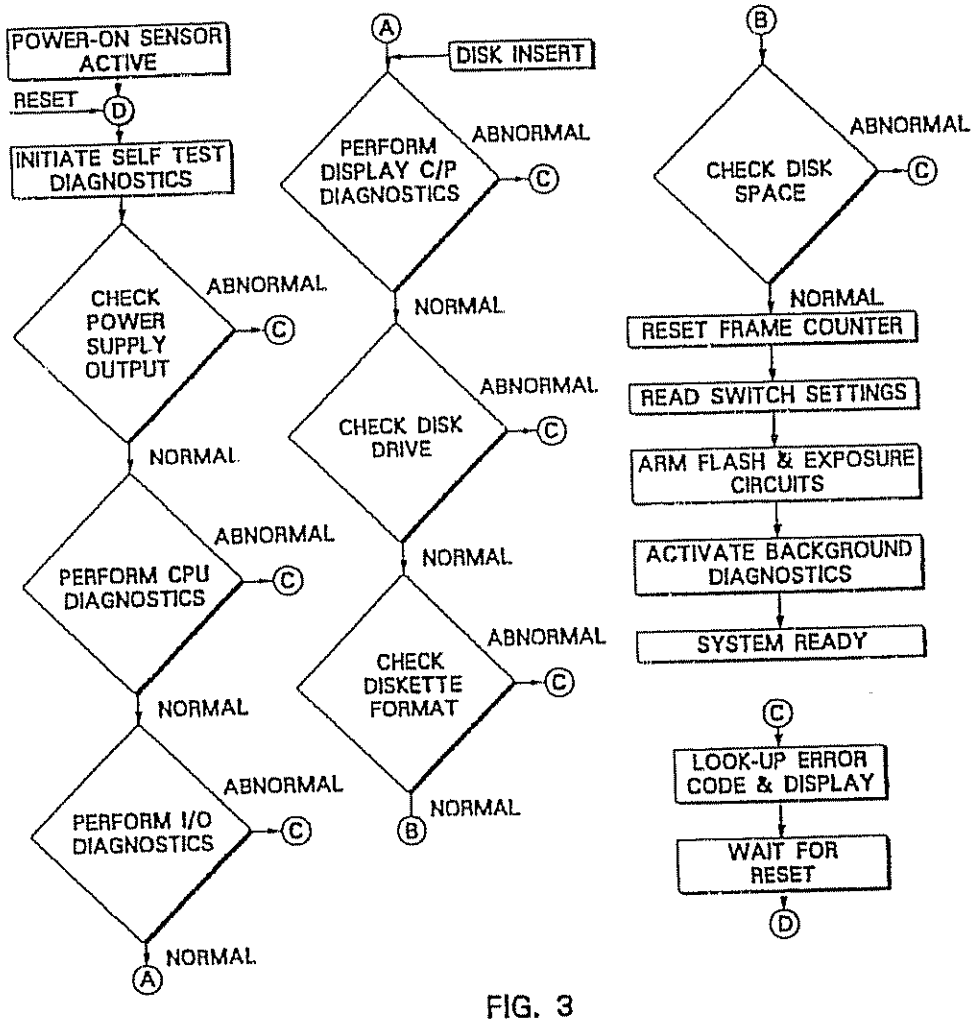
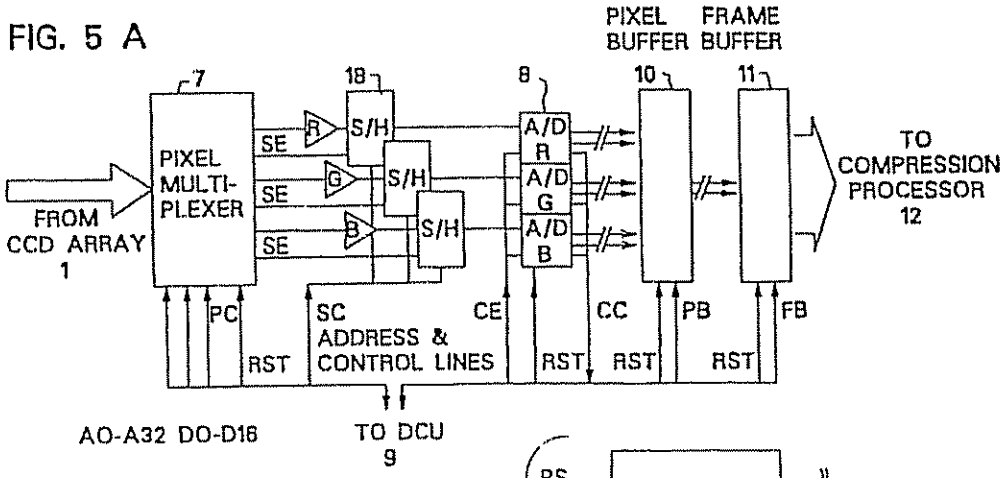

POWER-ON SENSOR ACTIVE
RESET
D
INITIATE SELF TEST DIAGNOSTICS
CHECK POWER SUPPLY OUTPUT
ABNORMAL
C
NORMAL
PERFORM CPU DIAGNOSTICS
ABNORMAL
C
NORMAL
PERFORM I/O DIAGNOSTICS
ABNORMAL
C
NORMAL
A
A
DISK INSERT
PERFORM DISPLAY C/P DIAGNOSTICS
ABNORMAL
C
NORMAL
CHECK DISK DRIVE
ABNORMAL
C
NORMAL
CHECK DISKETTE FORMAT
ABNORMAL
C
NORMAL
B
B
CHECK DISK SPACE
ABNORMAL
C
NORMAL
RESET FRAME COUNTER
READ SWITCH SETTINGS
ARM FLASH & EXPOSURE CIRCUITS
ACTIVATE BACKGROUND DIAGNOSTICS
SYSTEM READY
C
LOOK-UP ERROR CODE & DISPLAY
WAIT FOR RESET
D

FIG. 3

FIG. 5 A



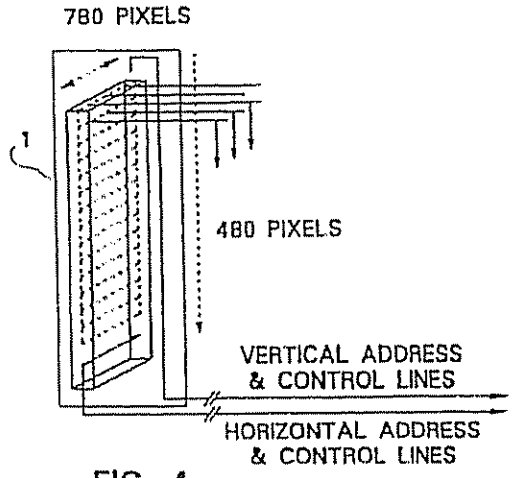


FIG. 4

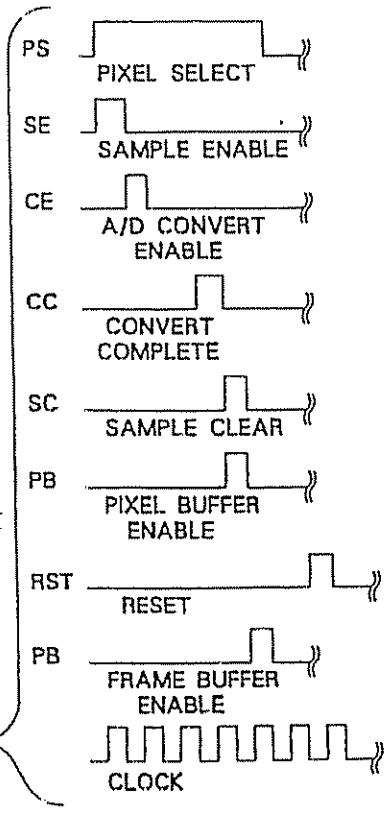


FIG. 5B

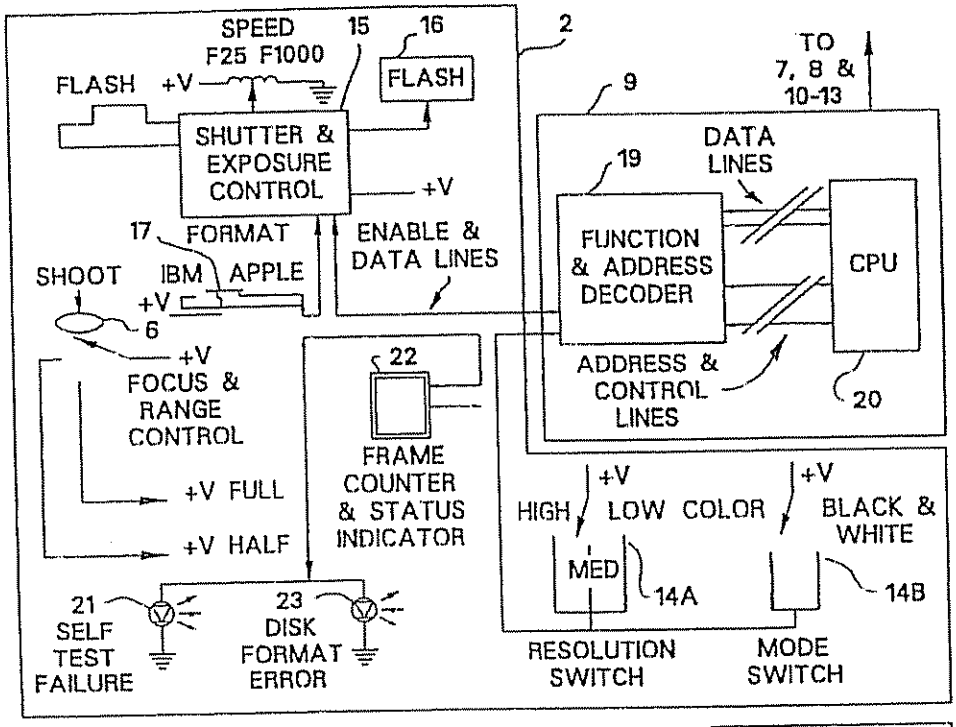


FIG. 6

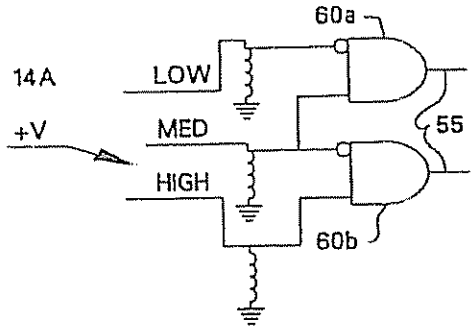


FIG. 6A

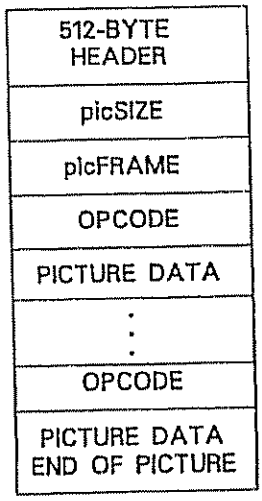


FIG.6B

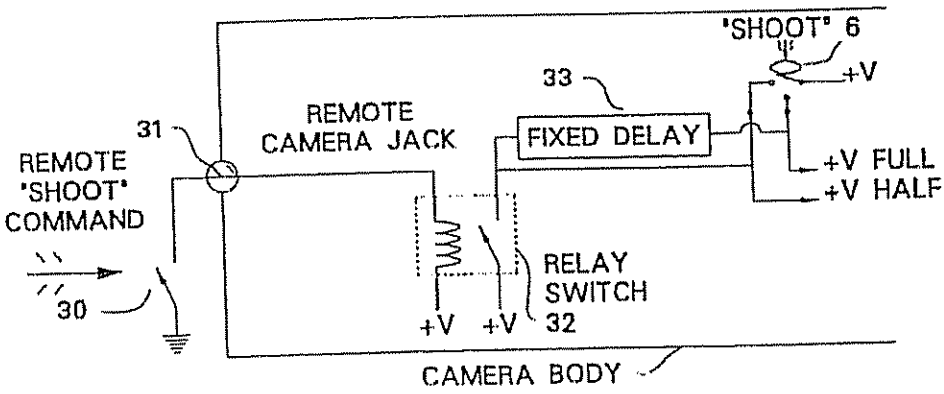

"SHOOT" 6
+V
33
31
REMOTE CAMERA JACK
FIXED DELAY
REMOTE "SHOOT" COMMAND
+V FULL
+V HALF
RELAY SWITCH 32
30
+V +V
CAMERA BODY

FIG. 6C

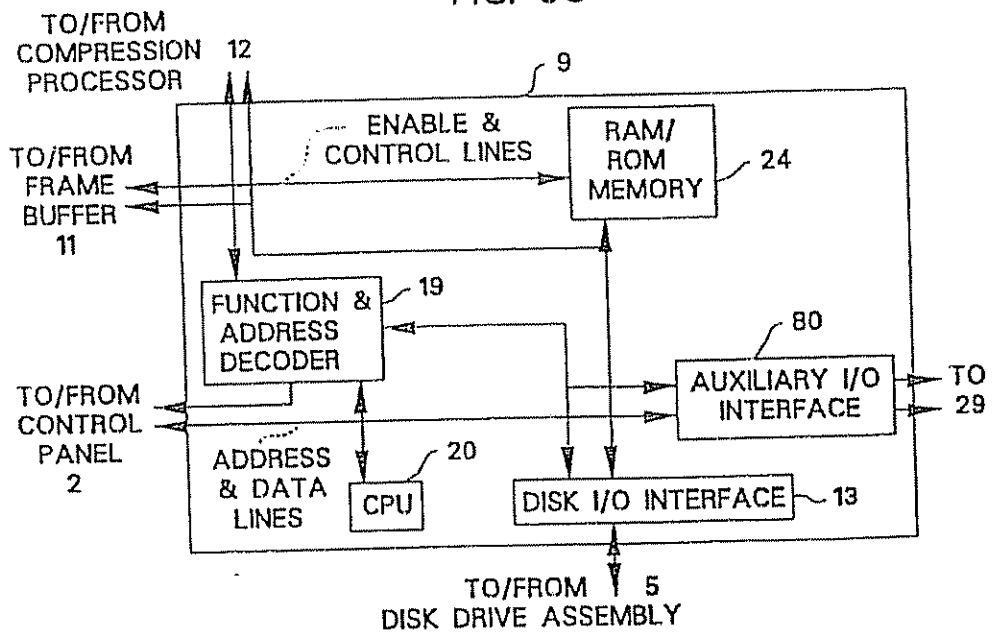

TO/FROM COMPRESSION PROCESSOR 12
9
ENABLE & CONTROL LINES
RAM/ ROM MEMORY 24
TO/FROM FRAME BUFFER 11
FUNCTION & ADDRESS DECODER 19
80
AUXILIARY I/O INTERFACE
TO 29
TO/FROM CONTROL PANEL 2
ADDRESS & DATA LINES
CPU 20
DISK I/O INTERFACE 13
TO/FROM 5 DISK DRIVE ASSEMBLY

FIG. 7

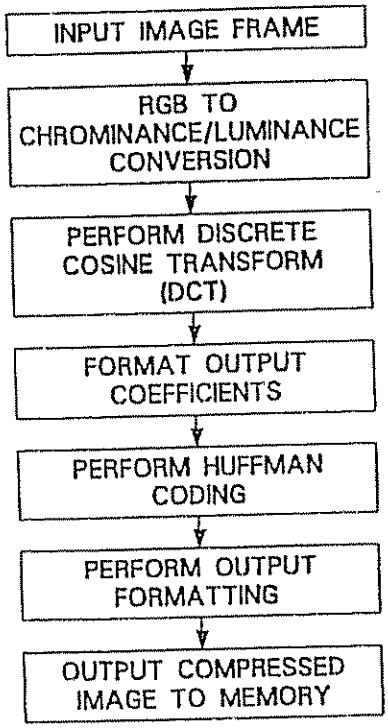


FIG. 8

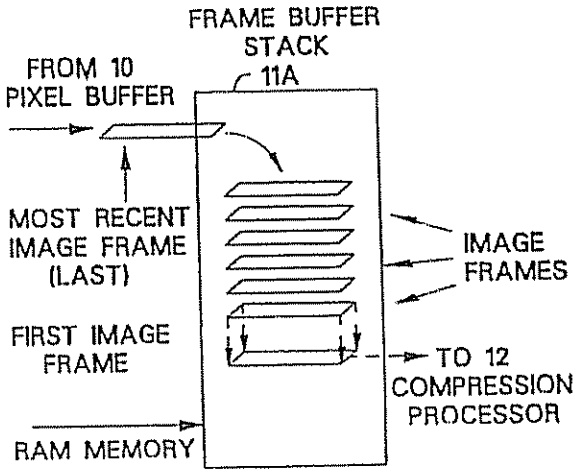


FIG. 13

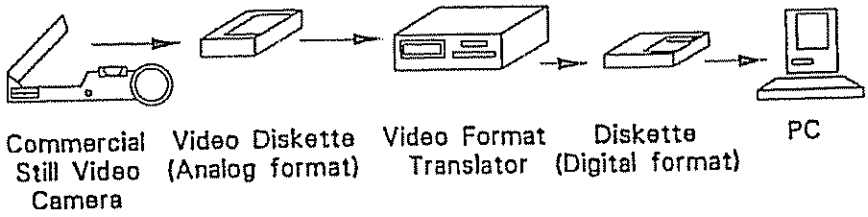


FIG. 10

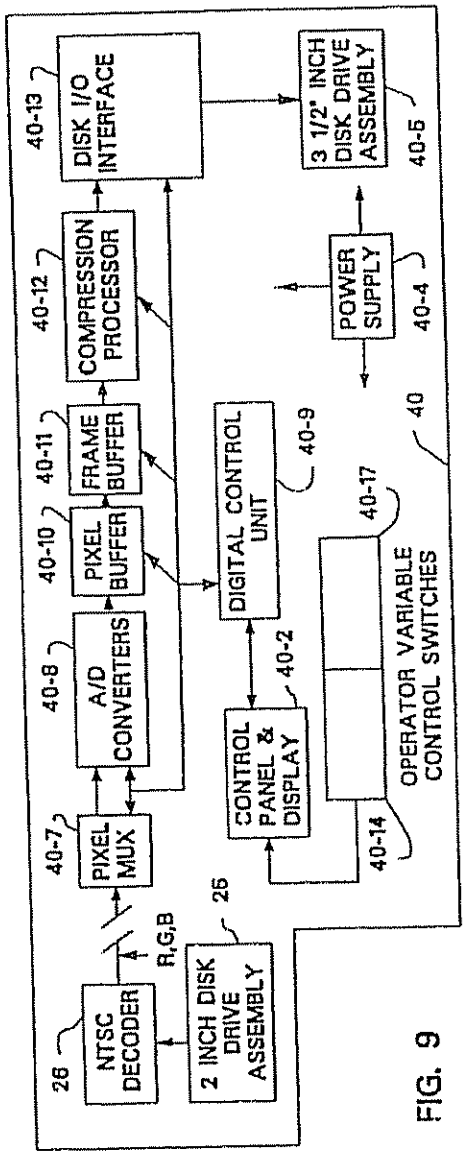

26
NTSC DECODER
R,G,B
25
2 INCH DISK DRIVE ASSEMBLY
40-7
PIXEL MUX
40-8
A/D CONVERTERS
40-10
PIXEL BUFFER
40-11
FRAME BUFFER
40-12
COMPRESSION PROCESSOR
40-13
DISK I/O INTERFACE
40-2
CONTROL PANEL & DISPLAY
40-9
DIGITAL CONTROL UNIT
40-14
40-17
OPERATOR VARIABLE CONTROL SWITCHES
40
40-4
POWER SUPPLY
3 1/2" INCH DISK DRIVE ASSEMBLY
40-5

FIG. 9

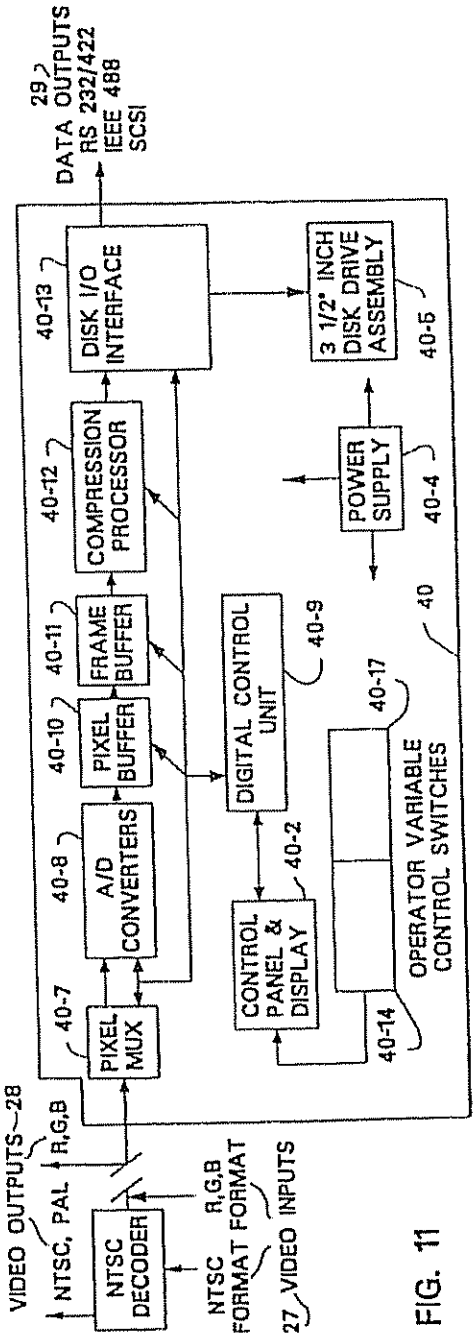

29
DATA OUTPUTS
RS 232/422
IEEE 488
SCSI
VIDEO OUTPUTS
28
NTSC, PAL
R,G,B
NTSC DECODER
R,G,B
NTSC FORMAT
27
VIDEO INPUTS
40-7
PIXEL MUX
40-8
A/D CONVERTERS
40-10
PIXEL BUFFER
40-11
FRAME BUFFER
40-12
COMPRESSION PROCESSOR
40-13
DISK I/O INTERFACE
40-2
CONTROL PANEL & DISPLAY
40-9
DIGITAL CONTROL UNIT
40-14
40-17
OPERATOR VARIABLE CONTROL SWITCHES
40
40-4
POWER SUPPLY
3 1/2" INCH DISK DRIVE ASSEMBLY
40-5

FIG. 11

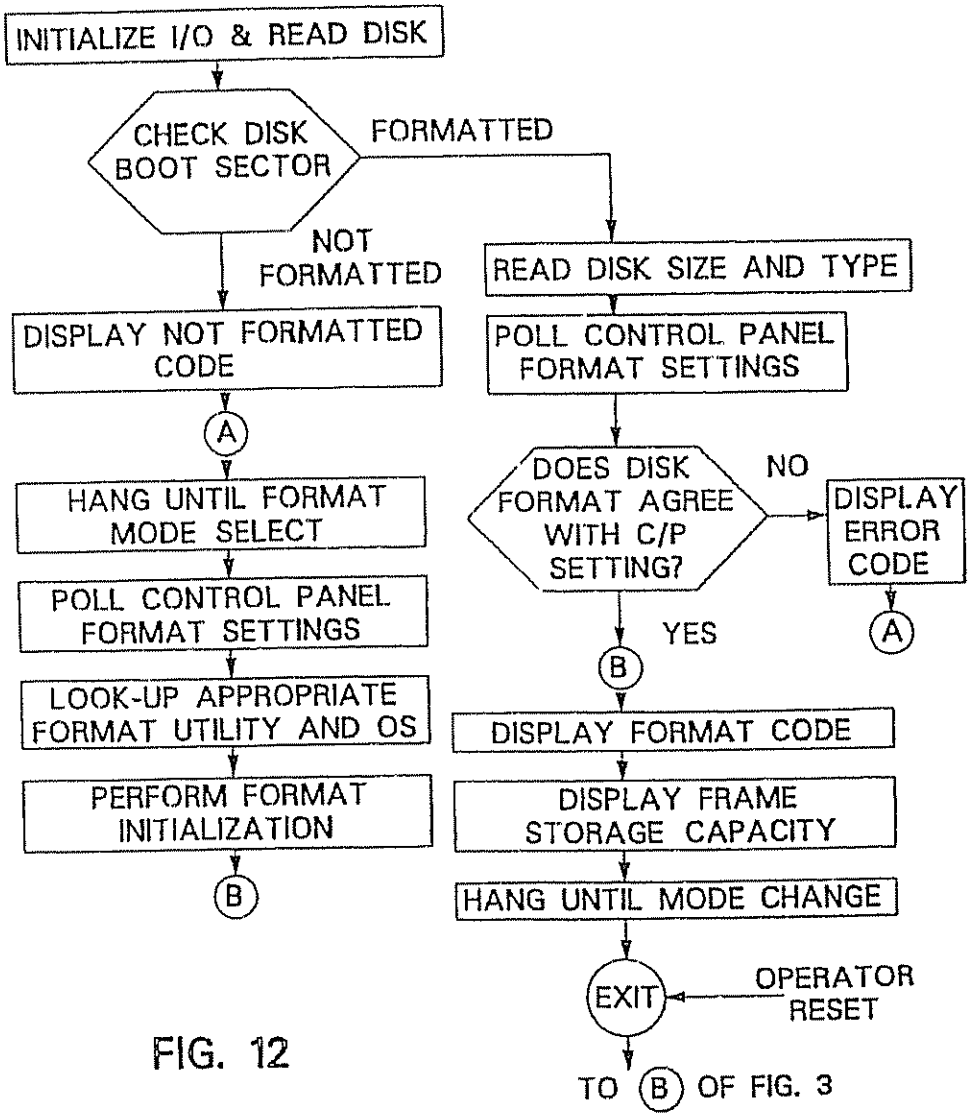

INITIALIZE I/O & READ DISK
CHECK DISK BOOT SECTOR
FORMATTED
NOT FORMATTED
READ DISK SIZE AND TYPE
DISPLAY NOT FORMATTED CODE
POLL CONTROL PANEL FORMAT SETTINGS
A
DOES DISK FORMAT AGREE WITH C/P SETTING?
NO
DISPLAY ERROR CODE
A
HANG UNTIL FORMAT MODE SELECT
YES
B
POLL CONTROL PANEL FORMAT SETTINGS
DISPLAY FORMAT CODE
LOOK-UP APPROPRIATE FORMAT UTILITY AND OS
DISPLAY FRAME STORAGE CAPACITY
PERFORM FORMAT INITIALIZATION
HANG UNTIL MODE CHANGE
B
EXIT
OPERATOR RESET
TO B OF FIG. 3

FIG. 12

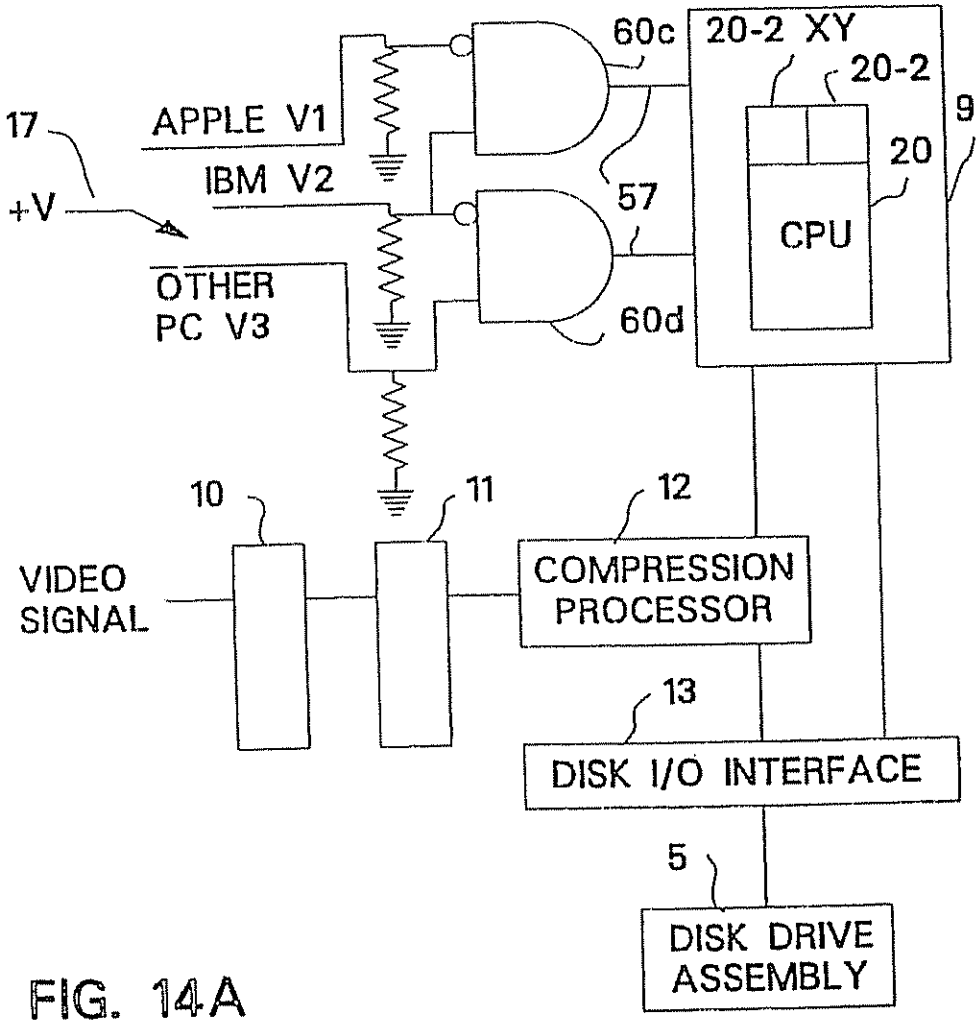

17
+V
APPLE V1
IBM V2
OTHER
PC V3
60c
57
60d
20-2 XY
20-2
20
CPU
9
10
11
12
VIDEO
SIGNAL
COMPRESSION
PROCESSOR
13
DISK I/O INTERFACE
5
DISK DRIVE
ASSEMBLY

FIG. 14A

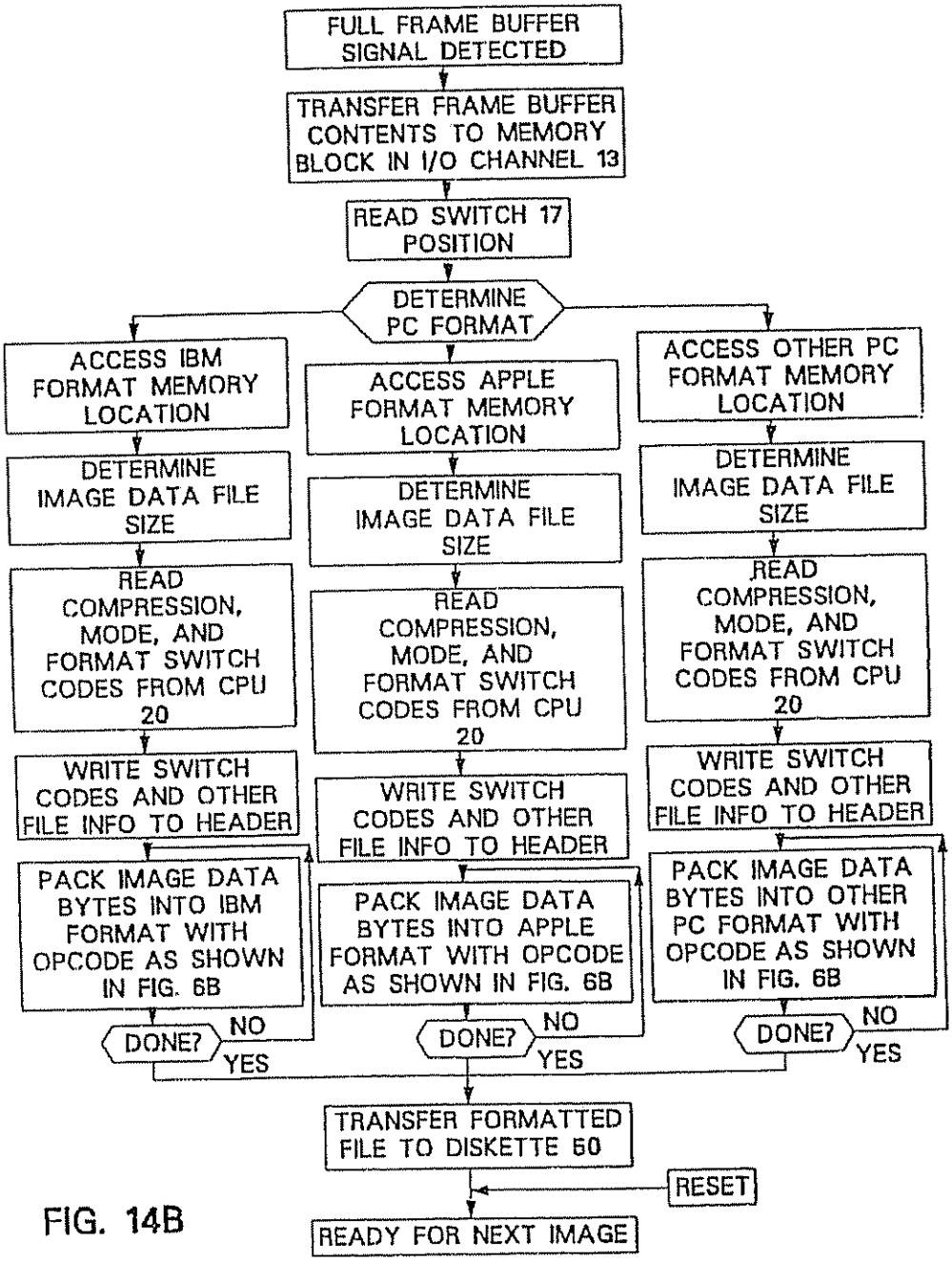

FULL FRAME BUFFER SIGNAL DETECTED
TRANSFER FRAME BUFFER CONTENTS TO MEMORY BLOCK IN I/O CHANNEL 13
READ SWITCH 17 POSITION
DETERMINE PC FORMAT
ACCESS IBM FORMAT MEMORY LOCATION
ACCESS APPLE FORMAT MEMORY LOCATION
ACCESS OTHER PC FORMAT MEMORY LOCATION
DETERMINE IMAGE DATA FILE SIZE
DETERMINE IMAGE DATA FILE SIZE
DETERMINE IMAGE DATA FILE SIZE
READ COMPRESSION, MODE, AND FORMAT SWITCH CODES FROM CPU 20
READ COMPRESSION, MODE, AND FORMAT SWITCH CODES FROM CPU 20
READ COMPRESSION, MODE, AND FORMAT SWITCH CODES FROM CPU 20
WRITE SWITCH CODES AND OTHER FILE INFO TO HEADER
WRITE SWITCH CODES AND OTHER FILE INFO TO HEADER
WRITE SWITCH CODES AND OTHER FILE INFO TO HEADER
PACK IMAGE DATA BYTES INTO IBM FORMAT WITH OPCODE AS SHOWN IN FIG. 6B
PACK IMAGE DATA BYTES INTO APPLE FORMAT WITH OPCODE AS SHOWN IN FIG. 6B
PACK IMAGE DATA BYTES INTO OTHER PC FORMAT WITH OPCODE AS SHOWN IN FIG. 6B
DONE?
NO
YES
DONE?
NO
YES
DONE?
NO
YES
TRANSFER FORMATTED FILE TO DISKETTE 50
RESET
READY FOR NEXT IMAGE

FIG. 14B

ELECTRONIC STILL VIDEO CAMERA WITH DIRECT PERSONAL COMPUTER (PC) COMPATIBLE DIGITAL FORMAT OUTPUT

This is a continuation of U S patent application Ser No 08/712,493, filed Sep 11, 1996, which is a continuation of U S patent application Ser No 08/098,787, filed Jul 29, 1993, now U S Pat No 5,576,757, which is a continuation of U S patent application Ser. No 07/878,603, filed May 5, 1992, now abandoned, which is a continuation of U S patent application Ser. No 07/615,848, filed Nov 20, 1990 and now U S Pat No 5,138,459

BACKGROUND OF THE INVENTION

1 Field of the Invention

This invention generally relates to an electronic still video camera and in particular to an improved electronic still camera which converts a still picture of an object or scene into an operator selectable compressed digital signal format for storage utilizing a compression/decompression algorithm, such as the Joint Photographic Experts Group (JPEG) algorithm standard for example, formatted into Personal Computer (PC) compatible format retaining the images' color information, and stored on a PC compatible memory diskette For example, the diskette can be a three and a half (3½) inch digital diskette The digital diskette is removeable from the electronic camera for direct insertion into a PC which contains the previously loaded corresponding decompression algorithm whereby the digital image is in a format compatible for immediate use with word processing, desk top publishing, data base, and multi-media applications

2 Description of the Prior Art

FIG 1 is a schematic block diagram showing structure of a conventional prior art electronic still camera system, in which a CCD image sensor element 1*a* converts a still image of an object into an analog color video signal when the shutter control circuitry 2*a* is activated The output color video signal of the image sensor element is then routed to the signal processing subsystem 3*a* where the signal is converted to National Television System Committee (NTSC) or other composite video formats (such as the European video standard Phase Alternating Line-PAL) and logged in analog format onto a mass memory storage device such as an analog video floppy disk, Electrically Erasable Programmable Read Only Memory (EEPROM), analog audio cassette, bubble memory, or other storage device 5*a* Power is supplied by a rechargeable/removeable battery system 4*a*

An electronic camera that converts an image into electronic image signals and transferred to a memory storage device is disclosed in the following: U S Pat No. 4,131,919; U S Pat No 4,456,931; U S Pat No 4,758,883; U S Pat No 4,803,554; and U S Pat No 4,837,628

Conventional prior art electronic still cameras, for example of the types disclosed in the aforementioned references, produce an electronic signal corresponding to a desired image in analog format such as the National Television System Committee (NTSC) or similar on magnetic or electronic storage media for either permanent or temporary storage to facilitate viewing on a television or video monitor With the current state of the art, it is expensive and time consuming to convert the analog image equivalent to a digital format for direct utilization with PC software applications Currently, to convert an image captured on an electronic still camera to a PC compatible format one must convert the signal back to either a composite NTSC or RGB video signal and use a conversion device such as a "frame grabber" (a digital circuit board installed into PCs that convert video images into PC compatible formats) of the type sold commercially by Aapps Corporation, Orange Micro, RasterOps, and others or convert the image to a hard-copy print (a photograph) and utilize an electronic "scanner", a piece of equipment that connects to a PC, which converts an image into a digital format The later technique is employed extensively within the desktop publishing industry

SUMMARY OF THE INVENTION

It is the object of this invention to provide an improved electronic still camera with operator selectable picture compression in one of a plurality of operator selectable digital data formats recordable on a standard removeable magnetic diskette common to personal computers

It is a further object of this invention to provide an improved electronic still camera that provides digital image files for immediate and direct incorporation into popular word processing, desktop publishing, and other software programs on PCs

It is another object of this invention is to provide an improved electronic still camera that, under user selection, can record and store still images selectively compressed in a directly insertable digital memory storage device into a PC in either color or black and white formats thus facilitating storage of a large number of images with the signal flag indicating the degree of compression selected by the operator as well as the color/black and white mode selection being stored as digital values on the digital memory storage device with each image frame

An additional object of this invention to provide an electronic still camera device that can rapidly capture a series of images automatically as well as singularly Also, this camera provides multiple outputs in both video format for monitor and display of images and digital formats to facilitate data transmission, additional processing, or storage to a variety of storage media

It is still another object of this invention is to provide a more efficient electronic still camera that can take a still picture with operator selectable high, medium, or low resolution in either color or black and white by electronic shutter and exposure control by utilizing a variety of electro-optical sensors including Charge Coupled Devices (CCD), Infrared (IR), and Ultra Violet (UV) which can be directly or remotely controlled by analog, digital, or radio frequency (RF) control signals

A further object of this invention is to provide a programmable video picture translator device for efficiently converting electronic still images in analog composite video format into digital data format readable by a PC This translator device also provides additional video inputs and outputs for capturing video images, monitoring video images on monitors and displays, and can transmit either compressed or unprocessed digital image data through a variety of output I/O channels in various formats such as serial, parallel, etc Also, this invention can incorporate sound/voice with images thru additional interface circuitry and audio digitizers

Finally, it is the object of this invention to provide an electronic still camera that is efficient in design and permits extended periods of portable operation and which provides the user with operational status through the use of continuous internal self-test software routines and operator displays

BRIEF DESCRIPTION OF THE DRAWINGS

FIG 1 is a schematic block diagram of a conventional prior art electronic still camera

FIG 2 is a schematic block diagram of the of the overall structure of an electronic still camera embodying the present invention

FIG 2A is an illustration showing one embodiment of an audio data file, data format flag, compression level, and color/black and white mode selection values stored on a digital memory diskette storage device

FIG 3 is a flowchart showing the power-up and continuous self-test sequence in accordance with one aspect of the present invention

FIG 4 is an example of a ½" CCD array utilizable in accordance with one aspect of the present invention

FIG 5A is a schematic block diagram showing the image signal to digital signal conversion logic in accordance with one aspect of the present invention

FIG 5B is a logic and timing diagram for the image signal to digital signal conversion logic in accordance with one aspect of the present invention

FIG 6 is an example of the control panel logic in accordance with one aspect of the present invention

FIG 6A is an example of one embodiment of switch logic of the control panel switches and controls utilizable in accordance with one aspect of the present invention

FIG 6B is an example of the PICT image file format based upon the published standard provided by Apple Computer, Inc

FIG 6C is an alternate embodiment of the current invention embodying remote operation

FIG 7 is a simplified block diagram of the digital control unit in accordance with one aspect of the present invention

FIG 8 is a flowchart showing the steps of the image compression algorithm in accordance with one aspect of the present invention

FIG 9 is a block diagram of a video format translator device in accordance with one aspect of the present invention

FIG 10 is a block diagram illustrating the operation of a translator device in accordance with one aspect of the present invention

FIG 11 is an alternative embodiment of the video format translator in accordance with another aspect of the present invention showing additional video inputs and data outputs

FIG 12 is an alternate embodiment of the invention showing an optional diskette format utility flowchart

FIG 13 is an alternate embodiment of a frame buffer utilizable in accordance with another aspect of the present invention showing a frame buffer stack permitting multiple shot mode

FIG 14A is a block diagram of an embodiment of the format select logic in accordance with one aspect of the present invention

FIG 14B is a flow diagram illustrating the steps of the format selection logic operations

DESCRIPTION OF THE PREFERRED EMBODIMENT

FIG 2 is a schematic block diagram of the preferred embodiment of an electronic still camera in accordance with the principals of the invention Referring to FIG 2, an image optical pick-up element 1, which for example could be a Charge Coupled Device (CCD) (or an Infrared (IR) or Ultraviolet (UV) sensor), converts a still image of an object into an electric signal when a picture "shoot" command is

initiated by the operator via control panel 2 When taking a picture, focusing and shutter speed are controlled by a lens system and shutter speed selection mechanism under control of the digital control unit 9 The camera, like other still video cameras, employs an electronic shutter system that controls a charge storage time in a CCD array onto which an image of an object is focused through the lens system

When the "shoot" control 6 is half depressed (see FIG 6) a power supply voltage is supplied from the rechargeable batteries 4 to the electronic circuits and digital control unit 9, control panel 2, and the disk drive assemble 5 The exposure control circuitry not shown generates appropriate horizontal and vertical transfer pulses as well as field shift pulses under control of the reference clock timing and control signals provided by the digital control unit 9 type for driving the CCD device and pre-processing circuitry This design may be of any type well known in the art for example those cited in U S Pat Nos 4,131,919 and 4,456,931 and any similar designs well known in the prior art

An alternate embodiment of the present invention that provides remote operation of the camera is shown in FIG 6C When remote "Shoot" control 30 is activated by any means for example manually, or by radiant, or electronic energy, a control signal is generated and routed through the external jack 31, located on the external camera body The external control 30 is electrically connected to the external jack 31 by a twisted-pair conductive cable assembly that is familiar to those skilled in the art Upon receipt of the externally generated "shoot" command, the relay switch 32 is activated and provides internal switch closure This closure of switch 32 then initiates the process previously described and privides the half V+ voltage previously described The full V+ is provided via the fixed delay 33, the value chosen to allow the diskette drive assembly 5 (FIG 2) and associated control circuitry to initialize prior to receiving image data

When the "shoot" control is fully depressed in either embodiment, the shutter controller 15 (FIG 6) generates a shutter pulse that generates control signals for the A/D converters 8 allowing the image/picture data signal in the sample and hold circuitry of the pixel multiplexer 7 to be converted into a digital signal Control and address instructions of the type well known in the art are generated from the digital control unit 9 to facilitate the storage of the digital image data within the pixel buffer 10 and frame buffer 11 Upon completion of image conversion, the contents of the frame buffer are transferred to the compression processor 12 which for example may be of the many versions currently offered commercially such as C-Cube's (San Jose, Calif) four chip Application Specific Integrated Circuit (ASIC) set In the compression processor 12, the Joist Photographic Experts Group (JPEG), a part of the International Standards Organization (ISO) which is a subset of the International Telegraph and Telephone Committee (CCITT), image compression algorithm fully described in Report # JTC1/SC2/WG8 dated 1985 is performed under control of the digital control unit 9 to compress the size of the image A variable selectable compression ratio of up to 50:1 is performed on the digital image frame Other compression ratios are operator selectable via the control panel 2 switches 14A and 14B (FIG 6) The compressed digital frame is then formatted into either an IBM PC/Clone (such as GIFF) or Apple Macintosh (such as PICT II) image file format depending on the setting selected by the operator for a user switch 17 (FIG 6) position on the control panel 2 After formatting, the file is written into a temporary memory buffer within the disk input/output I/O) interface circuit 13 which, under the com-

mand of the digital control unit 9, controls the high density (1 4 Mbyte storage capacity) disk drive unit 5 Following file transfer to the diskette e g , the frame counter display 22 on the control panel 2 is updated by appropriate control signals and the camera is ready to undergo the same procedure for the next image Power to the electronic circuits and disk drive system is terminated following release of the "shoot" control switch 6

In accordance with the preferred embodiment of this invention, it is permissible for the user to select various resolution quality image recording levels with the higher levels being at the expense of memory diskette storage capacity The position of switches 14A and 14B for example could represent a unique digital mark or word that denotes the respective switch position and is sensed during initial power application and periodically during operation FIG 6A illustrates typical logic AND gate circuits 60*a* and 60*b* utilizable in conjunction with switches 14A and 14B or switch 17 to generate appropriate signals to designate respective switch positions and generate appropriate control signals from The switch positioned in the High position for high resolution allows only four to five images to be stored, while Med switch position for medium resolution allows approximately twenty five images to be stored, and Low for low resolution allows up to fifty images to be stored on a single diskette Also, by selecting black and white mode instead of color via switch 14B, the operator may select additional storage capacity since storage is increased by a factor greater than three (one element per pixel versus three for color) Various image resolution combinations are permissible because the operator can select a different resolution and mode setting for each image prior to image signal capture This is accomplished by marking or "tagging" each image frame data information signal with the resolution and mode of each image as it is written onto the memory diskette in any suitable manner, for example as shown in FIG 2A With reference to FIG 2A, diskette 50 has tracks 51*a*, 52*b* 52*n* With reference to track 52*b* there is shown a representative portion of segment 53 depicting a typical image file information format having digital bit 54 depicting color mode, and digital bits 55 representing compression resolution level markings or tags With reference to color mode tag 54 it can be seen that if switch 14B is in the color position tag 54 is recorded as a logical "one" or true- conversely if bit 54 is recorded as a logical "zero" it corresponds to the black and white position of switch 14B Similarly as shown switch 14A would record in memory position 55 a binary zero" for low resolution, a binary "one" for medium resolution and a binary "two" for high resolution selections by the operator By incorporating this "tagging" approach, it is possible for the decompression algorithm, loaded into any PC prior to use or written onto the memory storage diskette along with the image data, to automatically determine the appropriate level of compression associated with image file and execute decompression efficiently

Still another alternate embodiment in accordance with this invention incorporates an acoustic digitizer circuit which digitizes sound There are several digitizers commercially available such as the Apple Computer Inc Musical Instrument Data Interface (MIDI) adaptor The output of this digitizer may be selectively connected to the CPU 20 (FIG 7) via an additional I/O interface similar to the auxiliary V/O interface 80 The sound or audio associated with each image can be recorded, digitized, and stored on the diskette device on available tracks in an identical manner'previously described (FIG 2A) An image file in accordance with this embodiment would be appropriately marked or tagged with the corresponding digitized audio file 56 (FIG 2A) Upon playback on a sound configured PC, both the image and the corresponding audio would then be viewed and heard simultaneously

It should be noted that a major advantage a camera in accordance with the present invention has over conventional still video cameras is that a camera according to this invention is capable of storing multiple digital images in semiconductor memory temporarily at a rapid rate while, simultaneously, the image compression processor 12, file formatter software algorithm. and disk I/O interface 13 that stores formatted files continue to function in concert together at a slower rate. This efficient design coupled with VLSI low power, high speed semiconductor memory devices (10 & 11 FIG 5A and 24 FIG 7) allows this operational capability

Like most other still video and conventional film cameras, when the "shoot" control 6 (FIG 6) is fully depressed, a control signal is generated from the digital control unit 9 that generates a trigger signal on the control panel 2 to cause a flash unit 16 (FIG 6) to irradiate a flash of light onto the subject image

During initial camera operation, the user first inserts a diskette such as a standard three and a half inch or similar storage medium Various memory diskette sizes and formats are suitable for the invention However, for the preferred embodiment either a double-density (800 Kbytes of storage) or a high-density (1 4 Mbytes of storage) diskette in a three and a half inch format which are readily available from various commercial sources such as Sony, Maxell and Verbatim The user must then select the desired PC format (IBM PC/Clone or Apple Macintosh, etc) via switch 17 (FIG 6) on the control panel 2 As shown in FIG 3., after turning on the power switch or inserting a diskette 50, the digital control unit 9 performs a self test of all internal circuitry, battery, disk drive unit, and control panel Should any failures be detected, an appropriate error indicator is illuminated on the control panel During the power-on sequence (see FIG 3 and FIG 12), the inserted diskette 50 is automatically checked for formatting consistencies in accordance with the format selected by the format switch 17 on the control panel 2 (IBM/Apple/etc) and for available storage space by checking the boot block on the diskette, a technique that will be familiar to those skilled in the art Should any inconsistencies be detected, an error indicator is illuminated on the control panel (ie, disk full, unformatted, etc) The operator frame counter display 22 (FIG 6) is then updated to show the maximum number of pictures available based upon indicated operator selections (color/black and white), diskette type (double versus high density), and capacity (partially full versus empty diskette) During operation, the operator can selectively erase a frame and record over it if desired by selecting the erase mode of operation from the control peel and toggling the forward/ reverse control

The optics for the preferred embodiment of the invention is a commercially available one-half inch (½") color CCD device having a pixel grid array of 780×488 as pictorially depicted in FIG 4 This results in 380.640 pixel elements which results in a commercially acceptable quality resolution image as will be understood by those skilled in the art In a color imaging device (CCD array) photoelectric elements, such as photodiodes, are arranged in a two dimensional array with optical filters for R (red), G (green), and B (blue) Various arrangements of optical filters are well known and the arrangement of optical filters is not limited to

a particular one with this invention During operation each pixel stores a charge corresponding to the amount of incident light The RGB components of each pixel's charge is sequentially read out via a horizontal/vertical addressing scheme that will be familiar to those skilled in the art

As shown in FIG 5A; each charge when addressed, is amplified and processed in a sample and hold (S/H) circuit 18 The analog voltage in each S/H circuit is digitized by an associated analog to digital (A/D) converter 8 The digital values are routed and collected in the pixel buffer 10 Following completion of discrete pixel element conversion and subsequent formatting in the pixel buffer which is under Control Processor Unit (CPU) 20 software control, the output of the full pixel buffer is routed to the frame buffer 11 by digital control unit 9 This process continues until a complete frame is collected within the frame buffer The general digital logic and timing and control signals for this circuitry is shown in FIG 5B The timing is provided by a master clock that is an integral part of the CPU microprocessor For example, the MOTOROLA 68040 microprocessor has a clock speed of approximately 40 Megahertz (MHZ) which results in a clock period of 25 nanoseconds (nsec) This clock pulse is used by the function and address decoder 19 (FIG 6) to generate the address and control signals shown in FIG 5B as would be understood by those skilled in the art The circuit of the present invention may be designed by one skilled in the art to function with a variety of microprocessor architectures and is not limited to any one in particular One can see from the timing chart that the S/H circuit is allowed (via the SE command) to charge to a voltage level indicative of the analog voltage impinging upon the pixel element (via the PS command) After a fixed time period, the A/D converters are enabled (via the CE command) to begin conversion of the analog voltage value on the S/H Upon completion of conversion, a conversion completion signal (CC) is generated by the A/D and routed back to the S/H circuit (via the SC command which is generated by the function and address controller 19) to discharge the stored analog voltage in anticipation of the next pixel element conversion process Next, the output of the A/D converter 8 is clocked into the pixel buffer 10 (via the PB command) When the pixel buffer 10 is full, the output is clocked out to the frame buffer 11 (via the FB command) and the pixel multiplexer address circuitry selects the next pixel for conversion Reset signals (RST) are sent to all circuit elements to allow these devices to reset prior to receiving the next analog value

Another novel concept of the present invention as illustrated in FIGS 5A and 5B utilizes a technique of paralleling the S/H and A/D devices for each pixel element thus accelerating the image signal analog-to-digital conversion process This is accomplished by eliminating the serial S/H and A/D path typical of prior art still video camera designs In addition, high-speed, low-power devices available from Sony. Burr-Brown, Datel. Analog Devices, and others facilitate the increased conversion throughput of the S/H and AID circuits with pixel conversion times of less than 150 nanoseconds (nsec) For example, Sony's video A/D converter Device part number CXA1016P/K performs up to 50 million samples per second or 20 nsec per conversion This device, or similar, may be used in the preferred embodiment of the present invention As explained previously. prior art still video camera designs multiplex each signal component into a common/singular A/D path to reduce the number of components and power consumption However. in accordance with another aspect of the present invention components such as C-MOS and ECL devices coupled with miniaturized packaging techniques such as surface mount devices (SMD) and ASIC technology make it feasible to incorporate these devices in a parallel design in order to realize a substantial increase in conversion speed with no appreciable increase in power consumption Therefore, this design approach provides significant conversion throughput increases over previous designs

The extremely high conversion speed in accordance with another concept of the present invention makes multiple high-speed camera operation possible in an alternate embodiment For example, total conversion time required for the aforementioned CCD array utilizing the circuit of the present invention (FIG. 5A) requires approximately 380, 640×150 nsec or 38 milliseconds (msec) Additional time (approximately 5 msec) is required for timing and control signal latency Thus, total conversion time for a complete image frame prior to compression processing and logging to the memory storage diskette 50 is less than fifty msec This allows for approximately 20 images to be captured in a one second period By adding additional RAM 11A (FIG 13) or other forms of commercially available random access memory to the frame buffer 11, image frames could be "pushed" onto a semiconductor memory stack for temporary storage allowing the compression processor and data interface circuitry to perform their respective functions at a slower rate. As shown in FIG 13, each unprocessed image frame would be recorded or "pulled" from the stack on a "First-In, Firs-Out" (FIFO) manner until all images in the stack queue were processed and written to the storage diskette via the disk I/O circuitry 13

As shown in FIG 6, control panel settings are monitored by the CPU 20, a microprocessor, thus allowing the appropriate timing, control, and signal processing to be effected properly The microprocessor 20 may be of the type 68040 manufactured by MOTOROLA, Intel's 80386 series, or equivalent microprocessors which specifications are commercially available and are incorporated herein by reference The microprocessor utilization of this invention, which is in the digital control unit 9, transmits commands and status to specific controls, functions, and displays in the control panel as well as receiving both circuit status/control data and operator commands through polling the operator switch settings 14A, 14B, and 17 via the bidirectional function and address decoder 19 This approach allows the user to know immediately how much storage capacity remains in the image storage diskette 50 as well as the camera's overall operational and functional status through the use of status displays 21, 22, and 23 and ongoing software self-tests running in the background as depicted in FIG 3 An example of this would be a low battery situation First, the digital control unit 9 would detect a failure in the self-test mode Next the self-test light emitting diode 21 (FIG 6) would be illuminated and an appropriate error display would be illuminated in the status display 22 thus providing the user with an exact indication of the error Another example illustrating the operation of this embedded microprocessor type of control approach is the format switch 17 (FIG 6) The position of the format switch 17 is sensed upon power application Following diskette insertion, the boot block on the diskette is compared with the format switch 17 setting (IBM/clone or Apple) and if the format does not match or if the disk 50 is unformatted, the disk format status light emitting diode 23 would be illuminated and an appropriate error display would be illuminated in the status display 22 thus prompting the user to take appropriate corrective measures

An alternate embodiment of the present invention involves adding an auxiliary I/O interface circuit or port to

the digital control unit 9 As shown if FIG 7 the auxiliary I/O port 80 connects in a manner similar to the Disk I/O interface 13 This additional I/O channel provides for external control and monitor of all timing and control signals internal to the camera In addition, it allows for the image data to be routed past or around the compression processor out to any additional internal or external device such as an optical disk storage device, digital analyzer, or other data processors that might be desired

FIG 7 shows the digital control unit 9 The microprocessor 20 architecture here is typical to one familiar with the art The frame buffer 11 (FIG 5A) receives and stores the outputs of the pixel buffer 10 until a complete frame of image data is received Then, the CPU 20, under software control, issues a control signal to the optics logic in the shutter and control circuitry 15 (FIG 6) thus resetting those functions for future image recording The full frame buffer 11, upon command from the CPU 20, transfers it's data into the compression processor 12 (FIG 2) which performs thousands of levels of parallel pipeline processing on the image data The compressed image frame is then written out to the mass memory RAM (Random Access Memory) 24 where it is temporarily stored until transferred to the disk drive assembly 5 via the disk I/O interface circuitry 13

Referring to FIG 8, a flowchart shows the steps involved in the image compression process performed by the image compression processor 12 (FIG 2) in accordance with the preferred embodiment of the present invention The output of the frame buffer 11 is transferred into the input of the image compression processor 12 under the control of the digital control unit 9 As previously described, the setting of switch 14A (FIG 6) is read by the CPU 20 (FIG 7) to determine the image resolution quality desired Depending on the operator selected setting of switch 14A, the unique digital word generated by the AND gate 60*a–b* (FIG 6A) which is activated by the selected position of switch 14A is routed to image compression processor 12 via CPU 20 (FIG 7) which selects for example a predetermined digital memory location containing the appropriate corresponding compression ratio parameters under program control The compression processor uses this command value for example to establish the size of the covariance matrix and a threshold for acceptance for the variances produced by the Discrete Cosine Transformation (DCT) transform coefficients Next, the digital image signals are converted from the RGB format previously discussed in connection with FIGS 2, 5, and 6 into luminance and chrominance signals The luminance and chrominance signals subsequently undergo a DCT The cosine transformed signals are then quantized and are then processed for Huffman coding The Huffman coded image signals are then formatted into a form that facilitates format processing into various PC compatible formats (GIFF, PICT2, etc) For a more complete understanding of the image compression process reference may be made to I E E E Catalog No EH0231-1, Library of Congress No 85-60384 published by the I E E E Society dated 1985 and incorporated herein by reference

Of the two traditional classes of image compression techniques, spatial coding and transform coding, transform coding techniques lend themselves well for this application due to computational simplicity Transform coding techniques that provide good visual fidelity include: Karhunen-Loeve transform (KLT), Fourier, cosine, sine, and Hadamard The KLT algorithm offers the best visual fidelity but suffers from serious computational complications due to extremely large matrix size Several alternate algorithms that offer reasonable visual fidelity that are computationally feasible for this invention include the Fast Fourier Transform (FFT). Discrete Cosine Transform (DCT). and Discrete Sine Transform (DST) The DCT was adopted by the JPEG as the preferred algorithm due to computational simplicity and performance

It should be noted that the Joint Photographic Experts Group (JPEG) (composed of experts from many companies including IBM, AT&T, Digital Equipment Corp, and INTEL) compression/decompression standard was developed in 1985 in response to the lack of interoperability between image and processing equipment due to numerous proprietary standards held by each manufacturer The JPEG standard provides image compression effectively up to 75 times or greater depending on the visual fidelity desired The JPEG standard is widely used in industry as an alternative to proprietary algorithms such as Intel's own proprietary standard called DVI which was initially developed by RCA before being sold to INTEL, the integrated Circuit manufacturer INTEL offers it's own firmware compression processor incorporating their DVI standard delivering compression ratios in excessive of 100:1 However, a new international standard called MPEG is due to be announced in the 1991 time frame from the JPEG arid should offer compression ratios of 275:1 and greater. In the preferred embodiment of the present invention, the JPEG standard is the preferred algorithm chosen with the incorporation of the the MPEG standard or other similar standard in the future when available commercially An alternate embodiment of the present invention would be the incorporation of various proprietary compression algorithm standards such as DVI

The compression/decompression algorithm firmware implementation of the JPEG algorithm is available commercially from various sources including C-Cube, Electronics for imaging, Storm Technology, Burr-Brown, Spectral Innovations Inc , INTEL, and others The implementation of this algorithm for the present invention may incorporate the integrated circuit set commercially available from C-Cube Their four chip ASIC JPEG algorithm implementation is performed in three basic steps: first. the image is divided into 8-by-8 pixel squares and applies a discrete cosine transform (DCT) to each square resulting in 64 frequency values; second. these frequencies are put through a quantization algorithm to eliminate unimportant frequencies; third, the remaining values are run through a Huffman coding scheme to encode the most frequently occurring values using the fewest bits A compatible software implementation of the JPEG algorithm is available commercially from Aladdin Systems, Radius Inc , Kodak, and others

Those skilled in the art will be familiar with the process and the commercially available software and firmware chipsets that are currently available on the market The present invention incorporates both available firmware chipsets in the camera and software for use in the PC for decompression The decompression algorithm can be written onto the camera's diskette 50 prior to any image data recording This allows the PC user to take the diskette 50 to a PC and directly incorporate the image data because the image file selected by the user is automatically decompressed transparent to the user The algorithm can be written onto an unused track 52 or sector combination on the diskette as shown on FIG 2A Alternatively, the decompression algorithm can be loaded onto a PC before inserting a diskette 50 containing compressed image data In the latter embodiment the resolution and mode values 54 and 55 (FIG 2A) for each representative image would be read from diskette 50 in order to appropriately control the selection and activation of the appropriate corresponding decompression algorithm

As shown in FIG 7, the output of the image compression processor 12 is routed to the RAM memory 24 where the compressed image is formatted for either the PICT II or GIFF format depending on the setting of format switch 17 (FIG 6) It should be noted that a large number of image formats for PCs exist PICT and GIFF are the most common for the Apple and IBM PC s and are therefore the preferred formats for the present invention although other formats can be easily incorporated into the design by changing the software format routines These software image formats are commercially available from many sources most notably Apple computers for PICT and IBM for GIFF An example of the PICT format is pictorially shown in FIG 6B as will be familiar to those skilled in the computer arts Once formatting is complete, the formatted image data is transferred to the disk I/O interface 13 for transfer to the magnetic recording diskette 50

FIG 9 and FIG 10 illustrate the preferred embodiment of the video format translator device in accordance with another aspect of this invention that converts other still video camera formats for example on two inch video diskette to this invention's selectable PC compatible digital format The general concept of operation is shown in FIG 10 In FIG 9 correspond parts and subassemblies in translator 40 are shown with like numbers corresponding to FIGS 2 and 6 having a 40 hyphenation prefix designation and such parts and subassemblies perform similar functions to those described above with reference to FIGS 2 and 6 Referring again to FIG 9, the translator 40 incorporates the same components utilized in the digital circuit card assembly which houses both the digital control unit 9 and optics processing circuits (pixel multiplexer 7. A/D 8. etc 10–13) The major difference is that the CCD array 1 is replaced with an input disk drive 25, for example a two inch (2") video disk drive assembly, and an NTSC video format decoder 26 which converts the composite video signal to an RGB format for processing as described previously

FIG 11 displays an alternate embodiment of the video format translator device 40 of the present invention that shows optional inputs 27 and outputs 28 and 29 The exact same circuitry is utilized that was used for the translator device 40 as shown in FIG 9 except that inputs 27 for either an NTSC/PAL format or RGB format video signal is provided This allows video signals from other sources such as a cable TV, CAMCORDER, or other video signal source to be digitized and archived in a PC compatible format Also, provisions for video output jacks 28 are made to allow either viewing of the image/video source prior to or during image recording Finally provisions are made to provide a data output 29 to allow connection to other PC peripherals such as a communications modem, larger/smaller disk drive assembly, optical disk, specialty display or signal processor/analyzer Either a standard serial, parallel, or Small Computer Standard Interface (SCSI) data port can be readily connected to the auxiliary I/O interface 80

FIG 12 depicts an alternate feature of an embodiment of the present invention that shows how an inserted diskette 50 that is either unformatted or formatted for a undesired (e g , not corresponding to the setting of switch 17-FIG 6) PC configuration would be automatically properly formatted for use with a camera in accordance with another aspect of this invention This capability allows the user of this invention to forego the requirement to pre-format the storage medium (diskette) on a PC prior to using it in the camera operated in accordance with the present invention With reference to FIG 3 the power-on sequence process would result in an abnormal diskette format error if the format of an inserted diskette 50 did not correspond to the operator selected format switch 17 (FIG 6) In accordance with the automatic diskette format option, CPU 20 of digital control unit 9 in response to the abnormal diskette format error would initiate the diskette format process illustrated in FIG 12 Upon completion of the diskette format process illustrated in FIG 12, the power-on sequence illustrated in FIG 3 would continue from step B

Referring now to FIG 14A, there is shown a schematic block diagram of the format selection logic in accordance with another aspect of the present invention During the power-on sequence as described in connection with FIGS 3 and 12. processor 20 of control unit 9 initiates a format selection switch sample and test routine as more fully described in the flow diagram illustrated in FIG 14B Switch 17 is illustrated in FIG 14A in the Apple PC position and logic level v1 is applied as inputs to logic gates 60c and 60*d* As illustrated in FIG 2A, the format signals 57 for the Apple PC format is a logic "zero" and conversely the format signal or tag 57 if the format switch 17 were in the IBM PC or other computer type position would be a logic "one" and "two" respectively In response to the logic "zero" indicating Apple PC format. processor 20 accesses a unique memory location XY of format memory 20-2 which for example may comprise any random access memory with two megabytes storage capacity The data format for the operator selectable predetermined number of computer architectures, similar in content and arrangement to those illustrated in FIG 6B for an Apple PC would be stored in memory 20-2 which would be addressed in response to the other operator selectable position of switch 17 to generate the other unique codes 57 as shown in FIG 2A Processor 20 in response to a stored format subroutine more particularly shown in FIG 14B contains the allocation of data memory addresses in disk input/output interface unit 13 in accordance with the picture image file format as illustrated in FIG 6B Thus the digital video data information signals generated by compression processor 12 are appropriately formatted and stored in memory storage disk drive 5 to insure compatibility with the format selected by the operator by selectively positioning switch 17

Those skilled in the art will recognize the many alterations, additions or changes of the preferred embodiment may be made without departing from the scope of the following claims

What is claimed is:

1 A digital camera for taking pictures and storing them in a removable storage device in the camera, said digital camera apparatus comprising:

an image pick-up unit for generating and outputting a digital image signal photoelectrically converted from an image incident thereon, and

a digital control unit for formatting said digital image signal in one of a plurality of computer formats

* * * * *

EXHIBIT E

US006323899B1

(12) **United States Patent**
Roberts et al.

(10) Patent No.: US 6,323,899 B1
(45) Date of Patent: *Nov. 27, 2001

(54) PROCESS FOR USE IN ELECTRONIC CAMERA

(75) Inventors: Marc K. Roberts, Burke; Matthew A. Chikosky, Springfield; Jerry A. Speasl, Vienna, all of VA (US)

(73) Assignee: St. Clair Intellectual Property Consultants, Inc., Grosse Pointe, MI (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days

This patent is subject to a terminal disclaimer

(21) Appl. No.: 09/541,285

(22) Filed: Apr. 3, 2000

Related U.S. Application Data

(63) Continuation of application No. 08/651,562, filed on May 22, 1996, now Pat. No. 6,094,219, which is a continuation of application No. 08/098,787, filed on Jul. 29, 1993, now Pat. No. 5,576,757, which is a continuation of application No. 07/878,603, filed on May 5, 1992, now abandoned, which is a continuation of application No. 07/615,848, filed on Nov. 20, 1990, now Pat. No. 5,138,459

(51) Int. Cl.[7] H04N 5/225

(52) U.S. Cl. 348/220; 348/231; 348/207

(58) Field of Search 348/207, 220, 348/221, 222, 230, 232, 233, 239, 231, 552; 358/909, 906.1; H04N 5/225

(56) References Cited

U.S. PATENT DOCUMENTS

4,758,883	*	7/1988	Kawahara et al	348/222
5,016,107	*	5/1991	Sasson et al	348/231
5,034,804	*	7/1991	Sasaki et al	348/232
5,153,730	*	10/1992	Nagasaki et al	348/231
5,764,286		6/1998	Kawamura et al	348/232

FOREIGN PATENT DOCUMENTS

1-114286	5/1989	(JP)
1-248785	10/1989	(JP)
2-140874	6/1990	(JP)
2-202782	8/1990	(JP)
2-208779	8/1990	(JP)
2-222385	9/1990	(JP)
2-257780	10/1990	(JP)

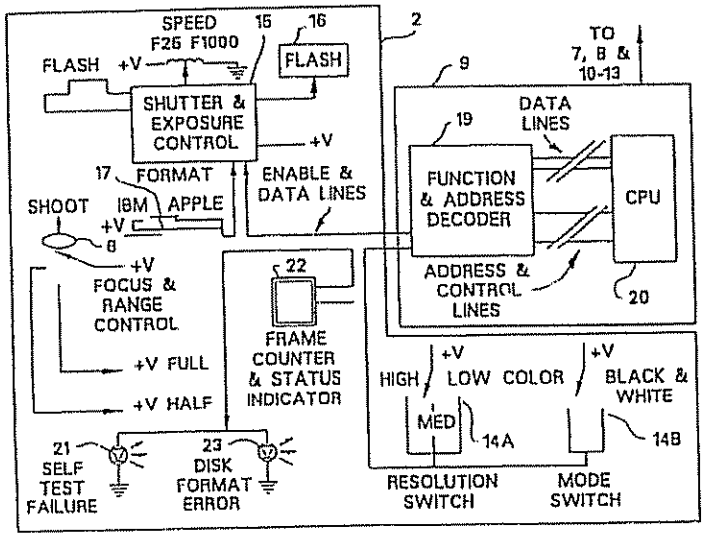
* cited by examiner

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(74) *Attorney, Agent, or Firm*—Harness, Dickey & Pierce, P.L.C.

(57) ABSTRACT

A process for use in an electronic camera generates a digital image signal corresponding to an image incident on an image pick-up unit of the camera, formats the digital image signal in one of a plurality of computer image file formats and stores the formatted image file in a storage device of the camera

4 Claims, 11 Drawing Sheets



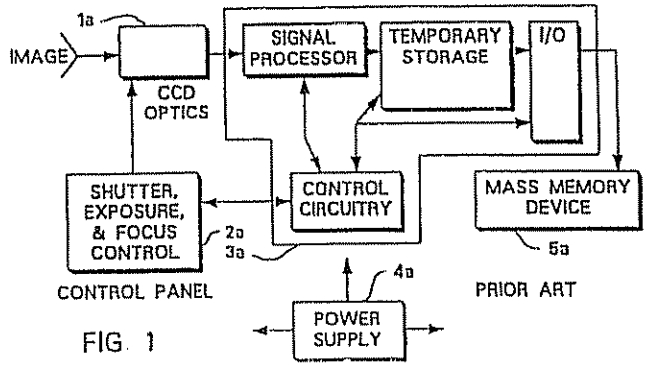

1a
IMAGE
CCD OPTICS
SIGNAL PROCESSOR
TEMPORARY STORAGE
I/O
SHUTTER, EXPOSURE, & FOCUS CONTROL
2a
3a
CONTROL CIRCUITRY
MASS MEMORY DEVICE
5a
CONTROL PANEL
4a
POWER SUPPLY
PRIOR ART

FIG. 1

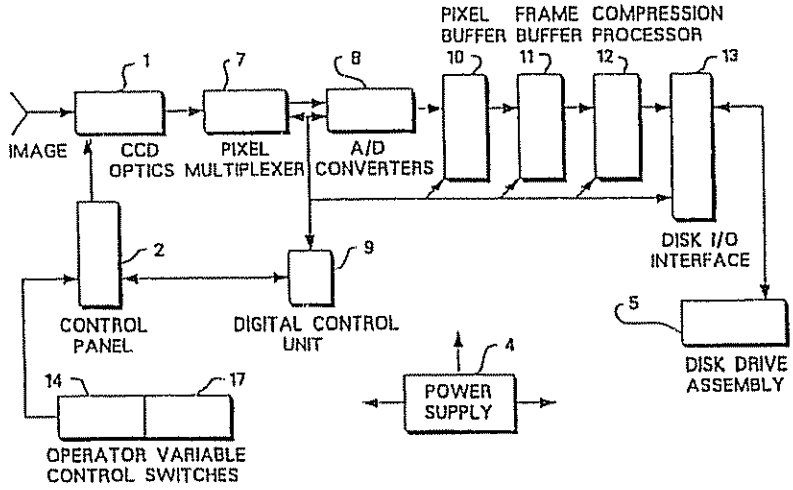

PIXEL BUFFER
FRAME BUFFER
COMPRESSION PROCESSOR
1
7
8
10
11
12
13
IMAGE
CCD OPTICS
PIXEL MULTIPLEXER
A/D CONVERTERS
DISK I/O INTERFACE
2
9
5
CONTROL PANEL
DIGITAL CONTROL UNIT
DISK DRIVE ASSEMBLY
4
14
17
POWER SUPPLY
OPERATOR VARIABLE CONTROL SWITCHES

FIG. 2

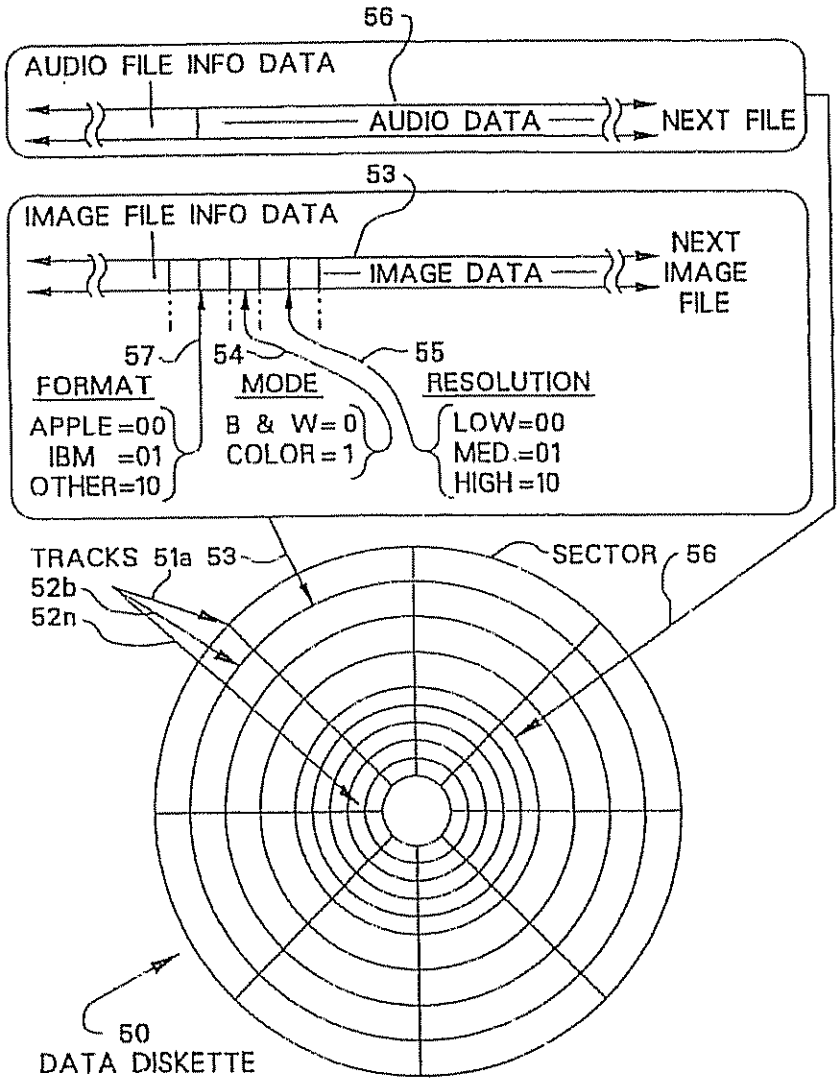

56
AUDIO FILE INFO DATA
AUDIO DATA
NEXT FILE
53
IMAGE FILE INFO DATA
IMAGE DATA
NEXT IMAGE FILE
57
54
55
FORMAT
MODE
RESOLUTION
APPLE=00
IBM =01
OTHER=10
B & W=0
COLOR=1
LOW=00
MED.=01
HIGH=10
TRACKS 51a 53
52b
52n
SECTOR 56
50
DATA DISKETTE

FIG. 2A

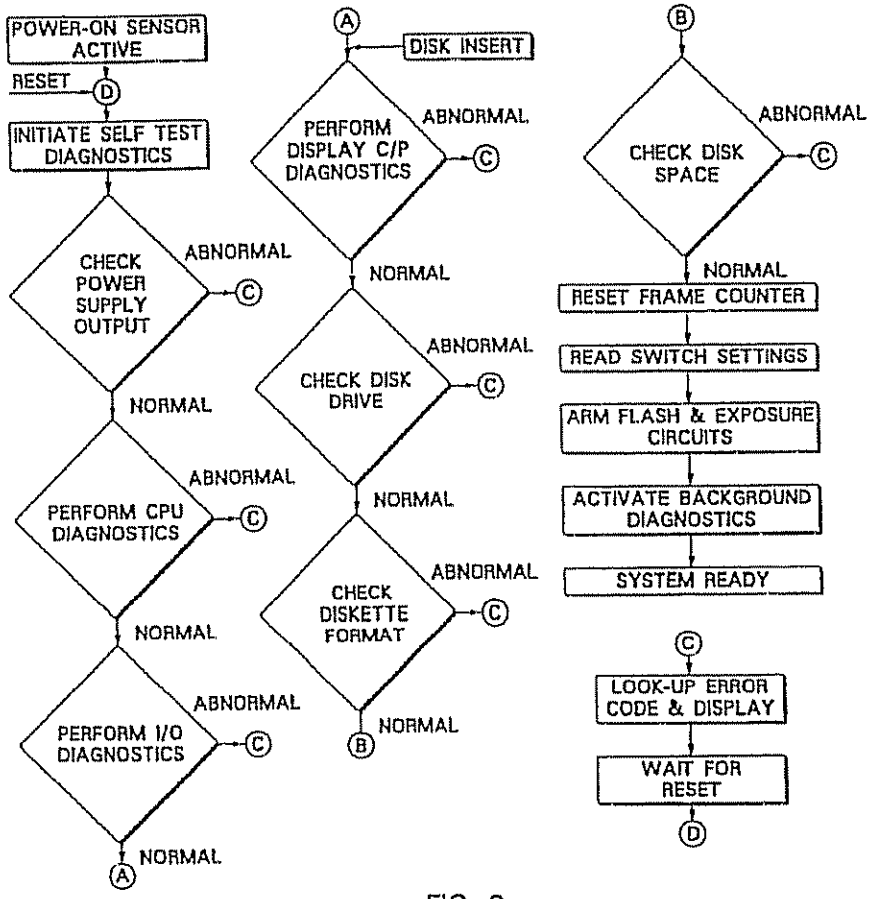
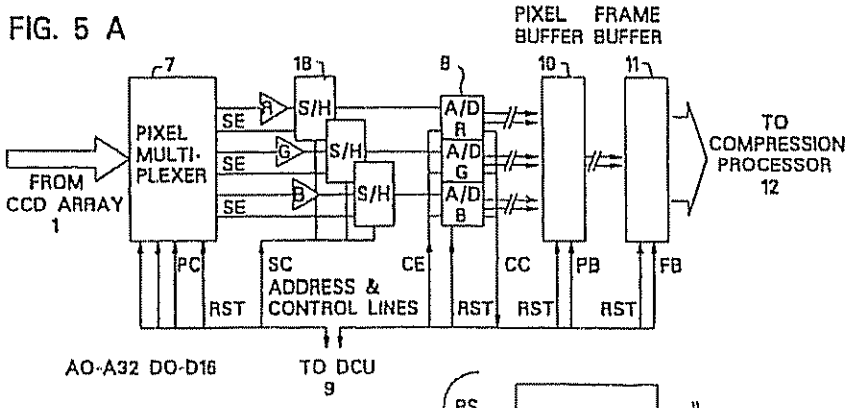

POWER-ON SENSOR ACTIVE
RESET
D
INITIATE SELF TEST DIAGNOSTICS
CHECK POWER SUPPLY OUTPUT
ABNORMAL
C
NORMAL
PERFORM CPU DIAGNOSTICS
ABNORMAL
C
NORMAL
PERFORM I/O DIAGNOSTICS
ABNORMAL
C
NORMAL
A
A
DISK INSERT
PERFORM DISPLAY C/P DIAGNOSTICS
ABNORMAL
C
NORMAL
CHECK DISK DRIVE
ABNORMAL
C
NORMAL
CHECK DISKETTE FORMAT
ABNORMAL
C
NORMAL
B
B
CHECK DISK SPACE
ABNORMAL
C
NORMAL
RESET FRAME COUNTER
READ SWITCH SETTINGS
ARM FLASH & EXPOSURE CIRCUITS
ACTIVATE BACKGROUND DIAGNOSTICS
SYSTEM READY
C
LOOK-UP ERROR CODE & DISPLAY
WAIT FOR RESET
D

FIG. 3

FIG. 5 A



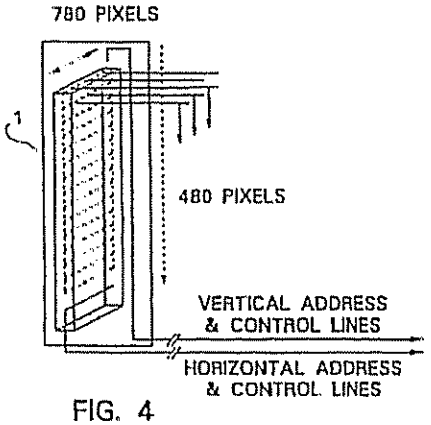


FIG. 4

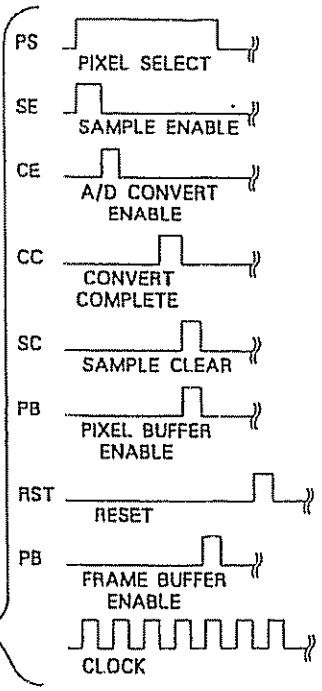


FIG. 5B

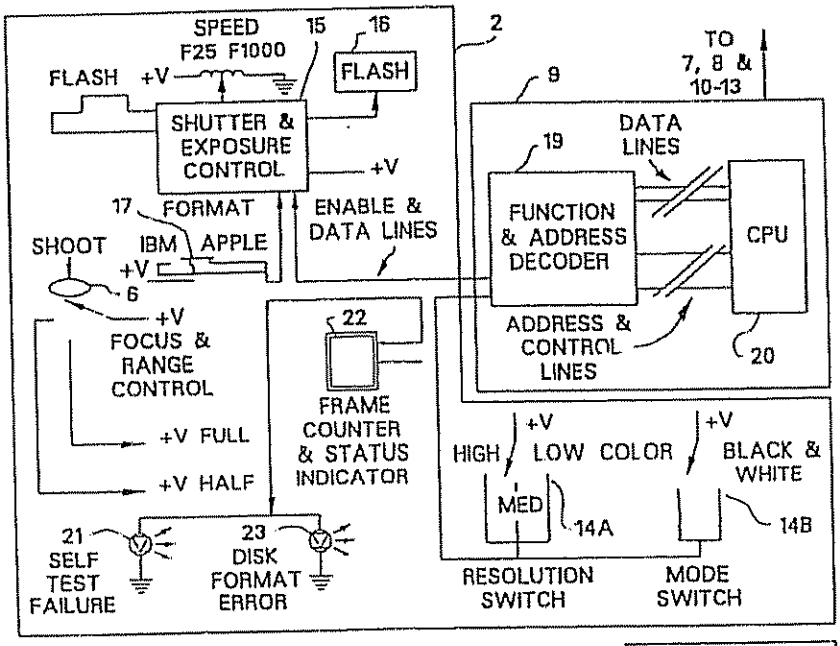


FIG. 6

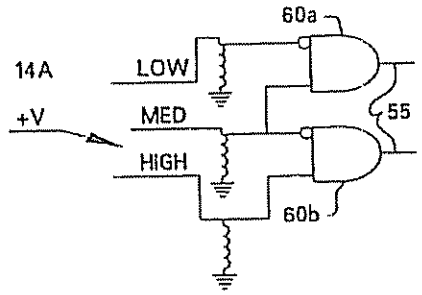


FIG. 6A

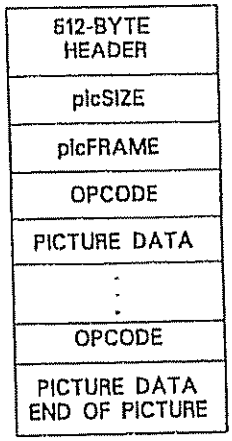


FIG.6B

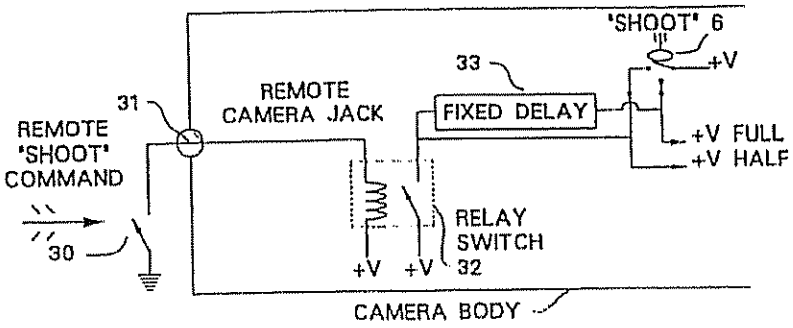

'SHOOT' 6
+V
33
31
REMOTE CAMERA JACK
FIXED DELAY
REMOTE 'SHOOT' COMMAND
+V FULL
+V HALF
RELAY SWITCH
30
+V +V
32
CAMERA BODY

FIG. 6C

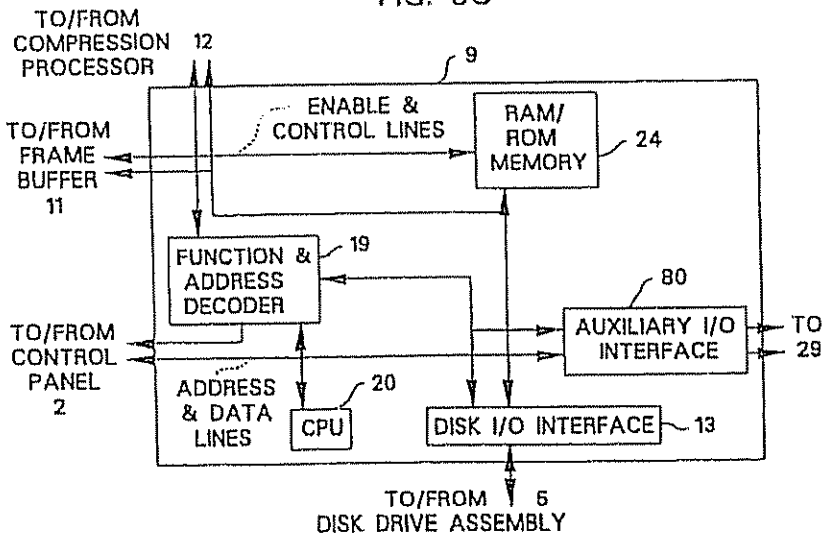

TO/FROM COMPRESSION PROCESSOR
12
9
ENABLE & CONTROL LINES
RAM/ ROM MEMORY
24
TO/FROM FRAME BUFFER 11
FUNCTION & ADDRESS DECODER
19
80
AUXILIARY I/O INTERFACE
TO 29
TO/FROM CONTROL PANEL 2
ADDRESS & DATA LINES
20
CPU
DISK I/O INTERFACE
13
TO/FROM 6 DISK DRIVE ASSEMBLY

FIG. 7

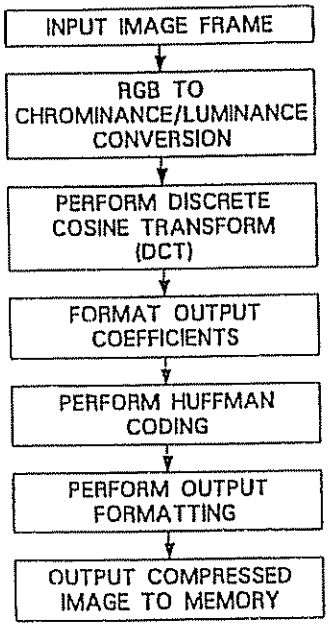


FIG. 8

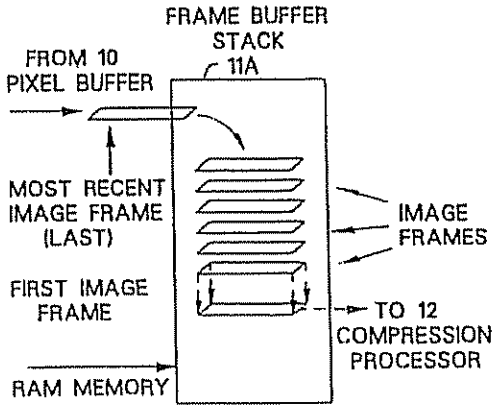


FIG. 13

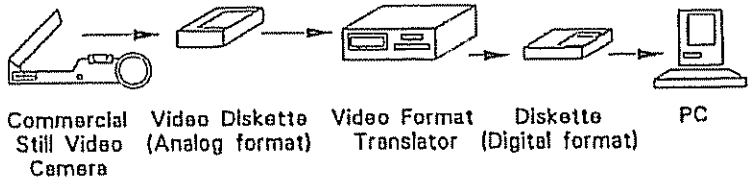


FIG. 10

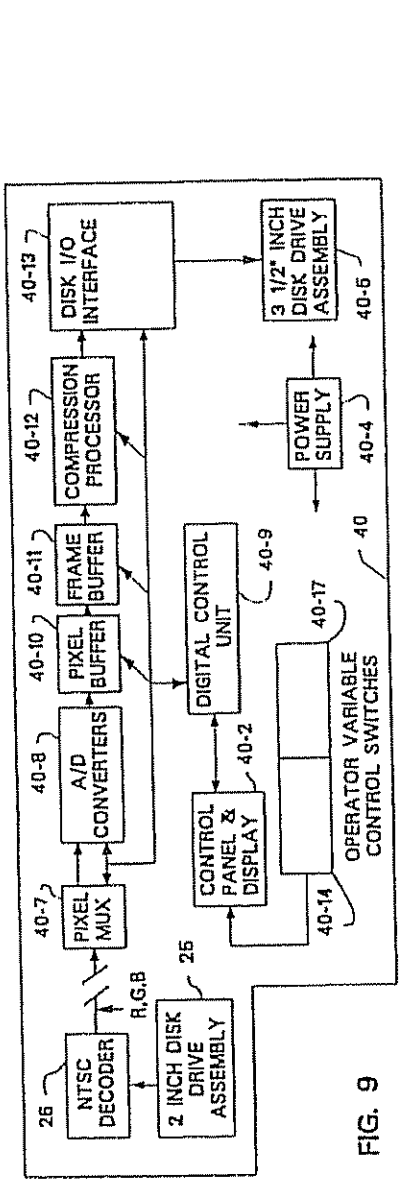

26
NTSC DECODER
R,G,B
25
2 INCH DISK DRIVE ASSEMBLY
40-7
PIXEL MUX
40-8
A/D CONVERTERS
40-10
PIXEL BUFFER
40-11
FRAME BUFFER
40-12
COMPRESSION PROCESSOR
40-13
DISK I/O INTERFACE
CONTROL PANEL & DISPLAY
40-2
DIGITAL CONTROL UNIT
40-9
40-17
OPERATOR VARIABLE CONTROL SWITCHES
40-14
40
POWER SUPPLY
40-4
3 1/2" INCH DISK DRIVE ASSEMBLY
40-6

FIG. 9

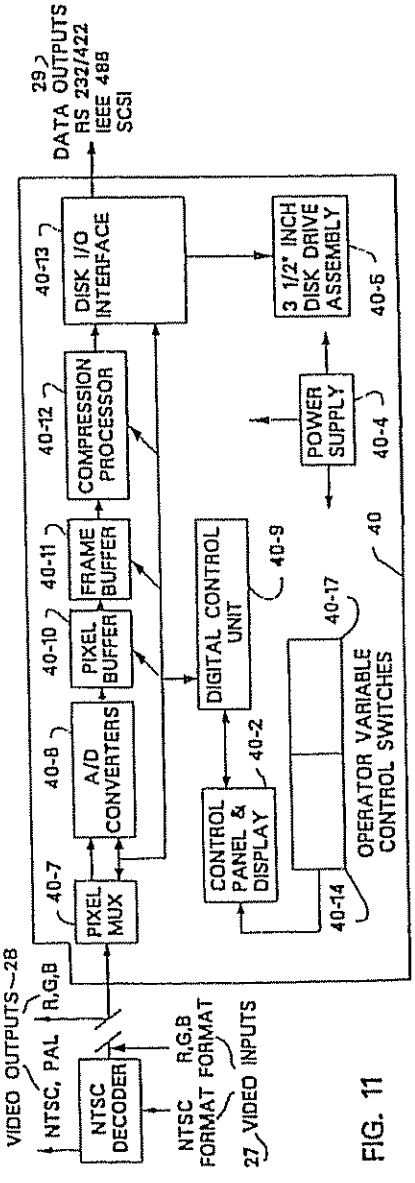

29
DATA OUTPUTS RS 232/422 IEEE 488 SCSI
VIDEO OUTPUTS
28
NTSC, PAL
R,G,B
NTSC DECODER
NTSC FORMAT
R,G,B
27
VIDEO INPUTS
40-7
PIXEL MUX
40-8
A/D CONVERTERS
40-10
PIXEL BUFFER
40-11
FRAME BUFFER
40-12
COMPRESSION PROCESSOR
40-13
DISK I/O INTERFACE
CONTROL PANEL & DISPLAY
40-2
DIGITAL CONTROL UNIT
40-9
40-17
OPERATOR VARIABLE CONTROL SWITCHES
40-14
40
POWER SUPPLY
40-4
3 1/2" INCH DISK DRIVE ASSEMBLY
40-6

FIG. 11

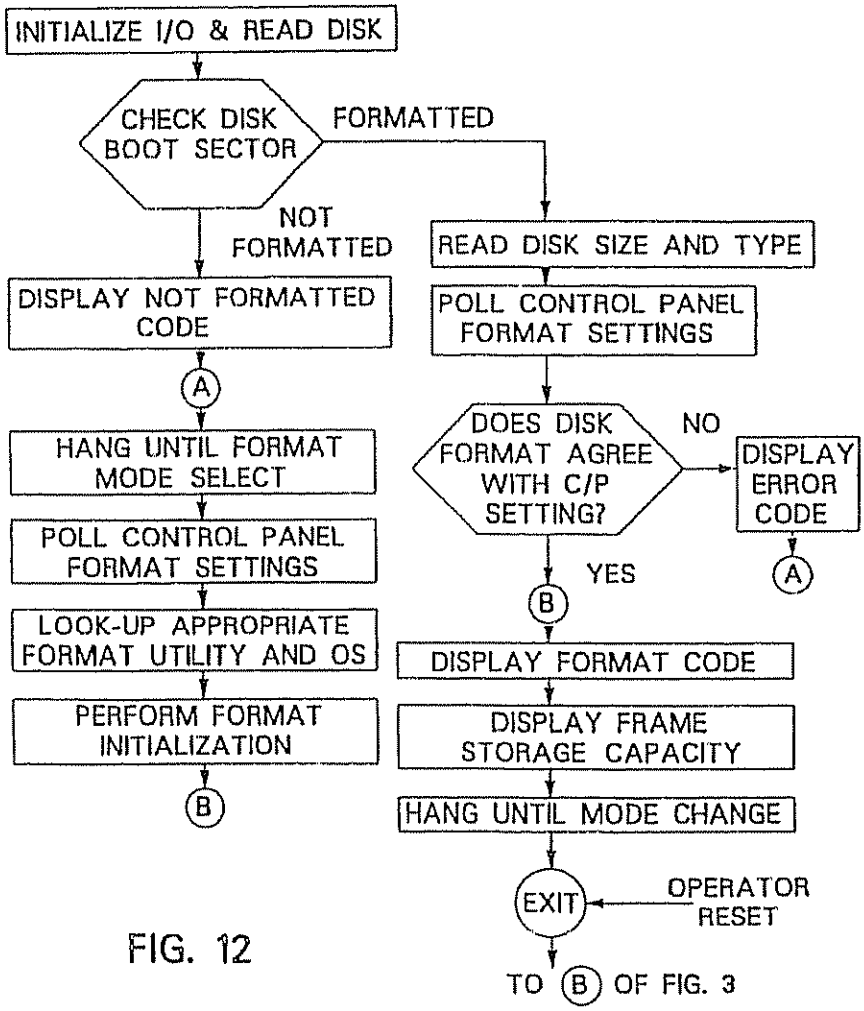

INITIALIZE I/O & READ DISK
CHECK DISK BOOT SECTOR
FORMATTED
NOT FORMATTED
DISPLAY NOT FORMATTED CODE
A
HANG UNTIL FORMAT MODE SELECT
POLL CONTROL PANEL FORMAT SETTINGS
LOOK-UP APPROPRIATE FORMAT UTILITY AND OS
PERFORM FORMAT INITIALIZATION
B
READ DISK SIZE AND TYPE
POLL CONTROL PANEL FORMAT SETTINGS
DOES DISK FORMAT AGREE WITH C/P SETTING?
NO
DISPLAY ERROR CODE
A
YES
B
DISPLAY FORMAT CODE
DISPLAY FRAME STORAGE CAPACITY
HANG UNTIL MODE CHANGE
EXIT
OPERATOR RESET
TO B OF FIG. 3

FIG. 12

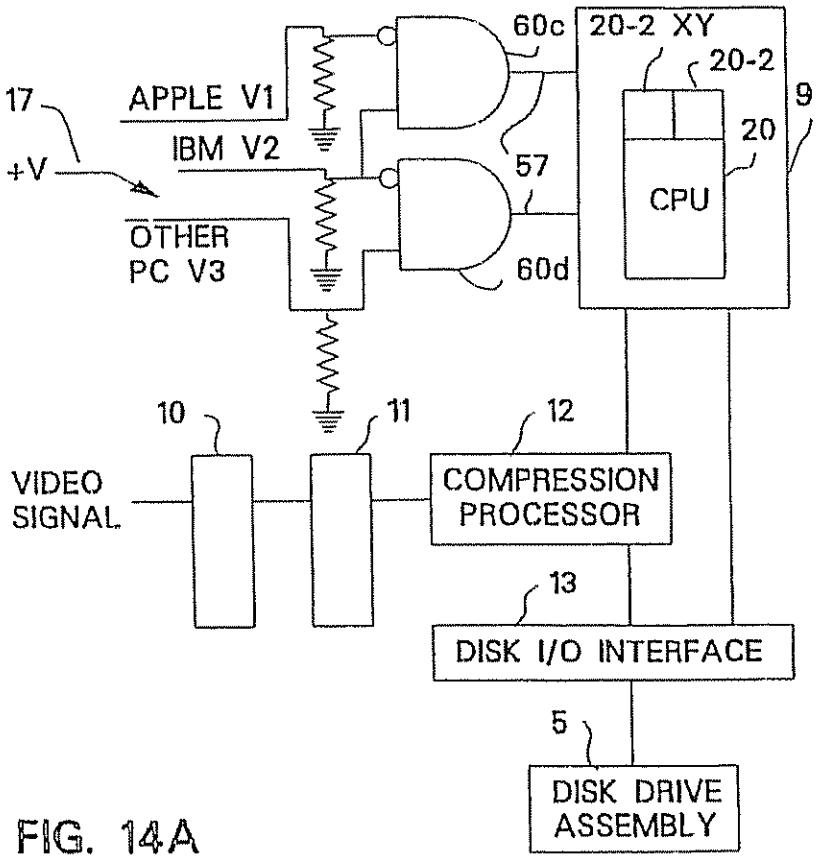

17
+V
APPLE V1
IBM V2
OTHER
PC V3
60c
57
60d
20-2 XY
20-2
20
CPU
9
10
11
12
VIDEO
SIGNAL
COMPRESSION
PROCESSOR
13
DISK I/O INTERFACE
5
DISK DRIVE
ASSEMBLY

FIG. 14A

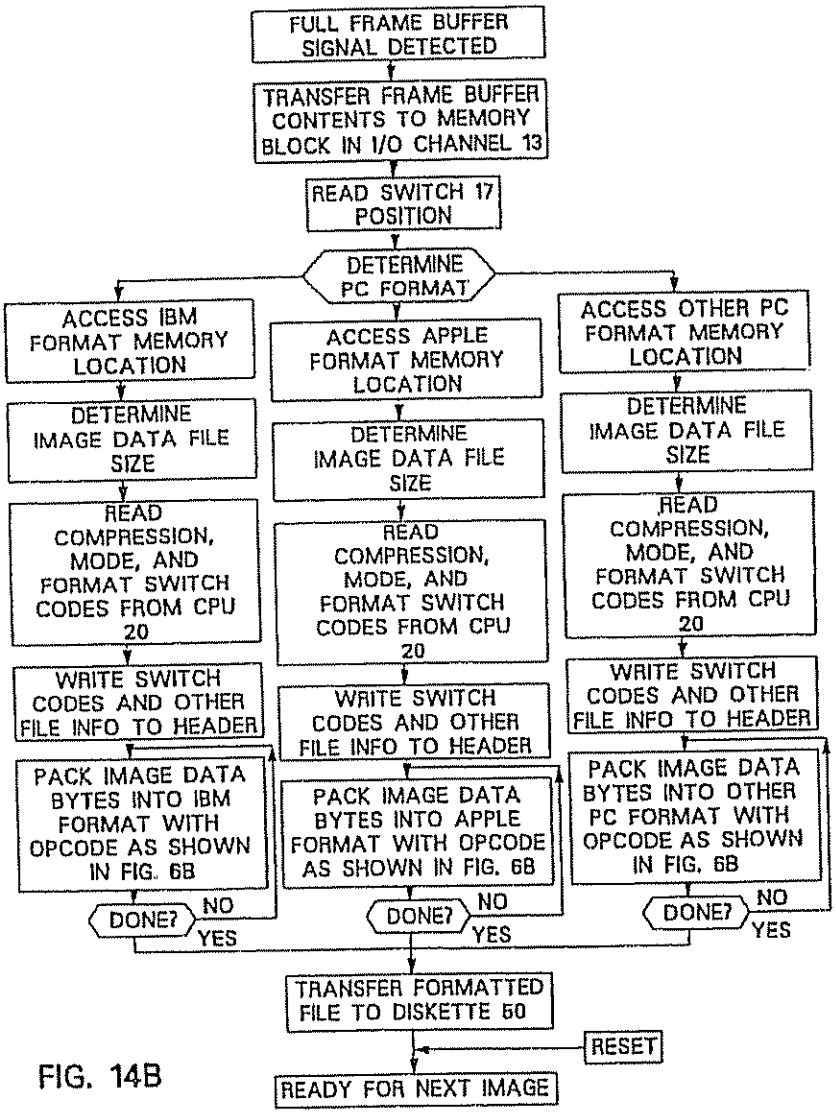

FULL FRAME BUFFER SIGNAL DETECTED
TRANSFER FRAME BUFFER CONTENTS TO MEMORY BLOCK IN I/O CHANNEL 13
READ SWITCH 17 POSITION
DETERMINE PC FORMAT
ACCESS IBM FORMAT MEMORY LOCATION
ACCESS APPLE FORMAT MEMORY LOCATION
ACCESS OTHER PC FORMAT MEMORY LOCATION
DETERMINE IMAGE DATA FILE SIZE
DETERMINE IMAGE DATA FILE SIZE
DETERMINE IMAGE DATA FILE SIZE
READ COMPRESSION, MODE, AND FORMAT SWITCH CODES FROM CPU 20
READ COMPRESSION, MODE, AND FORMAT SWITCH CODES FROM CPU 20
READ COMPRESSION, MODE, AND FORMAT SWITCH CODES FROM CPU 20
WRITE SWITCH CODES AND OTHER FILE INFO TO HEADER
WRITE SWITCH CODES AND OTHER FILE INFO TO HEADER
WRITE SWITCH CODES AND OTHER FILE INFO TO HEADER
PACK IMAGE DATA BYTES INTO IBM FORMAT WITH OPCODE AS SHOWN IN FIG. 6B
PACK IMAGE DATA BYTES INTO APPLE FORMAT WITH OPCODE AS SHOWN IN FIG. 6B
PACK IMAGE DATA BYTES INTO OTHER PC FORMAT WITH OPCODE AS SHOWN IN FIG. 6B
DONE?
NO
YES
DONE?
NO
YES
DONE?
NO
YES
TRANSFER FORMATTED FILE TO DISKETTE 50
RESET
READY FOR NEXT IMAGE

FIG. 14B

PROCESS FOR USE IN ELECTRONIC CAMERA

This is a continuation of U.S. patent application Ser No 08/651,562, filed May 22, 1996, U.S Pat No. 6,094,219, which is a continuation of U.S. patent application Ser. No. 08/098,787 filed Jul 29, 1993 U S Pat No 5,576,757 which is a continuation of U S patent application Ser No 07/878,603, filed May 5, 1992, now abandoned, which is a continuation of U.S patent application Ser No 07/615,848, filed Nov 20, 1990 and now U S Pat No 5,138,459

BACKGROUND OF THE INVENTION

1 Field of the Invention

This invention generally relates to an electronic still video camera and in particular to an improved electronic still camera which converts a still picture of an object or scene into an operator selectable compressed digital signal format for storage utilizing a compression/decompression algorithm, such as the Joint Photographic Experts Group (JPEG) algorithm standard for example, formatted into Personal Computer (PC) compatible format retaining the images' color information, and stored on a PC compatible memory diskette For example, the diskette can be a three and a half (3½) inch digital diskette The digital diskette is removeable from the electronic camera for direct insertion into a PC which contains the previously loaded corresponding decompression algorithm whereby the digital image is in a format compatible for immediate use with word processing, desk top publishing, data base and multi-media applications

2 Description of the Prior Art

FIG 1 is a schematic block diagram showing structure of a conventional prior art electronic still camera system, in which a CCD image sensor element 1*a* converts a still image of an object into an analog color video signal when the shutter control circuitry 2*a* is activated. The output color video signal of the image sensor element is then routed to the signal processing subsystem 3*a* where the signal is converted to National Television System Committee (NTSC) or other composite video formats (such as the European video standard Phase Alternating Line-PAL) and logged in analog format onto a mass memory storage device such as an analog video floppy disk, Electrically Erasable Programmable Read Only Memory (EEPROM), analog audio cassette, bubble memory, or other storage device 5*a* Power is supplied by a rechargeable/removeable battery system 4*a*

An electronic camera that converts an image into electronic image signals and transferred to a memory storage device is disclosed in the following: U S Pat. Nos 4,131,919; 4,456 931; 4,758,883; 4,803.554; and 4,837, 628

Conventional prior art electronic still cameras, for example of the types disclosed in the aforementioned references, produce an electronic signal corresponding to a desired image in analog format such as the National Television System Committee (NTSC) or similar on magnetic or electronic storage media for either permanent or temporary storage to facilitate viewing on a television or video monitor With the current state of the art, it is expensive and time consuming to convert the analog image equivalent to a digital format for direct utilization with PC software applications Currently, to convert an image captured on an electronic still camera to a PC compatible format one must convert the signal back to either a composite NTSC or RGB video signal and use a conversion device such as a "frame grabber" (a digital circuit board installed into PCs that convert video images into PC compatible formats) of the type sold commercially by Aapps Corporation, Orange Micro, RasterOps, and others or convert the image to a hard-copy print (a photograph) and utilize an electronic "scanner", a piece of equipment that connects to a PC, which converts an image into a digital format The later technique is employed extensively within the desktop publishing industry

SUMMARY OF THE INVENTION

It is the object of this invention to provide an improved electronic still camera with operator selectable picture compression in one of a plurality of operator selectable digital data formats recordable on a standard removeable magnetic diskette common to personal computers

It is a further object of this invention to provide an improved electronic still camera that provides digital image files for immediate and direct incorporation into popular word processing, desktop publishing, and other software programs on PCs

It is another object of this invention is to provide an improved electronic still camera that under user selection, can record and store still images selectively compressed in a directly insertable digital memory storage device into a PC in either color or black and white formats thus facilitating storage of a large number of images with the signal flag indicating the degree of compression selected by the operator as well as the color/black and white mode selection being stored as digital values on the digital memory storage device with each image frame

An additional object of this invention to provide an electronic still camera device that can rapidly capture a series of images automatically as well as singularly Also, this camera provides multiple outputs in both video format for monitor and display of images and digital formats to facilitate data transmission, additional processing, or storage to a variety of storage media

It is still another object of this invention is to provide a more efficient electronic still camera that can take a still picture with operator selectable high, medium, or low resolution in either color or black and white by electronic shutter and exposure control by utilizing a variety of electro-optical sensors including Charge Coupled Devices (CCD), Infrared (IR), and Ultra Violet (UV) which can be directly or remotely controlled by analog, digital, or radio frequency (RF) control signals

A further object of this invention is to provide a programmable video picture translator device for efficiently converting electronic still images in analog composite video format into digital data format readable by a PC This translator device also provides additional video inputs and outputs for capturing video images, monitoring video images on monitors and displays, and can transmit either compressed or unprocessed digital image data through a variety of output I/O channels in various formats such as serial, parallel, etc Also, this invention can incorporate sound/voice with images thru additional interface circuitry and audio digitizers

Finally, it is the object of this invention to provide an electronic still camera that is efficient in design and permits extended periods of portable operation and which provides the user with operational status through the use of continuous internal self-test software routines and operator displays

BRIEF DESCRIPTION OF THE DRAWINGS

FIG 1 is a schematic block diagram of a conventional prior art electronic still camera

FIG 2 is a schematic block diagram of the of the overall structure of an electronic still camera embodying the present invention

FIG 2A is an illustration showing one embodiment of an audio data file, data format flag, compression level, and color/black and white mode selection values stored on a digital memory diskette storage device

FIG 3 is a flowchart showing the power-up and continuous self-test sequence in accordance with one aspect of the present invention

FIG 4 is an example of a ½" CCD array utilizable in accordance with one aspect of the present invention

FIG 5A is a schematic block diagram showing the image signal to digital signal conversion logic in accordance with one aspect of the present invention

FIG. 5B is a logic and timing diagram for the image signal to digital signal conversion logic in accordance with one aspect of the present invention

FIG 6 is an example of the control panel logic in accordance with one aspect of the present invention

FIG 6A is an example of one embodiment of switch logic of the control panel switches and controls utilizable in accordance with one aspect of the present invention

FIG 6B is an example of the PICT image file format based upon the published standard provided by Apple Computer, Inc

FIG 6C is an alternate embodiment of the current invention embodying remote operation

FIG 7 is a simplified block diagram of the digital control unit in accordance with one aspect of the present invention

FIG 8 is a flowchart showing the steps of the image compression algorithm in accordance with one aspect of the present invention.

FIG 9 is a block diagram of a video format translator device in accordance with one aspect of the present invention

FIG 10 is a block diagram illustrating the operation of a translator device in accordance with one aspect of the present invention

FIG 11 is an alternative embodiment of the video format translator in accordance with another aspect of the present invention showing additional video inputs and data outputs

FIG 12 is an alternate embodiment of the invention showing an optional diskette format utility flowchart

FIG 13 is an alternate embodiment of a frame buffer utilizable in accordance with another aspect of the present invention showing a frame buffer stack permitting multiple shot mode

FIG 14A is a block diagram of an embodiment of the format select logic in accordance with one aspect of the present invention

FIG 14B is a flow diagram illustrating the steps of the format selection logic operations

DESCRIPTION OF THE PREFERRED EMBODIMENT

FIG 2 is a schematic block diagram of the preferred embodiment of an electronic still camera in accordance with the principals of the invention Referring to FIG 2, an image optical pick-up element 1, which for example could be a Charge Coupled Device (CCD) (or an Infrared (IR) or Ultraviolet (UV) sensor), converts a still image of an object into an electric signal when a picture "shoot" command is initiated by the operator via control panel 2 When taking a picture, focusing and shutter speed are controlled by a lens system and shutter speed selection mechanism under control of the digital control unit 9 The camera, like other still video cameras, employs an electronic shutter system that controls a charge storage time in a CCD array onto which an image of an object is focused through the lens system

When the "shoot" control 6 is half depressed (see FIG 6), a power supply voltage is supplied from the rechargeable batteries 4 to the electronic circuits and digital control unit 9, control panel 2, and the disk drive assembly 5 The exposure control circuitry not shown generates appropriate horizontal and vertical transfer pulses as well as field shift pulses under control of the reference clock timing and control signals provided by the digital control unit 9 type for driving the CCD device and pre-processing circuitry This design may be of any type well known in the art for example those cited in U S Pat Nos 4,131,919 and 4,456,931 and any similar designs well known in the prior art

An alternate embodiment of the present invention that provides remote operation of the camera is shown in FIG 6C When remote "Shoot" control 30 is activated by any means for example manually, or by radiant, or electronic energy, a control signal is generated and routed through the external jack 31, located on the external camera body The external control 30 is electrically connected to the external jack 31 by a twisted-pair conductive cable assembly that is familiar to those skilled in the art Upon receipt of the externally generated "shoot" command, the relay switch 32 is activated and provides internal switch closure This closure of switch 32 then initiates the process previously described and provides the half V+ voltage previously described The full V+ is provided via the fixed delay 33, the value chosen to allow the diskette drive assembly 5 (FIG 2) and associated control circuitry to initialize prior to receiving image data

When the 'shoot' control is fully depressed in either embodiment, the shutter controller 15 (FIG. 6) generates a shutter pulse that generates control signals for the A/D converters 8 allowing the image/picture data signal in the sample and hold circuitry of the pixel multiplexer 7 to be converted into a digital signal Control and address instructions of the type well known in the art are generated from the digital control unit 9 to facilitate the storage of the digital image data within the pixel buffer 10 and frame buffer 11 Upon completion of image conversion, the contents of the frame buffer are transferred to the compression processor 12 which for example may be of the many versions currently offered commercially such as C-Cube's (San Jose, Calif.) four chip Application Specific Integrated Circuit (ASIC) set In the compression processor 12, the Joint Photographic Experts Group (JPEG), a part of the International Standards Organization (ISO) which is a subset of the International Telegraph and Telephone Committee (CCITT), image compression algorithm fully described in Report # JTC1/SC2/WG8 dated 1985 is performed under control of the digital control unit 9 to compress the size of the image A variable selectable compression ratio of up to 50:1 is performed on the digital image frame Other compression ratios are operator selectable via the control panel 2 switches 14A and 14B (FIG 6) The compressed digital frame is then formatted into either an IBM PC/Clone (such as GIFF) or Apple Macintosh (such as PICT II) image file format depending on the setting selected by the operator for a user switch 17 (FIG 6) position on the control panel 2 After formatting, the file is written into a temporary memory buffer within the disk input/output (I/O) interface circuit 13 which, under the

command of the digital control unit 9, controls the high density (1 4 Mbyte storage capacity) disk drive unit 5 Following file transfer to the diskette e g , the frame counter display 22 on the control panel 2 is updated by appropriate control signals and the camera is ready to undergo the same procedure for the next image Power to the electronic circuits and disk drive system is terminated following release of the "shoot" control switch 6

In accordance with the preferred embodiment of this invention, it is permissible for the user to select various resolution quality image recording levels with the higher levels being at the expense of memory diskette storage capacity The position of switches 14A and 14B for example could represent a unique digital mark or word that denotes the respective switch position and is sensed during initial power application and periodically during operation FIG 6A illustrates typical logic AND gate circuits 60*a* and 60*b* utilizable in conjunction with switches 14A and 14B or switch 17 to generate appropriate signals to designate respective switch positions and generate appropriate control signals from The switch positioned in the High position for high resolution allows only four to five images to be stored, while Med switch position for medium resolution allows approximately twenty five images to be stored, and Low for low resolution allows up to fifty images to be stored on a single diskette Also, by selecting black and white mode instead-of color via switch 14B, the operator may select additional storage capacity since storage is increased by a factor greater than three (one element per pixel versus three for color) Various image resolution combinations are permissible because the operator can select a different resolution and mode setting for each image prior to image signal capture. This is accomplished by marking or "tagging" each image frame data information signal with the resolution and mode of each image as it is written onto the memory diskette in any suitable manner, for example as shown in FIG 2A With reference to FIG 2A, diskette 50 has tracks 51*a*, 52*b*, 52*n* With reference to track 52*b* there is shown a representative portion of segment 53 depicting a typical image file information format having digital bit 54 depicting color mode and digital bits 55 representing compression resolution level markings or tags With reference to color mode tag 54 it can be seen that if switch 14B is in the color position tag 54 is recorded as a logical "one" or true-conversely if bit 54 is recorded as a logical zero" it corresponds to the black and white position of switch 14B Similarly as shown switch 14A would record in memory position 55 a binary 'zero' for low resolution, a binary "one" for medium resolution and a binary "two" for high resolution selections by the operator. By incorporating this "tagging" approach, it is possible for the decompression algorithm loaded into any PC prior to use or written onto the memory storage diskette along with the image data, to automatically determine the appropriate level of compression associated with image file and execute decompression efficiently

Still another alternate embodiment in accordance with this invention incorporates an acoustic digitizer circuit which digitizes sound There are several digitizers commercially available such as the Apple Computer Inc Musical Instrument Data Interface (MIDI) adaptor The output of this digitizer may be selectively connected to the CPU 20 (FIG 7) via an additional I/O interface similar to the auxiliary I/O interface 80 The sound or audio associated with each image can be recorded, digitized, and stored on the diskette device on available tracks in an identical manner previously described (FIG 2A) An image file in accordance with this embodiment would be appropriately marked or tagged with the corresponding digitized audio file 56 (FIG 2A) Upon playback on a sound configured PC, both the image and the corresponding audio would then be viewed and heard simultaneously

It should be noted that a major advantage a camera in accordance with the present invention has over conventional still video cameras is that a camera according to this invention is capable of storing multiple digital images in semiconductor memory temporarily at a rapid rate while, simultaneously, the image compression processor 12, file formatter software algorithm, and disk I/O interface 13 that stores formatted files continue to function in concert together at a slower rate. This efficient design coupled with VLSI low power, high speed semiconductor memory devices (10 & 11 FIG 5A and 24 FIG 7) allows this operational capability

Like most other still video and conventional film cameras, when the 'shoot" control 6 (FIG 6) is fully depressed, a control signal is generated from the digital control unit 9 that generates a trigger signal on the control panel 2 to cause a flash unit 16 (FIG 6) to irradiate a flash of light onto the subject image

During initial camera operation, the user first inserts a diskette such as a standard three and a half inch or similar storage medium Various memory diskette sizes and formats are suitable for the invention However, for the preferred embodiment either a double-density (800 Kbytes of storage) or a high-density (1 4 Mbytes of storage) diskette in a three and a half inch format which are readily available from various commercial sources such as Sony, Maxell, and Verbatim. The user must then select the desired PC format (IBM PC/Clone or Apple Macintosh, etc) via switch 17 (FIG 6) on the control panel 2. As shown in FIG 3; after turning on the power switch or inserting a diskette 50, the digital control unit 9 performs a self test of all internal circuitry, battery, disk drive unit, and control panel. Should any failures be detected, an appropriate error indicator is illuminated on the control panel During the power-on sequence (see FIG 3 and FIG 12), the inserted diskette 50 is automatically checked for formatting consistencies in accordance with the format selected by the format switch 17 on the control panel 2 (IBM/Apple/etc) and for available storage space by checking the boot block on the diskette, a technique that will be familiar to those skilled in the art Should any inconsistencies be detected, an error indicator is illuminated on the control panel (ie. disk full, unformatted, etc.) The operator frame counter display 22 (FIG 6) is then updated to show the maximum number of pictures available based upon indicated operator selections (color/black and white), diskette type (double versus high density), and capacity (partially full versus empty diskette) During operation, the operator can selectively erase a frame and record over it if desired by selecting the erase mode of operation from the control panel and toggling the forward/reverse control

The optics for the preferred embodiment of the invention is a commercially available one-half inch (½") color CCD device having a pixel grid array of 780x488 as pictorially depicted in FIG 4 This results in 380,640 pixel elements which results in a commercially acceptable quality resolution image as will be understood by those skilled in the art In a color imaging device (CCD array) photoelectric elements, such as photodiodes are arranged in a two dimensional array with optical filters for R (red), G (green), and B (blue) Various arrangements of optical filters are well known and the arrangement of optical filters is not limited to

a particular one with this invention During operation each pixel stores a charge corresponding to the amount of incident light The RGB components of each pixel's charge is sequentially read out via a horizontal/vertical addressing scheme that will be familiar to those skilled in the art

As shown in FIG 5A; each charge, when addressed, is amplified and processed in a sample and hold (S/H) circuit 18 The analog voltage in each S/H circuit is digitized by an associated analog to digital (A/D) converter 8. The digital values are routed and collected in the pixel buffer 10 Following completion of discrete pixel element conversion and subsequent formatting in the pixel buffer which is under Control Processor Unit (CPU) 20 software control, the output of the full pixel buffer is routed to the frame buffer 11 by digital control unit 9 This process continues until a complete frame is collected within the frame buffer The general digital logic and timing and control signals for this circuitry is shown in FIG 5B The timing is provided by a master clock that is an integral part of the CPU microprocessor For example, the MOTOROLA 68040 microprocessor has a clock speed of approximately 40 Megahertz (MHZ) which results in a clock period of 25 nanoseconds (nsec.) This clock pulse is used by the function and address decoder 19 (FIG. 6) to generate the address and control signals shown in FIG 5B as would be understood by those skilled in the art The circuit of the present invention may be designed by one skilled in the art to function with a variety of microprocessor architectures and is not limited to any one in particular. One can see from the timing chart that the S/H circuit is allowed (via the SE command) to charge to a voltage level indicative of the analog voltage impinging upon the pixel element (via the PS command) After a fixed time period, the A/D converters are enabled(via the CE command) to begin conversion of the analog voltage value on the S/H Upon completion of conversion, a conversion completion signal (CC) is generated by the A/D and routed back to the S/H circuit (via the SC command which is generated by the function and address controller 19) to discharge the stored analog voltage in anticipation of the next pixel element conversion process Next, the output of the A/D converter 8 is clocked into the pixel buffer 10 (via the PB command) When the pixel buffer 10 is full the output is clocked out to the frame buffer 11 (via the FB command) and the pixel multiplexer address circuitry selects the next pixel for conversion Reset signals (RST) are sent to all circuit elements to allow these devices to reset prior to receiving the next analog value

Another novel concept of the present invention as illustrated in FIGS 5A and 5B utilizes a technique of paralleling the S/H and A/D devices for each pixel element thus accelerating the image signal analog-to-digital conversion process This is accomplished by eliminating the serial S/H and A/D path typical of prior art still video camera designs In addition high-speed low-power devices available from Sony, Burr-Brown, Datel, Analog Devices, and others facilitate the increased conversion throughput of the S/H and A/D circuits with pixel conversion times of less than 150 nanoseconds (nsec) For example, Sony's video A/D converter Device part number CXA1016P/K performs up to 50 million samples per second or 20 nsec per conversion This device, or similar, may be used in the preferred embodiment of the present invention As explained previously, prior art still video camera designs multiplex each signal component into a common/singular A/D path to reduce the number of components and power consumption However, in accordance with another aspect of the present invention components such as C-MOS and ECL devices coupled with miniaturized packaging techniques such as surface mount devices (SMD) and ASIC technology make it feasible to incorporate these devices in a parallel design in order to realize a substantial increase in conversion speed with no appreciable increase in power consumption Therefore, this design approach provides significant conversion throughput increases over previous designs

The extremely high conversion speed in accordance with another concept of the present invention makes multiple high-speed camera operation possible in an alternate embodiment For example, total conversion time required for the aforementioned CCD array utilizing the circuit of the present invention (FIG. 5A) requires approximately 380, 640x150 nsec or 38 milliseconds (msec) Additional time (approximately 5 msec) is required for timing and control signal latency Thus, total conversion time for a complete image frame prior to compression processing and logging to the memory storage diskette 50 is less than fifty msec This allows for approximately 20 images to be captured in a one second period By adding additional RAM 11A (FIG 13) or other forms of commercially available random access memory to the frame buffer 11, image frames could be "pushed" onto a semiconductor memory stack for temporary storage allowing the compression processor and data interface circuitry to perform their respective functions at a slower rate. As shown in FIG 13, each unprocessed image frame would be recorded or "pulled" from the stack on a "First-In, First-Out" (FIFO) manner until all images in the stack queue were processed and written to the storage diskette via the disk I/O circuitry 13

As shown in FIG 6, control panel settings are monitored by the CPU 20, a microprocessor, thus allowing the appropriate timing, control, and signal processing to be effected properly The microprocessor 20 may be of the type 68040 manufactured by MOTOROLA Intel's 80386 series or equivalent microprocessors which specifications are commercially available and are incorporated herein by reference The microprocessor utilization of this invention, which is in the digital control unit 9, transmits commands and status to specific controls, functions, and displays in the control panel as well as receiving both circuit status/control data and operator commands through polling the operator switch settings 14A, 14B, and 17 via the bidirectional function and address decoder 19 This approach allows the user to know immediately how much storage capacity remains in the image storage diskette 50 as well as the camera's overall operational and functional status through the use of status displays 21, 22, and 23 and ongoing software self-tests running in the background as depicted in FIG 3 An example of this would be a low battery situation. First, the digital control unit 9 would detect a failure in the self-test mode Next, the self-test light emitting diode 21 (FIG 6) would be illuminated and an appropriate error display would be illuminated in the status display 22 thus providing the user with an exact indication of the error Another example illustrating the operation of this embedded microprocessor type of control approach is the format switch 17 (FIG 6) The position of the format switch 17 is sensed upon power application Following diskette insertion, the boot block on the diskette is compared with the format switch 17 setting (IBM/clone or Apple) and if the format does not match or if the disk 50 is unformatted, the disk format status light emitting diode 23 would be illuminated and an appropriate error display would be illuminated in the status display 22 thus prompting the user to take appropriate corrective measures

An alternate embodiment of the present invention involves adding an auxiliary I/O interface circuit or port to

the digital control unit 9 As shown it FIG 7 the auxiliary I/O port 80 connects in a manner similar to the Disk I/O interface 13 This additional I/O channel provides for external control and monitor of all timing and control signals internal to the camera In addition it allows for the image data to be routed past or around the compression processor out to any additional internal or external device such as an optical disk storage device digital analyzer or other data processors that might be desired

FIG 7 shows the digital control unit 9 The microprocessor 20 architecture here is typical to one familiar with the art The frame buffer 11 (FIG 5A) receives and stores the outputs of the pixel buffer 10 until a complete frame of image data is received Then, the CPU 20, under software control, issues a control signal to the optics logic in the shutter and control circuitry 15 (FIG 6) thus resetting those functions for future image recording The full frame buffer 11, upon command from the CPU 20, transfers it's data into the compression processor 12 (FIG 2) which performs thousands of levels of parallel pipeline processing on the image data The compressed image frame is then written out to the mass memory RAM (Random Access Memory) 24 where it is temporarily stored until transferred to the disk drive assembly 5 via the disk I/O interface circuitry 13

Referring to FIG 8, a flowchart shows the steps involved in the image compression process performed by the image compression processor 12 (FIG 2) in accordance with the preferred embodiment of the present invention The output of the frame buffer 11 is transferred into the input of the image compression processor 12 under the control of the digital control unit 9. As previously described, the setting of switch 14A (FIG 6) is read by the CPU 20 (FIG 7) to determine the image resolution quality desired. Depending on the operator selected setting of switch 14A, the unique digital word generated by the AND gate 60*a–b* (FIG 6A) which is activated by the selected position of switch 14A is routed to image compression processor 12 via CPU 20 (FIG. 7) which selects for example a predetermined digital memory location containing the appropriate corresponding compression ratio parameters under program control The compression processor uses this command value for example to establish the size of the covariance matrix and a threshold for acceptance for the variances produced by the Discrete Cosine Transformation (DCT) transform coefficients Next, the digital image signals are converted from the RGB format previously discussed in connection with FIGS 2 5, and 6 into luminance and chrominance signals The luminance and chrominance signals subsequently undergo a DCT. The cosine transformed signals are then quantized and are then processed for Huffman coding The Huffman coded image signals are then formatted into a form that facilitates format processing into various PC compatible formats (GIFF PICT2 etc) For a more complete understanding of the image compression process reference may be made to I E E E. Catalog No. EH0231-1, Library of Congress No. 85-60384 published by the I E E E Society dated 1985 and incorporated herein by reference

Of the two traditional classes of image compression techniques, spatial coding and transform coding transform coding techniques lend themselves well for this application due to computational simplicity Transform coding techniques that provide good visual fidelity include: Karhunen-Loeve transform (KLT), Fourier, cosine, sine, and Hadamard The KLT algorithm offers the best visual fidelity but suffers from serious computational complications due to extremely large matrix size Several alternate algorithms that offer reasonable visual fidelity that are computationally feasible for this invention include the Fast Fourier Transform (FFT), Discrete Cosine Transform (DCT), and Discrete Sine Transform (DST) The DCT was adopted by the JPEG as the preferred algorithm due to computational simplicity and performance

It should be noted that the Joint Photographic Experts Group (JPEG) (composed of experts from many companies including IBM, AT&T Digital Equipment Corp. and INTEL) compression/decompression standard was developed in 1985 in response to the lack of interoperability between image and processing equipment due to numerous proprietary standards held by each manufacturer The JPEG standard provides image compression effectively up to 75 times or greater depending on the visual fidelity desired The JPEG standard is widely used in industry as an alternative to proprietary algorithms such as Intel's own proprietary standard called DVI which was initially developed by RCA before being sold to INTEL, the integrated Circuit manufacturer INTEL offers it's own firmware compression processor incorporating their DVI standard delivering compression ratios in excessive of 100:1 However, a new international standard called MPEG is due to be announced in the 1991 time frame from the JPEG and should offer compression ratios of 275:1 and greater In the preferred embodiment of the present invention, the JPEG standard is the preferred algorithm chosen with the incorporation of the the MPEG standard or other similar standard in the future when available commercially An alternate embodiment of the present invention would be the incorporation of various proprietary compression algorithm standards such as DVI

The compression/decompression algorithm firmware implementation of the JPEG algorithm is available commercially from various sources including C-Cube, Electronics for imaging, Storm Technology, Burr-Brown, Spectral Innovations Inc., INTEL, and others The implementation of this algorithm for the present invention may incorporate the integrated circuit set commercially available from C-Cube Their four chip ASIC JPEG algorithm implementation is performed in three basic steps: first, the image is divided into 8-by-8 pixel squares and applies a discrete cosine transform (DCT) to each square resulting in 64 frequency values; second, these frequencies are put through a quantization algorithm to eliminate unimportant frequencies; third, the remaining values are run through a Huffman coding scheme to encode the most frequently occurring values using the fewest bits A compatible software implementation of the JPEG algorithm is available commercially from Aladdin Systems, Radius Inc , Kodak, and others

Those skilled in the art will be familiar with the process and the commercially available software and firmware chipsets that are currently available on the market The present invention incorporates both available firmware chipsets in the camera and software for use in the PC for decompression The decompression algorithm can be written onto the camera s diskette 50 prior to any image data recording This allows the PC user to take the diskette 50 to a PC and directly incorporate the image data because the image file selected by the user is automatically decompressed transparent to the user The algorithm can be written onto an unused track 52 or sector combination on the diskette as shown on FIG 2A Alternatively, the decompression algorithm can be loaded onto a PC before inserting a diskette 50 containing compressed image data In the latter embodiment the resolution and mode values 54 and 55 (FIG 2A.) for each representative image would be read from diskette 50 in order to appropriately control the selection and activation of the appropriate corresponding decompression algorithm

As shown in FIG 7, the output of the image compression processor 12 is routed to the RAM memory 24 where the compressed image is formatted for either the PICT II or GIFF format depending on the setting of format switch 17 (FIG 6) It should be noted that a large number of image formats for PCs exist. PICT and GIFF are the most common for the Apple and IBM PC's and are therefore the preferred formats for the present invention although other formats can be easily incorporated into the design by changing the software format routines These software image formats are commercially available from many sources most notably Apple computers for PICT and IBM for GIFF. An example of the PICT format is pictorially shown in FIG 6B as will be familiar to those skilled in the computer arts Once formatting is complete, the formatted image data is transferred to the disk I/O interface 13 for transfer to the magnetic recording diskette 50

FIG 9 and FIG 10 illustrate the preferred embodiment of the video format translator device in accordance with another aspect of this invention that converts other still video camera formats for example on two inch video diskette to this invention's selectable PC compatible digital format. The general concept of operation is shown in FIG 10 In FIG 9 correspond parts and subassemblies in translator 40 are shown with like numbers corresponding to FIG 2 and 6 having a 40 hyphenation prefix designation and such parts and subassemblies perform similar functions to those described above with reference to FIGS 2 and 6 Referring again to FIG 9, the translator 40 incorporates the same components utilized in the digital circuit card assembly which houses both the digital control unit 9 and optics processing circuits (pixel multiplexer 7, A/D 8 etc 10–13) The major difference is that the CCD array 1 is replaced with an input disk drive 25, for example a two inch (2") video disk drive assembly, and an NTSC video format decoder 26 which converts the composite video signal to an RGB format for processing as described previously

FIG 11 displays an alternate embodiment of the video format translator device 40 of the present invention that shows optional inputs 27 and outputs 28 and 29 The exact same circuitry is utilized that was used for the translator device 40 as shown in FIG. 9 except that inputs 27 for either an NTSC/PAL format or RGB format video signal is provided This allows video signals from other sources such as a cable TV, CAMCORDER, or other video signal source to be digitized and archived in a PC compatible format. Also, provisions for video output jacks 28 are made to allow either viewing of the image/video source prior to or during image recording Finally, provisions are made to provide a data output 29 to allow connection to other PC peripherals such as a communications modem larger/smaller disk drive assembly, optical disk, specialty display or signal processor/analyzer Either a standard serial, parallel, or Small Computer Standard Interface (SCSI) data port can be readily connected to the auxiliary I/O interface 80

FIG 12 depicts an alternate feature of an embodiment of the present invention that shows how an inserted diskette 50 that is either unformatted or formatted for a undesired (e.g., not corresponding to the setting of switch 17-FIG 6) PC configuration would be automatically properly formatted for use with a camera in accordance with another aspect of this invention This capability allows the user of this invention to forego the requirement to pre-format the storage medium (diskette) on a PC prior to using it in the camera operated in accordance with the present invention With reference to FIG 3 the power-on sequence process would result in an abnormal diskette format error if the format of an inserted diskette 50 did not correspond to the operator selected format switch 17 (FIG 6) In accordance with the automatic diskette format option CPU 20 of digital control unit 9 in response to the abnormal diskette format error would initiate the diskette format process illustrated in FIG 12 Upon completion of the diskette format process illustrated in FIG. 12, the power-on sequence illustrated in FIG 3 would continue from step B

Referring now to FIG 14A, there is shown a schematic block diagram of the format selection logic in accordance with another aspect of the present invention During the power-on sequence as described in connection with FIGS 3 and 12, processor 20 of control unit 9 initiates a format selection switch sample and test routine as more fully described in the flow diagram illustrated in FIG 14B Switch 17 is illustrated in FIG 14A in the Apple PC position and logic level v1 is applied as inputs to logic gates 60e and 60f As illustrated in FIG 2A, the format signals 57 for the Apple PC format is a logic "zero" and conversely the format signal or tag 57 if the format switch 17 were in the IBM PC or other computer type position would be a logic "one" and "two" respectively In response to the logic "zero" indicating Apple PC format, processor 20 accesses a unique memory location XY of format memory 20-2 which for example may comprise any random access memory with two megabytes storage capacity The data format for the operator selectable predetermined number of computer architectures, similar in content and arrangement to those illustrated in FIG. 6B for an Apple PC would be stored in memory 20-2 which would be addressed in response to the other operator selectable position of switch 17 to generate the other unique codes 57 as shown in FIG 2A Processor 20 in response to a stored format subroutine more particularly shown in FIG 14B contains the allocation of data memory addresses in disk input/output interface unit 13 in accordance with the picture image file format as illustrated in FIG 6B Thus the digital video data information signals generated by compression processor 12 are appropriately formatted and stored in memory storage disk drive 5 to insure compatibility with the format selected by the operator by selectively positioning switch 17

Those skilled in the art will recognize the many alterations, additions or changes of the preferred embodiment may be made without departing from the scope of the following claims

What is claimed is:

1 For use in an electronic camera having an image pick-up unit and a storage device, a process for taking and storing digital pictures, the process comprising:

generating a digital image signal corresponding to an image incident on the image pick-up unit;

formatting the digital image signal in one of a plurality of computer image file formats; and

storing the formatted image file in the storage device

2 A process as in claim 1, wherein the storage device is removable

3 For use in an electronic camera having an image pick-up unit and a storage device, a process for taking and storing digital pictures, the process comprising:

selecting one of a plurality of computer image file formats in the camera;

generating a digital image signal corresponding to an image incident on the image pick-up unit;

formatting the digital image signal in the selected computer image file format; and

storing the formatted computer image file in the storage device

4 A process as in claim 3, wherein the storage device is removable

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