IN THE UNITED STATES DISTRICT COURT
FOR THE DISTRICT OF DELAWARE

MEMORTY INTEGRITY, LLC Plaintiff, v. INTEL CORPORATION, Defendant.	Civil Action No. _____ JURY TRIAL DEMANDED

COMPLAINT FOR PATENT INFRINGEMENT

Plaintiff Memory Integrity, LLC ("MI"), by way of this Complaint for Patent Infringement ("Complaint") against the above-named Defendant Intel Corporation ("Intel"), alleges as follows:

NATURE OF THE ACTION

1. This is an action for patent infringement arising under the Patent Laws of the United States, Title 35 of the United States Code.

THE PARTIES

2. Plaintiff MI is a limited liability company organized under the laws of the State of Delaware with a place of business at 1220 N. Market Street, Suite 806, Wilmington, Delaware 19801.

3. On information and belief, Defendant Intel Corporation is a corporation organized under the laws of the State of Delaware with its principal place of business at 2200 Mission College Boulevard, Santa Clara, California.

JURISDICTION AND VENUE

4. This Court has subject matter jurisdiction under 28 U.S.C. §§ 1331 and 1338.

5. On information and belief, Intel is subject to the jurisdiction of this Court by virtue of the fact that it is organized under the laws of the State of Delaware. On information and belief, Intel is also subject to the jurisdiction of this Court by reason of its acts of patent infringement which have been committed in this Judicial District, and by virtue of its regularly conducted and systematic business contacts in this State. As such, Intel has purposefully availed itself of the privilege of conducting business within this Judicial District; has established sufficient minimum contacts with this Judicial District such that it should reasonably and fairly anticipate being haled into court in this Judicial District; and at least a portion of the patent infringement claims alleged herein arise out of or are related to one or more of the foregoing activities.

6. Venue is proper in this judicial district under 28 U.S.C. §§ 1391(c) and 1400(b).

THE PATENTS-IN-SUIT

7. On November 13, 2007, United States Patent No. 7,296,121 (the "'121 Patent"), entitled "Reducing Probe Traffic in Multiprocessor Systems," was duly and legally issued by the United States Patent and Trademark Office. A true and correct copy of the '121 Patent is attached as Exhibit A to this Complaint.

8. MI is the assignee and owner of the right, title and interest in and to the '121 Patent, including the right to assert all causes of action arising under said patent and the right to any remedies for infringement of it.

9. On September 5, 2006, United States Patent No. 7,103,636 (the "'636 Patent"), entitled "Methods and Apparatus for Speculative Probing of a Remote Cluster," was duly and legally issued by the United States Patent and Trademark Office. A true and correct copy of the '636 Patent is attached as Exhibit B to this Complaint.

10. MI is the assignee and owner of the right, title and interest in and to the '636 Patent, including the right to assert all causes of action arising under said patent and the right to any remedies for infringement of it.

11. On September 12, 2006, United States Patent No. 7,107,409 (the "'409 Patent"), entitled "Methods and Apparatus for Speculative Probing at a Request Cluster," was duly and legally issued by the United States Patent and Trademark Office. A true and correct copy of the '409 Patent is attached as Exhibit C to this Complaint.

12. MI is the assignee and owner of the right, title and interest in and to the '409 Patent, including the right to assert all causes of action arising under said patent and the right to any remedies for infringement of it.

13. October 29, 2013, United States Patent No. 8,572,206 (the "'206 Patent"), entitled "Transaction Processing Using Multiple Protocol Engines," was duly and legally issued by the United States Patent and Trademark Office. A true and correct copy of the '206 Patent is attached as Exhibit D to this Complaint.

14. MI is the assignee and owner of the right, title and interest in and to the '206 Patent, including the right to assert all causes of action arising under said patent and the right to any remedies for infringement of it.

15. The '121 Patent, '636 Patent, '409 Patent, and '206 Patent are referred to collectively herein as the "Patents-in-Suit."

COUNT I – INFRINGEMENT OF U.S. PATENT NO. 7,296,121

16. The allegations set forth in the foregoing paragraphs 1 through 15 are hereby realleged and incorporated herein by reference.

17. In violation of 35 U.S.C. § 271(a), Intel has directly infringed and continues to directly infringe, both literally and under the doctrine of equivalents, the '121 Patent, including

but not limited to claim 1, by making, using, offering for sale, selling, and importing multicore processors that utilize a probe filtering unit to reduce probe traffic (the "'121 Patent Accused Processors"), as well as boards and systems (the "'121 Patent Accused Boards") containing or supporting the '121 Patent Accused Processors, and by performing methods that practice the subject matter claimed in one or more claims of the '121 Patent in the United States, including within this Judicial District, without the authority of MI. For example, Intel has directly infringed the '121 Patent by making and selling Intel's Sandy Bridge processors. The '121 Patent Accused Processors include, but are not limited to, Intel's Sandy Bridge, Ivy Bridge, Nehalem, and Westmere processors. The '121 Patent Accused Boards include, but are not limited to, Intel's S2400, S2600 and S4600 families of server boards. The '121 Patent Accused Processors and the '121 Patent Accused Boards are referred to herein collectively as the "'121 Patent Accused Instrumentalities."

18. Intel has had actual knowledge of the '121 Patent and its infringement of that patent since at least the date of service of this Complaint.

19. Intel is inducing infringement of the '121 Patent under 35 U.S.C. § 271(b) since at least the date of service of this Complaint by actively aiding and abetting others (including its direct and indirect customers) whose making, using, offering for sale, selling, and importing of the '121 Patent Accused Instrumentalities and systems containing the '121 Patent Accused Instrumentalities constitutes direct infringement. Intel has engaged in these actions with either the specific intent to cause infringement or with willful blindness to the infringement that it is causing. For example, Intel's actions that actively induces its customers to directly infringe at least claim 25 of the '121 Patent include selling the '121 Patent Accused Instrumentalities and providing instructions and technical support regarding use of the '121 Patent Accused

Instrumentalities, where the use of the '121 Patent Accused Instrumentalities during normal operation by Intel's customers infringes at least claim 25 of the '121 Patent. The use of the '121 Patent Accused Instrumentalities during normal operation directly infringes claim 25 of the '121 Patent in at least the following manner:

(a) To the extent that the preamble is construed to be a limitation on the claim, the Accused Instrumentalities comprise a plurality of processing nodes (cores). The cores are connected in a point-to-point architecture and each core has an associated L1 and L2 cache memory;

(b) One of the cores requests access to a memory line by transmitting a probe to the probe filtering unit (Cache Box);

(c) The Cache Box evaluates the probe to determine whether a valid copy of the memory line is in any of the caches by using filtering information stored in the Core Valid bits, which are representative of the states associated with selected ones of the caches;

(d) The Cache Box transmits the probe only to selected ones of the cores identified in the evaluating step;

(e) The Cache Box accumulates responses from the selected cores; and

(f) The Cache Box responds to the original request from the first core.

20. Intel is also committing contributory infringement of the '121 Patent under 35 U.S.C. § 271(c) since at least the date of service of this Complaint by importing, offering for sale, and selling the '121 Patent Accused Instrumentalities to others, including but not limited to its customers, knowing and/or being willfully blind to the fact that these products constitute a material part of the invention, were especially made or especially adapted for use in an

infringement of the ’121 Patent, and include components that have no substantial non-infringing uses. For example, the ‘121 Patent Accused Instrumentalities constitute a material part of the claimed invention at least because they contain all of the components that perform the method of reducing probe traffic in a computer system as claimed in claim 25 of the ‘121 Patent. The ‘121 Patent Accused Instrumentalities were made or especially adapted for use in an infringement of the ‘121 Patent and have no substantial non-infringing uses at least because they contain components whose only purpose is to reduce probe traffic in a computer system as claimed in claim 25 of the ‘121 Patent. The use of the ‘121 Patent Accused Instrumentalities by Intel’s customers during normal operation directly infringes claim 25 of the ‘121 Patent in at least the following manner:

(a) To the extent that the preamble is construed to be a limitation on the claim, the Accused Instrumentalities comprise a plurality of processing nodes (cores). The cores are connected in a point-to-point architecture and each core has an associated L1 and L2 cache memory;

(b) One of the cores requests access to a memory line by transmitting a probe to the probe filtering unit (Cache Box);

(c) The Cache Box evaluates the probe to determine whether a valid copy of the memory line is in any of the caches by using filtering information stored in the Core Valid bits, which are representative of the states associated with selected ones of the caches;

(d) The Cache Box transmits the probe only to selected ones of the cores identified in the evaluating step;

(e) The Cache Box accumulates responses from the selected cores; and

(f) The Cache Box responds to the original request from the first core.

21. MI has been harmed by Intel's infringing activities with respect to the '121 Patent.

COUNT II – INFRINGEMENT OF U.S. PATENT NO. 7,103,636

22. The allegations set forth in the foregoing paragraphs 1 through 21 are hereby realleged and incorporated herein by reference.

23. In violation of 35 U.S.C. § 271(a), Intel has directly infringed and continues to directly infringe, both literally and under the doctrine of equivalents, the '636 Patent, including but not limited to claim 22, by making, using, offering for sale, selling, and importing systems and boards (the "'636 Patent Accused Boards") containing or supporting two more Intel Sandy Bridge, Ivy Bridge, Nehalem, or Westmere family processors (the "'636 Patent Accused Processors") and by performing methods that practice the subject matter claimed in one or more claims of the '636 Patent in the United States, including within this Judicial District, without the authority of MI. For example, Intel has directly infringed the '636 Patent by making and using systems and boards containing two or more Intel Sandy Bridge processors. The '636 Patent Accused Processors include, but are not limited to, Intel's Sandy Bridge-EN, Sandy Bridge-EP, Ivy Bridge-EN, Ivy Bridge-EP, Ivy Bridge-EX, Nehalem-EX, Nehalem-EP, Westmere-EX, and Westmere-EP processors. The '636 Patent Accused Boards include, but are not limited to, Intel's S2400, S2600 and S4600 families of server boards. The '636 Patent Accused Processors and the '636 Patent Accused Boards are referred to herein collectively as the "'636 Patent Accused Instrumentalities."

24. Intel has had actual knowledge of the '636 Patent and its infringement of that patent since at least the date of service of this Complaint.

25. Intel is inducing infringement of the '636 Patent under 35 U.S.C. § 271(b) since at least the date of service of this Complaint by actively aiding and abetting others (including its direct and indirect customers) whose making, using, offering for sale, selling, and importing systems containing two or more of the '636 Patent Accused Processors constitutes direct infringement. Intel has engaged in these actions with either the specific intent to cause infringement or with willful blindness to the infringement that it is causing. For example, Intel's actions that actively induces its customers to directly infringe at least claim 22 of the '636 Patent include selling the '636 Patent Accused Instrumentalities which are designed to be combined together and providing instructions and technical support regarding how to use and combine the '636 Patent Accused Instrumentalities. Intel's customers' systems containing two or more of the '636 Patent Accused Processors directly infringe claim 22 of the '636 Patent in at least the following manner:

(a) To the extent that the preamble is construed to be a limitation on the claim, each of the processors in the system contains a cache coherence controller (Cache Box);

(b) The Cache Box includes interface circuitry that is coupled to the local cores in the processor via the ring interconnect. The interface circuitry is also coupled to a Cache Box in the other processor via the ring interconnect and an inter-processor link;

(c) The Cache Box also includes a protocol engine that is coupled to the interface circuitry, and which receives a cache access request from one of the local cores in the first processor and sends a speculative probe to the other processor in the system via the inter-processor link.

26. Intel is also committing contributory infringement of the ‘636 Patent under 35 U.S.C. § 271(c) since at least the date of service of this Complaint by importing, offering for sale, and selling the ‘636 Patent Accused Instrumentalities to others, including but not limited to its customers, knowing and/or being willfully blind to the fact that these products constitute a material part of the invention, were especially made or especially adapted for use in an infringement of the ’636 Patent, and include components that have no substantial non-infringing uses. For example, each of the ‘636 Patent Accused Processors constitutes a material part of the claimed invention at least because it contains the cache coherence controller, interface circuitry, and protocol engine as claimed in claim 22. Each of the ‘636 Patent Accused Processors was made or especially adapted for use in an infringement of the patent and has no substantial non-infringing uses at least because it contains circuitry within the protocol engine whose only purpose is to implement the speculative probing feature as claimed in claim 22. Intel’s customers directly infringe at least by combining two or more of the ‘636 Patent Accused Processors to make infringing systems, and by using, offering for sale, selling, and importing such systems. Intel’s customers’ systems containing two or more of the ‘636 Patent Accused Processors directly infringe claim 22 of the ‘636 Patent in at least the following manner:

(a) To the extent that the preamble is construed to be a limitation on the claim, each of the processors in the system contains a cache coherence controller (Cache Box);

(b) The Cache Box includes interface circuitry that is coupled to the local cores in the processor via the ring interconnect. The interface circuitry is also coupled to a Cache Box in the other processor via the ring interconnect and an inter-processor link;

(c) The Cache Box also includes a protocol engine that is coupled to the interface circuitry, and which receives a cache access request from one of the local cores in the first processor and sends a speculative probe to the other processor in the system via the inter-processor link.

27. MI has been harmed by Intel's infringing activities with respect to the '636 Patent.

COUNT III – INFRINGEMENT OF U.S. PATENT NO. 7,107,409

28. The allegations set forth in the foregoing paragraphs 1 through 27 are hereby realleged and incorporated herein by reference.

29. In violation of 35 U.S.C. § 271(a), Intel has directly infringed and continues to directly infringe, both literally and under the doctrine of equivalents, the '409 Patent, including but not limited to claim 1, by making, using, offering for sale, selling, and importing systems and boards (the "'409 Patent Accused Boards") containing or supporting two more Intel Sandy Bridge, Ivy Bridge, Nehalem, or Westmere family processors (the "'409 Patent Accused Processors") and by performing methods that practice the subject matter claimed in one or more claims of the '409 Patent in the United States, including within this Judicial District, without the authority of MI. For example, Intel has directly infringed the '409 Patent by making and using systems and boards containing two or more Intel Sandy Bridge processors. The '409 Patent Accused Processors include, but are not limited to, Intel's Sandy Bridge-EN, Sandy Bridge-EP, Ivy Bridge-EN, Ivy Bridge-EP, and Ivy Bridge-EX, Nehalem-EX, Nehalem-EP, Westmere-EX, and Westmere-EP processors. The '409 Patent Accused Boards include, but are not limited to, Intel's S2400, S2600 and S4600 families of server boards. The '409 Patent Accused Processors and the '409 Patent Accused Boards are referred to herein collectively as the "'409 Patent Accused Instrumentalities."

30. Intel has had actual knowledge of the ‘409 Patent and its infringement of that patent since at least the date of service of this Complaint.

31. Intel is inducing infringement of the ‘409 Patent under 35 U.S.C. § 271(b) since at least the date of service of this Complaint by actively aiding and abetting others (including its direct and indirect customers) whose making, using, offering for sale, selling, and importing systems containing two or more of the ‘409 Patent Accused Processors constitutes direct infringement. Intel has engaged in these actions with either the specific intent to cause infringement or with willful blindness to the infringement that it is causing. For example, Intel’s actions that actively induces its customers to directly infringe at least claim 1 of the ‘409 Patent include selling the ‘409 Patent Accused Instrumentalities which are designed to be combined together and providing instructions and technical support regarding how to use and combine the ‘409 Patent Accused Instrumentalities. Intel’s customers’ systems containing two or more of the ‘409 Patent Accused Processors directly infringe claim 1 of the ‘409 Patent in at least the following manner:

(a) The first processor includes a plurality of cores and a cache coherence controller (Cache Box); the cores and the Cache Box are interconnected in a point-to-point architecture via the ring interconnect;

(b) The second processor also includes a plurality of cores and a cache coherence controller (Cache Box); the cores and the Cache Box in the second processor are interconnected in a point-to-point architecture via a ring interconnect; the Cache Box in the first processor is coupled to the Cache Box in the second processor via the inter-processor link;

(c) The Cache Box in the first processor is configured to receive a cache access request from one of the local cores in the first processor and to send a probe to the local cores before the cache access request is received by a serialization point in the second processor via the inter-processor link.

32. Intel is also committing contributory infringement of the ‘409 Patent under 35 U.S.C. § 271(c) since at least the date of service of this Complaint by importing, offering for sale, and selling the ‘409 Patent Accused Instrumentalities to others, including but not limited to its customers, knowing and/or being willfully blind to the fact that these products constitute a material part of the invention, were especially made or especially adapted for use in an infringement of the ’409 Patent, and include components that have no substantial non-infringing uses. For example, each of the ‘409 Patent Accused Processors constitutes a material part of the claimed invention at least because it contains the plurality of processors and the cache coherence controller configured to send a probe as claimed in claim 1. Each of the ‘409 Patent Accused Processors was made or especially adapted for use in an infringement of the patent and has no substantial non-infringing uses at least because it contains components within the cache coherence controller whose only purpose is to send a probe as claimed in claim 1. Intel’s customers directly infringe at least by combining two or more of the ‘409 Patent Accused Processors to make infringing systems, and by using, offering for sale, selling, and importing such systems. Intel’s customers’ systems containing two or more of the ‘409 Patent Accused Processors directly infringe claim 1 of the ‘409 Patent in at least the following manner:

(a) The first processor includes a plurality of cores and a cache coherence controller (Cache Box); the cores and the Cache Box are interconnected in a point-to-point architecture via the ring interconnect;

(b) The second processor also includes a plurality of cores and a cache coherence controller (Cache Box); the cores and the Cache Box in the second processor are interconnected in a point-to-point architecture via a ring interconnect; the Cache Box in the first processor is coupled to the Cache Box in the second processor via the inter-processor link;

(c) The Cache Box in the first processor is configured to receive a cache access request from one of the local cores in the first processor and to send a probe to the local cores before the cache access request is received by a serialization point in the second processor via the inter-processor link.

33. MI has been harmed by Intel's infringing activities with respect to the '409 Patent.

COUNT IV – INFRINGEMENT OF U.S. PATENT NO. 8,572,206

34. The allegations set forth in the foregoing paragraphs 1 through 33 are hereby realleged and incorporated herein by reference.

35. In violation of 35 U.S.C. § 271(a), Intel has directly infringed and continues to directly infringe, both literally and under the doctrine of equivalents, the '206 Patent, including but not limited to claim 30, by making, using, offering for sale, selling, and importing multicore processors that utilize the claimed interconnection controller (the "'206 Patent Accused Processors"), as well as boards and systems (the "'206 Patent Accused Boards") containing the '206 Patent Accused Processors, and by performing methods that practice the subject matter claimed in one or more claims of the '206 Patent in the United States, including within this Judicial District, without the authority of MI. For example, Intel has directly infringed the '206 Patent by making and selling Intel's Sandy Bridge-EN and Sandy Bridge-EP processors. The '206 Patent Accused Processors include, but are not limited to, Intel's Sandy Bridge-EN, Sandy

Bridge-EP, Ivy Bridge-EN, Ivy Bridge-EP, Ivy Bridge-EX, Nehalem-EX, and Westmere-EX processors. The '206 Patent Accused Boards include, but are not limited to, Intel's S2400, S2600 and S4600 families of server boards. The '206 Patent Accused Processors and the '206 Patent Accused Boards are referred to herein collectively as the "'206 Patent Accused Instrumentalities."

36. Intel has had actual knowledge of the '206 Patent and its infringement of that patent since at least the date of service of this Complaint.

37. Intel is inducing infringement of the '206 Patent under 35 U.S.C. § 271(b) since at least the date of service of this Complaint by actively aiding and abetting others (including its direct and indirect customers) whose making, using, offering for sale, selling, and importing of the '206 Patent Accused Instrumentalities and systems containing the '206 Patent Accused Instrumentalities constitutes direct infringement. Intel has engaged in these actions with either the specific intent to cause infringement or with willful blindness to the infringement that it is causing. For example, Intel's actions that actively induces its customers to directly infringe at least claim 39 of the '206 Patent include selling the '206 Patent Accused Instrumentalities and providing instructions and technical support regarding use of the '206 Patent Accused Instrumentalities, where the use of the '206 Patent Accused Instrumentalities during normal operation by Intel's customers infringes at least claim 39 of the '206 Patent. The use of the '206 Patent Accused Instrumentalities during normal operation directly infringes claim 39 of the '206 Patent in at least the following manner:

(a) To the extent that the preamble is construed to be a limitation on the claim, the '206 Patent Accused Instrumentalities comprise a plurality of processing nodes (cores). They also include an interconnection controller comprising a plurality of Cache

Boxes and a Home Agent that are coupled to the cores. The Cache Boxes and the Home Agent include a plurality of protocol engines that are configured to process memory transactions, including a remote protocol engine in the Cache Box that processes transactions directed to remote memory and a local protocol engine in the Home Agent that processes transactions directed to local memory;

(b) The interconnection controller receives a first memory transaction from one of the cores;

(c) The interconnection controller circuitry selects one of the protocol engines using a slice ID derived from the address specified in the memory transaction;

(d) The selected protocol engine processes the memory transaction in accordance with a MESIF cache coherence protocol.

38. Intel is also committing contributory infringement of the ‘206 Patent under 35 U.S.C. § 271(c) since at least the date of service of this Complaint by importing, offering for sale, and selling the ‘206 Patent Accused Instrumentalities to others, including but not limited to its customers, knowing and/or being willfully blind to the fact that these products constitute a material part of the invention, were especially made or especially adapted for use in an infringement of the ’206 Patent, and include components that have no substantial non-infringing uses. For example, the ‘206 Patent Accused Instrumentalities constitute a material part of the claimed invention at least because they contain all of the components that perform the method of processing memory transactions in a cluster in accordance with a cache coherence protocol as claimed in claim 39 of the ‘206 Patent. The ‘206 Patent Accused Instrumentalities were made or especially adapted for use in an infringement of the ‘206 Patent and have no substantial non-infringing uses at least because they contain components whose only purpose is to process

memory transactions in a cluster in accordance with a cache coherence protocol as claimed in claim 39 of the '206 Patent. The use of the '206 Patent Accused Instrumentalities by Intel's customers during normal operation directly infringes claim 39 of the '206 Patent in at least the following manner:

(a) To the extent that the preamble is construed to be a limitation on the claim, the '206 Patent Accused Instrumentalities comprise a plurality of processing nodes (cores). They also include an interconnection controller comprising a plurality of Cache Boxes and a Home Agent that are coupled to the cores. The Cache Boxes and the Home Agent include a plurality of protocol engines that are configured to process memory transactions, including a remote protocol engine in the Cache Box that processes transactions directed to remote memory and a local protocol engine in the Home Agent that processes transactions directed to local memory;

(b) The interconnection controller receives a first memory transaction from one of the cores;

(c) The interconnection controller circuitry selects one of the protocol engines using a slice ID derived from the address specified in the memory transaction;

(d) The selected protocol engine processes the memory transaction in accordance with a MESIF cache coherence protocol.

39. MI has been harmed by Intel's infringing activities with respect to the '206 Patent.

JURY DEMAND

40. MI demands a jury trial on all issues and claims so triable.

PRAYER FOR RELIEF

WHEREFORE, MI prays for judgment as follows:

a. An adjudication that Intel has infringed the Patents-in-Suit;

b. An award of damages to be paid by Intel adequate to compensate MI for past infringement of the Patents-in-Suit, and any continuing or future infringement through the date such judgment is entered, including prejudgment and post-judgment interest, costs, expenses and an accounting of all infringing acts including but not limited to those acts not presented at trial;

c. An order that Intel pay an ongoing royalty in an amount to be determined for any continued infringement after the date judgment is entered; and

d. Such further relief at law and in equity as the Court may deem just and proper.

Respectfully submitted,

Dated: November 1, 2013

STAMOULIS & WEINBLATT LLC

/s/ Richard C. Weinblatt

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