IN THE UNITED STATES DISTRICT COURT
FOR THE DISTRICT OF DELAWARE

NATIONAL SEMICONDUCTOR CORPORATION,	)
	) Civil Action No. _____
Plaintiff,	)
v.	) JURY TRIAL DEMANDED
LSI CORPORATION and AGERE SYSTEMS INC.,	)
Defendants.	)

COMPLAINT FOR PATENT INFRINGEMENT

Plaintiff National Semiconductor Corporation ("National") alleges the following:

JURISDICTION AND VENUE

1. This is a civil action for patent infringement, arising under the patent laws of the United States, 35 U.S.C. §101 et seq. This Court has subject matter jurisdiction under 28 U.S.C. §§ 1331 and 1338. Venue is proper in this judicial district under 28 U.S.C. §§ 1391 and 1400(b).

THE PARTIES

2. Plaintiff National is a Delaware corporation with a principal place of business located at 2900 Semiconductor Drive, Santa Clara, California.

3. On information and belief, Defendant LSI Corporation ("LSI") is a Delaware corporation with a principal place of business at 1621 Barber Lane, Milpitas, California.

4. On information and belief, Defendant Agere Systems Inc. ("Agere") is a Delaware corporation with a principal place of business at 1110 American Parkway NE, Allentown, Pennsylvania. On information and belief, Agere is a subsidiary of LSI.

THE PATENTS IN SUIT

5. On January 28, 1986, United States Patent No. 4,567,058 ("the '058 Patent") entitled *Method For Controlling Lateral Diffusion Of Silicon In A Self-Aligned $TISI_2$ Process* was duly and legally issued to Yun. B. Koh. The '058 Patent expired on July 27, 2004. A true and correct copy of the '058 Patent is attached hereto and incorporated by reference as Exhibit A. The patent has been duly and legally assigned to National.

6. On August 24, 1993, United States Patent No. 5,239,440 ("the '440 Patent") entitled *Electrostatic Discharge Protection for Integrated Circuits* was duly and legally issued to Richard B. Merrill. The '440 Patent expires on August 24, 2010. A true and correct copy of the '440 Patent is attached hereto and incorporated by reference as Exhibit B. The patent has been duly and legally assigned to National.

COUNT ONE

(Infringement of U.S. Patent No. 4,567,058)

7. National realleges paragraphs 1-6 of this Complaint.

8. On information and belief, LSI and Agere (collectively, "Defendants") directly, indirectly, contributorily, and/or by inducement, literally or under the doctrine of equivalents, infringed the '058 Patent by their manufacture, use, sale, offer for sale, and/or importation of products, within this judicial district and elsewhere in the United States, that infringed one or more claims of the '058 Patent. Examples of infringing

products include, but are not limited to, the Brasica, LUC3X51FT 100Base TX/FX, the DSP1641B Digital Signal Processor, the CSP1034 Digital Signal Processor, the T7531A Digital Signal Processor, and the MS241C3 27 HDD Read Channel. Defendants are liable for their infringement of the '058 Patent pursuant to 35 U.S.C. §271.

9. Upon information and belief, Defendants were aware of the '058 Patent prior to its expiration but recklessly continued to make, use, sell, offer for sale, and/or import products, knowing that such actions constituted a high likelihood of infringement of the '058 Patent. Defendants' infringement of the '058 Patent was thus willful.

COUNT TWO

(Infringement of U.S. Patent No. 5,239,440)

10. National realleges paragraphs 1-6 of this Complaint.

11. On information and belief, Defendants directly, indirectly, contributorily, and/or by inducement, literally or under the doctrine of equivalents, have infringed and continue to infringe the '440 Patent by their manufacture, use, sale, offer for sale, and/or importation of products, within this judicial district and elsewhere in the United States, that infringe one or more claims of the '440 Patent. Examples of infringing products include, but are not limited to, the LU5M31 Sonet/SDH 155.622/2488 Mbits/s Gigabit Media Access Controller, the Brasica, the LUC3X51FT 100Base-TX/FX, the DSP1641B Digital Signal Processor, the T1034AH Codec, the Agere/LSI USB and FireWire products (such as part numbers US 344S and FW323), and the Agere hard disk read channel products (such as part numbers MS241C3, LU 5241c, and 4387). Defendants are liable for their infringement of the '440 Patent pursuant to 35 U.S.C. §271.

12. Upon information and belief, Defendants were aware of the '440 Patent prior to the filing of this Complaint but recklessly continue to make, use, sell, offer for sale, and/or import products, knowing that such actions constitute a high likelihood of infringement of the '440 Patent. Defendants' infringement of the '440 Patent is thus willful.

PRAYER FOR RELIEF

WHEREFORE, Plaintiff National requests that judgment be entered in its favor and against Defendants as follows:

1. Declaring that United States Patent No. 4,567,058 was valid and enforceable;

2. Declaring that Defendants infringed one or more claims of United States Patent No. 4,567,058;

3. Awarding monetary damages arising from Defendants' infringement of United States Patent No. 4,567,058, including treble damages due to Defendants' willful infringement, to National, together with prejudgment and post-judgment interest, in an amount to be determined at trial;

4. Declaring that United States Patent No. 5,239,440 is valid and enforceable;

5. Declaring that Defendants have infringed one or more claims of United States Patent No. 5,239,440;

6. Permanently enjoining Defendants, their officers, agents, employees, and those acting in privity with them, from further infringement, contributory infringement, and/or inducing infringement of United States Patent No. 5,239,440;

7. Awarding monetary damages arising from Defendants' infringement of United States Patent No. 5,239,440, including treble damages due to Defendants' willful infringement, to National, together with prejudgment and post-judgment interest, in an amount to be determined at trial;

8. Declaring this case an "exceptional case" within the meaning of 35 U.S.C. § 285 and awarding treble damages and attorney fees and costs to National; and

9. Awarding National such other relief as the Court deems just and proper.

DEMAND FOR JURY TRIAL

Pursuant to Rule 38 of the Federal Rules of Civil Procedure, National demands a trial by jury on all issues triable of right by a jury.

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Dated: July 25, 2008
875565

EXHIBIT A

United States Patent [19]

Koh

[11] **Patent Number: 4,567,058**

[45] **Date of Patent: Jan. 28, 1986**

[54] **METHOD FOR CONTROLLING LATERAL DIFFUSION OF SILICON IN A SELF-ALIGNED $TISi_2$ PROCESS**

[75] Inventor: **Yun B. Koh**, Sunnyvale, Calif.

[73] Assignee: **Fairchild Camera & Instrument Corporation**, Mountain View, Calif.

[21] Appl. No.: **634,937**

[22] Filed: **Jul. 27, 1984**

[51] **Int. Cl.**[4] **B05D 3/06**; B05D 5/12; B44C 1/22; C03C 15/00

[52] **U.S. Cl.** **427/55**; 156/643; 156/662; 427/93; 427/399

[58] **Field of Search** 427/53.1, 55, 87, 93, 427/399; 156/643, 662

[56] **References Cited**

PUBLICATIONS

Wahl, G. et al, *The CVD Deposition of Ti–Si Containing Coating on Ni–Base Super Alloys*, pp. 685–698, Electrochemical Society, N.J., 1981.

Shibata, T. et al., *Metal Silicon Reactions Induced by CW Scanned Laser and Electron Beams*, Stanford Electronic Laboratory, Mar. 1981, pp. 637–644.

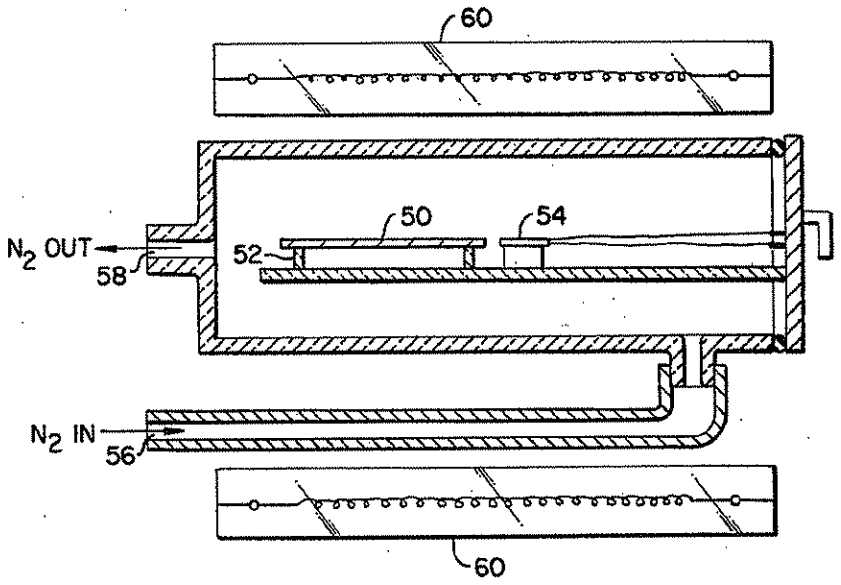
Primary Examiner—Michael R. Lusignan

Attorney, Agent, or Firm—Townsend and Townsend

[57] **ABSTRACT**

An improved method for forming a titanium silicide layer comprising placing a silicon layer overcoated with titanium in an ambient atmosphere of ultrapure nitrogen and heating the overcoated layer with radiation from a tungsten-halogen source.

18 Claims, 8 Drawing Figures



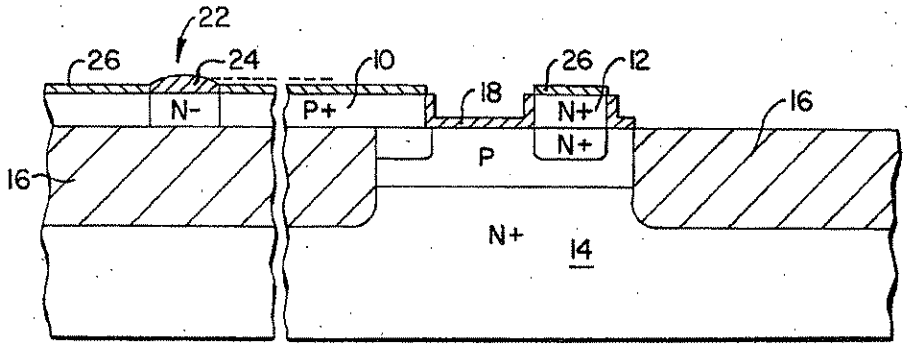


FIG. 1A.

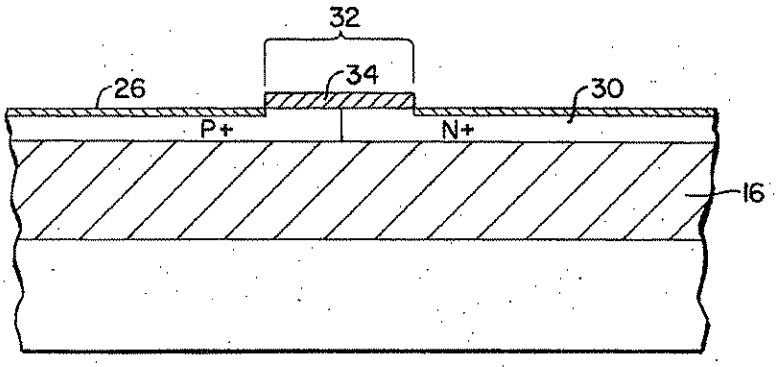


FIG. 1B.

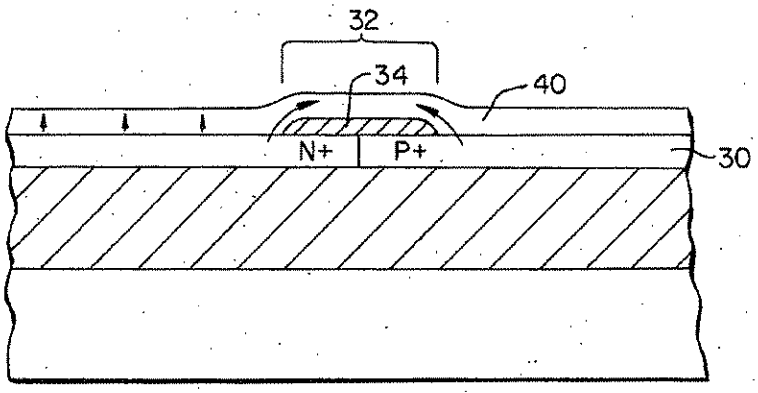


FIG. 2.

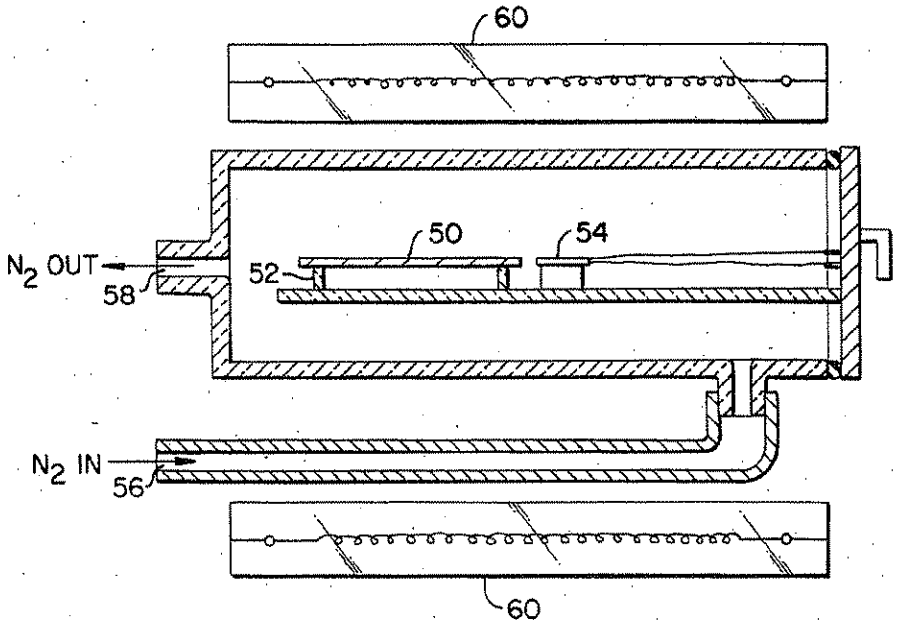


FIG. 3.

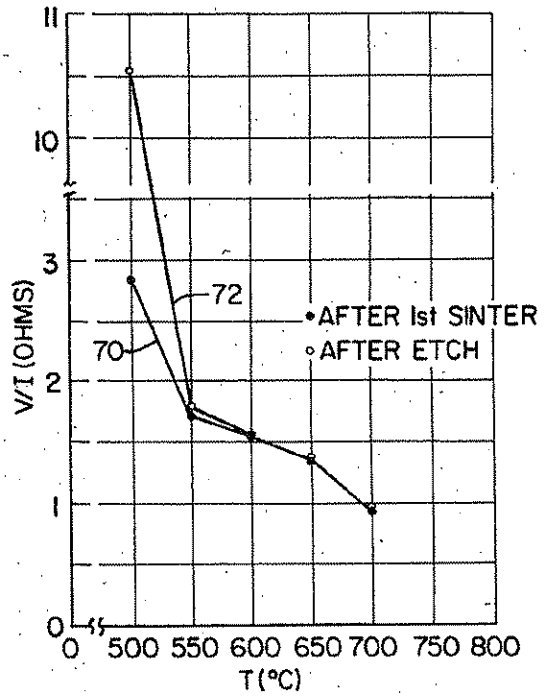

11
10
3
2
1
0
V/I (OHMS)
72
70
•AFTER Ist SINTER
◦AFTER ETCH
0 500 550 600 650 700 750 800
T(°C)

FIG._4A.

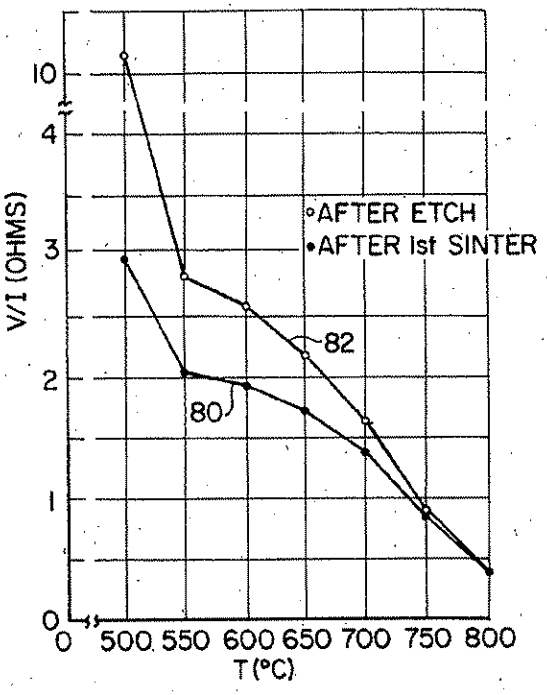

10
4
3
2
1
0
V/I (OHMS)
◦AFTER ETCH
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82
80
0 500 550 600 650 700 750 800
T(°C)

FIG._4B.



FIG. 5A.

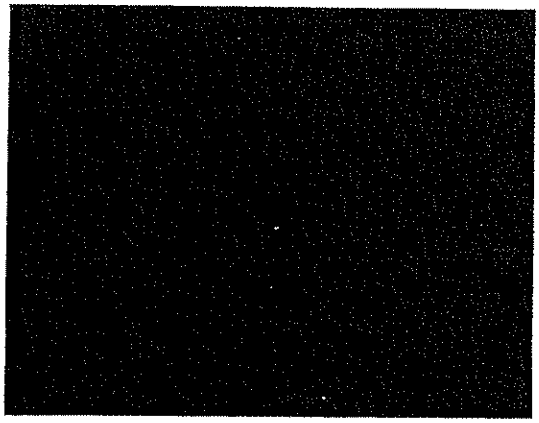


FIG. 5B.

METHOD FOR CONTROLLING LATERAL DIFFUSION OF SILICON IN A SELF-ALIGNED $TISI_2$ PROCESS

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates generally to semiconductor processing, and more particularly to preventing lateral diffusion of silicon during the formation of a titanium silicide layer.

2. Description of the Prior Art

An important technique for reducing the scale of monolithic semiconductor structures to two micrometers is a self-aligned titanium silicide process.

In this process, titanium silicide is formed on the upper surface of a polycrystalline silicon (poly) line to dramatically increase the conductivity of the poly line and to obviate the need for an extra masking step to form metal contacts. These lines are generally formed over a field oxide layer formed on the upper surface of a monocrystalline silicon substrate. A pair of poly lines may terminate on the exposed surface of the substrate with a small gap formed between the terminal ends of the lines.

Often it is necessary to prevent titanium silicide formation over selected regions of exposed silicon. A passivating oxide layer is formed over these selected regions and utilized to prevent titanium silicide formation.

For example, a resistor, diode, or other active device may be formed in a region of a poly line. If the titanium silicide layer overcoated this region, then the active device would be short circuited. Alternatively, the terminal ends of a pair of lines may form the base and emitter contacts of a bipolar transistor. If the titanium silicide layer overcoated the exposed region of the substrate, disposed between these terminal ends, then the transistor would be shorted. Accordingly, the passivating oxide layer is utilized to prevent titanium silicide formation over these active regions.

In the self-aligned titanium silicide process, the entire upper surface of the structure, including the substrate and poly lines, is overcoated with a layer of titanium. A first region of the titanium layer overcoats the passivating oxide layer while a second region overcoats the exposed surfaces of the polycrystalline silicon lines.

Subsequently, the entire structure is sintered in an ambient atmosphere of a selected gas to convert the titanium disposed over the exposed surface of the polysilicon into titanium silicide.

Ideally, the titanium disposed over the passivating oxide layer is not converted into titanium silicide but remains metallic titanium.

Next, the metallic titanium is selectively etched from the structure. Thus, titanium silicide layers with their edges self-aligned to the edges of the passivating oxide layer are formed.

Unfortunately, the ideal titanium to titanium silicide conversion process described above is not realized in practice. During this conversion process, silicon atoms diffuse vertically and laterally into the titanium layer. It is the vertical diffusion which causes the titanium disposed over the exposed surface of the silicon to convert into titanium silicide. However, the lateral diffusion of the silicon atoms also causes titanium silicide to form over the passivating oxide layer. Unless the conversion rate is carefully controlled a titanium silicide layer may be formed over the passivating oxide layer, thereby

forming a titanium silicide connection over the passivating oxide layer and shorting out the active device disposed below the passivating layer.

Additionally, silicon oxide itself reacts with the metallic titanium to form various conducting compounds. These compounds are not completely removed from the surface of the oxide during the selective etch process. Thus, leakage currents from either the transistor or the active device diminish the performance of the structure.

Accordingly, new processes are being actively developed to reduce lateral diffusion and prevent the formation of leakage currents.

SUMMARY OF THE INVENTION

The present invention provides a novel method for reducing lateral diffusion of silicon into titanium during the titanium to titanium silicide conversion process and for removing residual conductive material from the surface of the field oxide layer overcoating a silicon substrate.

As described above, in the titanium silicide self-aligned process, a passivating oxide layer is disposed on the exposed surface of either a poly line or monocrystalline layer. The upper surfaces of the silicon and the oxide are overcoated by a titanium layer. The entire structure is then sintered to convert the regions of the titanium layer disposed over exposed silicon into titanium silicide.

In a preferred embodiment of the present invention, the titanium overcoated structure is placed in an airtight chamber and an ambient atmosphere of ultrapure gaseous nitrogen is introduced in the chamber. The structure is then exposed to radiation from Tungsten-halogen lamps to heat the structure to a predetermined temperature for a predetermined time. This heating, or sintering, converts the regions of the titanium layer overcoating the exposed surface of poly or monocrystalline silicon into titanium silicide.

Typically, this sintering process has been performed in an argon gas atmosphere. The reaction time of the titanium to titanium silicide conversion process is extremely fast in the argon ambient thereby precluding control of the rate of the reaction. Consequently, it was impossible to control the rate of titanium silicide formation so that the titanium metal above the exposed regions of silicon could be completely converted while preventing the formation of titanium silicide connections over the passivating oxide layer.

The success of self alignment is dependent on how well the lateral diffusion of silicon is controlled, without sacrificing vertical diffusion for the maximum silicide growth on the exposed silicon regions. The utilization of a nitrogen ambient slows the rate of conversion sufficiently to allow precise control of the rate of conversion. In a nitrogen ambient the rate of reaction increases slowly over a broad temperature range. Thus, the reaction temperature may vary without catastrophically increasing the reaction rate. This slow rate of change is important since temperature control during the reaction is imprecise. Accordingly, a temperature and reaction time may be selected to fully convert the titanium disposed over the exposed silicon while retarding lateral diffusion to prevent the formation of a titanium silicide layer over the passivating oxide layer.

According to one aspect of the invention, approximately 600 Angstroms of titanium is deposited on the

structure. Active structures, or gaps on the order of two micrometers, are overcoated by passivating oxide layer. The structure is then heated to a temperature of between about 500° to about 800° Centigrade by exposing the structure to radiation from the tungsten halogen lamp for approximately ten seconds.

According to another aspect of the invention, after the termination of the sintering step described above, unconverted metallic titanium is selectively etched from the surface of the structure. Because the primary goal of the above sintering step was to convert metallic titanium to titanium silicide on the exposed silicon surfaces without forming titanium silicide connections over the passivating oxide regions the conductivity of the titanium silicide layer has not been maximized. Thus, after the selective etching process has been completed the structure is sintered a second time in a nitrogen ambient including a trace of oxygen. This oxygen oxidizes the trace conductive residues left on the oxide surfaces and increases the isolation of the active devices in the structure. It lowers reverse junction leakage currents by two orders of magnitude.

BRIEF DESCRIPTION OF THE DRAWINGS

FIGS. **1A** and 1B are cross-sectional views of a semiconductor structure having polysilicon lines overcoated with titanium silicide.

FIG. **2** is a cross-sectional view of an active device in a polysilicon line.

FIG. **3** is a schematic diagram of an apparatus utilized for performing the method of the present invention.

FIGS. **4A** and **4B** are graphs depicting the titanium to titanium silicide conversion rate in argon and nitrogen ambient atmospheres, respectively.

FIGS. **5A** and **5B** are photographs illustrating the effect of the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

The present invention is a method for reducing lateral diffusion of silicon during a titanium silicide self-aligned process and for removing residual conductive traces from the surfaces of the field oxide layers on a structure formed by the process. To better understand the invention, a brief description of a semiconductor structure formed by a titanium silicide self-aligned process and the steps for forming the titanium silicide layer will be presented. Next, the lateral diffusion or "crawl out" problem will be described with reference to FIG. **2**. Finally, the process of the present invention will be described with reference to FIGS. **3** and **4**.

Referring now to FIG. **1**, a cross-sectional view of a bipolar semiconductor structure utilizing polysilicon contact lines with titanium silicide layers formed thereon to increase the conductivity of the polysilicon lines is presented. In FIG. **1A**, the poly lines form base and emitter contacts **10** and **12**, respectively, of a bipolar transistor. The emitter contact **12** is an N^+ doped polycrystalline silicon line with a terminal end disposed on the exposed surface of a monocrystalline silicon substrate **14**. The base contact line **10** is a P^+ doped polycrystalline line with a terminal end disposed over the surface of the monocrystalline substrate and with the remainder disposed over the isolation field oxide region **16** of the semiconductor structure. The exposed surface of the silicon substrate **14** positioned between the terminals of the emitter and base contact lines **12** and **10** is overcoated with a passivating oxide layer **18**.

The resistor **22** is overcoated by a second passivating layer **24**. The surface of the polysilicon lines **10** and **12** not covered by a passivating oxide layer is termed the exposed surface regions while those surfaces covered with a passivating oxide layer **24**, for example, the surface of the N^- resistor **22**, are termed unexposed surface regions. The exposed surface regions of the polysilicon lines **10** and **12** are covered with a titanium silicide layer **26**.

In FIG. **1B** another section of the semiconductor structure is depicted. There, a polysilicon line **30** is disposed on the field oxide of the semiconductor structure. A P^+/N^+ diode **32** is formed in the polysilicon line **30**. The diode is overcoated by a third passivating oxide layer **34**. The exposed surface of the polysilicon line is overcoated by a titanium silicide layer **26**. Two distinct silicon structures are illustrated in FIGS. **1A** and **1B**. In the first, the passivating oxide layer is disposed over an active device formed in a polysilicon line. In the second, the passivating oxide layer is disposed over the surface region of the monocrystalline substrate positioned in the gap between the terminal ends of two poly lines.

It is the purpose of the passivating oxide layers **18**, **24** and **34** to prevent the formation of titanium silicide over the surface of the silicon disposed thereunder.

As depicted in FIGS. **1A** and **1B**, the titanium silicide layer **26** overcoating the exposed surfaces of the polysilicon lines **10**, **12**, and **30** is interrupted by passivating oxide layers **18**, **24**, and **34** disposed over active devices in the semiconductor structure. These interruptions in the titanium silicide layer **26** are critical to the functions of the various active devices. For example, consider the N^- resistor **22**. If the titanium silicide layer extended across the passivating oxide layer **24** overcoating the resistor **22** then current would flow through the layer **26**, thereby short circuiting the resistor **22**. The situation for the diode **32** is similar. Further, if the titanium silicide layer extended over the passivating layer **18** disposed over the portion of the silicon substrate **14** positioned in the gap between the terminals of the emitter and base contact lines **10** and **26** these terminals would be shorted, thereby shorting out the transistor.

The titanium silicide layers are prevented from forming over the passivating oxide layers **18**, **24**, and **34** by a self-aligned process. This process will now be described with reference to FIG. **2**. In FIG. **2** an intermediate step in the formation of the N^+/P^+ diode **32** is depicted. The passivating oxide layer **34** overcoating the diode **32** was formed by therma oxidation of a window etched in a silicon nitride layer disposed over the polysilicon line **30**. This silicon nitride layer was subsequently removed, leaving all the upper surface of the polysilicon line **30** exposed except for the region under the passivating oxide layer **34**. Subsequently, a titanium layer **40** was deposited over the entire structure. This titanium layer **40** is utilized to form the titanium silicide layer overcoating the exposed regions of the polysilicon lines.

The self-alignment of the edges of the titanium silicide layer to the edges of the passivating oxide layer is achieved by the following process. The titanium overcoated structure is sintered by heating the structure to a predetermined temperature for a predetermined time. This heat causes the titanium over the exposed surfaces of the polysilicon line **30** to react with the polysilicon to form titanium silicide. The titanium disposed over the passivating oxide layer **34** is not reacted and remains metallic titanium. Subsequently, the structure is placed

in an etching solution, typically $NH_4OH + H_2O_2$ (1:3 by volume), which selectively etches metallic titanium from the surface of the silicon structure. Thus, titanium silicide layers **26** are formed only over the exposed surfaces of the polysilicon line and all conductive material is removed from the surface of the passivating oxide layer **34**. Note also that since the titanium layer **40** extends over the entire surface of the structure that this selective etching process also removes conductive material from the surfaces of the field oxide layer **16**.

Unfortunately, undesired reactions take place in the above-described sintering process that cause the formation of titanium silicide over the surface of the passivating oxide layer and the formation of other conducting titanium compounds on the exposed surface of the field oxide layer **16**.

The titanium silicide formed on the surface of the passivating oxide layer **34** is formed by lateral diffusion of silicon from the exposed surface of the polysilicon line **30**. During the sintering process silicon atoms diffuse into the titanium layer **40**. It is this diffusion that contributes to the conversion of the titanium into titanium silicide. The reaction must proceed at a predetermined rate for a predetermined time to completely convert the titanium disposed over the exposed regions of the polysilicon line into titanium silicide to maximize the magnitude of the conductivity of the polysilicon line **30**. While this vertical diffusion is taking place, silicon atoms are also diffusing laterally into the metallic titanium disposed over the passivating oxide layer **34**. If the reaction proceeds for a sufficient period of time the atoms diffusing from opposite sides of the passivating oxide layer will from a titanium silicide layer completely overcoating the passivating oxide layer, thus forming a titanium silicide connection thereover. Accordingly, the rate of reaction and time of reaction must be controlled to complete convert the titanium disposed over the exposed regions while preventing the formation of a titanium silicide connection over the passivating oxide layer **34**. This control of the lateral diffusion problem is the most critical factor to the success of the titanium self-alignment process. The method of the present invention provides a good control over the lateral diffusion problem and thereby allows the formation of active devices in the semiconductor structure on the scale of 1–2 microns.

Additionally, metallic titanium reacts with the silicon dioxide itself to form certain ternary conductive titanium compounds. These compounds are not completely removed by the selective etching process, thus leaving conductive residues on the surface of the field oxide regions. These conductive residues cause leakage currents which degrade the performance of the bipolar active devices. Accordingly, means for removing these conductive residues are highly desirable and provided by the present invention.

In FIG. **3** the apparatus used for performing the process of the present invention is depicted. The apparatus includes an airtight chamber **50** with a substrate holder **52** disposed therein. The substrate holder **52** includes a thermocouple **54** for measuring the temperature of the substrate. The air chamber includes a gas inlet **56** for introducing selected gases into the chamber and a gas outlet **58** for removing gases from the chamber. Banks of tungsten halogen lamps **60** are utilized to heat a structure mounted on the substrate holder **52**.

In practice, a heatpulse 210T manufactured by AG Associates of Palo Alto, Calif. was utilized for performing the process of the invention. In this reactor the structure is exposed to intense radiation from the tungsten halogen lamps **60** for periods of about 10 seconds. In existing processes, the airtight chamber is filled with an ambient atmosphere of argon gas during the heating step.

FIG. **4A** is a graph depicting the rate of titanium to titanium silicide conversion for a 600 Angstrom thick titanium layer in an ambient atmosphere of argon. Referring now to FIG. **4A**, the temperature of the reaction is given by the position of the line on the X axis while the resistivity in ohms of the silicide is given by the position on the Y axis. A first line **70** depicts the resistivity as a function of temperature after the first sintering step has been completed. A second line **72** depicts the resistivity as a function of the temperature after the first etch has been completed. The difference between these lines **70** and **72** is an indication of the rate at which the conversion of titanium to titanium silicide is progressing.

As described above, metallic titanium is removed in the selective etching step. Thus, if metallic titanium remained after the sintering step were completed, the resistivity would be greater after the selective etch than before the selective etch because the resistivity of metallic titanium is much less than the resistivity of titanium silicide. For example, at 500° C. there is a large difference between the resistivity before and after the selective etch, thus indicating that a large amount of metallic titanium remains unconverted at 500° C. At 550° C. there is little difference in resistivity indicating that the entire thickness of titanium had been converted to titanium silicide. Note that above 550° C. the conversion of titanium to titanium silicide is completed in the 10 second sintering period, thereby indicating an extremely high conversion rate. Note also from the graph that significant control of the conversion rate in an argon ambient may only be achieved in the 500° C. to 550° C. temperature range. Once the temperature of the substrate is above 550° C. the conversion rate is very high and uncontrollable.

As described above with reference to FIG. **2**, during the sintering step the diffusion of silicon atoms into the metallic titanium layer proceeds both vertically and laterally. Thus, the rate of reaction determines the time required to convert all the titanium disposed above the exposed surface of the polysilicon line into titanium silicide and also determines the distance over the passivating oxide layer over which titanium silicide will be formed. Since the structure is heated for a period of about 10 seconds the control of the reaction rate is achieved through temperature control. However, due to limitations in existing reaction chambers, precise temperature control is not achievable. Because of the narrow temperature range over which the reaction could be controlled in an argon ambient it was found that significant production problems resulted from shorts due to lateral diffusion or "crawl out" during the fabrication of two micron scale structures. Temperature drifts outside of the 550° C. range caused the titanium to titanium silicide conversion reaction to proceed at such a high rate that titanium silicide connections were formed over the passivating oxide layers.

In the present invention, the sintering step is performed in an ambient atmosphere of ultrapure nitrogen (N_2). FIG. **4B** depicts the resistivity to temperature curves of the silicide for a 600 Angstrom thick metallic titanium layer deposited on the structure. A first line **80**

depicts the dependence of the resistivity on temperature after the first sintering step and a second line 82 depicts the dependence of resistivity temperature after the completion of the first etch. From the discussion above relating to FIG. 4A, it is apparent that the reaction proceeds at a controllable rate from a temperature of 500° C. up to a temperature of about 800° C. Thus the temperature range over which the reaction may be controlled is great enough to compensate for the difficulties in obtaining precise temperatures during the reaction process.

Experimental results indicate that lateral diffusion or "crawl out" problem is substantially reduced utilizing the techniques of the present invention. Referring now to FIGS. 5A and B, an example of the control of lateral diffusion afforded by the present invention is depicted. In FIG. 5A a photograph of titanium silicide overcoated poly lines formed at 800° C. for ten seconds in an N_2 ambient is shown. In FIG. 5B the same line structure formed at 800° C. in 10 seconds in an argon ambient is depicted. Note that the structure formed in the argon ambient has greater than 5 microns lateral diffusion or "crawl out" and that all lines are shorted. In contrast, the structure in FIG. 5A shows clean line definition with no lateral diffusion or "crawl out."

As described above, the primary goal of the sintering step is to completely convert the titanium disposed above the exposed polysilicon regions into titanium silicide while preventing the formation of titanium silicide connections over the passivating oxide layers. The subsequent selective etch removes metallic titanium from the surface of the passivating oxide layers, thereby removing the lateral diffusion or "crawl out" problem. The conductivity of the titanium silicide overcoated polysilicon lines is substantially increased by resintering the structure in an N_2 ambient, at a higher temperature after the etch.

It was discovered that significant leakage currents developed after the selective etch process had been completed. These leakage currents were attributed to traces of conductive residues formed by interaction of the metallic titanium layer with the surface of the field oxide layer itself. These conductive residues were not removed during the selective etching process. Accordingly, a trace of oxygen was introduced into the ambient atmosphere during the second sintering step to oxidize the conductive residues into nonconductive materials. These magnitude of the above-described leakage currents was found to be significantly reduced after this oxidation step.

The foregoing is a detailed description of a preferred embodiment of the invention. Although specific materials, thicknesses, and processes have been described to illustrate and explain the invention, these details should not be interpreted as limiting the invention, which instead, is defined by the scope of the appended claims.

What is claimed is:

1. A method for forming a titanium silicide layer on the surface of a silicon layer comprising the steps of:
   - overcoating the surface of the silicon layer with titanium;
   - placing said overcoated silicon layer in an ambient atmosphere of ultrapure nitrogen; and
   - exposing said overcoated silicon layer to radiation from a tungsten-halogen source to heat said overcoated layer.

2. The method of claim 1 further comprising the step of:
   - controlling the intensity of said radiation and the time period of said exposure to heat said silicon layer to a predetermined temperature.

3. The method of claim 2 further comprising the steps of:
   - selecting said period of time to be about 10 seconds;
   - selecting the thickness of said titanium layer to be about 600 Angstroms; and
   - selecting said predetermined temperature to be in the range of about 500° C. to about 800° C.

4. A method for forming a titanium silicide coating on the exposed surface region of a silicon structure, with the upper surface of the silicon structure being divided into an unexposed region overcoated with a first oxide layer and an exposed region not overcoated with the first oxide layer, and with the exposed region of the silicon structure and the upper surface of said first oxide layer being overcoated with a titanium layer, said method comprising the steps of:
   - placing said overcoated silicon structure into an airtight chamber;
   - providing an ambient atmosphere in said airtight chamber of ultrapure, gaseous nitrogen (N_2); and
   - sintering said titanium layer by exposing said structure to radiation from a tungsten-halogen source, said radiation being of a predetermined intensity, and said exposure being for a predetermined period of time to form a layer of titanium silicide along the exposed surface of said silicon structure.

5. The method of claim 4 further comprising the step of:
   - selecting the magnitude of said predetermined intensity and said period of time to fully react the titanium disposed above said exposed surface while preventing lateral diffusion from forming a titanium silicide connection over said oxide layer.

6. The method of claim 5 further comprising the step of:
   - providing a silicon structure comprising a monocrystalline, silicon substrate, overcoated with a field oxide layer, having a polysilicon line disposed on the surface of said field oxide layer with said first oxide layer disposed on the upper surface of said polysilicon line and with the remaining upper surface of said polysilicon line being said exposed surface.

7. The method of claim 6 further comprising the step of:
   - positioning said first oxide layer over an active device disposed in said polysilicon line.

8. The method of claim 5 further comprising the step of:
   - selecting said silicon structure to be a monocrystalline silicon substrate with a pair of polycrystalline silicon (poly) lines with the terminal ends of said poly lines separated by a gap disposed on the upper surface of said monocrystalline substrate.

9. The method of claim 8 further comprising the step of:
   - positioning said oxide layer in the gap separating said poly lines to cover the upper surface of said substrate positioned in said gap.

10. The method of claim 7 or claim 9 further comprising the step of:
   - providing an oxide layer with a cross-sectional dimension of about two micrometers.

11. The method of claim 10 further comprising the step of:

selecting said period of time to be about ten seconds.

12. The method of claim 11 further comprising the step of:

selecting the intensity of said radiation to heat said structure to a temperature in the range of about 500° C. to about 800° C.

13. The method of claim 12 further comprising the step of:

selecting the thickness of said oxide layer to be about 600 Angstroms.

14. The method of claim 7 further comprising the step of:

selecting said active device to be a resistor.

15. The method of claim 7 further comprising the step of:

selecting said active device to be a diode.

16. A method for forming a titanium silicide coating on the exposed surface region of a silicon structure, with the upper surface of the silicon structure being divided into an unexposed region overcoated with a first oxide layer or a field oxide layer and an exposed region not overcoated with the first oxide layer or field oxide layer, and with the exposed region of the silicon structure and the upper surface of said first oxide layer being overcoated with a titanium layer, said method comprising the steps of:

placing said overcoated silicon structure in an airtight chamber;

providing an ambient atmosphere in said airtight chamber of ultrapure, gaseous nitrogen (N_2);

sintering said titanium layer by exposing said structure to radiation of a predetermined intensity, from a tungsten-halogen source, for a predetermined period of time to form a layer of titanium silicide along the exposed surface of said silicon structure;

selectively etching titanium from the upper surface of said first oxide layer and said field oxide layer;

providing an ambient atmosphere of gaseous nitrogen (N_2) including a trace of oxygen (O_2);

resintering said structure by reexposing the structure to said radiation to increase the conductivity of the titanium silicide layer formed by said first sintering step and to oxidize trace amounts of conductive material on the surface of said oxide layers to reduce leakage from active devices in said polysilicon line.

17. A method of removing conductive titanium compounds from the surface of a silicon dioxide layer comprising the steps of:

placing said layer in an ambient atmosphere of nitrogen and a trace of oxygen; and

exposing said layer to radiation from a tungsten-halogen source to heat said layer.

18. The method of claim 17 further comprising the step of:

controlling said trace of oxygen to be about 0.1% of the ambient atmosphere.

* * * * *

EXHIBIT B

US005239440A

United States Patent [19]

Merrill

[11] Patent Number: 5,239,440

[45] Date of Patent: Aug. 24, 1993

[54] **ELECTROSTATIC DISCHARGE PROTECTION FOR INTEGRATED CIRCUITS**

[75] Inventor: **Richard B. Merrill**, Daly City, Calif.

[73] Assignee: **National Semiconductor Corporation**, Santa Clara, Calif.

[21] Appl. No.: **930,492**

[22] Filed: **Aug. 14, 1992**

Related U.S. Application Data

[63] Continuation of Ser. No. 452,879, Dec. 19, 1989, abandoned.

[51] **Int. Cl.**[5] **H02H 9/04**; H02H 3/22

[52] **U.S. Cl.** **361/91**; 361/56

[58] **Field of Search** 361/56, 58, 91, 98, 361/111; 357/23.13

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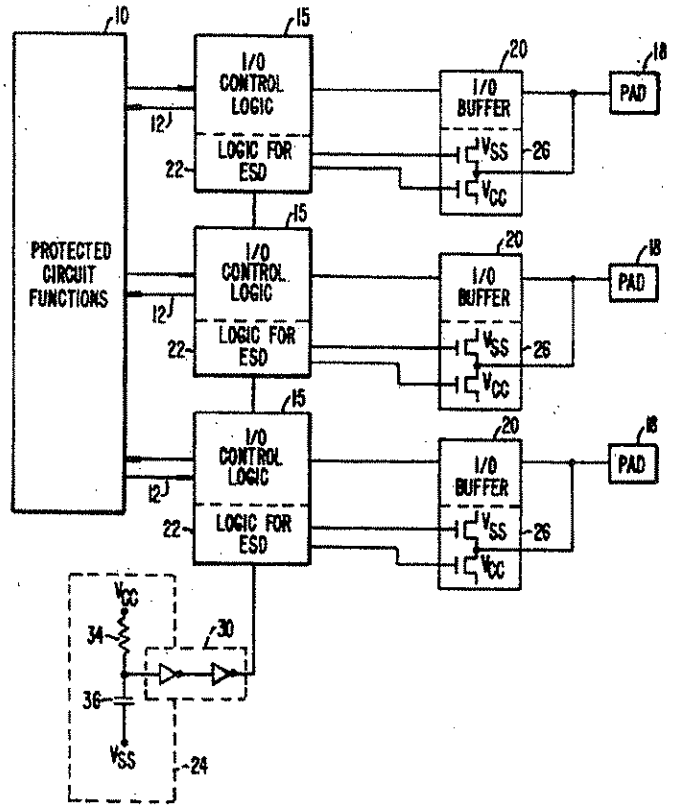
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Primary Examiner—Steven L. Stephan
Assistant Examiner—D. R. Haszko
Attorney, Agent, or Firm—Townsend and Townsend Khourie and Crew

[57] **ABSTRACT**

A circuit is disclosed for protecting an integrated circuit or another circuit from damage due to electrostatic discharge. The protection circuit includes a triggering circuit and a clamping circuit. In response to an electrostatic discharge, the triggering circuit turns on the clamping circuit to clamp a node of the protected circuit to both an upper and a lower potential. This allows the electrostatic discharge to dissipate harmlessly to either potential source, depending upon its polarity. Preferably, the triggering circuit consists of a resistor-capacitor network which generates the required control signal every time power is supplied to the circuit being protected, while the clamping circuit consists of a pair of transistors for connecting an input pin to both the high and low potential sources. Typically, one protection circuit is coupled to each input/output pin of the integrated circuit being protected.

13 Claims, 5 Drawing Sheets



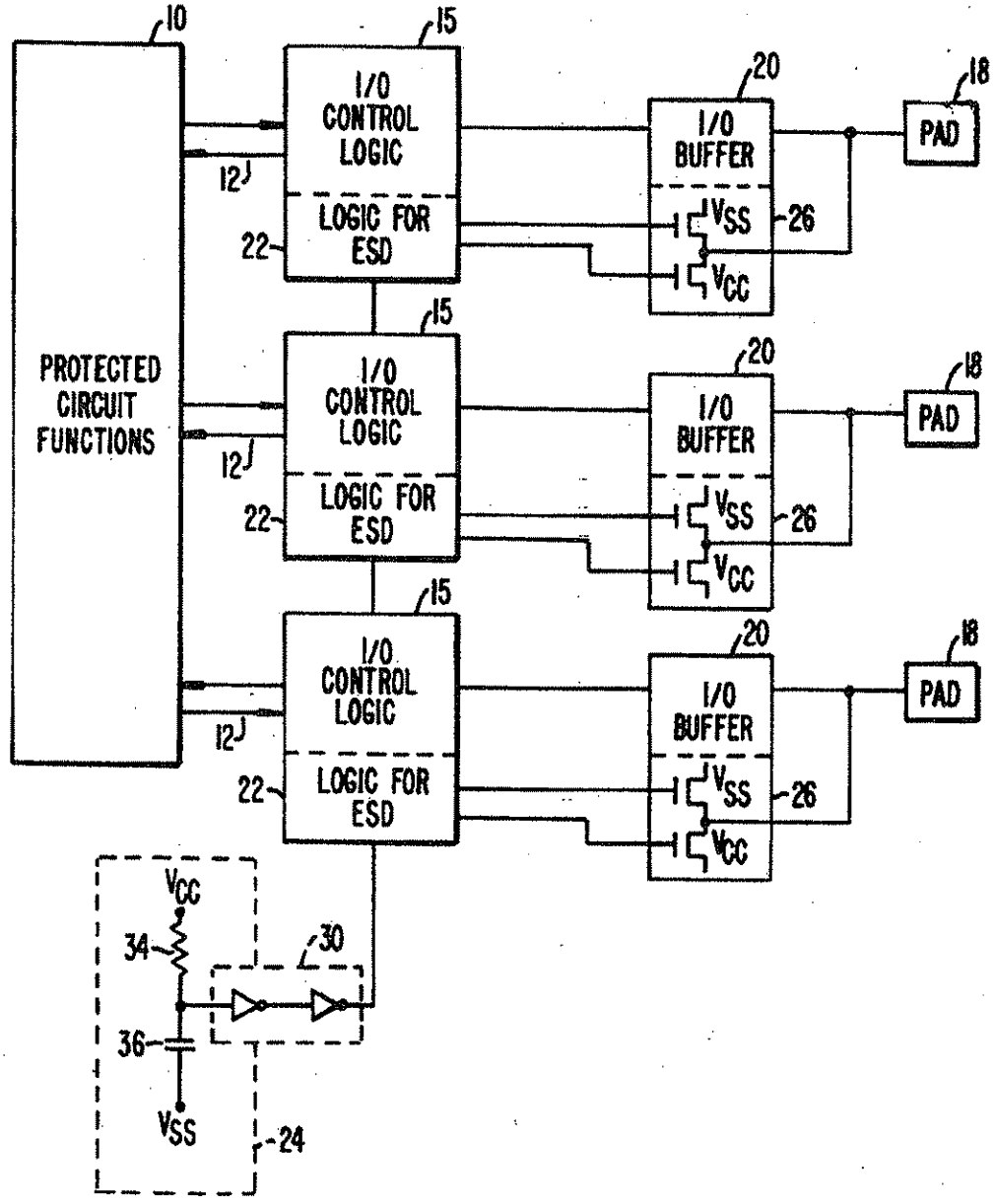

10
15
I/O CONTROL LOGIC
LOGIC FOR ESD
20
I/O BUFFER
18
PAD
12
22
26
V_{SS}
V_{CC}
PROTECTED CIRCUIT FUNCTIONS
34
30
36
24

FIG. 1.

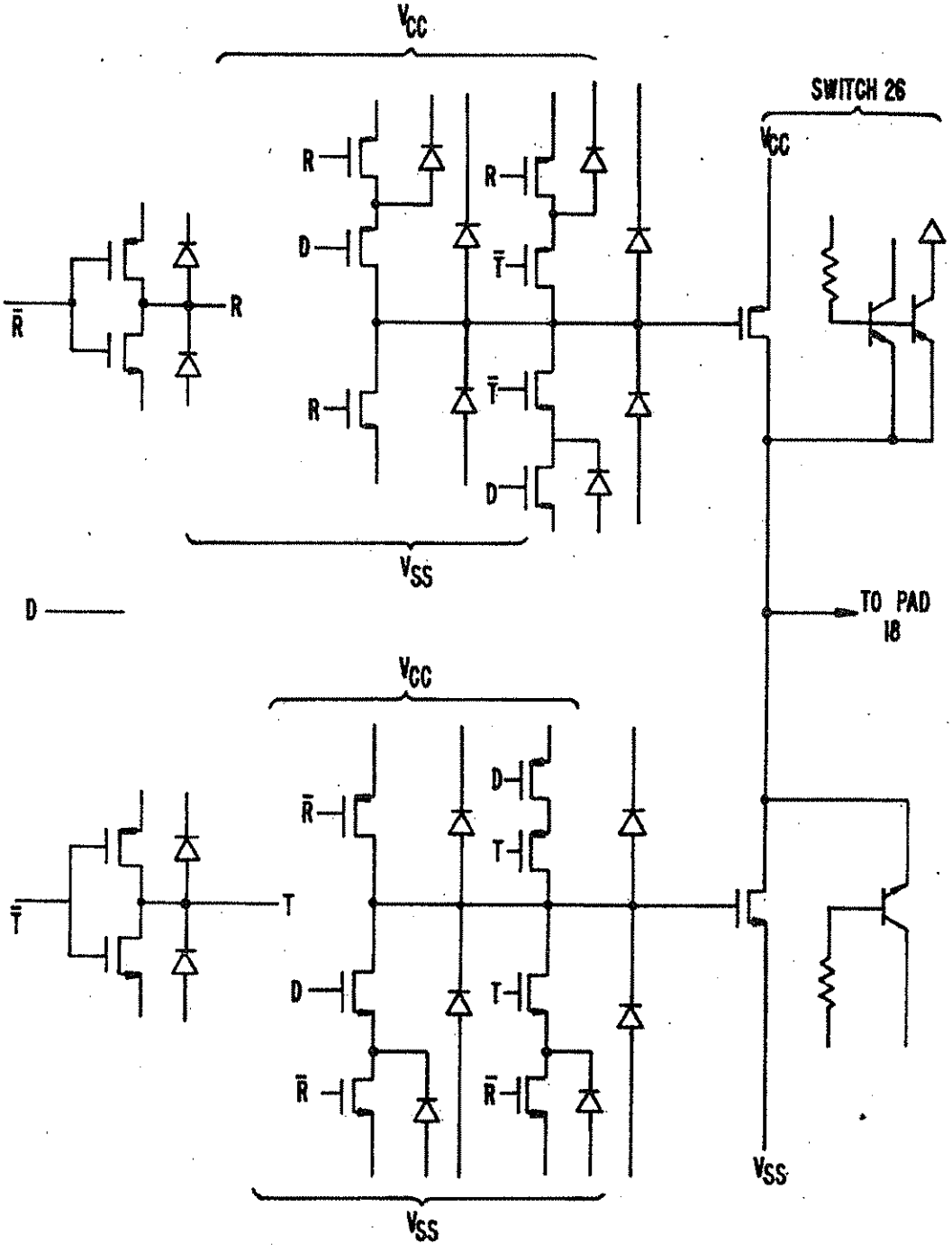

V_{CC}
SWITCH 26
V_{CC}
R
D
R
$\bar{T}$
$\bar{R}$
R
R
$\bar{T}$
D
V_{SS}
D
TO PAD 18
V_{CC}
D
$\bar{R}$
T
$\bar{T}$
T
D
T
$\bar{R}$
$\bar{R}$
V_{SS}
V_{SS}

FIG_2.

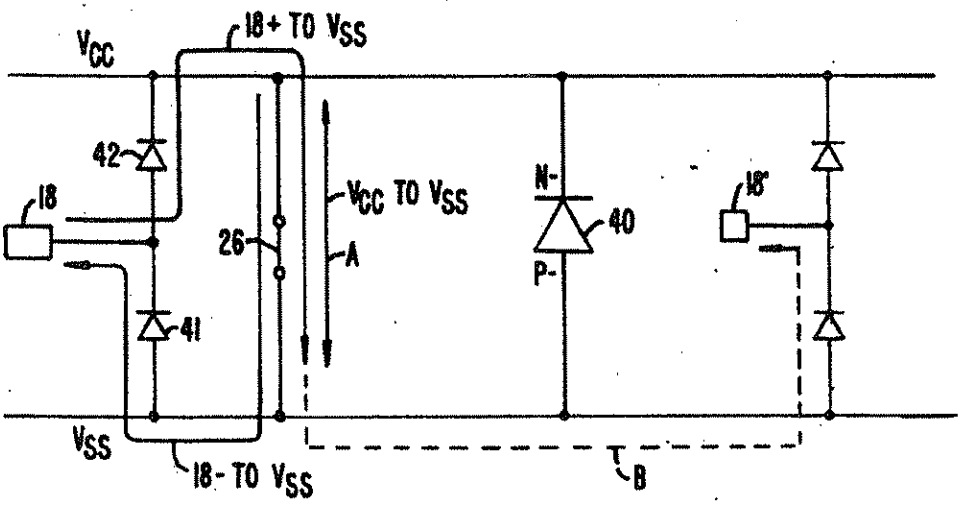


FIG._3.

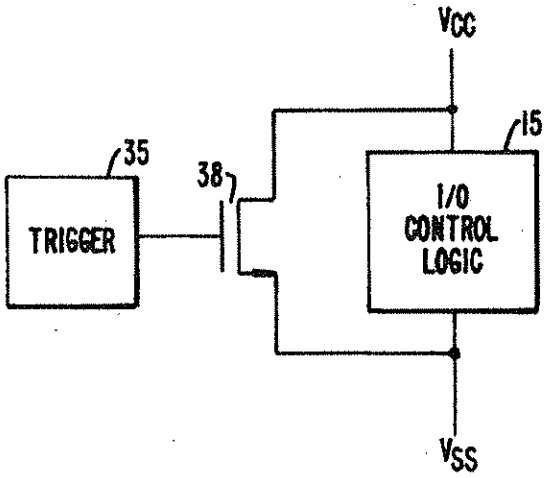


FIG._4.

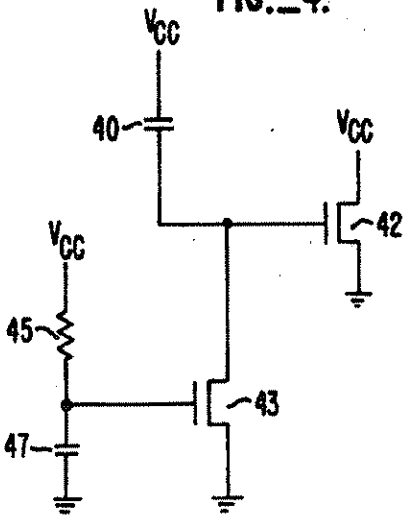


FIG._5.

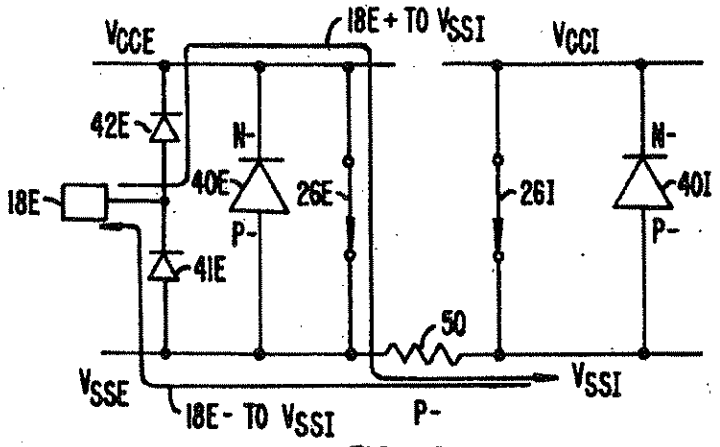


FIG._6A.

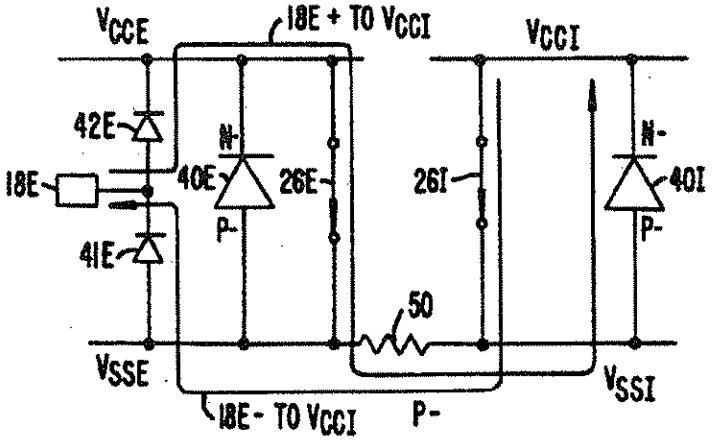


FIG._6B.

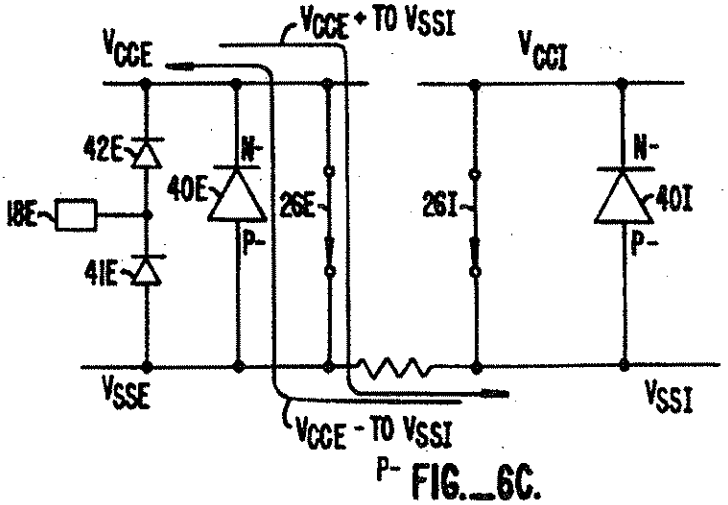


FIG._6C.

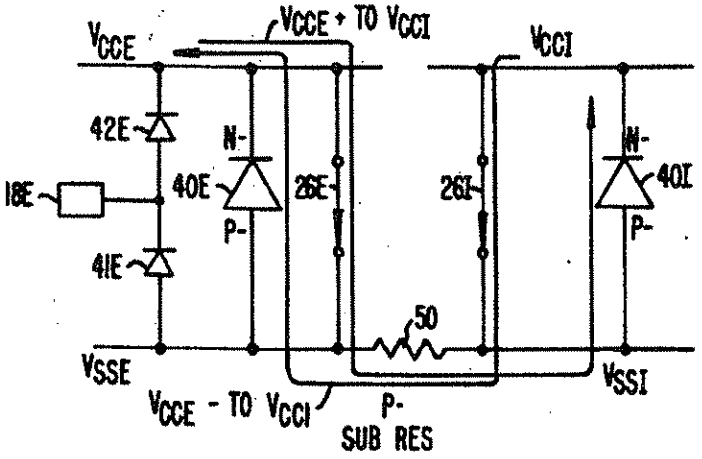


FIG._6D.

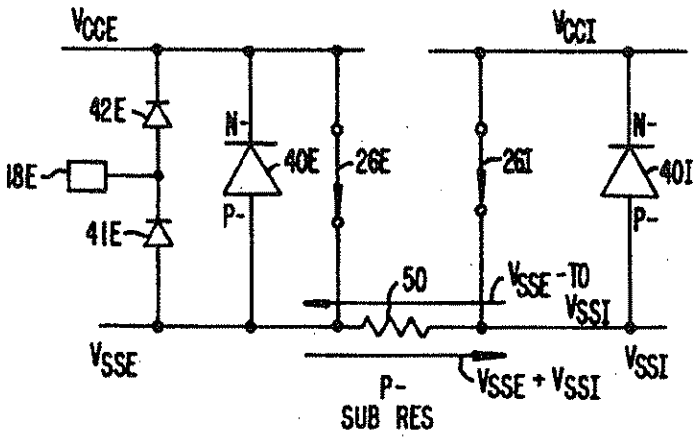


FIG._6E.

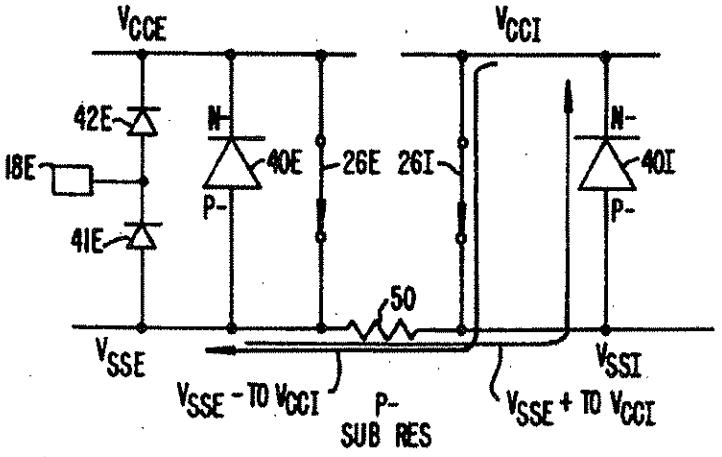


FIG._6F.

ELECTROSTATIC DISCHARGE PROTECTION FOR INTEGRATED CIRCUITS

This is a continuation of application Ser. No. 07/452,879 filed Dec. 19, 1989, now abandoned.

BACKGROUND OF THE INVENTION

1. Field of the Invention

This invention relates to electrostatic discharge protection circuits. More particularly, the invention relates to an electrostatic discharge protection circuit used to protect field effect transistor circuits, especially those with features of one micron or smaller.

2. Description of the Prior Art

Integrated circuits employing field effect devices, commonly termed MOS integrated circuits, have a history of susceptibility to electrostatic discharge. Given the decreasing size of circuit features with ever-improving process technology, static electricity generated by daily activity alone can destroy or substantially harm many MOS circuits. The circuits most susceptible to damage are usually finished circuits which have been packaged, but not yet installed into a finished product. Once installed, other means can protect the chip from damage.

An electrostatic discharge typically occurs when the circuit is touched by an individual handling the circuit before installation; when a static discharge occurs as the packaged circuit slides on its pins across another surface; or more generally, whenever the circuit is exposed to static electricity. Overall, damage from electrostatic discharges is the cause of over half of the devices returned by customers.

One traditional method for protecting integrated circuit devices employing field effect transistors from electrostatic discharge is to use diodes. These diodes are coupled between the input paths of the circuit and the pins to which the power supplies are connected. With electrostatic discharge events of one polarity the diodes are forward-biased, and with discharges of the opposite polarity they are reverse-biased. Normally the discharge that causes the diodes to become reverse-biased is the more problematic, because voltages and power surges seen by the internal logic circuits are higher than for the forward-biased case. Other methods used for protecting MOS circuits from electrostatic discharge damage are almost always variations on the diode clamping system described above.

The traditional methods described above usually function satisfactorily for circuits with large features. As the features of integrated circuits, however, approach one micron and smaller, lower voltages than those which damage larger features can destroy the diodes and the circuit. A more serious problem with double diode clamps is that they are not readily subject to analysis by circuit simulation software. In other words, it has typically been a "hit or miss" approach with double diode clamps to protect circuits from electrostatic discharge. This hit or miss approach inhibits and delays product development, adding trial and error design cycles to product release.

Another complication with electrostatic discharge problems is the increasingly higher customer standards in device reliability and performance. The military, in particular, by imposing standards such as Military Standard 883C have significantly increased the product performance standard over the old standard. This has

the acceptability of previous electrostatic discharge protection techniques.

SUMMARY OF THE INVENTION

This invention provides electrostatic discharge protection circuitry that allows circuit fabrication and analysis using common methods. In particular, the technique of this invention provides a low impedance switch which dissipates static electricity, yet is transparent to normal circuit operation. The circuit of the preferred embodiment satisfies military specifications, and is capable of protecting the newest substantially decreased feature sizes of MOS integrated circuits, not heretofore possible. The invention also protects integrated circuits prior to their installation on circuit boards.

The invention provides a switch between the power supplies driving the integrated circuit, typically Vcc and Vss, that is turned on only during the electrostatic discharge event. Using this technique, an electrostatic discharge event of polarity that would normally reverse-bias the circuits input diodes now can be shunted through forward-biased diodes and a short circuit between Vss and Vcc.

Additionally, electrostatic discharge events of a polarity that tended to reverse-bias the input diodes tends to supply power to Vcc/Vss. This invention makes use of the effect to provide power to the logic that controls the low impedance Vcc/Vss switch.

In the cases of discharges during handling or when not in place on a printed circuit board, the discharge will power up the circuit causing the logic circuit to operate to turn on the clamp. The clamp then allows the electrostatic charge to dissipate through whatever material contacts the circuit pins.

The electrostatic discharge protection circuit of a preferred embodiment is easily fabricated on a chip using well known fabrication processes. The circuit is small, and therefore integrates easily onto an integrated circuit chip with the normal circuitry otherwise present. Importantly, the protection circuit is transparent to the protected circuit's normal operation.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** is a block diagram of a preferred embodiment of the electrostatic discharge protection circuit illustrating its relationship with a circuit being protected.

FIG. **2** illustrates a typical circuit employed to activate the electrostatic discharge protection circuit.

FIG. **3** illustrates the current paths for various discharge polarities between a pin or pins and power supplies.

FIG. **4** illustrates an alternative embodiment of the electrostatic discharge protection circuit.

FIG. **5** illustrates a further alternative electrostatic discharge protection circuit.

FIGS. **6A** to **6F** depict current paths for discharge polarities in multiple supply circumstances.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

FIG. **1** illustrates a preferred embodiment of the electrostatic discharge protection circuit in block form as employed to protect another circuit. As shown in FIG. **1**, a protected circuit **10** has a series of input/output nodes **12**. For simplicity, only three such nodes are shown in the figure; however, it should be understood that in a typical embodiment there may be hundreds of

such nodes. The protected circuit can have any function, but typically will be a digital logic circuit such as a gate array or the like. Data, addresses, and other signals destined for the protected circuit are received at bonding pads **18**, typically positioned around the periphery of an integrated circuit on which all of the circuitry of FIG. **1** is formed. These signals then are supplied to input/output buffers **20** and to input/output control logic **15** before reaching the protected circuit. Of course, in a similar manner, signals originating within the protected circuit, which are destined for circuits outside the integrated circuit being protected, are supplied from the protected circuit through the control logic **15** and buffers **20** to bonding pads **18**.

Importantly, in addition to the conventional circuitry described, the circuit shown in FIG. **1** includes some additional logic **22** for controlling or "triggering" the electrostatic discharge protection circuit **24, 30**. This is described below.

The electrostatic discharge circuit provides a clamp **26** which also acts as a switch, that is, by appropriate means, such as logic **22** turned on between Vcc and Vss, during an electrostatic discharge event. This results in the electrostatic discharge event being discharged in a direction that would normally reverse-bias the input diodes, the worst case in prior art devices. The event thus is shunted through the forward-biased diodes and the short between Vss and Vcc. Because an electrostatic discharge event in the direction that tends to reverse-bias the traditional input diodes is of a polarity that tends to power up Vcc and Vss, this circuit helps provide power to the logic **22** that controls the low impedance switch.

In essence, the trigger circuit **24** shown in FIG. **1** controls the clamps **26** to short Vcc to Vss, or power to ground, whenever an electrostatic discharge event occurs. By adjusting the values of the resistor and capacitor components of the trigger, shorter or longer periods may be employed. In the preferred embodiment, logic circuit **22** is connected through a buffer **30** to the resistor-capacitor circuit **24**. Buffer circuit **30** steps the voltage up from the RC circuit before it is applied to the logic circuit **22**. The capacitor **36** of the trigger circuit is connected to Vss, while the resistor **34** is connected to Vcc.

In operation, the protection circuit uses some of the voltage from the accumulating static electricity to enable the logic **22** to turn on the clamp **26** to dissipate the excess voltage. Because an electrostatic discharge event occurs much faster than 1 microsecond, the RC bypass circuit **24** is set so that the circuit time constant of resistor **34** and capacitor **36** are such that the low impedance switch is on for a period of time in excess of the electrostatic discharge event. A preferred time constant is about 1 microsecond, because it is slow enough to allow the discharge to power the logic circuit and enable the complementary transistors int eh low impedance switch.

The RC bypass circuit **24** is designed not to trigger during normal power supply ramp-up. This is achieved by setting the RC time constant greater than the ESD time constant and less than the circuit board's regular power supply rise time.

Placing the clamp **26** in the I/O buffer **20**, while placing the inverter at the logic output, effectively shields the logic circuit from static electricity damage, yet allows the logic circuit **15** to function normally.

FIG. **2** is a schematic diagram illustrating the extra logic added in block **22** of FIG. **1** to provide electrostatic discharge protection. The circuit shown in FIG. **2** receives three input signals, a reset signal $\overline{R}$ from circuit **24**, a data signal D and a signal $\overline{T}$. Under normal protected circuit conditions only D and T are active. In the event of an electrostatic discharge, however, $\overline{R}$ will go to a low voltage to turn on the low impedance switch **26** on the right-hand side of the circuit. The low impedance switch connects Vcc to Vss, discharging the electrostatic event.

FIG. **3** is a diagram illustrating the discharge paths for several different electrostatic conditions. The circuit of FIG. **3** includes a Vcc rail and a Vss rail. The clamp circuit **26** described in conjunction with FIG. **1** is illustrated as a switch **26'** in FIG. **3**.

To explain the discharge paths, switch **26'** is shown in a closed position as it would be after triggering by an electrostatic event. The diodes **41** and **42** shown in the figure are the input diodes associated with each bonding pad, while the large diode **40** represents the diode formed by the N conductivity type wells and P conductivity type substrate in a typical CMOS semiconductor structure. As shown by the path designated A, if either Vcc or Vss is charged positively with respect to the other, the discharge would be dissipated through the switch to the other rail.

On the other hand, if the electrostatic discharge causes Vcc to be biased positively with respect to the bonding pad **18**, the discharge will flow through switch **26'** and then through diode **41** to bonding pad **18**. If pad **18** is biased more positive than Vss, then the discharge is dissipated through a path from the bonding pad through diode **42**, and thensthrough switch **26'** to Vss.

Also illustrated in FIG. **3** is the pad-to-pad discharge path. If bonding pad **18** is biased by the electrostatic discharge event more positively than pad **18'**, then the charge will be dissipated along path B. If pad **18'** is positive compared to pad **18**, then the charge will be dissipated in a corresponding manner.

FIG. **4** is an alternative embodiment in which the control logic **15** is protected by a trigger circuit **35** driving a single large transistor **38**, instead of the clamp discussed above. The source and drain of the transistor are coupled between Vcc and Vss. During an electrostatic event, the trigger is activated, turning on transistor **38** for a short time to dissipate the excess charge to the power supply, regardless of the polarity of the discharge. Trigger **35** can employ any standard triggering technique. For example, in one embodiment it is activated each time the circuit is turned on by using an RC network such as network **24** in FIG. **1**.

A further embodiment of our invention is shown in FIG. **5**, illustrating a different trigger circuit. As shown therein, a capacitor **40** is connected between Vcc and a field effect transistor **42**. The gate of field effect transistor **42** is, in turn, connected to another field effect transistor **43**, while the source and drain are connected between Vcc and ground. Transistor **43** is connected between the gate of transistor **42** and ground, with the gate of transistor **43** being coupled to an RC network formed by resistor **45** and capacitor **47**.

In operation, a voltage spike or discharge on Vcc will charge capacitor **40** turning on transistor **42** to short Vcc to ground whenever a spike occurs. The RC network has a time constant of about 2 microseconds and prevents Vcc from being connected to Vss (not shown) except during power up or during a pulse on Vcc. In the

preferred embodiment, capacitor **40** and **47** will each be about 2 picofarads, and resistor **45** will be about 1 megohm.

FIGS. **6A–6F** illustrate current paths for discharges of various polarities in a multiple pin circumstance. For an integrated circuit to comply with military standards, it must be capable of dissipating an electrostatic charge of any polarity applied to any one of the multiple power supplies used to drive a circuit. The dissipation of charge in these circumstances is shown in FIGS. **6A–6F**. Each of the figures depicts the input diodes, the substrate N-well diode, and the clamp circuit described in conjunction with earlier figures herein. Corresponding components have been given the same reference numeral in each figure. Each figure also shows the circuitry for each of two pins--pin E and pin I, each pin driven by different power supplies. All pins on an integrated circuit are effectively connected together through a substrate resistance, and this resistance is represented by a resistor **50** shown between the electrostatic discharge protection circuit for pin E and the circuit for pin I.

In FIG. **6A** two electrostatic discharge current paths are depicted. The first current path shows current flow for a circumstance in which the input pin **18E** is biased positively with respect to VssI. In this circumstance, the current flow through the upper diode **42E** to VccE, then through clamp **26E** and substrate resistor **50** to VssI. As also shown in FIG. **6A**, if instead VssI is biased negatively with respect to VssI, then current flow is through resistor **50** and lower diode **41E** to pad **18E**.

FIG. **6B** illustrates two current paths for circumstances in which the input pin is biased positively and negatively with respect to VccI of another pin on the circuit. In the case in which the input pin **18E** is biased positively with respect to VccI, then current flow is through the upper diode **42E**, the low impedance switch **26E**, the substrate resistor **50**, and finally diode **40I** to VccI. For the circumstance in which VccI is biased more positively than the input pin **18E**, then current flow is through switch **26I**, substrate resistor **50**, and lower diode **41E** to pad **18E**.

FIG. **6C** depicts the circumstances in which VccE is biased positively and negatively with respect to VssI. In the case of Vcc being more positive than VssI, the current flow is through switch **26E** in substrate resistor **50** to VssI. In the other circumstance, current flows from VssI through the diode **40E** to VccE.

FIG. **6D** illustrates circumstances in which VccE and VccI are biased with by the electrostatic event opposite polarities. As shown, the current paths are symmetrical. When VccI is biased more positively than VccE, current flows through switch **26I**, through substrate resistor **50** and through diode **40E** to VccE. If VccE is more positive than VccI, current flows in the opposite direction through switch **26E** and diode **40I**.

FIG. **6E** illustrates a simple case in which VssE and VssI are biased by the electrostatic event with respect to each other. As shown, current simply flows from the more positively biased to the less positively biased through the substrate resistor **50**.

FIG. **6F** illustrates the circumstance in which VccI and VssE are biased with respect to each other. In this case, current flowing from VccI passes through switch **26I** and resistor **50**. Current flowing in the opposite direction flows through resistor **50** and diode **40I**.

The techniques described herein were tested to assure their compliance with Military Standard **883C**. In one test various components were manufactured in a manner which allowed the electrostatic discharge techniques described herein to be selectively enabled and disabled. Each part was "zapped" at 3 KeV in accordance with the military specification on a IMCS 3000 ESD tester. All parts passed the test with the protection circuit enabled, and all failed with the circuit disabled.

An important advantage of all of the alternative embodiments described above is their ability to be simulated using conventional circuit simulation techniques. Prior art techniques for protecting circuits from electrostatic discharge were difficult to simulate, and consequently circuits employing them often required modification after fabrication of an integrated circuit employing them. Of course, making significant changes to an integrated circuit after its initial fabrication is extremely expensive and time consuming, often delaying shipment of the protected product for a considerable period. Such delays are highly disadvantageous. In addition, circuits employing the protective techniques described herein satisfy military specifications. According to one military specification, no damage to a circuit must occur if any or all pins are zapped to each of power and ground, and also with respect to other pins.

Although the foregoing has been a description of the preferred embodiment of the invention, it will be obvious to those of skill in the art that variations may be made without departing from the scope of the invention. For example, although in the preferred embodiment the protected circuit, the logic circuit implementing the electrostatic protection and the clamp circuit have all been described as employing field effect transistors, bipolar transistors may be used instead. The scope of the invention is set forth in the appended claims.

We claim:

1. A protection circuit for protecting a functional circuit from electrostatic discharge, the functional circuit having a power supply with a first potential, a low potential source with a potential lower than the first potential, and an input node connected between the power supply and the low potential source, the protection circuit comprising:

a first node connected between the power supply and the input node;

a second node connected between the low potential source and the input node;

triggering means for generating a control signal in response to an electrostatic discharge; and

switch means connected to the triggering means for switchably connecting the first node to the second node in response to the control signal.

2. A protection circuit as in claim **1** wherein the switch means comprises:

a first transistor connected between the input node of the functional circuit and the first node, and

a second transistor connected between the input node and the second node.

3. A protection circuit as in claim **2** wherein each of the first and second transistors is connected to receive the control signal and in response connected to input node to the corresponding first and second nodes.

4. A protection circuit as in claim **3** wherein each of the first and second transistors comprises a field effect transistor.

5. A protection circuit as in claim **1** wherein the triggering means comprises a resistor-capacitor network for triggering the switch means whenever an electrostatic discharge event occurs.

6. A protection circuit as in claim 5 wherein the resistor-capacitor network comprises a serially connected resistor and capacitor between the first node and the second node.

7. A protection circuit as in claim 6 wherein the resistor-capacitor network is chosen to have a time constant greater than the duration of the electrostatic discharge.

8. A protection circuit as in claim 1 wherein the switch means comprises a single transistor connected to the first node and the second node.

9. A protection circuit as in claim 8 wherein the single transistor comprises a field effect transistor having a control electrode connected to the trigger circuit.

10. A protection circuit as in claim 1 wherein the triggering circuit comprises:

a transistor connected between the first node and the second node, whereby an electrostatic discharge on the first node will turn on the transistor to connect the first node to ground.

11. An integrated circuit protected from electrostatic discharge comprising:

a functional circuit having a plurality of connection nodes for performing operations in response to signals supplied to the connection nodes, the functional circuit having a power supply with a first potential, a low potential source with a potential lower than the first potential, and at least a first connection node connected to the power supply and a second connection node connected to the low potential source;

a plurality of switch means, one connected to each of the corresponding ones of the plurality of connection nodes, each switch means for connecting that connection node to both the first and second connection nodes in response to a control signal; and

a triggering circuit for generating the control signal in response to an electrostatic discharge.

12. A protection circuit as in claim 11 wherein the triggering circuit also generates the control signal for a short time each time power is applied to the functional circuit is powered up.

13. An integrated circuit as in claim 12 wherein the triggering circuit is also connected between the first and second connection node.

* * * * *

UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO. : 5,239,440
APPLICATION NO. : 07/930492
DATED : August 24, 1993
INVENTOR(S) : Richard B. Merrill

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

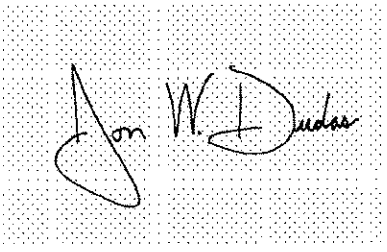
In Column 6, line 60, "connected to" should be --connects the--.

In Column 7, line 13, "trigger circuit" should be --triggering means--.

In Column 7, line 15, "circuit" should be --means--.

Signed and Sealed this

Eighteenth Day of December, 2007



JON W. DUDAS
Director of the United States Patent and Trademark Office

JS 44 (Rev. 12/07)

CIVIL COVER SHEET

The JS 44 civil cover sheet and the information contained herein neither replace nor supplement the filing and service of pleadings or other papers as required by law, except as provided by local rules of court. This form, approved by the Judicial Conference of the United States in September 1974, is required for the use of the Clerk of Court for the purpose of initiating the civil docket sheet. (SEE INSTRUCTIONS ON THE REVERSE OF THE FORM.)

I. (a) PLAINTIFFS

NATIONAL SEMICONDUCTOR CORPORATION

(b) County of Residence of First Listed Plaintiff _____
(EXCEPT IN U.S. PLAINTIFF CASES)

(c) Attorney's (Firm Name, Address, and Telephone Number)

Potter Anderson & Corroon LLP
P.O. Box 951, Wilmington, DE 19899 (302) 984-6100

DEFENDANTS

LSI CORPORATION and AGERE SYSTEMS INC.

County of Residence of First Listed Defendant _____
(IN U.S. PLAINTIFF CASES ONLY)
NOTE: IN LAND CONDEMNATION CASES, USE THE LOCATION OF THE LAND INVOLVED.

Attorneys (If Known)

II. BASIS OF JURISDICTION (Place an "X" in One Box Only)

- ☐ 1 U.S. Government Plaintiff
- ☑ 3 Federal Question (U.S. Government Not a Party)
- ☐ 2 U.S. Government Defendant
- ☐ 4 Diversity (Indicate Citizenship of Parties in Item III)

III. CITIZENSHIP OF PRINCIPAL PARTIES (Place an "X" in One Box for Plaintiff and One Box for Defendant)
(For Diversity Cases Only)

	PTF	DEF		PTF	DEF
Citizen of This State	☐ 1	☐ 1	Incorporated *or* Principal Place of Business In This State	☐ 4	☐ 4
Citizen of Another State	☐ 2	☐ 2	Incorporated *and* Principal Place of Business In Another State	☐ 5	☐ 5
Citizen or Subject of a Foreign Country	☐ 3	☐ 3	Foreign Nation	☐ 6	☐ 6

IV. NATURE OF SUIT (Place an "X" in One Box Only)

CONTRACT
- ☐ 110 Insurance
- ☐ 120 Marine
- ☐ 130 Miller Act
- ☐ 140 Negotiable Instrument
- ☐ 150 Recovery of Overpayment & Enforcement of Judgment
- ☐ 151 Medicare Act
- ☐ 152 Recovery of Defaulted Student Loans (Excl. Veterans)
- ☐ 153 Recovery of Overpayment of Veteran's Benefits
- ☐ 160 Stockholders' Suits
- ☐ 190 Other Contract
- ☐ 195 Contract Product Liability
- ☐ 196 Franchise

REAL PROPERTY
- ☐ 210 Land Condemnation
- ☐ 220 Foreclosure
- ☐ 230 Rent Lease & Ejectment
- ☐ 240 Torts to Land
- ☐ 245 Tort Product Liability
- ☐ 290 All Other Real Property

TORTS

PERSONAL INJURY
- ☐ 310 Airplane
- ☐ 315 Airplane Product Liability
- ☐ 320 Assault, Libel & Slander
- ☐ 330 Federal Employers' Liability
- ☐ 340 Marine
- ☐ 345 Marine Product Liability
- ☐ 350 Motor Vehicle
- ☐ 355 Motor Vehicle Product Liability
- ☐ 360 Other Personal Injury

PERSONAL INJURY
- ☐ 362 Personal Injury - Med. Malpractice
- ☐ 365 Personal Injury - Product Liability
- ☐ 368 Asbestos Personal Injury Product Liability

PERSONAL PROPERTY
- ☐ 370 Other Fraud
- ☐ 371 Truth in Lending
- ☐ 380 Other Personal Property Damage
- ☐ 385 Property Damage Product Liability

CIVIL RIGHTS
- ☐ 441 Voting
- ☐ 442 Employment
- ☐ 443 Housing/ Accommodations
- ☐ 444 Welfare
- ☐ 445 Amer. w/Disabilities - Employment
- ☐ 446 Amer. w/Disabilities - Other
- ☐ 440 Other Civil Rights

PRISONER PETITIONS
- ☐ 510 Motions to Vacate Sentence

Habeas Corpus:
- ☐ 530 General
- ☐ 535 Death Penalty
- ☐ 540 Mandamus & Other
- ☐ 550 Civil Rights
- ☐ 555 Prison Condition

FORFEITURE/PENALTY
- ☐ 610 Agriculture
- ☐ 620 Other Food & Drug
- ☐ 625 Drug Related Seizure of Property 21 USC 881
- ☐ 630 Liquor Laws
- ☐ 640 R.R. & Truck
- ☐ 650 Airline Regs.
- ☐ 660 Occupational Safety/Health
- ☐ 690 Other

LABOR
- ☐ 710 Fair Labor Standards Act
- ☐ 720 Labor/Mgmt. Relations
- ☐ 730 Labor/Mgmt.Reporting & Disclosure Act
- ☐ 740 Railway Labor Act
- ☐ 790 Other Labor Litigation
- ☐ 791 Empl. Ret. Inc. Security Act

IMMIGRATION
- ☐ 462 Naturalization Application
- ☐ 463 Habeas Corpus - Alien Detainee
- ☐ 465 Other Immigration Actions

BANKRUPTCY
- ☐ 422 Appeal 28 USC 158
- ☐ 423 Withdrawal 28 USC 157

PROPERTY RIGHTS
- ☐ 820 Copyrights
- ☑ 830 Patent
- ☐ 840 Trademark

SOCIAL SECURITY
- ☐ 861 HIA (1395ff)
- ☐ 862 Black Lung (923)
- ☐ 863 DIWC/DIWW (405(g))
- ☐ 864 SSID Title XVI
- ☐ 865 RSI (405(g))

FEDERAL TAX SUITS
- ☐ 870 Taxes (U.S. Plaintiff or Defendant)
- ☐ 871 IRS—Third Party 26 USC 7609

OTHER STATUTES
- ☐ 400 State Reapportionment
- ☐ 410 Antitrust
- ☐ 430 Banks and Banking
- ☐ 450 Commerce
- ☐ 460 Deportation
- ☐ 470 Racketeer Influenced and Corrupt Organizations
- ☐ 480 Consumer Credit
- ☐ 490 Cable/Sat TV
- ☐ 810 Selective Service
- ☐ 850 Securities/Commodities/ Exchange
- ☐ 875 Customer Challenge 12 USC 3410
- ☐ 890 Other Statutory Actions
- ☐ 891 Agricultural Acts
- ☐ 892 Economic Stabilization Act
- ☐ 893 Environmental Matters
- ☐ 894 Energy Allocation Act
- ☐ 895 Freedom of Information Act
- ☐ 900Appeal of Fee Determination Under Equal Access to Justice
- ☐ 950 Constitutionality of State Statutes

V. ORIGIN (Place an "X" in One Box Only)

☑ 1 Original Proceeding ☐ 2 Removed from State Court ☐ 3 Remanded from Appellate Court ☐ 4 Reinstated or Reopened ☐ 5 Transferred from another district (specify) ☐ 6 Multidistrict Litigation ☐ 7 Appeal to District Judge from Magistrate Judgment

VI. CAUSE OF ACTION

Cite the U.S. Civil Statute under which you are filing **(Do not cite jurisdictional statutes unless diversity)**:
patent laws of the United States, 35 U.S.C. Section 1, et seq.

Brief description of cause:
suit for patent infringement

VII. REQUESTED IN COMPLAINT:

☐ CHECK IF THIS IS A CLASS ACTION UNDER F.R.C.P. 23

DEMAND $

CHECK YES only if demanded in complaint:
JURY DEMAND: ☑ Yes ☐ No

VIII. RELATED CASE(S) IF ANY (See instructions): JUDGE _____ DOCKET NUMBER _____

DATE
7-25-08

SIGNATURE OF ATTORNEY OF RECORD

FOR OFFICE USE ONLY

RECEIPT # _____ AMOUNT _____ APPLYING IFP _____ JUDGE _____ MAG. JUDGE _____

INSTRUCTIONS FOR ATTORNEYS COMPLETING CIVIL COVER SHEET FORM JS 44

Authority For Civil Cover Sheet

The JS 44 civil cover sheet and the information contained herein neither replaces nor supplements the filings and service of pleading or other papers as required by law, except as provided by local rules of court. This form, approved by the Judicial Conference of the United States in September 1974, is required for the use of the Clerk of Court for the purpose of initiating the civil docket sheet. Consequently, a civil cover sheet is submitted to the Clerk of Court for each civil complaint filed. The attorney filing a case should complete the form as follows:

I. (a) Plaintiffs-Defendants. Enter names (last, first, middle initial) of plaintiff and defendant. If the plaintiff or defendant is a government agency, use only the full name or standard abbreviations. If the plaintiff or defendant is an official within a government agency, identify first the agency and then the official, giving both name and title.

(b) County of Residence. For each civil case filed, except U.S. plaintiff cases, enter the name of the county where the first listed plaintiff resides at the time of filing. In U.S. plaintiff cases, enter the name of the county in which the first listed defendant resides at the time of filing. (NOTE: In land condemnation cases, the county of residence of the "defendant" is the location of the tract of land involved.)

(c) Attorneys. Enter the firm name, address, telephone number, and attorney of record. If there are several attorneys, list them on an attachment, noting in this section "(see attachment)".

II. Jurisdiction. The basis of jurisdiction is set forth under Rule 8(a), F.R.C.P., which requires that jurisdictions be shown in pleadings. Place an "X" in one of the boxes. If there is more than one basis of jurisdiction, precedence is given in the order shown below.

United States plaintiff. (1) Jurisdiction based on 28 U.S.C. 1345 and 1348. Suits by agencies and officers of the United States are included here.

United States defendant. (2) When the plaintiff is suing the United States, its officers or agencies, place an "X" in this box.

Federal question. (3) This refers to suits under 28 U.S.C. 1331, where jurisdiction arises under the Constitution of the United States, an amendment to the Constitution, an act of Congress or a treaty of the United States. In cases where the U.S. is a party, the U.S. plaintiff or defendant code takes precedence, and box 1 or 2 should be marked.

Diversity of citizenship. (4) This refers to suits under 28 U.S.C. 1332, where parties are citizens of different states. When Box 4 is checked, the citizenship of the different parties must be checked. (See Section III below; federal question actions take precedence over diversity cases.)

III. Residence (citizenship) of Principal Parties. This section of the JS 44 is to be completed if diversity of citizenship was indicated above. Mark this section for each principal party.

IV. Nature of Suit. Place an "X" in the appropriate box. If the nature of suit cannot be determined, be sure the cause of action, in Section VI below, is sufficient to enable the deputy clerk or the statistical clerks in the Administrative Office to determine the nature of suit. If the cause fits more than one nature of suit, select the most definitive.

V. Origin. Place an "X" in one of the seven boxes.

Original Proceedings. (1) Cases which originate in the United States district courts.

Removed from State Court. (2) Proceedings initiated in state courts may be removed to the district courts under Title 28 U.S.C., Section 1441. When the petition for removal is granted, check this box.

Remanded from Appellate Court. (3) Check this box for cases remanded to the district court for further action. Use the date of remand as the filing date.

Reinstated or Reopened. (4) Check this box for cases reinstated or reopened in the district court. Use the reopening date as the filing date.

Transferred from Another District. (5) For cases transferred under Title 28 U.S.C. Section 1404(a). Do not use this for within district transfers or multidistrict litigation transfers.

Multidistrict Litigation. (6) Check this box when a multidistrict case is transferred into the district under authority of Title 28 U.S.C. Section 1407. When this box is checked, do not check (5) above.

Appeal to District Judge from Magistrate Judgment. (7) Check this box for an appeal from a magistrate judge's decision.

VI. Cause of Action. Report the civil statute directly related to the cause of action and give a brief description of the cause. **Do not cite jurisdictional statutes unless diversity.** Example: U.S. Civil Statute: 47 USC 553
Brief Description: Unauthorized reception of cable service

VII. Requested in Complaint. Class Action. Place an "X" in this box if you are filing a class action under Rule 23, F.R.Cv.P.

Demand. In this space enter the dollar amount (in thousands of dollars) being demanded or indicate other demand such as a preliminary injunction.

Jury Demand. Check the appropriate box to indicate whether or not a jury is being demanded.

VIII. Related Cases. This section of the JS 44 is used to reference related pending cases if any. If there are related pending cases, insert the docket numbers and the corresponding judge names for such cases.

Date and Attorney Signature. Date and sign the civil cover sheet.

AO FORM 85 RECEIPT (REV. 9/04)

United States District Court for the District of Delaware

Civil Action No. _____

ACKNOWLEDGMENT OF RECEIPT FOR AO FORM 85

NOTICE OF AVAILABILITY OF A UNITED STATES MAGISTRATE JUDGE TO EXERCISE JURISDICTION

I HEREBY ACKNOWLEDGE RECEIPT OF 1 COPIES OF AO FORM 85.

7/25/08
(Date forms issued)

Matthew D. Gordon
(Signature of Party or their Representative)

Matthew D. Gordon
(Printed name of Party or their Representative)

Note: Completed receipt will be filed in the Civil Action