IN THE UNITED STATES DISTRICT COURT
FOR THE DISTRICT OF DELAWARE

POWER INTEGRATIONS, INC., Plaintiff, v. BCD SEMICONDUCTOR CORPORATION and SHANGHAI SIM-BCD SEMICONDUCTOR MANUFACTURING CO., LTD., Defendants.	)	C.A. No. 07-633-JJF-LPS **REDACTED PUBLIC VERSION**

DECLARATION OF DR. THOMAS G. HABETLER

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Attorneys for Defendants BCD Semiconductor Corporation and Shanghai SIM-BCD Semiconductor Manufacturing, Co., LTD.

Dated: April 7, 2008

I, Thomas G. Habetler, declare as follows:

1. I have been retained by BCD Semiconductor Corp. and Shanghai SIM-BCD Semiconductor Manufacturing, Co., Ltd, to provide some expert opinions in this matter. I have extensive experience in the area of power supply controllers and electromagnetic interference. My curriculum vita is attached as Exhibit 1.

2. I have reviewed U.S. Patent No. 6,249,876 ("the '876 patent" attached as Exhibit 2) and understand the subject matter in that patent. I have also reviewed Judge Farnan's Order in *Power Integrations v. Fairchild*, attached as Exhibit 3, construing the claim terms in that patent.

3. I have also reviewed the declaration of Robert Blauschild dated January 25, 2008 (Exhibit 4), the data sheets attached as Exhibits A-C to his declaration, and the schematics attached as Exhibit D to his declaration, and certain portions from the transcript of his deposition on March 24, 2008 (Exhibit 5), which I reference below.

4. Also, I have reviewed actual schematics for the AP3700, attached as Exhibit 6 to this declaration, as well as several articles and patents I discuss below, and I offer the following opinions.

BACKGROUND

5. Power electronic circuits are circuits used to change the characteristics (voltage, current, and/or frequency) of electric power. In order to do this conversion efficiently, semiconductor switches and reactive elements are employed. In order to achieve small size and high power density, the switching frequency must be sufficiently high. As technology has progressed over the last 20 years, the switching frequency has gotten higher with better and more ideal semiconductor switches. This high-speed switching of relatively high

current and voltage causes emitted electromagnetic waves, referred to as "ElectroMagnetic Interference (EMI)." According to basic laws of electromagnetism, there is a magnetic field associated with any electrical current. As the frequency of the electromagnetic signal increases, the transmission distance of the signal also increases. A simple explanation for this is that low frequency, 60 Hz, power currents stay in the conductor, while radio waves at high frequency emit from antennae. The fast transition of the semiconductor switches from the off to on state, result in high frequency fields which are emitted in the air. The frequency of the electromagnetic field produced is primarily at the switching frequency. Nowadays, this frequency can easily be in the radio frequency range. EMI can be generated by a variety of devices including computers, power supplies, or other devices that use fast switching clocks.

6. This EMI can interfere with other electronic equipment and signals in proximity to the source, and is therefore undesirable, and is regulated by government agencies and subject to industry standards. Since it is necessary to operate the semiconductor switches at a certain frequency (referred to as Pulse Width Modulation (PWM)), the EMI is concentrated at or near the switching frequency.

7. The concept of spreading the spectrum of the voltage and current (and therefore the EMI) of power converters is nearly 40 years old (attached as Exhibit 7). In those days, the switching frequency was lower, and therefore acoustic noise was generated. By spreading the spectrum, the effect of the acoustic noise is reduced. Later on, as the switching frequencies got higher, EMI became the primary concern, since the frequency became higher than the audible range. The exact same techniques used to reduce the acoustic noise

were then applied to the problem of EMI reduction. The peaks at any one frequency can be reduced by spreading the spectrum over a wider range.

8. In order to achieve a spreading of the spectrum, many circuits use a randomized (including pseudo-random) switching pattern that maintains a constant average switching frequency. That is, the switching frequency is "dithered" from its nominal value in a way that contains certain statistical characteristics. There are many examples of this in the literature. The use of random or dithered switching has been proposed for all types of power electronic converters, including DC/DC converters and AC/AC converters (Exhibit 8).

9. Over the years, there have been many implementations of dithered or random PWM. The first implementations were purely analog, and generally injected a dithering signal directly into the PWM comparator. Later on, the use of the dithered clock signal in digital controllers was employed. In these cases, a counter addresses a quasi-random sequence in a look-up table (ROM). A D/A converter can then be used to create the dither signal added to the PWM triangle or sawtooth wave.

OBSERVATIONS ABOUT THE '876 PATENT.

10. It appears to me that the inventors in this patent believed that they were the first to use spread spectrum switching for EMI reduction. I see nothing in the patent acknowledging the work of others who recognized the used of spread-spectrum techniques in power circuits to reduce EMI. This is obviously not the case, as it has been around since 1970.

11. Moreover, in many publications since that time, there is some dimension of randomness to the added jittering. This is because a truly random (white noise) pattern would produce a completely flat spread spectrum. I see nothing in the '876 patent showing the inventors appreciated, or were even be aware of, this fact. The scheme shown in the '876 patent

introduces a deterministic spreading of the spectrum, and therefore much less EMI reduction is realized. I do not believe that the method used to spread the power spectrum employed in this patent is insightful, or valuable.

12. I understand from my review of at least one expert report (Exhibit 9) of Mr. Blauschild in the *Power Integrations v. Fairchild* case, that he believes that the design in the '876 patent was "a simple and elegant solution" to the problem of EMI mitigation. I find nothing in the patent to support that, as it appears to me the inventors believed they had in fact discovered the use of spread spectrum to reduce EMI, which they obviously did not.

13. Therefore, I do not think the inventors of the '876 patent were trying to provide an improvement to, or even a difference from, the random/pseudo-random dithering that had been well-known. Rather, it appears to me that the inventors were merely trying to spread out the EMI from a switch over several frequencies, which, as I said, was well known.

VALIDITY

14. I understand that a patent claim is invalid under 35 U.S.C. § 102 if all of the claim elements are found in a single prior-art reference, and that a patent claim is invalid under 35 U.S.C. § 103 if the subject matter of the claims would have been obvious to a person of ordinary skill in the art. I believe a person of ordinary skill in the art at the time the '876 patent was filed (1998) would have been an engineer with a master's degree in electrical engineering, which included some course in power electronics; or an engineer with a bachelor's degree and 2-4 years of work experience in power electronics.

15. In assessing validity, I reviewed the Request for Reexamination filed in the USPTO on November 9, 2006, (Exhibit 10) and the three references listed in that Request, U.S. Patent No. 4,638,417 (Martin) (Exhibit 11); Acoustic Noise Reduction In Sinusoidal PWM Drives

Using A Randomly Modulated Carrier, IEEE Transactions on Power Electronics, Vol. 6, No.3, p. 356 (published July 1991) by T.G. Habetler and D.M. Divan (Habetler) (Exhibit 8); and Programmed Pulsewidth Modulated Waveforms For Electromagnetic Interference Mitigation In DC-DC Converters, IEEE Transactions on Power Electronics, Vol. 8, No.4 (October 1993) by A.C. Wang and S. R. Sanders. (Wang) (Exhibit 12). I agree with the Request that each one of those references renders claim 1 of the '876 patent invalid.

16. In addition to the reasoning in that Request, I offer the observation that the key reason for distinguishing the references seems to be the presence of a memory between a counter and a D/A converter. As I believe Mr. Blauschild has explained in his deposition, where one draws the boundaries of a circuit is somewhat arbitrary. Exhibit 5, page 21, line 6 - page 23, line 10. As far as I am concerned, the memory can either be part of the counter or of a D/A converter. Broadly speaking, a counter is simply a "device capable of changing from one to the next of a sequence of distinguishable states upon receipt of an input signal." IEEE Standard Dictionary of Electrical and Electronic Terms (1984) (Exhibit 13), p, 204. Similarly, a D/A converter is simply a "device . . . that a converts a numerical input signal or code into an output signal some characteristic of which is proportional to the input." *Id.*, p. 251. I am not proposing a legal claim construction, but only pointing out that the terms in the '876 patent can have a broad meaning that would encompass a great deal of prior art. As explained below, if one tried a narrower meaning to exclude the prior art, the claims could not cover the AP3700.

17. **REDACTED** If the memories cannot be part of the digital-to-analog converters or the counters in the references I mentioned, then I see no

logical basis for making the decoder part of the digital-to-analog converter in the AP3700 power controller.

18.

REDACTED

19. Attached as Exhibits 14 - 16 are claim charts explaining why I believe claim 1 to be invalid under 35 U.S.C. § 102 over these references.

20. Several prior-art references had recognized that spread-spectrum techniques could reduce EMI in PWM controllers. Tetsuro Tanaka, Tamotsu Ninomiya and Koosuke Harada, "Random-Switching Control in DC-to-DC Converters," PESC Record, Vol. I, p. 500, 20th Annual IEEE Power Electronics -Specialists Conference (1989) (Exhibit 17); F.Lin and D.Y .Chen, "Reduction of Power Supply EMI Emission by Switching Frequency Modulation," IEEE Transactions on Power Electronics, Vol. 9, Issue 1 (Jan 1994) 137, p. 27 (1993) (Exhibit 18); D. A. Stone, B. Chambers & D. Howe, "Easing EMC Problems in Switched Mode Power Converters by Random Modulation of the PWM Carrier Frequency," (Stone I) Proceedings of 1995 International Conference on Power Electronics and Drive Systems, Vol.1 (Feb 1995), 327 (Exhibit 19); David Stone & Barry Chambers, "The Effect of Carrier Frequency Modulation of PWM Waveforms on Conducted EMC Problems in Switched Mode Power Supplies," (Stone II), EPE Journal, Vol. 5, No 3/4·p. 32 (January 1996) (Exhibit 20); D.A. Stone and B. Chambers, "Effect of Spread-Spectrum Modulation of Switched Mode Power Converter PWM Carrier Frequencies on Conducted EMI" (Stone III), Electronics Letters 77th, Vol. 31, No. 10, p. 769 (May 11, 1995) (Exhibit

21); Aleksandar M. Stankovic, George C. Verghese, and David J. Perreault, "Analysis and Synthesis of Randomized Modulation Schemes for Power Converters," Vol. 10, No. 6, p. 680 (November 1995) (Exhibit 22); Aleksandar Mihajla Stankovic, Random Pulse Modulation With Applications to Power Electronic Converters, Ph. D Thesis, page 23, Massachusetts Institute of Technology (1993) (Exhibit 23); S. Y. (Ron) Hui, Yash Shrivastava, S. Sathiakumar, K. K. Tse, and Henry Shu-Hung Chung, "A Comparison of Nondeterministic and Deterministic Switching Methods for DC–DC Power Converters," IEEE Transactions On Power Electronics, Vol. 13, No. 6, p. 1046 (November 1998) (Exhibit 24). Indeed, this is a problem with many types of clocks. Keith B. Hardin, John T. Fessler, Donald R. Bush, "Spread Spectrum Clock Generation for the Reduction of Radiated Emissions," IEEE International Symposium on Electromagnetic Compatibility, 1994 Symposium Record, p. 27 (Aug. 1994) (Exhibit 25).

21. Several prior-art references explain the value of spreading the frequencies at equal-spaced intervals. F. Lin, et al. (Exhibit 18) at 129; Stone I (Exhibit 19) at 328; Stone II (Exhibit 20) at 33-35; Stone III (Exhibit 22) at 769; Stankovic, et al. (Exhibit 22) at 683-85; Stankovic Thesis (Exhibit 23) at 96, et seq. Other references showed the use of a triangular wave signal to modulate the frequency. *See, e.g.*, Hardin (Exhibit 25) at 229.

22. Given these teachings, I believe a person of ordinary skill in the art seeking to reduce EMI in power converter circuits would have looked to techniques for reducing EMI from clock signals in other disciplines. Examples of such circuits are the Japanese Disclosure Number 58-27440 (Exhibit 26); and U.S. Patent Nos. 5,943,382 (Exhibit 27); 5,757,338 (Exhibit 28); 5,659,587 (Exhibit 29); 6,294,936 (Exhibit 30); and 5,488,627 (Exhibit 31). The claim charts explaining how those circuits relate to claim 1 are in Exhibits 32-37.

NONINFRINGEMENT

23.

REDACTED

24. I have also been asked to provide an opinion whether the term "control input" denotes any type of structure. I do not believe so. An input just means the place where some signal is received, and that signal can be electronic (e.g., voltage, current), electromagnetic (radio waves), optical, vibrational, etc. "Input" connotes no structure. It can be data, states, a device, a channel, a process, or a physical quantity. IEEE Dictionary *Exhibit 14) at 958. The term "control" just means the signal will be used for some function. Also, I note that claim 1 of the '876 patent uses the term "control input" to refer to both an input to a circuit and a signal. Exhibit 2, column 8, lines 42-54.

25. I have also been asked to provide an opinion on which portion in Figure 1 of the '876 patent performs the function as recited in the phrase "control input for varying the switching frequency." I believe the closest circuit element is node 123, which is a current summing node. That is the structure in Figure 1, the figure covered by claim 1, which comes closest to performing the function of varying the switching frequency.

26.

REDACTED

REDACTED

27.

REDACTED

[1] A truly random sequence of numbers contains all the spectral components from zero to infinity, and remains random for all time. This is often referred to as white noise. If we limit the bandwidth of the random sequence we refer to the signal as band-limited or "pink noise." Furthermore, any random sequence that approximates a truly random signal is referred to as "pseudo-random." Pseudo-random sequences are often sets of numbers that are reused or repeated iteratively in order to save memory or storage space. In a random PWM scheme, it is impractical to store a huge quantity of random numbers, so pseudo-random sequences consisting of a relatively small set of random numbers are used.

I declare under penalty of perjury under the laws of the United States of America that the foregoing is true and correct.

Executed this 7th day of April, 2008, at Atlanta, Georgia.



Thomas G. Habetler

EXHIBIT 1
(Curriculum Vitae - Thomas G. Habetler)

April 7, 2008

Thomas G. Habetler

Professor

Georgia Tech, School of Electrical and Computer Engineering

I. EARNED DEGREES

PhD	1989	University of Wisconsin	Electrical Engineering
MS	1984	Marquette University	Electrical Engineering
BSEE	1981	Marquette University	Electrical Engineering

II. EMPLOYMENT HISTORY

Professor	Georgia Institute of Technology	2000-present
Associate Professor	Georgia Institute of Technology	1995-2000
Assistant Professor	Georgia Institute. of Technology	1989-1995
Research Assistant	University of Wisconsin–Madison	1987-1989
Project Engineer	General Motors—Electro-Motive Division	1983-1985
Research Assistant	Marquette University	1981-1983
Co-op Plant Engineer	Western Publishing Co., Inc.	1979-1981

III. TEACHING

A. INDIVIDUAL STUDENT GUIDANCE - Ph.D. Students Graduated

1. Randy R. Schoen
   Graduated: September 1994
   Thesis Title: *On-Line, Current-Based Condition Monitoring of Three Phase Induction Machines*
   Employment: Currently employed as Senior Research Engineer with Loher Drive Systems, Atlanta, GA

2. Farrukh Kamran
   Graduated: December 1995
   Thesis Title: *A New Topology and Unified Control for AC/DC/AC Converters for Uninterruptible Power Supply Applications*
   Employment: Currently employed as Assistant Professor, Ghulam Ishaq Khan Institute of Engineering Sciences and Technology, Pakistan

3. Kevin D. Hurst
   Graduated: October 1996

Thesis Title: *Transducerless Control And Monitoring Of Induction Machines Using Magnetic Saliency Harmonics*
Employment: Currently employed as Senior Research Engineer with GM - Detroit Diesel Allison

4. Caryn M. Riley
   Graduated: August 1998
   Thesis Title: *Current-Based Sensorless Vibration Monitoring of Small AC Machines*
   Employment: Currently employed as Research Engineer with Georgia Tech - NEETRAC.

5. M. Alex Cash
   Graduated: June 1998
   Thesis Title: *Insulation Fault Prediction in Induction Machines*
   Employment: Currently employed as a Senior Engineer – Air Force Research Lab, Eglin AFB, FL

6. Leon M. Tolbert
   Graduated: June 1998
   Thesis Title: *New Multi-Level Carrier-Based Pulse Width Modulation Techniques Applied To A Diode Clamped Converter For Use As A Universal Power Conditioner*
   Employment: Assistant Professor, Dept. of Electrical Engineering, University of Tennessee, Knoxville

7. Antonio Ginart
   PhD, Summer 2001
   Thesis Title: *Single ended switching analog audio amplifier with dead zone*
   Employment: Assistant Professor, Simon Bolivar University, Caracas, Venezuela

8. Sang-Bin Lee
   PhD, Summer 2001
   Thesis Title: *Stator Resistance-based Temperature Monitoring for Line Connected Induction Machines*
   Employment: Assistant Professor, Korea University, Seoul, Korea

9. Rangarajam Tallam
   PhD, Fall 2001
   Thesis Title: *Current-Based Sensorless Detection of Stator Winding Turn Faults in Induction Machines*
   Employment: Research Engineer, Rockwell Automation – Allen Bradley Co., Milwaukee, WI

10. Wei-Chung Wu
    PhD, Fall 2001.
    Thesis Title: *On-Chip Charge Pumps*

Employment: Project Engineer, Texas Instruments, Dallas, TX

11. Ramzy Obaid
PhD, Summer 2003
Thesis Title: *Detection of rotating mechanical asymmetries in small induction machines*
Employment: Lecturer, Georgia Tech, School of ECE.

12. Jason Stack
PhD, Fall 2002
Thesis Title: *Fault signature detection for rolling element bearings in electric machines*
Employment: Senior Researcher, US Navy NAVSEA Laboratory, Panama City, FL.

13. Theocharis (Harry) Boukas
PhD, Summer 2003
Thesis Title: *Exact feedback linearization with state derivative feedback for high-performance field-oriented induction motor speed/position control*
Employment: Senior Project Engineer, Siemens Energy and Automation, Alpharetta, GA.

14. Dong-Myung Lee
PhD, Spring 2004
Thesis Title: *A voltage sag supporter with a PWM-switched autotransformer*
Employment: Senior Project Engineer, Samsung Electronics, Seoul, Korea

15. Xianghui Huang
PhD, Spring 2005
Thesis Title: *Diagnostics of Air Gap Eccentricity in Closed-Loop Drive-Connected Induction Motors*
Employment: Senior Research Engineer, General Electric Global Research Center, Schenectady, NY

16. Satish Rajagopalan
PhD, Summer 2006
Thesis title: *Detection of Rotor and Load Faults In Brushless DC (BLDC) Motors Operating Under Stationary and Non-Stationary Conditions*
Employment: Senior Engineer, EPRI Solutions, Lexington, KY

17. Long Wu
PhD, Fall 2006
Thesis Title: *Separating Load Torque Oscillation And Rotor Faults In Stator Current Based-Induction Motor Condition Monitoring*
Employment: Design Engineer, John Deere Corp., New Product Innovation Center, Fargo, ND

18. Zhi Gao
PhD, Fall 2006
Thesis title: *Sensorless Stator Winding Temperature Estimation For Induction Machines*
Employment: Senior Research Engineer, Schneider Electric / Square D, Center for Innovation and Technology (CIT), Raleigh, NC

19. Bin Lu
PhD, Fall 2006
Thesis title: *Energy Usage Evaluation And Condition Monitoring For Electric Machines Using Wireless Sensor Networks*
Employment: Lead Engineer, Eaton Corporation Innovation Center, Milwaukee, WI

20. Youngkook Lee
PhD, Summer 2007
Thesis title: Fault Diagnostics And Fault Tolerant Strategies For Interior PM Motor Drives In Hybrid Electric Vehicles
Employment: Senior Engineer, Hyundai Motor Co., Seoul, Korea

21. Wei Zhou
PhD, Fall 2007
Thesis topic: Bearing Fault Diagnostics for Induction Machines Using Adaptive Noise Cancellation
Employment: Research Engineer, Midwest Independent Transmission System Operator, Carmel, IN

CURRENT PHD STUDENTS

1. Pinjia Zhang
Fall 2006-present
Date passed prelim exam: Fall 2006
Thesis topic: Temperature estimation in induction machines using dc injection via soft-starters
Expected Graduation Date: Fall 2009

2. Yi Du
Fall 2006-present
Date passed prelim exam: Fall 2006
Thesis topic: Condition monitoring of medium voltage motors
Expected Graduation Date: Fall 2009

3. Stefan Grubic
Spring 2007-present
Date passed prelim exam: Fall 2006
Thesis topic: On-line insulation monitoring and surge testing of ac machines
Expected Graduation Date: Fall 2009

4. Siwei Cheng
   Fall 2007-present
   Date passed prelim exam: Fall 2007
   Thesis topic: Condition monitoring of automotive alternators
   Expected Graduation Date: Fall 2010

5. Jiaqi Liang
   Fall 2007-present
   Date passed prelim exam: Fall 2007
   Thesis topic: Model-based diagnostics for synchronous machines
   Expected Graduation Date: Fall 2010

B. OTHER TEACHING ACTIVITIES

Continuing Education

1. "Power Electronics Devices, Circuits, and Systems," Georgia Tech Continuing Education short course. Served as instructor for 8 hours (1/3 of course).
   March 9-11, 1994
   March 22-24, 1995
   June 27-29, 1995, at Georgia Power Co.
   April 1996
   April 1997
   June 1997 at Sandia National Labs
   March 1998 at GM-Delphi Electronics
   April 1998
   October 1998 at Otis Elevator Co.
   March 1999

2. "Conditioning Monitoring of Induction Machines," IEEE tutorial at Industry Applications Society Annual Meeting, co-instructor with R. Belmans and G. Kliman. Taught 1 hour of lecture.
   October 1995
   October 1996

3. "PWM Techniques for Voltage Source Inverters," IEEE tutorial at Power Electronics Specialists Conference, co-instructor with D.M. Divan and T.A. Lipo. Taught 1.5 hours of lecture. June 1990.

Curriculum Development

1. Courses EE6531, EE6525, EE4047 (together with R. Bass) have each been completely revised and updated. This includes a new course outline, text, and course notes.

2. EE 3301 and EE3070 have been developed for semesters, together with H. B. Püttgen.

IV. SCHOLARLY ACCOMPLISHMENTS

B.1. REFEREED JOURNAL PAPERS

The papers listed below which contain referrals to conference papers, were accepted for publication in conference proceedings before being submitted for transactions review. The Transactions and conference papers are peer reviewed in a separate process by different reviewers. In some cases the transactions papers have been updated or otherwise improved. The IEEE Industry Applications Society requires all Transactions papers to be previously presented at a conference. Presentation at a conference prior to Transactions publications is also common practice in the Power Electronics Society.

1. Habetler, T. G. and Divan, D. M., "Rectifier/inverter reactive component minimization," *IEEE Transactions on Industry Applications*, vol. 25, no. 2, pp. 307-316, March/April 1989. *Also see paper #IV.B.2.1.*

2. Habetler, T. G. and Divan, D. M., "Performance characterization of a new discrete pulse modulated current regulator," *IEEE Transactions on Industry Applications,* vol. 25, No. 6, pp. 1139-1148, Nov./Dec. 1989. *Also see paper #IV.B.2.2.*

3. Habetler, T. G. and Divan, D. M., "Acoustic noise reduction in sinusoidal pwm drives using a randomly modulated carrier," *IEEE Transactions on Power Electronics,* vol. 6, no. 3, pp. 356-363, July 1991. *Also see paper #IV.B.2.3.*

4. Habetler, T. G. and Divan, D. M., "Angle controlled current regulated rectifiers for ac/ac converters," *IEEE Transactions on Power Electronics,* vol. 6, no. 3, pp. 463-469, July 1991. *Also see paper #IV.B.2.4.*

5. Habetler, T. G. and Divan, D. M., "Control strategies for direct torque control using discrete pulse modulation," *IEEE Transactions on Industry Applications,* vol. 27, no. 5, pp. 893-901, Sept./Oct. 1991. *Also see paper #IV.B.2.5.*

6. Xue, X., Xu, X., Habetler, T. G. and Divan, D. M., "A stator flux oriented voltage source variable speed drive based on dc link measurement," *IEEE Transactions on Industry Applications,* vol. 27, no. 5, pp. 962-969, Sept./Oct. 1991. *Also see paper #IV.B.2.6.*

7. Habetler, T. G., Profumo, F., Pastorelli, M. and Tolbert, L. M., "Direct torque control of induction machines using space vector modulation," *IEEE Transactions on Industry Applications,* vol. 28, no. 5, pp. 1045-1053, Sept./Oct. 1992. *Also see paper #IV.B.2.8.*

8. Habetler, T. G., "A space vector based rectifier regulator for ac/dc/ac converters," *IEEE Transactions on Power Electronics*, vol. 8, no. 1, pp. 30-36, January 1993. *Also see paper #IV.B.2.7.*

9. Jiang, H., Dorsey, J., Habetler, T. G. and Eckroth, K. V., "A cost effective generator brake for improved generator transient response," *IEEE Transactions on Power Systems* vol. 9, no.4, pp. 1840-1846, Nov. 1994. *Also see paper #IV.B.2.17.*

10. Griva, G., Habetler, T. G. Profumo, F. and Pastorelli, M., "Performance evaluation of a direct torque controlled drive in the continuous pwm - square wave transition region," *IEEE Transactions on Power Electronics*, vol. 10, no. 4, pp. 464-471, July 1995. *Also see paper #IV.B.2.13.*

11. Kamran, F. and Habetler, T. G., "An improved dead-beat rectifier regulator using a neural network predictor," *IEEE Transactions on Power Electronics*, vol. 10, no. 4, pp. 504-510, July 1995. *See paper #IV.B.2.19.*

12. Schoen, R.R. and Habetler, T. G., "Effects of time-varying loads on rotor fault detection in induction machines," *IEEE Transactions on Industry Applications,* vol. 31, no. 4, pp. 900-906, July/Aug. 1995. *Also see paper #IV.B.2.16.*

13. Schoen, R. R., Lin, B. K., Habetler, T. G., Schlag, J. H., and Farag, S., "An unsupervised, on-line system for induction motor fault detection using stator current monitoring," *IEEE Transactions on Industry Applications,* vol. 31, no. 6, pp. 1274-1279, Nov./Dec. 1995. *Also see paper #IV.B.2.22.*

14. Schoen, R. R., Habetler, T. G., Kamran, F., and Bartheld, R. G., "Motor bearing damage detection using stator current monitoring," *IEEE Transactions on Industry Applications,* vol. 31, no. 6, pp. 1280-1286, Nov./Dec. 1995. *Also see paper #IV.B.2.23.*

15. Hurst, K. D. and Habetler, T. G., "Sensorless speed measurement using current harmonic spectral estimation in induction machine drives," *IEEE Transactions on Power Electronics*, vol. 11, no. 1, pp. 66-73, January 1996. *Also see paper #IV.B.2.20. This paper also appeared in the IEEE Press Book, "Sensorless Control of AC Motor Drives," edited by K. Rajashekara.*

16. Farag, S., Bartheld, R. G., and Habetler, T. G., "An integrated, on-line, motor protection system," *IEEE Industry Applications Magazine*, March/April 1996, pp. 21-26. *Also see paper #IV.B.2.25.*

17. Brassfield, W. R., Spée, R. and Habetler, T. G., "Direct torque control for brushless doubly-fed machines," *IEEE Transactions on Industry Applications,* vol. 32, no. 5, pp. 1098-1104, Sept./Oct. 1996. *Also see paper #IV.B.2.10.*

18. Schoen, R. R. and Habetler, T. G., "A new method of current-based condition monitoring in induction machines operating under arbitrary load conditions," *Journal of Power Systems and Electric Machines*, vol. 25, no. 2, pp. 141-152, February/March 1997. *Also see paper #IV.B.2.21.*

19. Burton, B.R., Kamran, F., Harley, R. G., Habetler, T. G., Brooke, M., and Poddar, R., "Identification and control of induction motor stator currents using fast on-line random training of a neural network," *IEEE Transactions on Industry Applications.* vol. 33, no. 3, pp. 697-704, May/June 1997. *Also see paper #IV.B.2.30.*

20. Hurst, K.D., Habetler, T.G., Griva, G., Profumo, F., Jansen, P.L., "A self-tuning closed-loop flux observer for sensorless torque control of standard induction machines," *IEEE Transactions on Power Electronics,* vol.12, no.5, p.807-815, July/Aug 1997. *Also see paper #IV.B.2.28.*

21. Hurst, K. D. and Habetler, T. G., "A comparison of spectral estimation techniques for sensorless speed detection in induction machines," *IEEE Transactions on Industry Applications,* vol. 33, no. 4, pp. 898-905, July/Aug 1997. *Also see paper #IV.B.2.29.*

22. Schoen, R. R. and Habetler, T. G., "Evaluation and implementation of a system to eliminate arbitrary load effects in current-based monitoring of induction machines," *IEEE Transactions on Industry Applications,* vol. 33, no. 6, pp. 1571-1577, Nov/Dec 1997. *Also see paper #IV.B.2.35.*

23. Habetler, T. G., Griva, G., Profumo, F. and Bettini, A., "Stator resistance tuning in a stator flux field oriented drive using an instantaneous hybrid flux estimator," *IEEE Transactions on Power Electronics*, vol. 13, no. 1, pp. 125-133, Jan 1998. *Also see paper #IV.B.2.14.*

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139. Wolbank, T.M.; Vogelsberger, M.A.; Stumberger, R.; Mohagheghi, S.; Habetler, T.G.; Harley, R.G.; "Comparison of Neural Network Types and Learning Methods for Self Commissioning of Speed Sensorless Controlled Induction Machines," *IEEE Power Electronics Specialists Conference, 2007*. 17-21 June 2007 Page(s):1955 – 1960.

140. Restrepo, J.; Viola, J.; Harley, R.; Habetler, T.; "Induction Machine Current Loop Neuro Controller Employing a Lyapunov based Training Algorithm," *2007 IEEE Power Engineering Society General Meeting*, 24-28 June 2007 Page(s):1 – 8

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of the 2007 IEEE Industry Applications Conference, 42nd IAS Annual Meeting, 23-27 Sept. 2007 Page(s):730 – 736.

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IV.C. OTHER PUBLICATIONS

1. Habetler, T. G., "Future trends in control and simulation of power electronic systems," *IEEE Industry Applications Society Workshop Proceedings on the Future of Electronic Power Processing and Conversion,* pp. 96-103, Transvaal, South Africa, August 1991. (invited paper)

2. Dorsey, J., Jiang, H., Habetler, T. G. and Qu, Z., "A new strategy for transient stability using augmented generator control and local dynamic braking," *Fourth Symposium for Specialists in Electric Operations and Expansion Planning*, Itaipu, Brazil, April 1994. (invited paper)

3. Habetler, T. G., "Power electronics: Trends in technology and education," *Proceeedings of the IEEE Workshop on the Teaching of Power Electronics,* Melbourne, Australia, July 1995. (invited paper)

4. Burton, B., Harley, R.G., and Habetler, T.G., "The application and hardware implementation of continually online trained neural networks for fast adaptive control and forecasting in power electronics systems," *Proceedings of the Third International Workshop on the Future of Electronic Power Processing and Conversion*, Skukuza, South Africa, July 1998, pp. 215-225. (invited paper)

5. Divan, D. M., Habetler, T. G. and Lipo, T. A., "PWM techniques for voltage source inverters," *IEEE Power Electronics Specialists Conference Tutorial Notes,* 1990.

D. PRESENTATIONS

1. Invited Seminar Presentation at the University of Aachen, Aachen, GERMANY, on "Control of PWM Rectifiers," June 1989.

2. Invited Lecturer for a series of lectures at the Politecnico di Torino, Turin, Italy, on "Resonant Link Converters," July 1989.

3. Invited Seminar Presentation at the University of Padova, Padua, Italy, on "Acoustic noise control in pwm drives," August 1989.

4. Invited Seminar at General Electric Corporate R&D Center, Schenectady, NY, on "Dead-beat space vector modulation of controlled rectifiers," January 18, 1991.

5. Invited Presentation at IEEE Industry Applications Society Atlanta Chapter Meeting, "Overview of induction machine drives," November 16, 1992.

6. Invited Seminar at Philips Research Laboratories, Briarcliff, NY, on "Control of PWM rectifiers," March 5, 1993.

7. Invited Seminar Presentation at the University of Padova, Padua, Italy, on "Research in electric machines at Georgia Tech," March 24, 1993.

8. Invited Seminar at Oak Ridge National Laboratories, Oak Ridge, TN, on "Research in electric machines at Georgia Tech," October 15, 1993.

9. Invited Seminar Presentation at Texas Tech University, Lubbock, TX, on "On-line condition monitoring in induction machines," November 18, 1993.

10. Invited Seminar Presentation at the University of Wisconsin, Madison, WI, on "On-line condition monitoring of induction motors," December 17, 1993.

11. Invited Seminar Presentation at the University of Catania, Catania, Italy, on "A new method for on-line fault prediction in induction machines operating under arbitrary load conditions," September 13, 1994.

12. Invited Seminar Presentation at Peterlongo, Inc., Milan, Italy, on "Sensorless control of induction machines using current spectral estimation," September 14, 1994.

13. Invited Seminar Presentation at the Politecnico di Torino, Turin, Italy, on "Sensorless control of induction machines using current spectral estimation," September 15, 1994.

14. Invited Seminar Presentation at General Electric Corporate R&D Center, Schenectady, NY, on "On-line condition monitoring of induction motors," November 11, 1994.

15. Invited Seminar Presentation at the University of Wisconsin, Madison, WI, on "A new random weight change neural network algorithm for power electronic applications," March 10, 1995.

16. Invited Seminar Presentation at the IEEE Melbourne Section Meeting, Melbourne, Australia, on "Applications of artificial intelligence in power electronics," July 4, 1995.

17. Invited Seminar Presentation at Reliance Electric Corp. R&D, Cleveland, OH, on "Sensorless speed measurement in induction machines," July 28, 1995.

18. Invited Seminar Presentation at the University of Palermo, Palermo, Italy, on "A new method for on-line fault prediction in induction machines operating under arbitrary load conditions," June 17, 1996.

19. Invited Seminar Presentation at General Electric Corporate R&D Center, Schenectady, NY, on "A new random weight change neural network algorithm for power electronic applications," July 9, 1996.

20. Invited Seminar Presentation at the University of Natal, Durban, South Africa, on "On-line condition monitoring of induction motors," August 27, 1996.

21. Invited Seminar Presentation at Texas Tech University, Lubbock, TX, on "An on-line trained neural network for a wide range of power electronic applications," November 20, 1998.

22. Invited Seminar Presentation at Eaton Corp. Innovation Center, Milwaukee, WI, on "An introduction to the use artificial neural networks (anns) and fuzzy logic in the control and fault diagnostics of electrical machines", July 12, 1999. Co-presenter with R. Harley.

23. Invited Seminar Presentation at Delphi Automotive Corp., Warren, MI, on "On-Line condition monitoring of induction motors," April 14, 2000. Co-presenter with R. Harley.

24. Invited by the Simon Bolivar University to present a seminar on "Condition monitoring of electrical machines", May 2001, the Simon Bolivar Technical University, Caracas, Venezuela.

25. Invited Seminar Presentation at the University of South Carolina, Columbia, SC, on "On-line condition monitoring of induction motors," April 29, 2002.

26. Invited Seminar Presentation at Iowa State University, Ames, IA, on "On-line condition monitoring of induction motors," April 30, 2002.

E. OTHER SCHOLARLY ACCOMPLISHMENTS

Patents Granted

1. "Induction machine protection device," U.S. Patent & Trademark Office Number 5,570,256, Oct. 29, 1996. Co-inventor with R. Schoen.

2. "Induction machine protection device," U.S. Patent & Trademark Office Number 5,644,458, July 1, 1997. Co-inventor with R. Schoen. (Continuation of 5,570,256.)

3. "Method and apparatus for predicting electric induction machine failure during operation," U.S. Patent & Trademark Office Number 5,629,870, May 1997. Co-inventor with J. Schlag and S. Farag.

4. "Method & Apparatus for Turn Fault Detection in Multiphase AC Machines," U.S. Patent & Trademark Office Number 6,034,664, March 28, 2000. Co-Inventor with M. A. Cash and G. B. Kliman.

5. "Method & Apparatus for Turn Fault Detection in Multiphase AC Machines," U.S. Patent & Trademark Office Number 6,236,227, May 22, 2001. Co-Inventor with M. A. Cash and G. B. Kliman.

6. "Detecting Polyphase Machine Faults Via Current Deviation" U.S. Patent and Trademark Office No. 6,172,509, January 9, 2001. Co-Inventor with M. A. Cash.

7. "Method and apparatus to detect a stator turn fault in an AC motor," U.S. Patent and Trademark Office No. 6,611,771, August 26, 2003. Co-Inventor with D. J. Gritter, R. G. Harley, and R. M. Tallam.

8. "Device and method for estimating the resistance of a stator winding for an AC induction motor," U.S. Patent and Trademark Office No. 6,621,291, September 16, 2003. Co-inventor with S-B Lee, and D. J. Gritter.

9. "Method and apparatus of detecting internal motor faults in an induction machine," U.S. Patent and Trademark Office No. 6,822,839, November 23, 2004.

10. "System and method for proactive motor wellness diagnosis," U.S. Patent and Trademark Office No. 7,075,327, July 11, 2006. Co-inventor with S.A. Dimino, R.R. Obaid, S. Krstic, M.P. Nowak, and Y. Liu.

11. "System and method for proactive motor wellness diagnosis," U.S. Patent and Trademark Office No. 7,336,455, February 26, 2008. Co-inventor with S.A. Dimino, R.R. Obaid, S. Krstic, M.P. Nowak, and Y. Liu. (Continuation of 7,075,327.)

12. "System and method for proactive motor wellness diagnosis based on potential mechanical faults," U.S. Patent and Trademark Office No. 7,117,125, October 3, 2006. Co-inventor with S.A. Dimino, R.R. Obaid, S. Krstic, M.P. Nowak, and Y. Liu.

Patents Applied For

1. "Electronic overload relay for mains-fed induction motors," U.S. Patent and Trademark Office Application No. 20060250154, Nov. 9, 2006. Co-inventor with Z. Gao, R. G. Harley, and R. S. Colby.

V. SERVICE

A. PROFESSIONAL CONTRIBUTIONS

1. Institute of Electrical and Electronics Engineers (IEEE):

   Division II Director-Elect (elected), 2006
   Division II Director (elected) and Member of IEEE Board of Directors, 2007 and 2008.
   Member, Fellow Committee, 2006-2008
   Member, Washington Interns in Science and Engineering (WISE) Selection Committee
   Member, Technical Activities Board (elected), 2007-2008.
   Chair, Ad-Hoc Committee on Society Membership

Member, IEEE Member Engagement and Life Cycle Committee

2. IEEE Power Electronics Society:

Senior Past President, 2005-2006.
Junior Past President, 2003-2004.
President (elected), 2001-2002.
Vice President of Operations (elected), 1999-2000.
Member-at-Large (elected), Administrative Committee, 1996-1999.
Chair, PESC Conference Steering Committee, 1998-present.
Chair, Publications Committee, 1997-1999.
Chair, Educational Activities Committee, 1995-1997.
Secretary, 1994-1995.
Chair, Membership and Publicity Committee, 1990-1993.
Member, Administrative Committee, 1990-present.
Member, Meetings Committee, 1991-present.
Member, Education Committee, 1989-1993.
Member, Publications Committee, 1992-1993.

3. IEEE Industry Applications Society:

Chair (elected), Industrial Power Converter Committee, 2000-2001.
Vice Chair (elected), Industrial Power Converter Committee, 1998-1999.
Secretary (elected), Industrial Power Converter Committee, 1996-1997.
Technical Program Chair, Industrial Power Converter Committee, 1998 and 1999, IAS Annual Meeting.
Member, Industrial Power Converter Committee, 1987-present.
Member, Industrial Drives Committee, 1988-present.
Member, Technical Program Committee for the Annual Meeting and Conference, 1992.

4. Chair, Technical Program Committee, IEEE Power Electronics Specialists Conference, 1995.

5. Co-Chair, Technical Program Committee, IEEE Industry Applications Society Workshop, "Future of Electronic Power Processing and Conversion," 1991, 1994 and 1998.

6. Member, IEEE Membership Development Committee, 1992-1993.

7. Treasurer, IEEE International Conference on Harmonics in Power Systems, 1990 and 1992.

8. Member, IEEE Power Electronics Specialists Conference Technical Program Committee, 1990-1999.

9. Member, Technical Program Committee, European Power Electronics Conference, 1991 and 1993.

10. Member, IEE of Japan/IEEE Joint IAS Power Conversion Conference Technical Program Committee, Yokohama, Japan, 1992.

11. Co-Chair, Technical Program Committee, 1997 IEEE Symposium on Diagnostics in Electric Machines, Power Electronics and Drives.

12. Chair, Publications Committee, IEEE Power Electronics Specialists Conference, 1999.

13. Chair, Publicity Committee, IEEE Power Electronics Specialists Conference, 1997.

14. Member of Site Review Team, NSF Engineering Center for Power Electronics Systems, VPI, Blacksburg, 1999.

B. Campus Contributions

1. Graduate Student Examination Committees

Student Name	Committee	Date	Chair
Mr. J. B. Franklin	PhD Qualifying Examination	August 1990	
Mr. R. D. Wallace	PhD Thesis Proposal PhD Reading and Thesis Defense	August 1990 November 1990	
Mr. D. G. Rouaud	PhD Thesis Proposal PhD Reading and Thesis Defense	November 1991 February 1992	
Mr. A. Khayatian	PhD Qualifying Examination PhD Thesis Proposal PhD Reading and Thesis Defense	January 1992 January 1993 August 1993	yes
Mr. R. Schoen	PhD Qualifying Examination PhD Thesis Proposal PhD Reading and Thesis Defense	January 1992 June 1994 August 1994	yes
Mr. K. Shouse	PhD Qualifying Examination PhD Thesis Proposal PhD Reading and Thesis Defense	July 1992 February 1993 August 1993	

Mr. K. Hurst	PhD Qualifying Examination PhD Thesis Proposal PhD Reading and Thesis Defense	May 1993 December 1995 October 1996	
Mr. P. Wung	PhD Thesis Proposal PhD Reading and Thesis Defense	May 1993 August 1993	yes
Mr. F. Kamran	PhD Qualifying Exam PhD Thesis Proposal PhD Reading and Thesis Defense	August 1993 December 1994 November 1995	
Mr. H. Jiang	PhD Qualifying Exam PhD Thesis Proposal PhD Reading and Thesis Defense	August 1993 December 1993 March 1994	
Mr. M. Al-Numay	PhD Qualifying Exam PhD Thesis Proposal PhD Reading and Thesis Defense	August 1993 March 1996 July 1997	yes
Mr. D. Pirovolou	PhD Qualifying Exam PhD Thesis Proposal PhD Reading and Thesis Defense	February 1994 March 1996 September 1996	yes
Ms. C. Riley	PhD Qualifying Exam PhD Thesis Proposal PhD Reading and Thesis Defense	March 1994 April 1998 August 1998	
Mr. M. Kumbale	MSEE Thesis Proposal MSEE Reading and Thesis Defense	March 1995 January 1996	yes
Mr. M. Alex Cash	PhD Qualifying Exam PhD Thesis Proposal PhD Reading and Thesis Defense	February 1996 December 1997 May 1998	
Mr. Brian Lin	PhD Qualifying Exam PhD Thesis Proposal	April 1995 March 1997	
Mr. Wonoh Kim	PhD Qualifying Exam	February 1997	yes
Mr. William Taylor	PhD Qualifying Exam PhD Thesis Proposal PhD Reading and Thesis Defense	August 1996 July 1997 November 1997	yes
Mr. Michael Ropp	PhD Qualifying Exam PhD Thesis Proposal PhD Thesis Defense	November 1998	
Ms. Jin Liu	PhD Qualifying Exam PhD Thesis Proposal PhD Reading and Thesis Defense	August 1997 December 1998 May 1999	

Mr. Antonio Ginart	PhD Qualifying Exam PhD Reading and Thesis Defense	May 1999 July 2001	Yes yes
Mr. Leon Tolbert	PhD Qualifying Exam PhD Thesis Proposal PhD Reading and Thesis Defense	June 1997 June 1998 May 1999	
Mr. Wei Chung Wu	PhD Qualifying Exam PhD Reading and Thesis Defense	May 1998 November 2001	 yes
Ms. Y. Yang	PhD Qualifying Exam	August 1998	
Mr. Sang-Bin Lee	PhD Qualifying Exam PhD Reading and Thesis Defense	May 1999 July 2001	 Yes

2. School of Electrical and Computer Engineering:

   Member, Student-Faculty Committee, 1989-1990.
   Member, Research Committee, 1990-1991.
   Member, Undergraduate Curriculum Committee, 1991-1996, 1999-2000.
   Member, Electrical Engineering Curriculum Revision Committee, 1993.
   Chair, Undergraduate Curriculum Committee, 1996-1997.

3. Elected Member, General Faculty Assembly, 1992-1995.

4. Elected Member, Academic Senate, 1992-1995, 2001-2004.

C. OTHER CONTRIBUTIONS

Engineering Consulting

1. Technology Brokers, Inc., Atlanta. Designed a multiply redundant power supply interface for computer switching equipment. October 1989-January, 1991, and January-October 1992.

2. Loher Drive Systems, Inc., Atlanta. Developed a computer program to calculate the synchronizing and damping torques in induction motors. December 1991.

3. Walt Disney, Inc., Orlando, FL. Consulted on a legal case involving a rail transit system. February 1991.

4. Ashley Royal, Atty-at-Law, Macon, GA. Consulted on a legal case involving an induction motor failure. March 1992.

5. Dosco Co., Inc., Abingdon, VA. Consulted on the design of a drive system for a mining vehicle. 1995.

6. Alvey, Inc., St. Louis, MO. Consulted on the protection of conveyor motors in a large material handling plant. December 1995.

7. Stamler Co., Inc., Lexington, KY. Consulted on the design of a drive system for a mining vehicle. April, 1996.

8. General Electric Corp R&D, Schenectady, NY. Consulted on the design and development of motor diagnostic equipment. August 1996.

9. ABB Combustion Engineering, Windsor, CT. Consulted on the protection of a nuclear reactor coolant pump motor. December 1996 – February 1998.

10. Integrated Electronics, West Allis, WI. Design of high performance drive. April-August, 1998

11. Frazer, Greene, Upchurch & Baker, L.L.C., Expert witness involving a drive manufacturer, Jan. – May, 1998.

12. Rockwell Allen-Bradley Corp., Milwaukee, WI, summer 1998 employment in Corporate R&D. Worked involved the design and analysis of inverter output filters for reduced dv/dt.

13. Eaton Corporation, Innovation Center, Milwaukee, WI, summer 1999, summer 2000, summer 2001, summer 2002 employment. Work involved induction machine diagnostics using neural networks.

14. Pepper-Hamilton, L.L.P., Expert witness in a patent infringement suit. Case went to trial. December, 1999 – May 2000.

15. Arsenal Research, Vienna, Austria, summer 2005 employment. Work involved sensorless motor bearing diagnostics.

D. Editorial and Reviewer Work for Technical Journals

1. Associate Editor for High Power Applications, *IEEE Transactions on Power Electronics,* 1993-1999. Approximately 15-25 papers per year were handled as Associate Editor.

2. Reviewer for *IEEE Transactions on Power Electronics,* 1989-present. Approximately 6-10 papers per year are reviewed for this journal.

3. Reviewer for *IEEE Transactions on Industry Applications,* 1988-present. Approximately 4-5 papers per year are reviewed for this journal.

4. Reviewer for *IEEE Transactions on Automatic Control,* 1990, 1999.

5. Reviewer for *IEEE Transactions on Aerospace and Electronic Systems*, 1991-1994.

6. Digest reviewer and session organizer for Power Electronics Specialists Conference, 1989-1994, 1998.

7. Digest reviewer for European Power Electronics Conference, 1991 and 1993.

8. Digest reviewer for Applied Power Electronics Conference, 1991-1993, 1997-1999.

9. Reviewer for 1992 IEEJ (Japan)/IEEE Power Conversion Conference–Yokohama.

10. Session Organizer and Reviewer, IEEE Industry Applications Society Annual Meeting and Conference, 1992.

11. Reviewer for IEEE Conference on Decision and Control, 1993.

12. Reviewer for IEEE Transactions on Industrial Electronics, 1993, 1997-1999.

13. Topic Chair and Session Organizer, Power Electronics Specialists Conference, 1994, 1999.

VI. GRANTS AND CONTRACTS

A. AS PI OR CO-PI

1. "On-line prediction of induction machine failures"
   Siemens Energy and Automation Industrial Controls Division
   Joint proposal with Schlag, J. H.
   Contract Period: 4/1/91 - 3/31/94
   Amount Requested: $547,974
   Amount Funded: $547,974

2. "Analysis and mitigation of acoustic noise in inverter driven machines for electric vehicles"
   Renault, Inc.
   Date of Grant: December 1991
   Amount Requested: $25,000
   Amount Funded: $25,000

3. "Hybrid electric vehicle virtual testbed"
   U.S. Advanced Research Projects Agency and NEETRAC
   Subcontract with GTRI
   Contract Period: 6/1/95 - 6/30/98
   Amount Requested: $310,000 for ECE (total project amount is $800,000)
   Amount Funded: $310,000 for ECE (total project amount is $800,000)

4. "Correlation of vibration and current spectral data in induction machines"
   General Electric Corporate R&D
   Date of Grant: November 1995
   Amount Requested: $25,000
   Amount Funded: $25,000

5. "Insulation fault detection and condition monitoring for ASD-connected motors"
   General Electric Corporate R&D
   Contract Period: 3/25/96 - 9/25/96
   Amount Requested: $25,000
   Amount Funded: $25,000

6. "Undergraduate mechatronics laboratory"
   National Science Foundation
   (Co-PI with Charles Ume, ME)
   Contract Period: 8/1/97 - 7/31/99
   Amount Requested: $60,000 for ECE (total project amount is $170,000)
   Amount Funded: $60,000 for ECE (total project amount is $170,000)

7. "Workshop on intelligent systems in power electronics"
   National Science Foundation
   Contract Period: 2/1/98 - 1/31/00
   Amount Requested: $30,000
   Result: $30,000 (3/1/98-3/1/00)

8. "Ground current mitigation in ac drives"
   Rockwell Automation Inc.
   Date of Grant: July 1, 1998
   Amount Requested: $15,000
   Amount Funded: $15,000

9. "Rotating fault detection and stator thermal failure prediction"
   Eaton Corporation
   Contract Period: 1/4/99-6/30/03
   Amount Requested: $426,338
   Amount Funded: $426,338

10. "Feasibility study for the use of neural network-based diagnostics for underground cable systems"
    NEETRAC Baseline Funding
    Co-PI with R. Hartlein and R. Harley
    Contract Period: 8/21/99-12/18/99
    Amount Requested: $45,500
    Amount Funded: $45,500

11. "On-chip power supplies"

State of Georgia - Yamacraw Initiative
Co-PI with P. Allen
Contract Period: 7/1/99-6/30/00
Amount Requested: $106,000
Amount Funded: $106,000

12. "Feasibility study for the use of neural network-based diagnostics for underground cable systems"
NEETRAC Baseline Funding
Phase One: Contract Period: July 1999-April 2000
Amount Requested:$45,500
Amount Funded: $45,500
Phase Two: Contract Period: May 2000-December 2000
Amount Requested:$38,500
Amount Funded: $38,500

13. "Power Electronics Short Course", Project #X-20-5M8
Dr. R. Harley as PI and Course Administrator. (Course presented by Dr. W. Sayle and Dr. M. Jovanovic)
ON-Semiconductor, Phoenix, AZ
Contract period: May 22-24, 2000
Amount Requested: $42,049
Amount Funded: $42,049

14. "Intelligent Electronic Overload Relays for Small Size Mains-Fed Induction Machines"
Square D Co.
Contract Period: 11/25/02-12/31/06
Amount Requested: $337,237
Amount Funded: $337,237

15. "Permanent Magnet Electrical Drive Diagnostics for Automotive Systems"
Delphi Automotive Systems/Saginaw Steering Systems
Contract Period: 3/1/02-2/28/05
Amount Requested: $165,384
Amount Funded: $165,384

16. "Separating Load And Fault Effects In Current-Based Motor Condition Monitoring"
University of Illinois/CEME
Contract Period: 8/29/03-6/30/06
Amount Requested: $35,000
Amount Funded: $35,000

17. "Motor Interface Architecture and Functionality For WTP"
Subcontractor to Eaton Corporation, Prime contractor: US Dept. of Energy.
Contract Period: 8/1/04-6/30/07
Amount Requested: $220,000

Amount Funded: $220,000

18. "Development Of Diagnosis Algorithms And Fail-Safe Strategies For Interior Permanent Magnet Machines,"
Hyundai Motor Company
Contract Period: 1/12/05-11/30/06
Amount Funded: $93,722

VII. PROFESSIONAL HONORS AND AWARDS

1. Fellow of the Institute of Electrical and Electronics Engineers (IEEE). Elected in 2002 with citation, ***"For contributions to electric motor control and condition monitoring."***

2. Industrial Drives Committee First Prize Paper Award at the IEEE Industry Applications Society Annual Conference, 1989.

3. Industrial Drives Committee Second Prize Paper Award at the IEEE Industry Applications Society Annual Conference, 1991.

4. Electric Machines Committee Second Prize Paper Award at the IEEE Industry Applications Society Annual Conference, 1994.

5. Electric Machines Committee Second Prize Paper Award at the IEEE Industry Applications Society Annual Conference, 2001.

6. Member, Eta Kappa Nu Honor Society.

7. Invited Session Chair, IEEE Power Electronics Specialists Conference, 1990, 1991, 1993, 1994, 1995, 1997, 1998, 1999.

8. Session Chair, IEEE Industry Applications Society Annual Conference and Meeting, 1990, 1992

9. Session Chair, IEEE International Conference on Harmonics in Power Systems, 1992.

10. Session Chair, IEE of Japan/IEEE Joint IAS Power Conversion Conference, 1993.

11. Session Chair, IEEE International Telecommunications Energy Conference, 2001.

EXHIBIT 2
(USP 6,249,876)

US006249876B1

(12) **United States Patent**
Balakrishnan et al.

(10) **Patent No.: US 6,249,876 B1**
(45) **Date of Patent: Jun. 19, 2001**

(54) **FREQUENCY JITTERING CONTROL FOR VARYING THE SWITCHING FREQUENCY OF A POWER SUPPLY**

(75) Inventors: **Balu Balakrishnan**; **Alex Djenguerian**, both of Saratoga; **Leif Lund**, San Jose, all of CA (US)

(73) Assignee: **Power Integrations, Inc.**, San Jose, CA (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **09/192,959**

(22) Filed: **Nov. 16, 1998**

(51) **Int. Cl.**[7] **G06F 1/04**
(52) **U.S. Cl.** **713/501**; 713/300; 713/503
(58) **Field of Search** 713/300, 320, 713/322, 500, 501, 503

(56) **References Cited**

U.S. PATENT DOCUMENTS

4,712,169	*	12/1987	Albach	363/89
4,930,063	*	5/1990	Henze et al.	363/91
5,459,392	*	10/1995	Mandelcorn	323/222
6,107,851	*	8/2000	Balakirshnan et al.	327/172

OTHER PUBLICATIONS

Ashok Bindra, "Power–Conversion Chip Cuts Energy Wastage in Off–Line Switchers," *Electronic Design*, pp. 46,48, Oct. 1998.

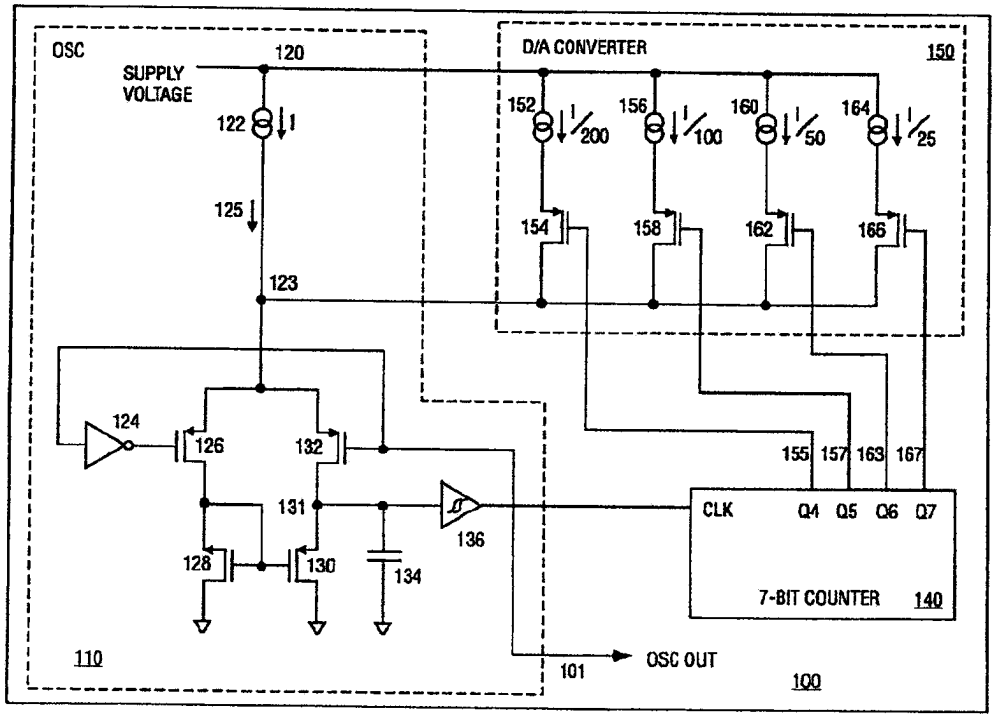
* cited by examiner

Primary Examiner—Dennis M. Butler
(74) *Attorney, Agent, or Firm*—Blakely, Sokoloff, Taylor & Zafman, LLP.

(57) **ABSTRACT**

EMI emission is reduced by jittering the switching frequency of a switched mode power supply. An oscillator with a control input for varying the oscillator's switching frequency generates a jittered clock signal. In one embodiment, the oscillator is connected to a counter clocked by the oscillator. The counter drives a digital to analog converter, whose output is connected to the control input of the oscillator for varying the oscillation frequency. In another embodiment, the oscillator is connected to a low frequency oscillator whose low frequency output is used to supplement the output of the oscillator for jittering the switching frequency. The invention thus deviates or jitters the switching frequency of the switched mode power supply oscillator within a narrow range to reduce EMI noise by spreading the energy over a wider frequency range than the bandwidth measured by the EMI test equipment.

32 Claims, 6 Drawing Sheets



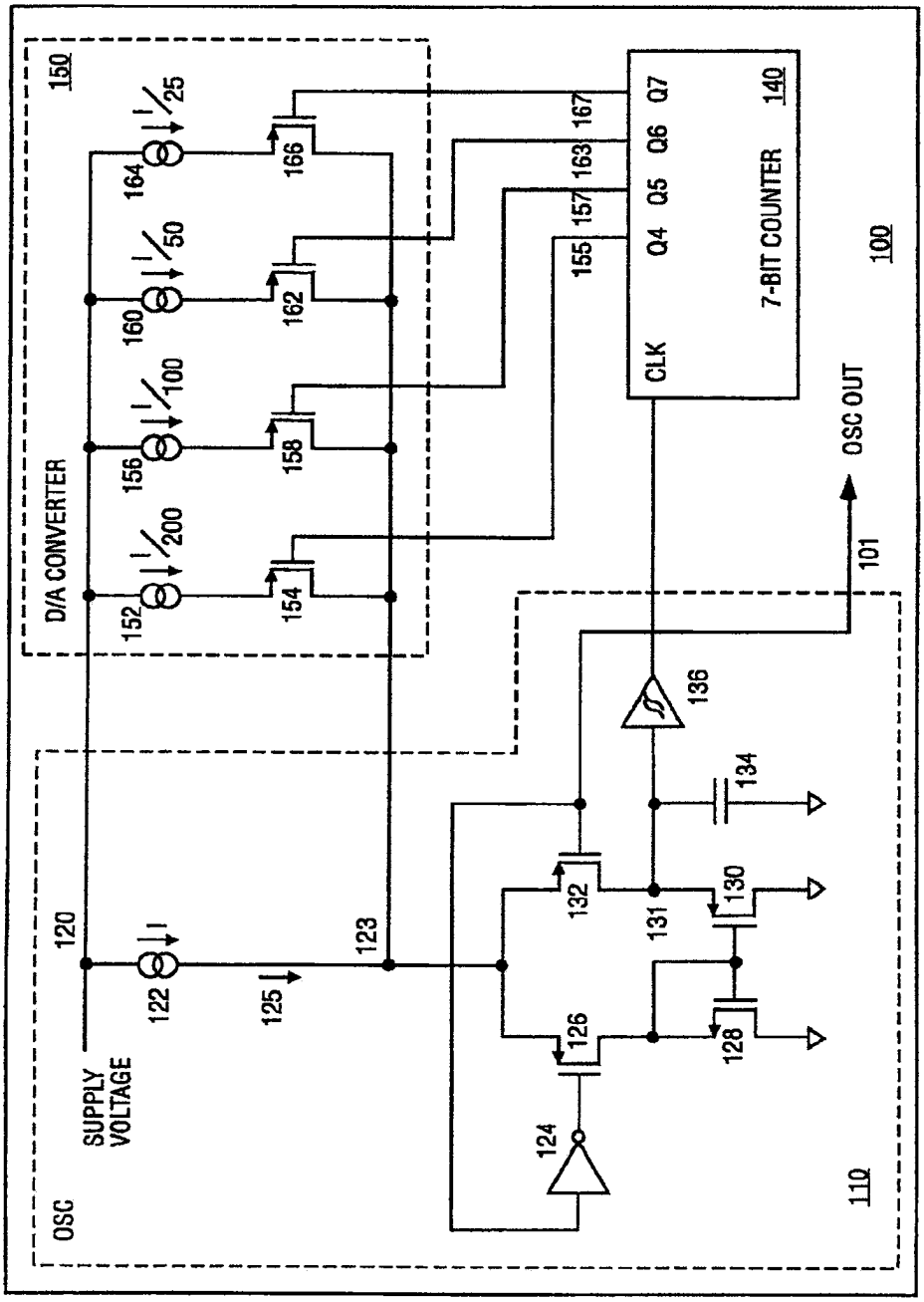

150
D/A CONVERTER
1/25
1/50
1/100
1/200
164
160
156
152
166
162
158
154
167
163
157
155
140
7-BIT COUNTER
Q7
Q6
Q5
Q4
CLK
100
OSC OUT
101
136
134
132
130
131
126
128
124
123
120
122
125
SUPPLY VOLTAGE
OSC
110

FIG. 1

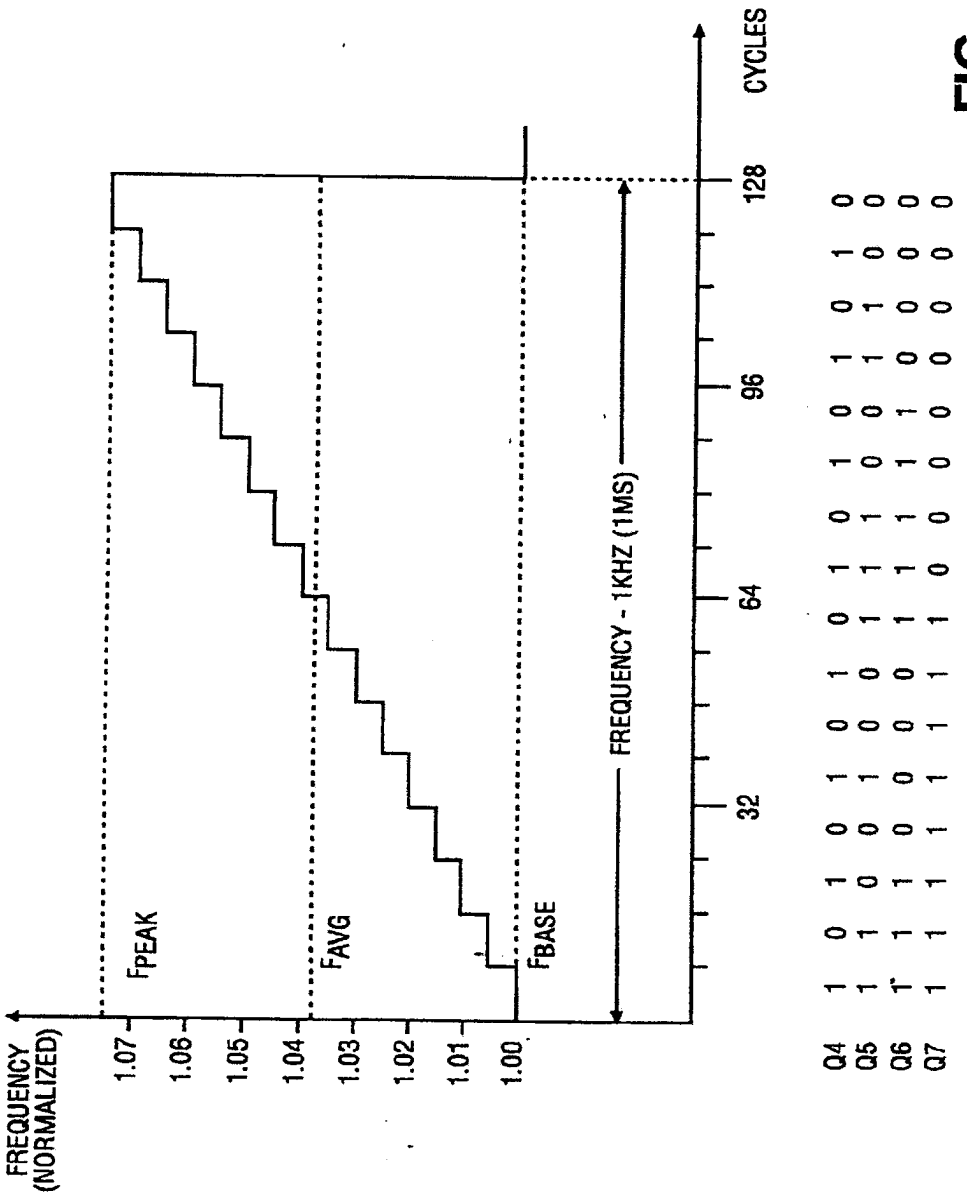

FREQUENCY (NORMALIZED)
1.07
1.06
1.05
1.04
1.03
1.02
1.01
1.00
FPEAK
FAVG
FBASE
FREQUENCY - 1KHZ (1MS)
CYCLES
32
64
96
128
Q4 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0
Q5 1 1 0 0 1 0 0 1 1 1 1 1 0 0 0 0
Q6 1 1 1 0 0 0 0 1 1 1 0 0 1 1 0 0
Q7 1 1 1 1 1 1 1 1 1 0 0 0 0 0 0 0

FIG. 2

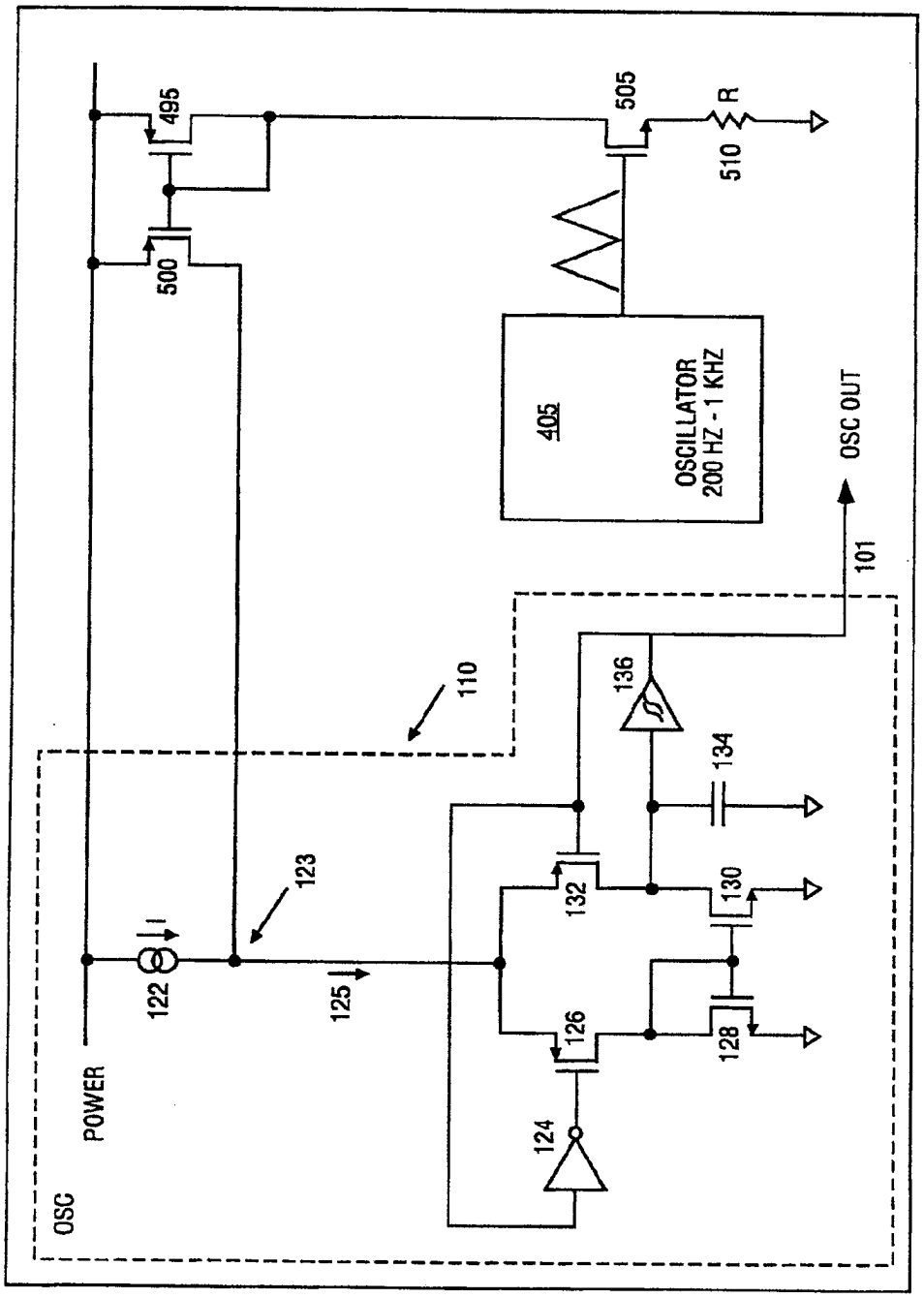

495
505
R
510
500
405
OSCILLATOR
200 HZ - 1 KHZ
OSC OUT
101
110
136
134
123
132
130
122
125
126
128
POWER
124
OSC

FIG. 3

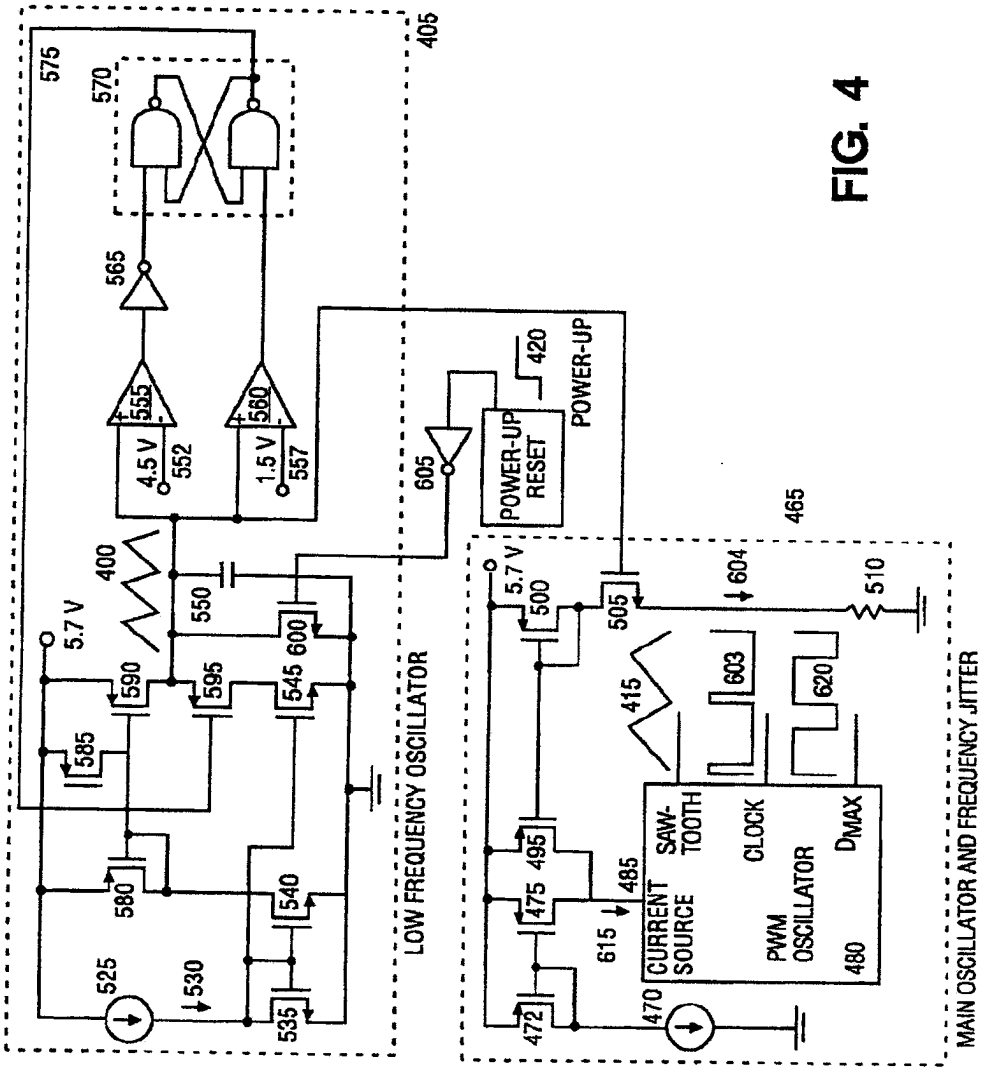

405
575
570
565
555
560
4.5 V
552
1.5 V
557
605
420
POWER-UP
POWER-UP RESET
400
550
600
5.7 V
590
595
545
585
580
540
525
530
535
LOW FREQUENCY OSCILLATOR
465
5.7 V
500
505
604
510
415
603
620
495
485
475
615
472
470
CURRENT SOURCE
SAW-TOOTH
CLOCK
PWM OSCILLATOR
DMAX
480
MAIN OSCILLATOR AND FREQUENCY JITTER

FIG. 4

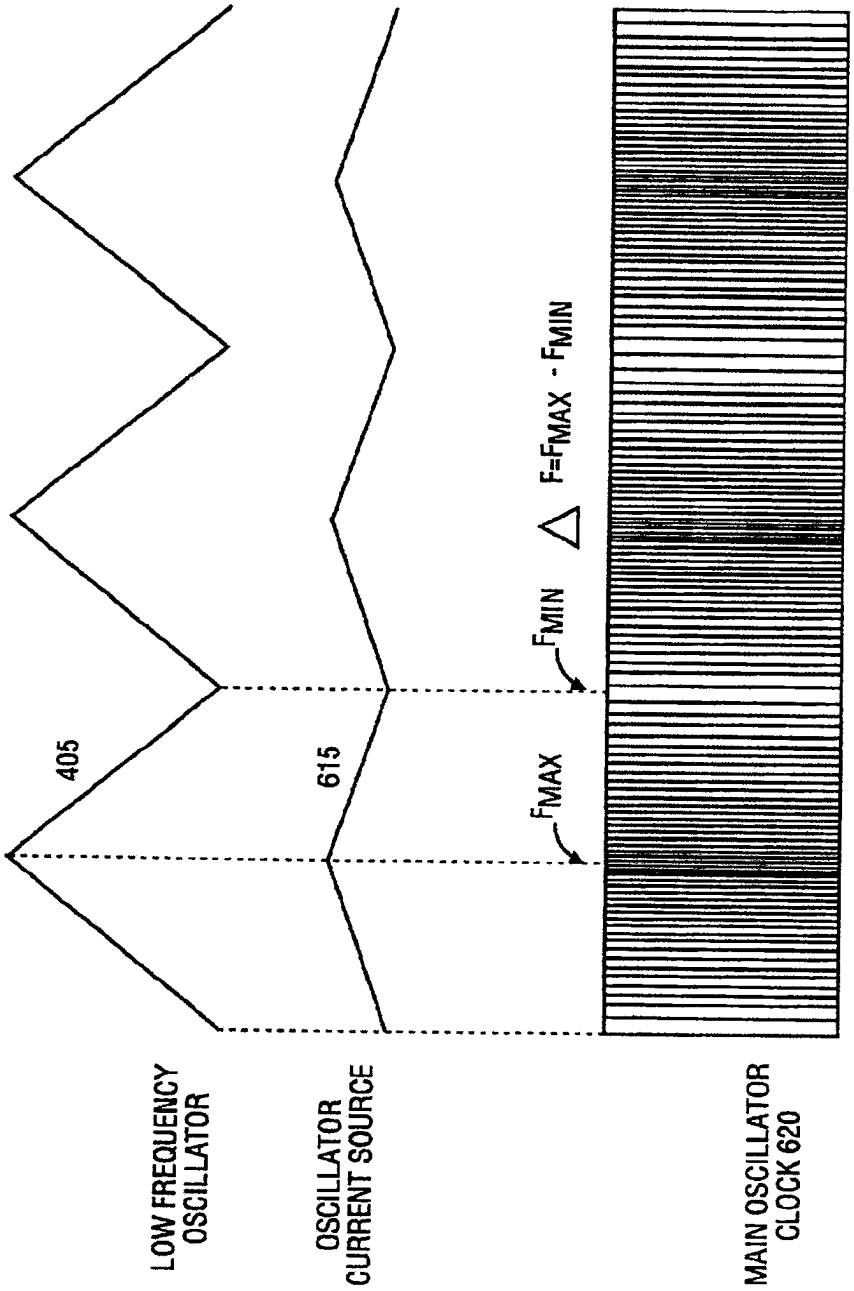

LOW FREQUENCY OSCILLATOR
OSCILLATOR CURRENT SOURCE
MAIN OSCILLATOR CLOCK 620
405
615
FMAX
FMIN
F=FMAX - FMIN

FIG. 5

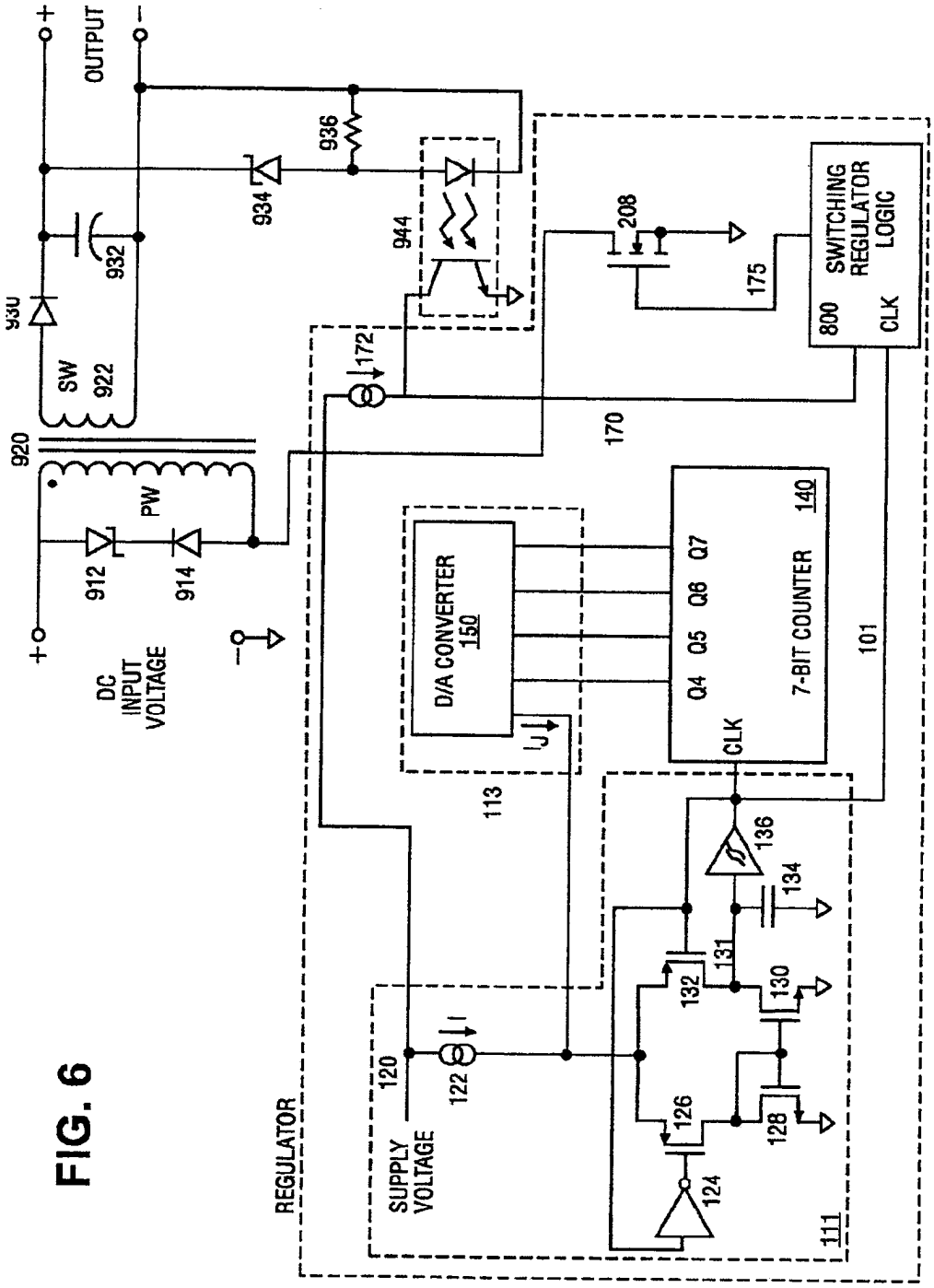

OUTPUT
+
-
936
934
944
932
930
SW
922
920
PW
912
914
DC
INPUT
VOLTAGE
208
175
SWITCHING
REGULATOR
LOGIC
800
CLK
172
170
D/A CONVERTER
150
Q4 Q5 Q6 Q7
7-BIT COUNTER
140
101
CLK
113
136
134
131
132
130
126
128
124
120
122
SUPPLY
VOLTAGE
REGULATOR
111

FIG. 6

FREQUENCY JITTERING CONTROL FOR VARYING THE SWITCHING FREQUENCY OF A POWER SUPPLY

BACKGROUND

The present invention relates to an off-line switched mode control system with frequency jittering.

Many products rely on advanced electronic components to cost-effectively provide the product with the desired functionality. These electronic components require power regulation circuitry to supply them with a clean and steady source of power. The development of switched mode power supply technology has led to power supplies operating at high frequency to achieve small size and high efficiency. Each switched mode power supply typically relies on an oscillator switching at a fixed switching frequency or alternatively a variable frequency (such as in a ringing choke power supply).

Due to the high frequency operation relative to the frequency of an alternating current (AC) power line, switched mode power supplies can exacerbate problems associated with electromagnetic interference (EMI). EMI noise is generated when voltage and current are modulated by the switching power supply. This electrical noise can be transferred to the AC power line.

In addition to affecting the operation of other electronics within the vicinity of the power supply by conduction, EMI induced noise on a power line may radiate or leak from the power line and affect equipment which is not even connected to the power line. Both conducted and radiated electrical noise may adversely affect or interfere with the operation of the electronic equipment. For example, EMI noise generated by the switching power supply can cause problems for communication devices in the vicinity of the power supply. Radiated high frequency noise components may become a part of the AC mains signal and may be provided to other devices in the power grid. Further, power supply radiated EMI can interfere with radio and television transmissions.

To address EMI related interference, several specifications have been developed by government agencies in the United States and in the European Community. These agencies have established specifications that define the maximum amount of EMI that can be produced by various classes of electronic devices. Since power supplies generate a major component of the EMI for electronic devices, an important step in designing such supplies that conform to the specifications is to minimize EMI emission to the acceptable limits of the various specifications.

EMI may be reduced in a power supply by adding snubbers and input filters. These components reduce the noise transferred to the power line and by so doing, also reduce the electric and magnetic fields of noise generated by the power line. While these methods can reduce EMI, they usually complicate the design process as well as increase the production cost. In practice, noise filtering components are added in an ad hoc manner and on a trial-and-error basis during the final design process when EMI is found to exceed the compliance limits specified by the regulatory agencies. This inevitably adds unexpected costs to the products.

Further, extra components can undesirably increase the size and weight of the power supply and thus the resulting product.

SUMMARY OF THE INVENTION

EMI emission is reduced by jittering the switching frequency of a switched mode power supply. In one aspect, a frequency jittering circuit varies the switching frequency using an oscillator for generating a switching frequency signal, the oscillator having a control input for varying the switching frequency. A digital to analog converter is connected to the control input for varying the switching frequency, and a counter is connected to the output of the oscillator and to the digital to analog converter. The counter causes the digital to analog converter to adjust the control input and to vary the switching frequency.

Implementations of the invention include one or more of the following. The oscillator has a primary current source connected to the oscillator control input. A differential switch may be used with first and second transistors connected to the primary current source; a third transistor connected to the first transistor; and a fourth transistor connected to the second transistor at a junction. A capacitor and one or more comparators may be connected to the junction. The digital to analog converter has one or more current sources, with a transistor connected to each current source and to the counter. The primary current source may generate a current I and each of the current sources may generate a current lower than I. The current sources may generate binary weighted currents. The largest current source may generate a current which is less than about 0.1 of I.

In a second aspect, a method for generating a switching frequency in a power conversion system includes generating a primary current; cycling one or more secondary current sources to generate a secondary current which varies over time; and supplying the primary and secondary currents to a control input of an oscillator for generating a switching frequency which is varied over time.

Implementations of the invention include one or more of the following. A counter may be clocked with the output of the oscillator. The primary current may be generated by a current source. If the primary current is I, each of the secondary current sources may generate a supplemental current lower than I and which is passed to the oscillator control input. The supplemental current may be binary-weighted. The largest supplemental current may be less than approximately 0.1 of I.

In another aspect, a method for generating a switching frequency in a power conversion system includes generating a primary voltage; cycling one or more secondary voltage sources to generate a secondary voltage which varies over time; and supplying the primary and secondary voltages to a control input of a voltage-controlled oscillator for generating a switching frequency which is varied over time.

Implementations of the invention include one or more of the following. Where the primary voltage is V, each of the secondary voltage sources may generate a supplemental voltage lower than V which may be passed to the voltage-controlled oscillator. The supplemental voltage may be binary-weighted.

In another aspect, a frequency jittering circuit for varying a power supply switching frequency includes an oscillator for generating a switching frequency signal, the oscillator having a control input for varying the switching frequency; and means connected to the control input for varying the switching frequency.

Implementations of the invention include one or more of the following. The means for varying the frequency may include one or more current sources connected to the control input; and a counter connected to the output of the oscillator and to the one or more current sources. The oscillator may include a primary current source connected to the control

input; and a differential switch connected to the primary current source. The differential switch may have first and second transistors connected to the primary current source; a third transistor connected to the first transistor; and a fourth transistor connected to the second transistor at a junction. A capacitor and a comparator may be connected to the junction. If the primary current source generates a current I, each of the current sources may generate a second current lower than the current I, further comprising a transistor connected to each current source connected to the counter. The means for varying the frequency may include one or more voltage sources connected to the control input; and a counter connected to the output of the oscillator and to the one or more voltage sources. The oscillator may include a primary voltage source connected to the control input; and a differential switch connected to the primary voltage source. The means for varying the frequency may include a capacitor; a current source adapted to charge the capacitor; and means for alternatingly charging and discharging the capacitor. One or more comparators may be connected to the capacitor and the means for alternatingly charging and discharging the capacitor.

In yet another aspect, a power supply includes a transformer, an oscillator for generating a signal having a frequency, the oscillator having a control input for varying the frequency of the signal, the oscillator including a primary current source connected to the control input; a differential switch connected to the primary current source; a capacitor connected to the differential switch; and a comparator connected to the differential switch. The power supply also includes a digital to analog converter connected to the control input, the analog to digital converter having one or more current sources, wherein the primary current source generates a current I and each of the current sources generates a current lower than I. A counter is connected to the output of the oscillator and to the current sources of the digital to analog converter. Further, a power transistor is connected to the primary winding of the transformer so that when the power transistor is modulated, a regulated power supply output is provided.

In another aspect, a power supply includes a transformer connected to an input voltage. The power supply includes an oscillator for generating a signal having a frequency, the oscillator having a control input for varying the frequency of the signal, the oscillator including: a primary current source connected to the control input; a differential switch connected to the primary current source; a capacitor connected to the differential switch; and a comparator connected to the differential switch. A circuit for varying the frequency is connected to the control input, the circuit having a capacitor; a current source adapted to charge and discharge the capacitor; one or more comparators connected to the capacitor to the current source for alternatingly charging and discharging the capacitor. Further, a power transistor is connected to the oscillator and to the primary winding. The power transistor modulates its output in providing a regulated power supply output.

Advantages of the invention include one or more of the following. The jittering operation smears the switching frequency of the power supply over a wide frequency range and thus spreads energy outside of the bandwidth measured by the EMI measurement equipment. By changing the oscillator frequency back and forth, the average noise measured by the EMI measurement equipment is reduced considerably.

Further, the invention provides the required jittering without requiring a large area on the regulator chip to implement a capacitor in a low frequency oscillator. Further, the invention minimizes effects caused by leakage current from transistors and capacitors associated with a low frequency oscillator. Thus, the jittering operation can be maintained even at high temperature which can increase current leakage.

Additionally, the invention reduces the need to add extra noise filtering components associated with the EMI filter. Therefore a compact and inexpensive power supply system can be built with minimal EMI emissions.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** is a schematic diagram of a digital frequency jittering device.

FIG. **2** is a plot illustrating the operation of the device of FIG. **1**.

FIG. **3** is a schematic diagram of an analog frequency jittering device.

FIG. **4** is a schematic diagram of an implementation of the device of FIG. **3**.

FIG. **5** is a timing diagram illustrating the operation of the frequency jitter device of FIG. **4**.

FIG. **6** is a schematic diagram of a switched mode power supply in accordance with the present invention.

DESCRIPTION

FIG. **1** shows a digital frequency jittering circuit **100**. The digital frequency jittering circuit **100** has a primary oscillator **110** which provides a clock signal to a counter **140**. The primary oscillator **110** typically operates between 100 kHz and 130 kHz. The counter **140** can be a seven bit counter. Each output of counter **140**, when clocked by primary oscillator **110**, represents a particular time interval. The outputs of the counter **140** are provided to a series of frequency jittering current sources **150**. The outputs of the series of frequency jittering current sources **150** are presented to the primary oscillator **110** to vary its frequency, as will be described below.

Primary oscillator **110** contains a primary current source **122** which provides a primary current (denoted as I) to node **123**. Current **125** to the node **123** is provided to the source of MOSFET transistors **126** and **132**. The drain of MOSFET transistor **126** is connected to the drain of an n-channel MOSFET transistor **128**. The source of transistor **128** is grounded, while the gate of the transistor **128** is connected to its drain. The gate of the transistor **128** is also connected to the gate of an n-channel MOSFET transistor **130**. The source of the transistor **130** is grounded while the drain is connected to the drain of the MOSFET transistor **132** at a node **131**. Transistors **126**, **128**, **130** and **132** form a differential switch. The output of comparator **136** is connected to the gate of the transistor **132** and to an inverter **124**. The output of inverter **124** is connected to the gate of transistor **126**. The comparator **136** has an input which is connected to node **131** and to a capacitor **134**. In combination, the transistors **126**, **128**, **130** and **132**, capacitor **134**, inverter **124**, current source **122** and comparator **136** form an oscillator. The output of the comparator **136** is provided as an oscillator output OSC_OUT **101** and is also used to drive the clock input of counter **140**.

Counter **140** has a plurality of outputs Q1–Q3 (not shown) which are not used. The remaining outputs Q4–Q7 are connected to a digital-to-analog (D-to-A) converter **150**, which may be implemented as a series of frequency jittering voltage sources or current sources. A Q4 output **155** is connected to the gate of a p-channel MOSFET transistor

154. A Q5 output 157 is connected to the gate of a p-channel MOSFET transistor 158. The Q6 output 163 is connected to the gate of a p-channel MOSFET transistor 162, and Q7 output 167 is connected to the gate of a p-channel MOSFET transistor 166. When D-to-A converter 150 is viewed as a plurality of current sources, the source of transistor 154 is connected to a jittering current source 152, which provides a current which is 1/200th of the current I generated by the current source 122. The source of MOSFET transistor 158 is connected to a current source 156 which provides a current that is 1/100th of the current I. The source of the MOSFET transistor 162 is connected to a jittering current source 160 which provides a current that is 1/50th of I. Finally, the source of the MOSFET transistor 166 is connected to a jittering current source 164 which provides a current that is 1/25th of the current I. The current sources 152, 156, 160 and 164 are binary-weighted, that is, the current source 164 provides twice the current provided by the current source 160, the current source 160 provides twice the current supplied by the current source 156 and the current source 156 provides twice the current provided by the current source 152.

Further, in one embodiment, the largest current source 164 may supply no more than 10% of the current I provided by the primary current source 122. The drain of transistors 154, 158, 162 and 166 are joined together such that the supplemental frequency jittering current sources of the D-to-A converter 150 can be provided to supplement the primary current source 122.

During operation, at every eight clock cycles, the counter output Q4 on line 155 changes state. Similarly, at every 16 clock cycles, the output Q5 on line 157 changes state and at every 32 clock cycles, the output Q6 on line 163 changes state, and every 64 clock cycles, the output Q7 on line 167 changes state. The entire counting cycle thereafter repeats itself.

Each time the output Q4 on line 155 is low, transistor 154 is turned on to inject current in the amount of I/200 to node 123 so that the total current 125 is 1.005I. Similarly, each time that the output Q5 on line 157 is low, transistor 158 is turned on to inject current in the amount of I/100 to node 123 so that the total current 125 is 1.01I. Further, each time that output Q6 on line 163 is low, transistor 162 is turned on to inject current in the amount of I/50 to node 123 so that the total current 125 is 1.02I. Finally, each time that the output Q7 on line 167 is low, the transistor 166 is turned on to inject current in the amount of I/25 to node 123 so that the total current 125 is 1.04I.

Additionally, when combinations of outputs Q4–Q7 are turned on, the outputs of the respective current sources 152, 156, 160 and 164 are added to the output of current source 122 to vary the frequency of the primary oscillator 110. In this manner, counter 140 drives a plurality of current sources to inject additional current to the main current source 122 such that the frequency of the primary oscillator 110 is varied.

The jittering operation of the embodiment of FIG. 1 is further illustrated in a chart in FIG. 2. A normalized operating frequency is plotted on the y-axis while the counting cycle as shown by the counter outputs Q4–Q7 is plotted on the x-axis. As shown in FIG. 2, as the counter counts upward to the maximum count of 128, the peak switching frequency is achieved. This peak switching frequency is normalized to be about 1.075 times the base switching frequency. Further, on average, the switching frequency is between 1.03 and 1.04 times the base switching frequency. Thus, the embodiment of FIG. 1 deviates the switching frequency of the oscillator within a narrow range. This deviation reduces EMI noise by spreading the energy over a wider frequency range than the bandwidth measured by the EMI test equipment such that the noise measured by the EMI test equipment is reduced considerably.

FIG. 3 shows an analog frequency jittering circuit. More details on the analog frequency jittering device are shown in co-pending U.S. application Ser. No. 09/080,774, entitled "OFFLINE CONVERTER WITH INTEGRATED SOFT START AND FREQUENCY JITTER," filed on May 18, 1998, the content of which is hereby incorporated by reference. In FIG. 3, the primary oscillator 110 provides an oscillator output on line OSC-OUT 101. An analog low frequency oscillator 405 is also provided. Primary oscillator 110 typically operates between a range of 30 to 300 kHz, while the low frequency oscillator 405 typically operates between a range of 5 Hz to 5 kHz. As discussed above, the switching frequency of the primary oscillator 110 is determined by the amount of current the primary oscillator uses to charge and discharge capacitor 134. The low frequency oscillator 405 varies this current within a narrow range to jitter the frequency of the primary oscillator 110.

The output of low frequency oscillator 405 is provided to a MOSFET transistor 505 connected to a resistor 510 and a current mirror including transistors 495 and 500. Transistor 500 is connected to node 123 so that extra current can be added to current source 122 feeding the primary oscillator. In this manner, the frequency of the primary oscillator 110 is shifted around a narrow range to reduce the EMI noise.

FIG. 4 shows a more detailed implementation of FIG. 3. As shown therein, main oscillator 465 has a current source 470 that is mirrored by current mirror transistors 472 and 475. Main oscillator drive current 615 is provided to current source input 485 of oscillator 480. The magnitude of the current input into current source input 485 determines the frequency of the oscillation signal 415 provided by oscillator 480. In order to vary the frequency of the oscillation signal 415, an additional current source 495 is provided within the main oscillator 465. The current source 495 is mirrored by current source mirror 500.

The current provided by current source 495 is varied as follows. Frequency variation signal 400 is provided to the gate of main oscillator transistor 505. As the magnitude of frequency variation signal 400 increases, so does the voltage at the source of main oscillator transistor 505 due to the increasing voltage at the gate of the transistor 505 and the relatively constant voltage drop between the gate and source of the transistor 505. As the voltage at the source of transistor 505 increases, so does the current 604 flowing through the resistor 510. The current flowing through the resistor 510 is the same as the current flowing through additional current source 500 which mirrors transistor 495.

Since the frequency variation signal 400 is a triangular waveform having a fixed period, as shown, the magnitude of the current input by additional current source mirror 500 will vary linearly with the magnitude of the rising and falling edges of the frequency variation signal 400. If the frequency variation signal 400 is a ramp signal, the frequency will linearly rise to a peak and then fall to its lowest value. In this way, the current 615 provided to current source input 485 of the oscillator 480 is varied in a known fixed range that allows for an easy and accurate frequency spread of the high frequency current. Further, the variance of the frequency is determined by the magnitude of the current provided by current source mirror 500, which is a function of the resistance of the resistor 510.

Frequency variation circuit **405** includes a current source **525** that produces a fixed magnitude current **530** that determines the magnitude of the frequency of the frequency variation signal **400**. Although the current **530** has a fixed magnitude, the frequency variation signal can be generated utilizing a variable magnitude current. If such variable current is generated, the frequency spread is not fixed in time but varies with the magnitude of current **530**. The fixed magnitude current **530** is fed into first transistor **535**, mirrored by second transistor **540** and third transistor **545**. The frequency variation signal **400** is generated by the charging and discharging of the capacitor **550**. Frequency variation circuit capacitor **550** has a relatively low capacitance, which allows for integration into a monolithic chip in one embodiment of low frequency oscillator **405**. The frequency variation signal **400** is provided to upper limit comparator **555** and lower limit comparator **560**. The output of upper limit comparator **555** will be high when the magnitude of the frequency variation signal **400** exceeds the upper threshold voltage on line **552** which is about 4.5 volts. The output of lower limit comparator **560** will be low when the magnitude of frequency variation signal **400** drops below lower threshold voltage on line **557** which is about 1.5 volts. The output of upper limit comparator **555** is provided to the frequency variation circuit inverter **565** the output of which is provided to the reset input of frequency variation circuit latch **570**. The set input of frequency variation circuit latch **570** receives the output of lower limit comparator **560**.

In operation, the output of lower limit comparator **560** will be maintained high for the majority of each cycle of frequency variation signal **400** because the magnitude of frequency variation signal will be maintained between the upper threshold on line **552**, 4.5 volts, and lower threshold on line **557**, 1.5 volts. The output of upper limit comparator **555** will be low until the magnitude of frequency variation signal **400** exceeds upper level threshold on line **552**. This means that the reset input will receive a high signal when the magnitude of the frequency variation signal **400** rises above the upper threshold signal on line **552**.

The charge signal **575** output by frequency variation circuit latch **570** will be high until the frequency variation signal **400** exceeds the upper threshold limit signal on line **552**. When the charge signal **575** is high, transistors **585** and **595** are turned off. By turning off transistors **585** and **595**, current can flow into the capacitor **550**, which steadily charges capacitor **550** and increases the magnitude of frequency variation signal **400**. The current that flows into the capacitor **550** is derived from current source **525** because the current through transistor **590** is mirrored from transistor **580**, which in turn is mirrored from transistor **535**.

During power up, when power-up signal **420** is low, the output of inverter **605** is high, which turns on transistor **600**, causing frequency variation signal **400** to go low. The frequency variation signal **400** starts from its lowest level to perform a soft start function during its first cycle of operation.

Referring to FIGS. **4** and **5**, FIG. **5** shows the operation of the analog frequency jittering device of FIG. **4**. In FIG. **5**, a frequency variation signal **405** is provided to the main oscillator **465**. The magnitude of the current **615** is approximately the magnitude of the frequency variation signal **405**, less the threshold voltage of transistor **505**, and divided by the resistance of the resistor **510** plus the magnitude of the current produced by the current source **475**. The current **615** varies with the magnitude of the frequency variation signal **405**. The variation of the current **615** in turn varies the frequency of the oscillator clock.

Referring now to FIG. **6**, a switched mode power supply is shown. Direct current (DC) input voltage is provided to a Zener diode **912** which is connected to a diode **914**. The diodes **912–914** together are connected in series across a primary winding of a transformer **920**. A secondary winding **922** is magnetically coupled to the primary winding of transformer **920**. One terminal of the secondary winding **922** is connected to a diode **930**, whose output is provided to a capacitor **932**. The junction between diode **930** and capacitor **932** is the positive terminal of the regulated output. The other terminal of capacitor **932** is connected to a second terminal of the secondary winding and is the negative terminal of the regulated output. A Zener diode **934** is connected to the positive terminal of the regulated output. The other end of Zener diode **934** is connected to a first end of a light emitting diode in an opto-isolator **944**. A second end of the light-emitting diode is connected to the negative terminal of the regulated output. A resistor **936** is connected between the negative terminal of the regulated output and the first end of the light-emitting diode of opto-isolator **944**. The collector of the opto-isolator **944** is connected to current source **172**. The output of current source **172** is provided to the switching regulator logic **800**.

Connected to the second primary winding terminal is the power transistor **208**. Power transistor **208** is driven by the switching regulator logic **800**. Switching regulator logic **800** receives a clock signal **101** from an oscillator **111**. A counter **140** also receives the clock signal **101** from the primary oscillator **111**. The outputs of counter **140** are provided to D-to-A converter **150**, which is connected to oscillator **111** for jittering the oscillation frequency. Alternatively, in lieu of counter **140** and a D-to-A converter **150**, an analog low frequency jittering oscillator may be used.

The foregoing disclosure and description of the invention are illustrative and explanatory thereof, and various changes in the size, shape, materials, components, circuit elements, wiring connections and contacts, as well as in the details of the illustrated circuitry and construction and method of operation may be made without departing from the spirit of the invention.

What is claimed is:

1. A digital frequency jittering circuit for varying the switching frequency of a power supply, comprising:

an oscillator for generating a signal having a switching frequency, the oscillator having a control input for varying the switching frequency;

a digital to analog converter coupled to the control input for varying the switching frequency; and

a counter coupled to the output of the oscillator and to the digital to analog converter, the counter causing the digital to analog converter to adjust the control input and to vary the switching frequency.

2. The circuit of claim **1**, wherein the oscillator further comprises a primary current source coupled to the oscillator control input.

3. The circuit of claim **2**, further comprising a differential switch, including:

first and second transistors coupled to the primary current source;

a third transistor coupled to the first transistor; and

a fourth transistor coupled to the second transistor at a junction.

4. The circuit of claim **3**, further comprising a capacitor coupled to the junction.

5. The circuit of claim **3**, further comprising one or more comparators coupled to the junction.

6. The circuit of claim 2, wherein the digital to analog converter has one or more secondary current sources.

7. The circuit of claim 6, further comprising a transistor coupled between each secondary current source and the counter.

8. The circuit of claim 6, wherein the primary current source generates a current I and each of the secondary current sources generates a current lower than I.

9. The circuit of claim 8, wherein the secondary current sources generate binary weighted currents.

10. The circuit of claim 8, wherein the largest secondary current source generates a current which is less than about 0.1 of I.

11. A method for generating a switching frequency in a power conversion system, comprising:

generating a primary current;

cycling one or more secondary current sources to generate a secondary current which varies over time; and

combining the secondary current with the primary current to be received at a control input of an oscillator for generating a switching frequency which is varied over time.

12. The method of claim 11 further comprising the step of clocking a counter with the output of the oscillator.

13. The method of claim 11 wherein the primary current is generated by a current source.

14. The method of claim 11 wherein the primary current is I and each of the secondary current sources generates a supplemental current lower than I, and further comprising passing the supplemental current to the oscillator control input.

15. The method of claim 14 further comprising binary-weighting the supplemental current.

16. The method of claim 14 wherein the largest supplemental current is less than approximately 0.1 of I.

17. A method for generating a switching frequency in a power conversion system, comprising:

generating a primary voltage;

cycling one or more secondary voltage sources to generate a secondary voltage which varies over time; and

combining the secondary voltage with the primary voltage to be received at a control input of a voltage-controlled oscillator for generating a switching frequency which is varied over time.

18. The method of claim 17 further comprising clocking a counter with the output of the oscillator.

19. The method of claim 17 wherein the primary voltage is V and each of the secondary voltage sources generates a supplemental voltage lower than V, further comprising passing the supplemental voltage to the voltage-controlled oscillator.

20. The method of claim 19, wherein the supplemental voltage is binary-weighted.

21. A frequency jittering circuit for varying a power supply switching frequency, comprising:

an oscillator for generating a signal having a switching frequency, the oscillator having a control input for varying the switching frequency; and

means coupled to the control input for varying the switching frequency, including:

one or more current sources coupled to the control input; and

a counter coupled to the output of the oscillator and to the one or more current sources.

22. The circuit of claim 21 wherein the oscillator further comprises:

a primary current source coupled to the control input; and

a differential switch coupled to the primary source.

23. The circuit of claim 22 wherein the oscillator further comprises:

first and second transistors coupled to the primary current source;

a third transistor coupled to the first transistor; and

a fourth transistor coupled to the second transistor at a junction.

24. The circuit of claim 22 further comprising a capacitor and a comparator coupled to the junction.

25. The circuit of claim 22 wherein the primary current source generates a current I and each of said one or more current sources generates a current lower than I.

26. The circuit of claim 22 wherein the primary current source generates a current I and each of said one or more current sources generates a second current lower than the current I, further comprising a transistor coupled to each current source connected to the counter.

27. The circuit of claim 21 further comprising a transistor coupled to each current source and to the counter.

28. The circuit of claim 21 wherein the oscillator further comprises:

a primary voltage source coupled to the control input; and

a differential switch coupled to the primary voltage source.

29. The circuit of claim 21 wherein the means for varying the frequency further comprises:

a capacitor; and

a current source adapted to charge and discharge the capacitor.

30. The circuit of claim 29 further comprising:

one or more comparators coupled to the capacitor; and

means coupled to the capacitor for alternatingly charging and discharging the capacitor.

31. A power supply having a transformer coupled to an input voltage, the transformer having a primary winding, the power supply comprising:

an oscillator for generating a signal having a frequency, the oscillator having a control input for varying the frequency of the signal, the oscillator including:

a primary current source coupled to the control input;

a differential switch coupled to the primary current source;

a capacitor coupled to the differential switch; and

a comparator coupled to the differential switch;

a digital to analog converter coupled to the control input, the digital to analog converter having one or more current sources, wherein the primary current source generates a current I and each of said one or more current sources generates a current lower that I;

a counter coupled to the output of the oscillator and to the current sources of the digital to analog converter; and

a power transistor coupled to the oscillator and to one terminal of the primary winding, the power transistor modulating its output in providing a regulated power supply output.

32. A power supply having a transformer coupled to an input voltage, the transformer having a primary winding, the power supply comprising:

an oscillator for generating a signal having a frequency, the oscillator having a control input for varying the frequency of the signal, the oscillator including:

a primary current source coupled to the control input;

a differential switch coupled to the primary current source;

a capacitor coupled to the differential switch; and

a comparator coupled to the differential switch

a circuit for varying the frequency, the circuit coupled to the control input, including:

a capacitor;

a current source adapted to charge and discharge the capacitor;

one or more comparators coupled to the capacitor and coupled to the current source for alternatingly charging and discharging the capacitor; and

a power transistor coupled to the oscillator and to one terminal of the primary winding, the power transistor modulating its output in providing a regulated power supply output.

* * * * *

UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO. : 6,249,876 B1
DATED : June 19, 2001
INVENTOR(S) : Balakrishnan et al.

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Column 10,
Line 2, please insert -- current -- after "primary".
Line 3, please delete "wherein the oscillator further" and insert -- wherein the differential switch further --.

Signed and Sealed this

Nineteenth Day of February, 2002

Attest:

Attesting Officer

JAMES E. ROGAN
Director of the United States Patent and Trademark Office

EXHIBIT 3
(Claims Construction Order dated March 31, 2006, *Power Integrations v. Fairchild Semiconductor, Inc.*, U.S. District Court - Delaware - Case No. 04-1371 JJF)

IN THE UNITED STATES DISTRICT COURT

FOR THE DISTRICT OF DELAWARE

POWER INTEGRATIONS, INC., a Delaware corporation,	:	
Plaintiff,	:	
v.	:	C.A. No. 04-1371-JJF
FAIRCHILD SEMICONDUCTOR INTERNATIONAL, INC., a Delaware corporation, and FAIRCHILD SEMICONDUCTOR CORPORATION, a Delaware corporation,	:	
Defendants.	:	

O R D E R

At Wilmington, this 31 day of March 2006, for the reasons discussed in the Memorandum Opinion issued this date;

IT IS HEREBY ORDERED that the following terms and/or phrases in U.S. Patent Nos. 4,811,075 (the "'075 patent"), 6,107,851 (the "'851 patent"), 6,229,366 (the "'366 patent"), 6,249,876 (the "'876 patent") are assigned the following meanings:

1. The term **"MOS transistor"** means "a metal oxide transistor."

2. The term **"substrate"** means "the physical material on which a transistor or microcircuit is fabricated."

3. The phrase **"a pair of laterally spaced pockets of semiconductor material of a second conductivity type within the substrate"** means "two laterally spaced pockets of semiconductor material of the opposite conductivity type from the substrate."

4. The phrase **"a surface adjoining layer of material of the first conductivity type on top of an intermediate portion of the extended drain region between the drain contact pocket and the surface adjoining positions"** is construed according to its plain meaning, and further construction by the Court is not required.

5. The phrase **"said top layer of material"** is construed according to its plain meaning when read in the context of the claim, and further construction by the Court is not required.

6. The term **"reverse bias voltage"** means "a voltage applied across a rectifying junction with a polarity that provides a high-resistance path."

7. The phrase **"substrate region thereunder which forms a channel"** is construed according to its plain meaning when read in the context of the claim, and further construction by the Court is not required.

8. The term **"frequency jittering"** means "varying the switching frequency of a switch mode power supply about a target frequency in order to reduce electromagnetic interference."

9. The term **"coupled"** means that "two circuits are coupled when they are connected such that voltage, current or control signals pass from one to another."

10. The term **"primary voltage"** means a "base or initial voltage" and the term is not defined by reference to the

source from which it may be generated.

11. The term **"secondary voltage"** means "a subsequent or additional voltage."

12. The term **"combining"** means "adding together."

13. The term **"supplemental voltage"** means "a voltage in addition to the primary voltage."

14. The term **"soft start circuit"** is a means-plus-function element. The functions of the various "soft start circuits" are construed in accordance with the plain meaning of the claims setting forth such soft start circuit functions. The corresponding structures related to the "soft start circuit" are shown in Figures 3, 6 and 9 of the '366 patent and described in the specification of the '366 patent at col. 6, ll. 7-17; col. 6, l. 35-col. 7, l. 18; col. 11, ll. 40-50 and col. 12, ll. 5-10.

15. The phrase **"frequency variation circuit"** means "a structure that provides the frequency variation signal."

16. The phrase **"frequency variation signal"** means "an internal signal that cyclically varies in magnitude during a fixed period of time and is used to modulate the frequency of the oscillation signal within a predetermined frequency range."

UNITED STATES DISTRICT JUDGE

EXHIBIT 4
(Declaration of Robert Blauschild dated January 25, 2008 and accompanying exhibits)

REDACTED

EXHIBIT 5
(Excerpts from Deposition of Robert Blauschild dated March 24, 2008, marked Highly Confidential)

REDACTED

EXHIBIT 6
(AP3700 Schematics BCDS000001-18)

REDACTED

EXHIBIT 7
(Self-Communicated Thyristor DC-to-DC Converter)

If the need for high reliability, efficiency, and economy is added, the choice of circuits and components becomes critical. For the square-wave inverter a frequency above the audio range was selected, which permitted the use of low-cost power ferrites without making unduly demands on the rise time of the power transistors or reducing the efficiency. Generation of acoustic noise is prevented—an additional benefit.

For current regulation a chopper-type transistor regulator is pulsewidth controlled by a small magnetic amplifier excited from an auxiliary driver. Though many transistor circuits are available for this purpose, a magnetic amplifier was preferred because of the simple method of current feedback, level setting, and inherent reliability. Since its speed of response is fast enough to eliminate most of the ripple still passing through the power-line filter, the latter could be designed simply as an RC network.

Performance Data

The overall efficiency is about the same as with a standard ballast, i.e., 75 percent; this is displayed in Table I. The same is true with the heat rise when assembled in the same size package, i.e., 45°C. The intensity ripple has been reduced from 50 percent (Fig. 1) to 0.4 percent and consists essentially of power-supply ripple passed through the filtering process; the inverter frequency which has a rise time of 2 μs is not noticeable, due to the relatively slow decay time of the phosphorescence coating.

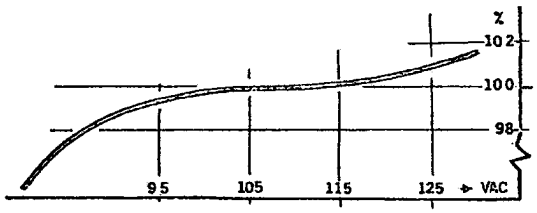


Fig. 3. Relative lamp intensity.

TABLE I

Power input	175 W
Power output	132 W
4 filaments	12 W
Losses	
Rectangular filter	15 W
Regulator	8 W
Square generator	20 W

The relative intensity as a function of line voltage variations is plotted in Fig. 3 and changes less than 1 percent for a 10-percent line voltage deviation around 115 volts nominal. Since the intensity variation reflects changes in lamp current it could be improved by using a photosensitive element in lieu of the current feedback.

Self-Commutated Thyristor DC-to-DC Converter

PATRICK W. CLARKE

Abstract—This paper describes an analysis of a thyristor dc-to-dc converter employing self-commutating circuitry. Energy is transferred between the input and output terminals by means of resonant networks.

Circuit techniques are described which reduce the acoustical noise and minimize the RF voltage spikes at the output terminal.

Introduction

SELF-COMMUTATED dc-to-dc converters usually employ *LC* resonant networks to provide thyristor commutation. The series capacitor commutated inverter is an example of this type of commutation system. See Fig. 1. The term "series capacitor" is used to indicate a circuit that is commutated by a capacitor in series with the load. A description of the circuit operation and other circuit variations may be found in [1]–[3]. In order to extend the load range and reduce the electrical stress on the thyristor devices of this type of circuit, it is necessary to circulate a minimum amount of energy in the system at all times. The circuit shown in Fig. 2 was developed to circumvent these difficulties. By decoupling the load from the commutating circuit the commutation of thyristors is made independent of the load.

An important feature of the converter design described in this paper is that the electrical stresses on the semiconductor devices are well defined, and are functions of passive components. These stresses can be calculated under all modes of operation. In particular the rates of rise of forward current and voltage, through and across the thyristor devices, respectively, are minimized. This is an important result, since most failures of thyristor devices in thyristor converters result from excessive rates of rise of forward current and voltages. These failures are commonly referred to as di/dt burnout or false triggering due to dv/dt.

This paper is divided into the following sections: 1) circuit description, a brief description of the circuit operation; 2) circuit analysis, in which expressions are developed to describe the peak current through the thyristor devices and establish component values; 3) noise, in which a means of reducing the acoustical annoyance of the con-

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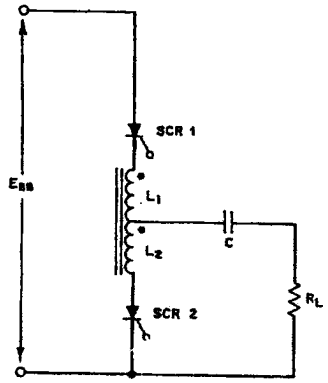

Fig. 1. Series capacitor commutated inverter.

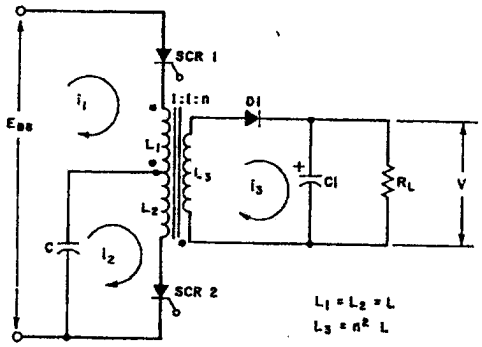

Fig. 2. Self-commutated dc-to-dc converter.

verter is described. In addition, a method of operation is employed which reduces the RF spikes normally appearing at the output of dc-to-dc converters.

Circuit Operation

When *SCR*1 is triggered on, with *SCR*2 off, a series resonant circuit is connected to the dc supply. The voltage across windings L_2 and L_3 will initially back bias *SCR*2 and *D*1, respectively. The capacitor voltage sinusoidally charges up towards $2E_{BB}$ minus the initial voltage on the capacitor. The voltage across the inductor winding L_1 is the difference between the input voltage E_{BB} and the capacitor voltage. As the capacitor charges up to a value greater than the input voltage, the voltage across L_1 reverses polarity. At some time after *SCR*1 is triggered on and the magnitude of the voltage on the capacitor is larger than E_{BB}, the voltage across winding L_3 is of sufficient magnitude to forward bias *D*1. When *D*1 conducts, the voltage of the windings will be clamped to the output voltage V, assuming that $L_1 = L_2 = L$, $L_3 = n^2L$, $C_1 \gg C$, and neglecting the effects of leakage reactances.

The current through *SCR*1 will decrease to zero, since any further current flow through *SCR*1 will continue to charge capacitor C and increase the reverse bias appearing across *SCR*1. *SCR*1 commutates off. The energy that has been stored in L_1 is now discharged to the load through *D*1. As was noted before, the voltage across L_1, L_2, and L_3 windings is constant and equal to V. The voltage across

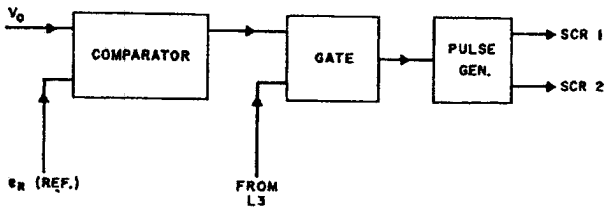

Fig. 3. Control system.

these windings is assumed constant, since it is possible to increase the value of C_1 arbitrarily until this condition is met to any precision desired. The current through *D*1 will be a ramp of current with a negative slope. This current is allowed to relax to zero before *SCR*2 is triggered on.

*SCR*2 is triggered to repeat the cycle and reverse the voltage across C. Energy is stored in L_2, *SCR*2 commutates off, and a ramp of current is discharged through *D*1. The voltage across C is now at its initial value. After the current through *D*1 has relaxed to zero, *SCR*1 can now be retriggered. The output voltage V can be regulated by controlling the triggering of the thyristors. A block diagram of the control system is shown in Fig. 3.

The output voltage V is compared to a reference voltage e_R by means of a comparator circuit. Whenever the output voltage is above a threshold level established by the reference, the comparator output biases the gate circuit in a manner to inhibit the free-running pulse generator. In addition, a signal is derived from the voltage appearing across L_3, such that at any time *D*1 is conducting, the gate circuit is biased to inhibit the blocking oscillator. The maximum frequency of the free-running pulse generator is equal to the maximum frequency of operation of the system. When the system is operating in a voltage-regulated mode, the system frequency is less than maximum. Thus the average output V is regulated at a value proportional to e_R.

Circuit Analysis

The current and voltage waveforms of the circuit shown in Fig. 2 are shown in Fig. 4.

At time $t = 0$, *SCR*1 is triggered on, *SCR*2 and *D*1 are biased off.

$$i_1 = [(E_{BB} - V_c)/Z_0] \sin \omega_0 t, \quad 0 \le t \le t_1$$

where V_c is the initial voltage on the capacitor, and Z_0 is the loop impedance.

$$Z_0 = (L/C)^{1/2}$$

$$\omega_0 = 1/(LC)^{1/2}.$$

The voltage across the capacitor C is

$$v_c = (1/C)\int i_1 \, dt, \quad 0 \le t \le t_1.$$

Then,

$$v_c = E_{BB} - (E_{BB} - V_c) \cos \omega_0 t, \quad 0 \le t \le t_1.$$

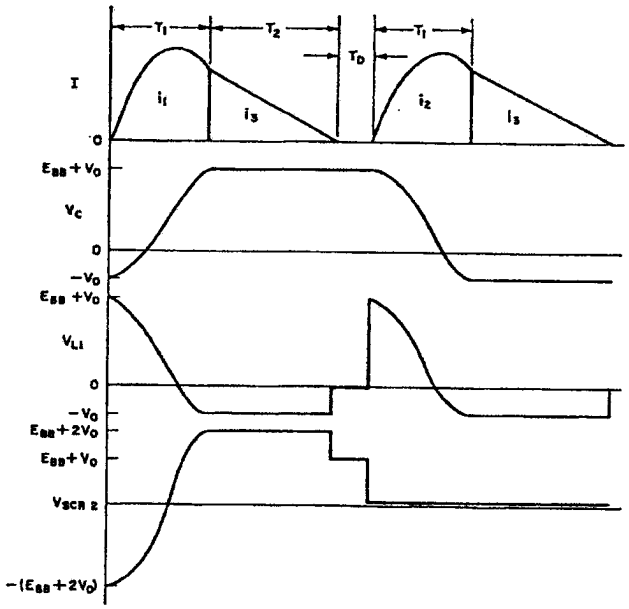

Fig. 4. Circuit waveforms.

The voltage across the primary winding of inductor is

$$v_L = E_{BB} - v_c$$

then

$$v_L = (E_{BB} - V_c)\cos\omega_0 t, \quad 0 \le t \le t_1.$$

The voltage across the secondary winding of the inductor is

$$v_L' = n(E_{BB} - V_c)\cos\omega_0 t, \quad 0 \le t \le t_1.$$

At $t = t_1$, v_L' will be equal to $-V$ (neglecting the voltage drop of $D1$).

Therefore

$$-V/n = (E_{BB} - V_c)\cos\omega_0 t_1$$

$$v_c\,|_{t=t_1} = E_{BB} + V/n$$

$$i_1\,|_{t=t_1+} = 0$$

since $SCR1$ has commutated at t_1.

The energy stored in the magnetic field will discharge through $D1$ to charge capacitor C_1.

$$V = n^2 L(di_3/dt), \quad t_1 \le t \le t_2$$

$$di_3/dt = V/n^2 L, \quad t_1 \le t \le t_2.$$

i_3 will have the shape of a linear ramp with a constant negative slope decaying to zero at the end of the cycle. The maximum value of i_3 can be found by considering the following. The energy stored in the commutating inductor must be a continuous function of time; the energy stored in the inductor just prior to the commutation of $SCR1$ is

$$\mathcal{E}_1 = \tfrac{1}{2}Li_1^2(t_1-).$$

The energy stored in the inductor just after $SCR1$ is commutated is

$$\mathcal{E}_2 = \tfrac{1}{2}n^2 Li_3^2(t_1+)$$

$$\mathcal{E}_1 = \mathcal{E}_2$$

therefore

$$i_3(t_1+) = i_2(t_1-)/n$$

$$di_3 = \Delta i_3 = i_3(t_1+)$$

$$= [(E_{BB} - V_c)/n](C/L)^{1/2}\sin\omega_0 t_1$$

$$dt = \Delta t = t_2.$$

Then

$$t_2 = [n(E_{BB} - V_c)\sin\omega_0 t_1]/\omega_0 V.$$

Sometime after i_3 has decayed to zero, $SCR2$ is triggered on:

$$i_2 = (E_{BB} + V/n)(C/L)^{1/2}\sin\omega_0 t,$$

$$t_1 + t_2 + t_D \le t \le 2t_1 + t_2 + t_D$$

where t_D is the delay between cycles, which is varied between zero and infinity by the control circuit.

$$T_s = t_1 + t_2 + t_D$$

where T_s is one-half the switching period.

Under steady-state conditions the average current through capacitor C is zero, and

$$i_{1av} = i_{2av}$$

$$\frac{(E_{BB} - V_c)}{2T_s}\int_0^{t_1}\sin\omega_0 t\,dt$$

$$= \frac{(E_{BB} + V/n)}{2T_s}\int_{T_s}^{t_1+T_s}\sin\omega_0(t - T_s)\,dt$$

$$V_c = -V/n.$$

Thus

$$\cos\omega_0 t_1 = \frac{-V/n}{E_{BB} + V/n}.$$

I_ϕ is defined as the maximum average output current at a specified output voltage V_ϕ, and input voltage E_{BB}. Let

$$V = V_\phi$$

$$\alpha = V_\phi/nE_{BB}.$$

Then

$$\cos\omega_0 t_1 = -\alpha/(1+\alpha)$$

$$\sin\omega_0 t_1 = (1+2\alpha)^{1/2}/(1+\alpha)$$

$$t_1 = (1/\omega_0)\cos^{-1}[-\alpha/(1+\alpha)]$$

$$t_2 = (1+2\alpha)^{1/2}/\omega_0\alpha$$

$$i_{3av} = \tfrac{1}{2}i_3(t_1+)(t_2/T_s).$$

The average output current will be a maximum when t_D is zero:

$$T_{s\,\min} = t_1 + t_2$$

$$I_\phi = \frac{1}{2}\times\frac{I_{pk}}{n}\times\frac{(1+2\alpha)^{1/2}}{1+\alpha}\frac{t_2}{T_{s\,\min}}$$

where I_{pk} is the peak value of the current through the

thyristors. The peak currents through the thyristors are the same, because the loop impedances and excitations are the same.

$$I_{pk} = (E_{BB} + V_\phi/n)(C/L)^{1/2}$$

$$\frac{T_{s\,min}}{t_2} = \frac{t_1}{t_2} + 1$$

$$\frac{T_{s\,min}}{t_2} = \frac{\alpha \cos^{-1}[-\alpha/(1+\alpha)] + (1+2\alpha)^{1/2}}{(1+2\alpha)^{1/2}}.$$

I_{pk} can now be specified in terms of I_ϕ and α; this is an important result, since I_ϕ, E_{BB}, and V_ϕ are given quantities, and n can be assigned a value. The circuit designer needs to know the peak current through the thyristors in order to select the thyristor he intends to use and determine the frequency of operation.

$$I_{pk} = \frac{2nI_\phi(1+\alpha)\{\alpha \cos^{-1}[-\alpha/(1+\alpha)] + (1+2\alpha)^{1/2}\}}{1+2\alpha}.$$

We can now solve for L and C:

$$C = \frac{I_{pk}t_1}{E_{BB}(1+\alpha)\cos^{-1}[-\alpha/(1+\alpha)]}$$

$$L = \frac{E_{BB}(1+\alpha)t_1}{I_{pk}\cos^{-1}[-\alpha/(1+\alpha)]}.$$

The maximum rate of rise of current through a thyristor is

$$di_{1,2}/dt\,|_{max} = \omega_0 I_{pk}$$

$$di_{1,2}/dt\,|_{max} = \frac{2nI_\phi(1+\alpha)\cos^{-1}[-\alpha/(1+\alpha)] \cdot \{\alpha \cos^{-1}[-\alpha/(1+\alpha)] + (1+2\alpha)^{1/2}\}}{t_1(1+2\alpha)}.$$

The maximum rate of rise of forward voltage across a thyristor is

$$\frac{dV_{1,2}}{dt} = \frac{E_{BB}(1+\alpha)\cos^{-1}[-\alpha/(1+\alpha)]'}{t_1}.$$

The minimum turn-off time provided by the circuit per thyristor is

$$t_{off} = \pi/2\omega_0 + t_2$$

$$t_{off} = \frac{t_1}{\cos^{-1}[-\alpha/(1+\alpha)]}\left[\frac{\pi}{2} + \frac{(1+2\alpha)^{1/2}}{\alpha}\right].$$

In order to simplify the design procedures, we can arbitrarily set t_1 equal to t_2. This condition applies for values of t_D greater than zero. When t_D is zero the system is operating in its current limit mode, and t_2 varies inversely proportional to V. When t_D is greater than zero, the control circuit is regulating the output to a constant value V_ϕ; the values of t_1 and t_2 are fixed and equal. For t_1 equal to t_2,

$$\frac{2\alpha \cos^{-1}[-\alpha/(1+\alpha)]}{(1+2\alpha)^{1/2}} = 1$$

thus

$$\alpha \simeq 0.8$$

$$\cos^{-1}[-\alpha/(1+\alpha)] \simeq 2.03$$

$$n \cong 1.25V_\phi/E_{BB}.$$

Then

$$I_{pk} = 5.58I_\phi V_\phi/E_{BB}$$

$$C = (t_1 I_{pk}/3.65E_{BB})\ \mu F$$

$$L = (t_1 E_{BB}/1.13I_{pk})\ \mu H$$

$$di_{1,2}/dt\,|_{max} = (2.03I_{pk}/t_1)\ A/\mu s$$

$$dV_{1,2}/dt\,|_{max} = (3.65E_{BB}/t_1)\ V/\mu s$$

$$t_{off} = 1.77t_1\ \mu s$$

where I_ϕ is given in amperes, E_{BB} in volts, and t_1 in microseconds. As noted above E_{BB}, V_ϕ, and I_ϕ are specified. t_1 is determined by the circuit designer by consulting the specifications for the thyristor device he intends to use. Once t_1 is determined, all of the above parameters can be calculated.

Efficiency

The above analysis was made on a lossless system. No attempt will be made here to develop an analysis for a system including losses. Most of the losses of the system will occur in the semiconductors, since the inductors and capacitors can be specified as high-Q components. It is convenient to modify the voltage values in the above equations to account for the major proportion of the losses in the following manner. Let

$$E_{BB} = E_{BB}' - 2V_{SCR}$$

$$V_\phi = V_\phi' + V_{diode}$$

where E_{BB}' and V_ϕ' are the given input and output voltages. V_{SCR} is the average forward conducting voltage drop across a thyristor, and V_{diode} is the average forward conducting voltage drop across the output diode. In practice, values of 1.5 volts for V_{SCR} and 1.0 volts for the diode have given useful results.

Voltage Regulation Characteristics

It can be shown that

$$V_\phi = nE_{BB}\left\{\frac{R_L C}{2T_s n^2} + \frac{1}{2}\left[\left(\frac{R_L C}{T_s n^2}\right)^2 + \frac{2R_L C}{T_s n^2}\right]^{1/2}\right\}$$

for

$$V_\phi/I_\phi \leq R_L \leq \infty.$$

In order to maintain the output voltage constant, the control circuit adjusts T_s such that the ratio R_L/T_s remains constant for a fixed value of E_{BB}.

Current Limit Operation

When $R_L \leq V_\phi/I_\phi$, the output voltage V will decrease below the regulated value. This is due to the fact that the control system monitors the energy in the commutating

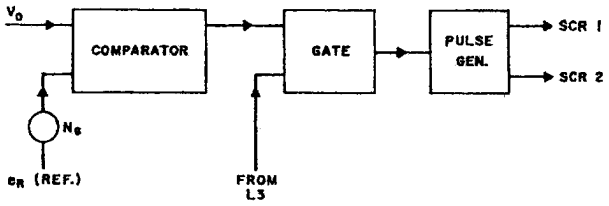

Fig. 5. Control system with random noise source.

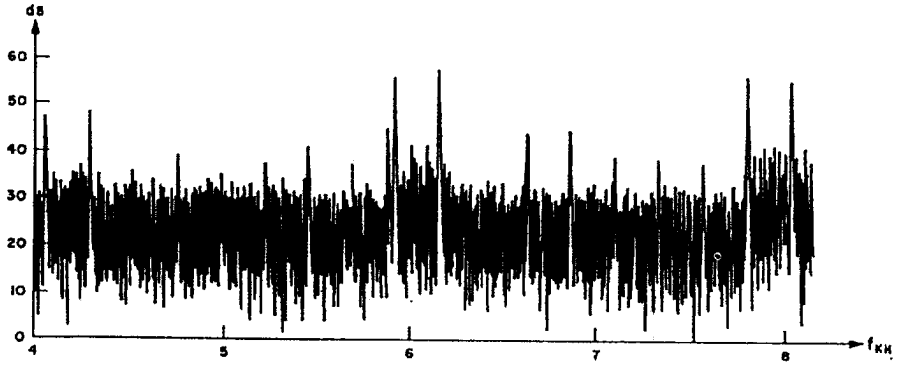

Fig. 6. Partial spectrum with random noise source in the control system.

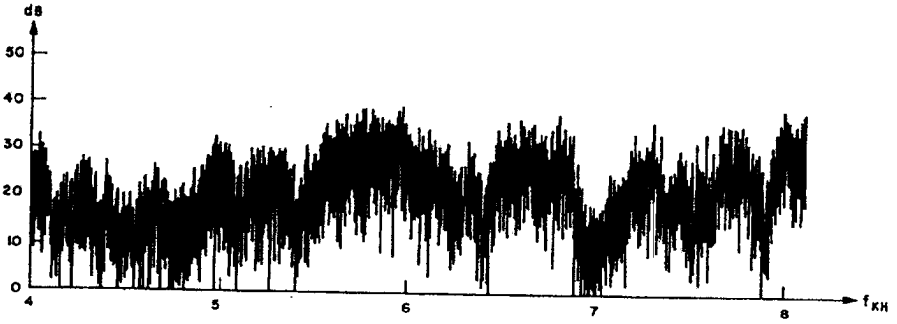

Fig. 7. Partial spectrum with random noise source shorted out.

inductor, and inhibits the pulse generator until the energy stored in the magnetic field of the commutating inductor is zero. t_2 will increase because the period required to discharge this energy becomes longer as the output voltage decreases; therefore the switching period T_s becomes longer. The system is now operating in the current limit mode, and the average output current is

$$i_{3av} = \tfrac{1}{2}(C/L)^{1/2} \cdot \left[\frac{nE_{BB} + 2V}{\frac{V}{nE_{BB}} \cos^{-1}\left[\frac{-V}{nE_{BB} + V}\right] + \left(1 + \frac{2V}{nE_{BB}}\right)^{1/2}} \right]$$

for

$$0 \leq R_L \leq V_\phi / I_\phi.$$

The short circuit current is

$$i_{3sc} = (nE_{BB}/2)(C/L)^{1/2}|_{V=0}.$$

It should be noted that when the system is operating into a short circuit, the stresses on the thyristors are less, the I_{pk}, dV/dt, di/dt are lower, and the turn-off time is longer than full load conditions of I_ϕ. The average current through the diode $D1$ will increase. The ratio of the short circuit to the maximum current at V_ϕ for a fixed value of E_{BB} is

$$i_{3sc}/(i_{3av}|_{V=V_\phi}) = 1.23.$$

Since the current in the inductor prior to the turn-on of a thyristor is zero, high rates of current rise di/dt through the thyristors are avoided.

Noise

Acoustical Noise

In order for the converter system to regulate over a load range from zero to full load, the switching frequency will

range from a very low value to the maximum design frequency f_0:

$$f_0 = 1/2(t_1 + t_2), \quad V = V_\phi.$$

As a result, the converter will be operated in the audible range for at least some load conditions. This condition could limit the usefulness of this style converter in some sensitive areas. Up to the present time the alternatives available to the circuit design were unpleasant. He had to use bulky enclosures, operate coils at reduced flux densities, etc., or operate above the audible spectrum. In general, each of these alternatives increased the cost of the system. The technique to be described, while it does not eliminate the acoustical noise entirely, reduces the magnitude of the problem.

A source of random noise is connected in series with the reference voltage e_R as shown in Fig. 5. The long-term average voltage of this source is zero; therefore, the long-term average output voltage V_ϕ will not differ if the source is shorted out. The effect of putting this noise source in series with the reference is to cause the value t_D to be randomly distributed about some center value. Therefore, at loads less than full load the converter will emit a hissing sound. This sound has a quality similar to air escaping from a radiator or an air hose. The quality of this sound remains constant over nearly the full load range. At extremely light loads the sound reduces to ticking sounds when the switching period becomes very long.

Fig. 6 shows an audio spectrum for a 200-watt converter with the noise source in the system. Fig. 7 shows the spectrum with the source shorted out. The main differences between the two spectrums are 1) in the case when the noise source is in the ambient, noise is shifted slightly upwards, 2) with the noise source shorted out, there are large spikes at the characteristic frequency of operation and its harmonics. It was observed that when an enclosure was placed around the converter, the noise was attenuated. When the system was operated with the noise source shorted, the tone penetrated the enclosure with hardly any noticeable attenuation. This effect is to be expected, since the acoustical energy is randomly distributed over a range of frequencies. The sound is no longer periodic and the reinforcing effect of standing waves is not present.

RF Noise

In most dc-to-dc converters the source of RF noise appearing at the output terminals of the converter is due to the commutation of diodes. A reverse bias voltage is abruptly switched across the diode while it is carrying current. This results in a spike of current flowing in the inverse direction through the diode. This current will continue to flow to reduce the stored charge at the junction of the diode to zero. The device impedance will now monotonically increase. Due to the inductances in the system, wire, etc., the inverse current continues to flow for a period of time and produces a voltage spike across the diode. This spike usually has frequency components in the RF region and is conducted to the terminals of the converter.

The current through diode $D1$ of this converter is relaxed to zero before a reverse bias is switched across it. As a result, the magnitude of the stored charge at the junction of the device is less at the time the reverse bias is switched across the device. The recovery time of the diode will be shorter and the resulting voltage spike will be smaller and easier to attenuate.

Conclusions

The circuit shown in Fig. 2 has been described and analyzed, and a series of design equations have been developed. The following features and results have been demonstrated.

1) The rate of reapplied forward voltage dv/dt, and the rate of current rise during the turn-on di/dt, for the thyristor devices are a function of L and C only and are independent of the load.

2) The minimum turn-off time is independent of the load.

3) The RF energy developed across the diode $D1$ can be minimized.

4) The load impedance R_L can be varied from zero to infinity.

5) High di/dt in the thyristors is avoided by permitting the current in the commutating inductor L to relax to zero before triggering the thyristors.

6) The feature outlined in 5) above also results in the system being short-circuit stable.

7) Single-frequency tones have been eliminated from the acoustical spectrum of the converter. This was accomplished by inserting a random noise source in series with the system's reference voltage. The audible sound emitted by the converter is considerably altered by this procedure and results in a converter which produces less acoustical annoyance.

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EXHIBIT 8
(Acoustic Noise Reduction in Sinusoidal PWM Drives Using a Randomly Modulated Carrier)

Acoustic Noise Reduction in Sinusoidal PWM Drives Using a Randomly Modulated Carrier

Thomas G. Habetler, *Member, IEEE*, and Deepakraj M. Divan, *Member, IEEE*

***Abstract*—Acoustic noise in an inverter-driven electric machine can be reduced by avoiding the concentration of harmonic energy in distinct tones. One method to spread out the harmonic spectrum without the use of programmed PWM is to cause the switching pattern to be random. It is proposed that the switching pattern can be randomized by modulating the triangle carrier in sinusoidal PWM with band-limited white noise. All the advantages of sinusoidal PWM are preserved with this technique. These include, real-time control, linear operation, good transient response and a constant average switching frequency. By controlling the bandwidth and rms value of the bandwidth limited noise modulation, it is shown that the instantaneous variation in switching frequency as well as the bandwidth of the energy spectrum in the machine can be specified within predetermined limits. Experimental results show the absence of acoustic noise concentrated at specific tones which is present with conventional sinusoidal modulation.**

I. Introduction

MODERN three phase motor drives in the medium to high power range typically switch at frequencies in the audio range. That is, above the fundamental frequency of the output voltage (6-step mode) and below 2 to 3 kHz. Acoustic noise in an electric machine is for the most part proportional to the square of the air gap flux density. The majority of the noise is then generated by harmonic flux waves interacting with the fundamental flux wave. The maximum noise, certainly from a psychological standpoint, is generated when the harmonic flux produced is concentrated at a particular frequency such as the switching frequency. It is desirable then to spread out the frequency spectrum of the harmonic voltage, and therefore current, in such a way as to eliminate the presence of specific tones.

A typical six-pulse bridge inverter feeding an induction machine is illustrated in Fig. 1. Certain types of switching regulators, such as the hysteresis current regulator [1], accomplish this spreading of the voltage spectrum inadvertently. The hysteresis regulator has a varying switching frequency which results in a voltage spectrum that does not have a large component at a particular frequency. However, the switching pattern, in the steady-state, is still

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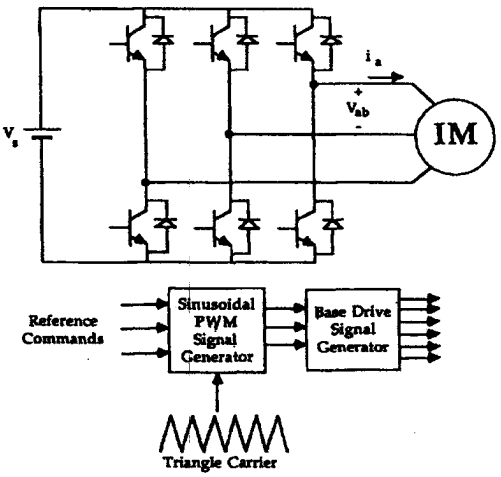

Fig. 1. Schematic for sinusoidal PWM voltage-sourced inverter feeding an induction motor load.

periodic since the switching instances are directly related to the current error. Therefore, the amount of acoustic noise generated depends on the nature of the load. The hysteresis regulator also has the problem of a widely varying switching frequency and low frequency beating is observed under light load conditions.

Alternative methods for acoustic noise reduction have been implemented through the use of harmonic control in programmed PWM schemes [2], [3]. In programmed PWM the switching frequency is maintained constant. The individual tones produced by the switching process are kept low by control of the switching angles. The problem with this approach is that discrete tones in the voltage spectrum still exist since the switching function is periodic. Also, programmed PWM schemes require many waveforms to be stored in memory for varying values of output fundamental magnitude. More critically, since programmed PWM stores the switching angles for a complete cycle of the output voltage it is only useful for acoustic noise reduction when the drive is operating in the steady state. The basic concept of programmed PWM only applies to steady state periodic waveforms. Programmed PWM is not applicable to current regulated drives which are quite often operating in the transient state. Pro-

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grammed PWM results in a slow transient response and somewhat nonlinear relationship of the output voltage with respect to the reference.

II. Modulated Carrier Sinusoidal PWM

An improved PWM scheme with acoustic noise reduction then must have a spectrum without energy concentrated at discrete frequencies and still not have a widely varying switching frequency. Real time control and a linear transfer function are also requisite features. In addition, the spectral energy fed into the motor load should be limited to a defined range. In that way, current in the machine at frequencies significantly below the switching frequency can be avoided. The reduction of machine-generated acoustic noise has been demonstrated with the regularly sampled sigma-delta modulator [4]. The acoustic noise reduction is attributed to the fact that the energy spectrum for this type of controller is spread out. The spectrum is spread in the sigma-delta modulator because the combination of the quantizer and the regular sampling generates a random switching pattern. The switching pattern is random since the error polarity, which is the output of the quantizer, and the sampling instant are not correlated. The concept of randomizing repetitive phenomena to reduce acoustic noise has been widely used for applications in other disciplines. An example is the random spacing or orientation of fan or propeller blades. Placement of gear teeth is also randomized to reduce noise. The same concept of randomizing a repetitive precess can be applied to PWM drives. The limitation of this type of modulation is the fact that the switching instants are discrete. Therefore, higher switching frequencies are required to achieve performance equivalent to PWM.

Reference [6] introduces another method for spreading the inverter output voltage spectrum to reduce acoustic noise. In this approach a random switching function is intentionally created to reduce acoustic noise. With this technique the average value of the regulator reference voltage, over a particular interval, T_n, is found using a triangle comparison. This average is denoted as V^*_{avg}. The T_n interval is divided up into r subintervals. For each of these subintervals, a uniformly distributed random number with expected value V^*_{avg} is generated. The inverter is switched high (or low) at each of the subintervals, depending on whether or not the value of the random number is above (or below) V^*_{avg}. This causes the energy spectrum of the unwanted components of output voltage to be almost flat. This scheme also has the advantage of real-time control. However, the requisite switching frequency for satisfactory performance is even higher than that necessary in discrete pulse switching. In [6], for a 60-Hz fundamental frequency of the output voltage, the switching frequency is 320 kHz.

Sinusoidal PWM has the desired feature of being a real-time linear amplifier with a constant switching frequency. The switching pattern for sinusoidal PWM is illustrated in Fig. 2. The pole (phase) switching function results from

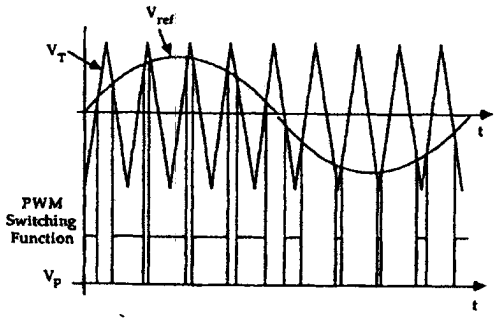


Fig. 2. Waveforms illustrating triangle carrier, reference wave and resulting pole switching function for conventional sinusoidal PWM.

the comparison of a voltage reference wave with a triangular carrier. The resulting output ac load voltage spectrum does, however, have a large component at the switching frequency which results in a tone that is radiated acoustically by the machine. The switching frequency, of course, is the frequency of the carrier or triangle wave, denoted ω_c. The spectrum of the resulting PWM voltage, V_p, is related to the carrier wave, V_T. For example, consider the case of zero modulation. Here V_p is a square wave which results from comparing V_c with zero, and is simply the derivative of the triangle carrier. It is proposed that modulating the carrier frequency in an appropriate manner will spread the energy that would otherwise exist in a tone at ω_c.

To maintain the linearity of the amplifier, it is necessary for the carrier wave to still have straight line segments, i.e., it must remain triangular. As in unmodulated sine-triangle PWM, it is assumed that the instantaneous carrier frequency is always much larger than the frequency of the reference, f_n. Then the duty cycle generated by the PWM comparison is maintained proportional to the value of the reference over one period of the carrier. However, if the slope of subsequent segments are varied, linearity is maintained. Let the instantaneous value of the carrier frequency, i.e., the frequency of a single straight line segment between time t_k and t_{k+1}, be given by

$$f_i = \frac{1}{T_i} = \frac{1}{t_{k+1} - t_k} = \frac{1}{T_c + T_n} \tag{1}$$

and

$$T_n = V_{max} n(t_k) \tag{2}$$

where T_n is the change in the period of any given segment due to the modulation, $n(\cdot)$ is the modulating function, and T_c is the average period of the carrier. This type of modulation is often referred to as frequency shift keying (FSK). Fig. 3 illustrates the carrier waveform.

It is clear that by restricting the magnitude of $n(t)$ in this scheme the switching frequency can be maintained within a predetermined range. It is also very important to constrain the spectrum of the output voltage, V_p, so that

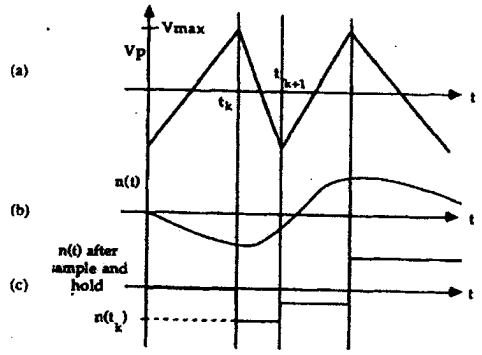


Fig. 3. Waveforms illustrating: (a) Triangle carrier with FSK-type modulation. (b) Modulating function. (c) Modulation function after sample and hole which defines slope of triangle.

substantial low frequency content does not exist. One approach would be to sinusoidally modulate the triangle wave around ω_c. If the magnitude of $n(t)$ is sufficiently small it can be surmised from frequency modulation theory that the bandwidth of the output voltage can be controlled. However, because of the low regular manner in which f_i changes, the tone is still detected. The acoustic noise produced by the machine sounds like a fast-changing tone.

III. Random Modulation

A better approach to sinusoidal modulation is a random modulation of the slope of the carrier waveform. Let the modulating function, $n(t)$, be a random function, say, Gaussian "white" (i.e., wideband) noise. Modulating with very high bandwidth noise results in a large instantaneous change in the triangle frequency. This eliminates the concentration of energy in a tone. It also results in a very wide spectrum for the output voltage, including substantial content at low frequencies which will cause low frequency currents to flow in the machine.

Since the fundamental component of the triangle wave is the primary source of acoustic noise, the higher frequency harmonics can be neglected. Let V_c be the output voltage without the modulated carrier. Then, ignoring components other than a single tone,

$$V_c(t) = A \cos \omega_c t. \tag{3}$$

If the modulating function has a narrow bandwidth, the spectral content of V_p, the output voltage, can be constrained within a specified range of frequencies. For the sake of analysis then, assume that the modulation is continuous. Therefore,

$$V_p(t) = A \cos [\omega_c t + \mu(t)] \tag{4}$$

where $\mu(t)$ is the change in instantaneous angle due to modulation. The autocorrelation function is

$$\begin{aligned} R(t) &= E\{V_p(t)\, V_p(t+\tau)\} \\ &= E\left\{\frac{A^2}{2} \cos [\omega_c t + \omega_c \tau + \mu(t+\tau) + \mu(\tau)]\right\} \\ &\quad + E\left\{\frac{A^2}{2} \cos [2\omega_c t + \omega_c \tau + \mu(t+\tau) + \mu(\tau)]\right\}. \end{aligned} \tag{5}$$

$E\{\bullet\}$ denotes the expected value operator. Since the noise has zero mean,

$$\begin{aligned} R(t) &= \frac{A^2}{2} E\{\cos [\mu(t+\tau) - \mu(t)]\} \cos \omega_c t \\ &= \frac{A^2}{2} \exp [R_\mu(t) - R_\mu(0)] \cos \omega_c t \end{aligned} \tag{6}$$

where $R_\mu(\bullet)$ is the autocorrelation function of the bandwidth limited noise. Therefore, the Fourier transform of the autocorrelation function which is the power spectrum is

$$S(\omega) = \frac{2}{\pi} \int_0^\infty \frac{A^2}{2} \exp [R_\mu(t) - R_\mu(0)] \cos \omega_c t \cos \omega t \, dt. \tag{7}$$

The frequency deviation, $\Delta\omega$, is the amount ω_i changes when $n(t)$ is at its peak value. Note $\Delta\omega$ also determines the total power of $n(t)$. Also define ω_n as the bandwidth or cutoff frequency for $n(t)$. The well-known rule of thumb known as Carson's Rule can be used for estimating the bandwidth, ω_{BW},

$$\omega_{BW} = 2\omega_n \left[1 + \frac{\Delta\omega}{\omega_n}\right]. \tag{8}$$

Carson's rule accurately predicts the bandwidth of a sinusoidal carrier continuously modulated with a band of Gaussian noise. In the FSK scheme presented here it can still be used to predict the bandwidth of V_p if the bandwidth of $n(t)$ is sufficiently below f_c. From (8) it can be seen that the bandwidth of the output voltage depends on the frequency band of the Gaussian noise as well as its amplitude. Carson's rule is merely meant to be a tool by which one can gain an estimate of the bandwidth of the noise modulated voltage. It also confirms the assumption that in order to eliminate substantial lower frequency content, the noise bandwidth must be limited. From Carson's rule, the noise source $n(t)$ must be bandwidth limited noise.

Besides simply controlling the bandwidth and amplitude of the noise, it may also be desired to vary other characteristics of the noise, depending on how machine-generated acoustic noise is affected. It is widely known that adding pre-emphasis causes the spectrum of the modulated voltage, $V_p(t)$, to roll-off at a faster rate than without pre-emphasis. Pre-emphasis implies that the amplitude of the noise linearly decreases over the frequency band. Without pre-emphasis the amplitude spectrum is

flat. The characteristics of the noise source can be precisely controlled using so-called "periodic" noise. This type of noise is simply the summation of desired frequency components with random phase. That is, for periodic band limited noise:

$$n_p(t) = \sum_{k \in S} N_p \sin(kt + \xi_k) \tag{9}$$

where S is the set of desired frequency components of n_p. N_p is the magnitude of the spectral components of the noise. N_p can be made a function of k to incorporate pre-emphasis. ξ_k is a uniformly distributed random number between 0 and 2π.

Since Carson's rule depends only on $\Delta\omega$, the minimum frequency component of $n(t)$ can be set to zero. In fact, it has been shown in [5] that the spectrum only changes slightly if the minimum frequency component of $n(t)$ is nonzero and is much less than the maximum frequency component.

IV. Implementation

A block diagram illustrating the implementation of the proposed random modulated sine-triangle PWM regulator is shown in Fig. 4. As can be seen from the figure, the random modulation is a very simple addition to an existing sine-triangle regulator. A sample and hold element is clocked at each peak of the triangle wave to hold the value of slope for the next segment.

The bandwidth limited noise source can be any Gaussian wide band white noise generator followed by a low pass filter, or a periodic noise generator. The white noise source can be obtained quite simply in a number of different manners, such as monolithic noise generator circuits, zener diode voltage, or a number of other semiconductor-based methods. However, the low pass filter requires a number of components including reactive elements. Also, the low pass filter should have a sharp cutoff in order to define the band of the output voltage as precisely as possible.

Fig. 5 shows another method for implementing the random carrier PWM regulator. In this approach the band limited noise generator is implemented using a lookup table, whose contents have been generated apriori, off line. That is, a large quantity of periodic random numbers can be computer generated and stored in some type of ROM. If the quantity of numbers is large, the repetition rate of the random numbers can be made large say, greater than one second, and will have no effect on the resulting voltage spectra. The output of the ROM is then sent through a digital to analog converter to get the slope of the triangle wave. With this approach the noise generator, hardware filters, and sample and hold element are not needed. In addition, since the noise is being generated off-line, any type of noise can be implemented, including periodic noise. It is then a simple matter to compare the acoustic noise generated by the machine as a function of the noise which modulates the carrier wave.

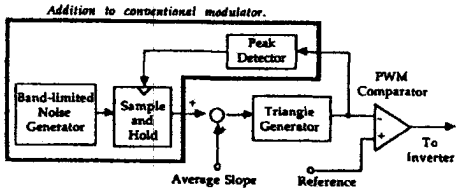


Fig. 4. Block diagram illustrating implementation of random carrier sinusoidal PWM regulator using analog noise generator.

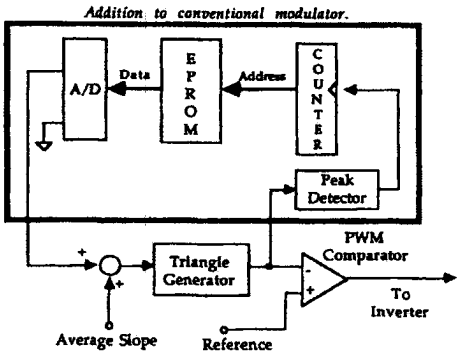


Fig. 5. Block diagram illustrating implementation of random carrier sinusoidal PWM regulator where noise source is generated digitally and stored in look-up table.

V. Experimental Results

An off-the-shelf 20-hp sinusoidal PWM inverter has been modified to include the random modulation scheme. The triangle carrier and the line switching function are shown in Fig. 6. Note that there is very little perceivable difference in the triangle wave with and without random modulation, since the instantaneous frequency is varying only slightly. Fig. 7 shows the harmonic spectrum of the Gaussian noise used to modulate the carrier. Note the effect of the added pre-emphasis which causes the lowest frequencies to be somewhat attenuated.

In all the results given, the output frequency is 17 Hz, the average switching frequency, $f_c = 1$ kHz; the cutoff frequency of the noise, $f_n = 500$ Hz for the band limited noise, and the peak frequency deviation, $\Delta f = 300$ Hz. The inverter is supplying an unloaded induction motor.

The line current at the induction machine terminals are shown in Fig. 8 with and without the random modulation. It is seen from this figure that the current is essentially unchanged due to the added random modulation. A linear scale plot of the line-line voltage spectra and the acoustic noise spectra are shown in Figs. 9 and 10 with and without random modulation. The acoustic noise spectra were measured with a sound pressure level meter, held in the same position for all measurements, with the microphone output connected to a spectrum analyzer. It is very important to note that the measured acoustic spectra are not meant to be absolute measurements of the acoustic noise

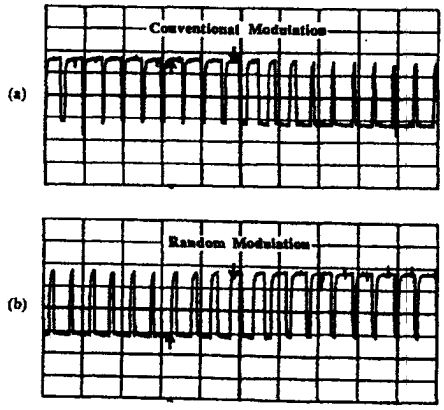


Fig. 6. Oscillograms of the pole switching functions. (a) Conventional sinusoidal modulation. (b) Randomly modulated sinusoidal PWM. Vert: 2 V/div. Horiz: 2 ms/div.

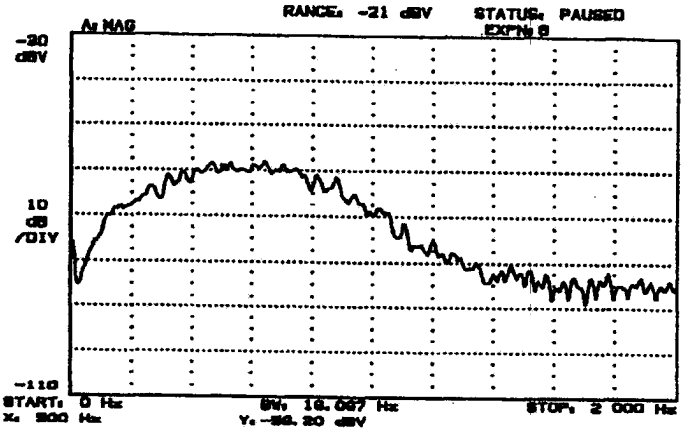


Fig. 7. Spectrum of noise used to modulate carrier waveform.

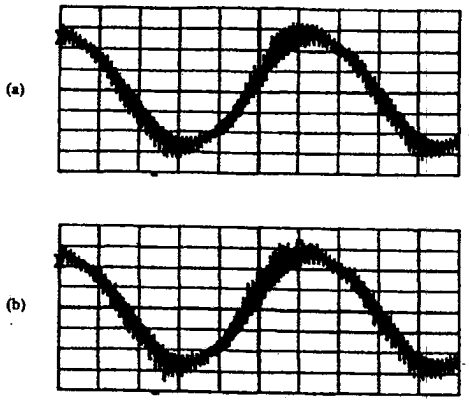
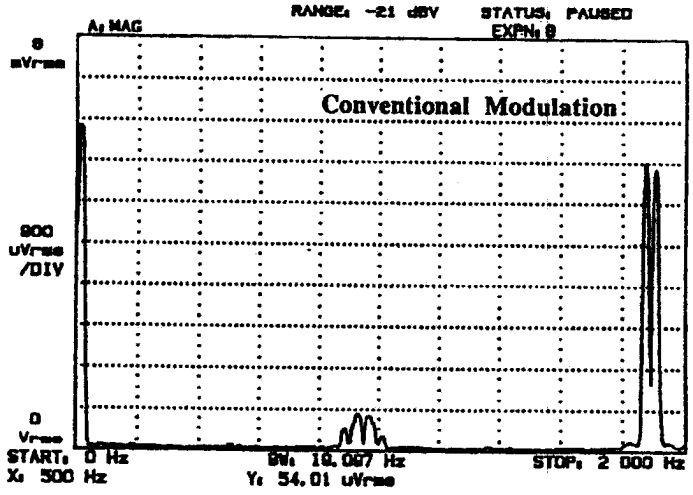
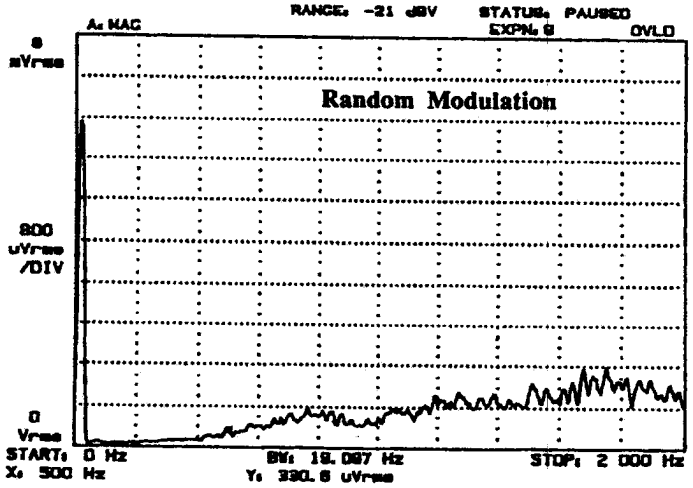


Fig. 8. Oscillograms of motor line current. (a) Conventional sinusoidal PWM. (b) Randomly modulated sinusoidal PWM. Vert: 10 A/div. Horiz: 10 ms/div.



(a)



(b)

Fig. 9. Spectra of ac load line-line voltage. (a) Conventional sinusoidal PWM. (b) Randomly modulated sinusoidal PWM.

produced by the machine. Rather, figures 9 and 10 are meant to serve as relative comparisons showing the effect of random modulation. From these figures it can be seen that no appreciable energy at low frequencies (below half the switching frequency) is delivered to the machine due to the random modulation.

In Figs. 9 and 10, note the dramatic reduction in the magnitude of the individual harmonics near the switching frequency in the randomly modulated spectra. For the particular motor used in the experimental part of the work, the total (rms) sound energy generated by the machine is not reduced by the random modulation. However, the energy spectrum of the noise is now spread to create a more appealing, less annoying sound.

VI. Conclusion

Acoustic noise in electric machines is caused by the interaction of the fundamental and harmonic flux densities. The annoying whine that the motor produces can be avoided by eliminating distinct tones in the applied voltage. It is proposed that an effective method of spreading the spectral content of the applied voltage is by randomly modulating the triangle carrier in sinusoidal PWM. In this

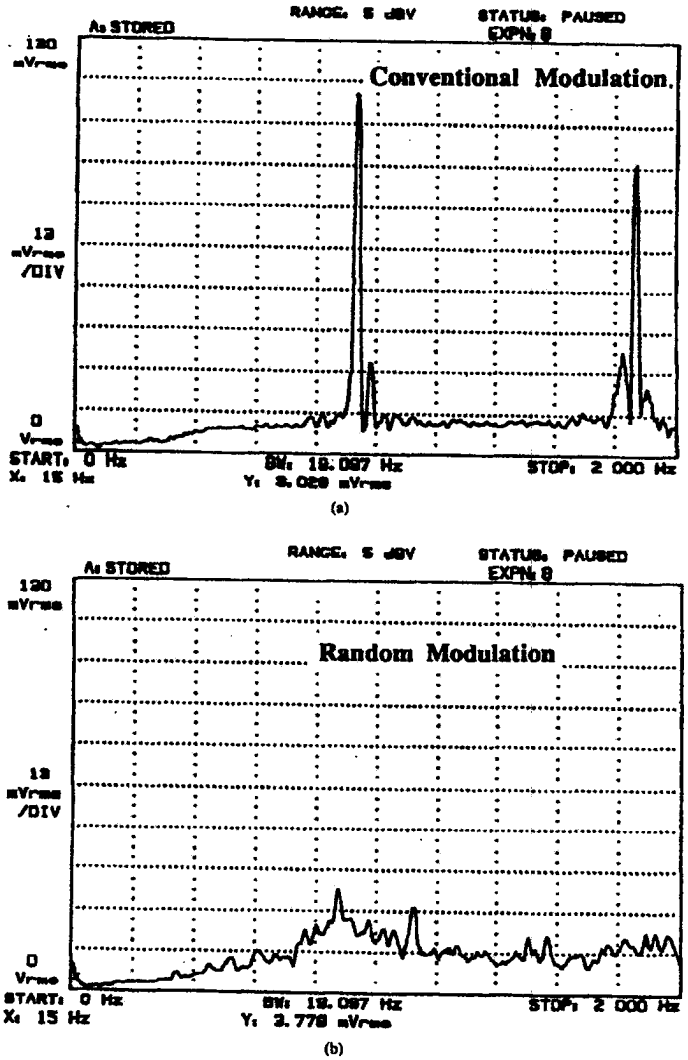


Fig. 10. Spectra of acoustic noise generated by induction machine. (a) Conventional sinusoidal PWM. (b) Randomly modulated sinusoidal PWM.

way, the energy in the tones around the switching frequency is spread out with subsequent reduction in peak values. The random modulator maintains the advantages of sinusoidal PWM including constant average switching frequency, linear amplification, and real-time control. The instantaneous switching frequency variation is small and can be predetermined. With the proposed scheme, the total level of the acoustic noise emitted by the machine remains constant. The acoustic noise, however, is more pleasing to the ear since the noise is now random. Experimental results illustrate the absence of tones in the voltage applied to an induction machine and in the spectrum of the acoustic noise generated by the machine.

Acknowledgment

This work has been supported through a scholarship to Thomas Habetler from the Electro-Motive Division of General Motors Corporation and through the Wisconsin Electric Machines and Power Electronics Consortium (WEMPEC). Special thanks is extended to Emerson Electric Co. for supplying the inverter used in the experimental work.

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Dr. Habetler was co-recipient of the 1989 first-prize paper award of the Industrial Drives Committee. He is a member of the IAS Industrial Power Converter Committee and Industrial Drives Committee.



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Dr. Divan has been a recepient of the Killam Scholarship while in his Ph.D. program and has also won various prize papers including the IEEE-IAS Best Paper Award for 1988–89. First prize paper for the Industrial Drives and Static Power Converter Committee in 1989, Third Prize Paper in the Power Semiconductor Committee and the 1983 third prize paper award of the Static Power Converter Committee of the IEEE Industry Applications Society. He is also a consultant for various industrial concerns. He has been the Program Chairman for the 1988 and 1989 Static Power Converter Committee of the IEEE-IAS. Program Chairman for PESC '91, and a Treasurer for PESC '89. He is also a Chairman of the Education Committee in the IEEE Power Electronics Society.

EXHIBIT 9
(Rebuttal and Supplemental Expert Reports - Dr. Robert Blauschild - *Power Integrations v. Fairchild Semiconductor,* U.S. District Court - Delaware: Case No. 04-1371-JJF)

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EXHIBIT 10
(Request for *Ex-Parte* Re-Examination dated November 9, 2006)

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Date: November 9, 2006

1. [X] This is a request for *ex parte* reexamination pursuant to 37 CFR 1.510 of patent number 6,249,876 issued June 19, 2001. The request is made by:

   [ ] patent owner. [X] third party requester.

2. [X] The name and address of the person requesting reexamination is:

   Sanjeet K. Dutta
   Orrick Herrington & Sutcliffe LLP
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3. [ ] a. A check in the amount of $_____ is enclosed to cover the reexamination fee, 37 CFR 1.20(c)(1);

   [X] b. The Director is hereby authorized to charge the fee as set forth in 37 CFR 1.20(c)(1) to Deposit Account No. 15-0665 (submit duplicative copy for fee processing); or

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4. [X] Any refund should be made by [ ] check or [X] credit to Deposit Account No. 15-0665. 37 CFR 1.26(c). If payment is made by credit card, refund must be to credit card account.

5. [X] A copy of the patent to be reexamined having a double column format on one side of a separate paper is enclosed. 37 CFR 1.510(b)(4)

6. [ ] CD-ROM or CD-R in duplicate, Computer Program (Appendix) or large table
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7. [ ] Nucleotide and/or Amino Acid Sequence Submission
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8. [X] A copy of any disclaimer, certificate of correction or reexamination certificate issued in the patent is included.

9. [X] Reexamination of claim(s) 1, 17, 18, 19 is requested.

10. [X] A copy of every patent or printed publication relied upon is submitted herewith including a listing thereof on Form PTO/SB/08, PTO-1449, or equivalent.

11. [ ] An English language translation of all necessary and pertinent non-English language patents and/or printed publications is included.

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12. [X] The attached detailed request includes at least the following items:

a. A statement identifying each substantial new question of patentability based on prior patents and printed publications. 37 CFR 1.510(b)(1)
b. An identification of every claim for which reexamination is requested, and a detailed explanation of the pertinency and manner of applying the cited art to every claim for which reexamination is requested. 37 CFR 1.510(b)(2)

13. [ ] A proposed amendment is included (only where the patent owner is the requester). 37 CFR 1.510(e)

14. [X] a. It is certified that a copy of this request (if filed by other than the patent owner) has been served in its entirety on the patent owner as provided in 37 CFR 1.33(c).
The name and address of the party served and the date of service are:

Blakeley, Sokoloff, Taylor, Zafman LLP
12400 Wilshire Boulevard, Seventh Floor
Los Angeles, CA 90025

Date of Service: November 9, 2006

[ ] b. A duplicate copy is enclosed since service on patent owner was not possible.

15. Correspondence Address: Direct all communication about the reexamination to:

[ ] The address associated with Customer Number:

OR

[X] Firm or Individual Name Sanjeet K. Dutta

Address 1000 Marsh Road

City Menlo Park | State CA | Zip 94025

Country USA

Telephone 650 614-7400 | Email

16. [X] The patent is currently the subject of the following concurrent proceeding(s):

[ ] a. Copending reissue Application No. _____
[ ] b. Copending reexamination Control No. _____
[ ] c. Copending Interference No. _____
[X] d. Copending litigation styled:

Power Integrations, Inc. v. Fairchild Semiconductor International, INC CA No. 04-1371-JJF

WARNING: Information on this form may become public. Credit card information should not be included on this form. Provide credit card information and authorization on PTO-2038.

Sanjeet Dutta
Authorized Signature

November 9, 2006
Date

Sanjeet K. Dutta
Typed/Printed Name

46,145
Registration No.

[ ] For Patent Owner Requester
[X] For Third Party Requester

PTO/SB/57 (04-05)
Approved for use through 04/30/2007. OMB 0651-0033
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

(Also referred to as FORM PTO-1465)

REQUEST FOR *EX PARTE* REEXAMINATION TRANSMITTAL FORM

Address to:
Mail Stop *Ex Parte* Reexam
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Attorney Docket No.: 10414-25

Date: November 9, 2006

1. [X] This is a request for *ex parte* reexamination pursuant to 37 CFR 1.510 of patent number 6,249,876 issued June 19, 2001. The request is made by:

   [ ] patent owner. [X] third party requester.

2. [X] The name and address of the person requesting reexamination is:

   Sanjeet K. Dutta
   Orrick Herrington & Sutcliffe LLP
   1000 Marsh Road, Menlo Park, CA 94025

3. [ ] a. A check in the amount of $_____ is enclosed to cover the reexamination fee, 37 CFR 1.20(c)(1);

   [X] b. The Director is hereby authorized to charge the fee as set forth in 37 CFR 1.20(c)(1) to Deposit Account No. 15-0665 (submit duplicative copy for fee processing); or

   [ ] c. Payment by credit card. Form PTO-2038 is attached.

4. [X] Any refund should be made by [ ] check or [X] credit to Deposit Account No. 15-0665. 37 CFR 1.26(c). If payment is made by credit card, refund must be to credit card account.

5. [X] A copy of the patent to be reexamined having a double column format on one side of a separate paper is enclosed. 37 CFR 1.510(b)(4)

6. [ ] CD-ROM or CD-R in duplicate, Computer Program (Appendix) or large table
   [ ] Landscape Table on CD

7. [ ] Nucleotide and/or Amino Acid Sequence Submission
   If applicable, items a. – c. are required.

   a. [ ] Computer Readable Form (CRF)
   b. Specification Sequence Listing on:

      i. [ ] CD-ROM (2 copies) or CD-R (2 copies); or
      ii. [ ] paper

   c. [ ] Statements verifying identity of above copies

8. [X] A copy of any disclaimer, certificate of correction or reexamination certificate issued in the patent is included.

9. [X] Reexamination of claim(s) 1, 17, 18, 19 is requested.

10. [X] A copy of every patent or printed publication relied upon is submitted herewith including a listing thereof on Form PTO/SB/08, PTO-1449, or equivalent.

11. [ ] An English language translation of all necessary and pertinent non-English language patents and/or printed publications is included.

This collection of information is required by 37 CFR 1.510. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Mail Stop *Ex Parte* Reexam, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**
If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

PTO/SB/57 (04-05)
Approved for use through 04/30/2007. OMB 0651-0033
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

12. [X] The attached detailed request includes at least the following items:

a. A statement identifying each substantial new question of patentability based on prior patents and printed publications. 37 CFR 1.510(b)(1)
b. An identification of every claim for which reexamination is requested, and a detailed explanation of the pertinency and manner of applying the cited art to every claim for which reexamination is requested. 37 CFR 1.510(b)(2)

13. [ ] A proposed amendment is included (only where the patent owner is the requester). 37 CFR 1.510(e)

14. [X] a. It is certified that a copy of this request (if filed by other than the patent owner) has been served in its entirety on the patent owner as provided in 37 CFR 1.33(c).
The name and address of the party served and the date of service are:

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Date of Service: November 9, 2006 ; or

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15. Correspondence Address: Direct all communication about the reexamination to:

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OR

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Address 1000 Marsh Road

City Menlo Park | State CA | Zip 94025

Country USA

Telephone 650 614-7400 | Email

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[ ] a. Copending reissue Application No. _____
[ ] b. Copending reexamination Control No. _____
[ ] c. Copending Interference No. _____
[X] d. Copending litigation styled:

Power Integrations, Inc. CA No. 04-1371-JJF
v.
Fairchild Semiconductor International, INC

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Sanjeet Dutta
Authorized Signature

November 9, 2006
Date

Sanjeet K. Dutta
Typed/Printed Name

46,145
Registration No.

[ ] For Patent Owner Requester
[X] For Third Party Requester

71338 U.S. PTO
90008326
11/09/06

REQUEST FOR *EX PARTE* REEXAMINATION OF U.S. PATENT NO. 6,249,876

71338 U.S. PTO
11/09/06

Attachment to Form PTO-1465
Providing Information about
Pat. No. 6,249,876
November 9, 2006
Express Mail No. [EV 859762242 US]

I. INTRODUCTION

Fairchild Semiconductor, Inc. ("Fairchild" or "Requester"), through these papers, requests that the Patent and Trademark Office grant this *ex parte* request to reexamine Claims 1, 17, 18, and 19 of U.S. Patent No. 6,249,876 ("the '876 patent") pursuant to the provisions of 35 U.S.C. §§ 302 *et seq.* and 37 C.F.R. § 1.510. A complete copy of the patent is enclosed as **Exhibit A**. A copy of the prosecution history of the '876 patent is attached as **Exhibit B**.

The inventors of the '876 patent are Balu Balakrisirshnan, Alex Djenguerian, and Leif Lund. Issuing on June 19, 2001, the '876 patent matured from U.S. Patent Application Serial No. 09/192,959. The '876 patent claims priority to the filing date of November 16, 1998. The '876 patent was assigned to Power Integrations, Inc. by its three listed inventors on November 13, 1998, recorded November 16, 1998 attached as **Exhibit E**. A certificate of correction issued on February 19, 2002.

Power Integrations sued Fairchild on October 20, 2004 for infringement of the '876 patent in the United States District Court for the District of Delaware (Civil Action No. 04-1371-JJF) ("the Litigation"). A claim construction order was entered on March 31, 2006. Six phrases relating to the scope of the '876 patent were construed by the Court. They are "frequency jittering," "coupled," "primary voltage," "secondary voltage," "combining," and "supplemental voltage." Power Integrations originally asserted Claims 1, 17, 18, and 19 during litigation. The

litigation was bifurcated into an infringement / damages phase and an invalidity phase. The infringement / damages trial took place from October 2-6, 2006. The jury found that certain Fairchild products infringed Claim 1 of the '876 patent. (Claims 17-19 were not tried.) The invalidity trial is scheduled to begin on December 4, 2006. A final judgment has not been entered in the case, and thus it is not yet ripe for appeal.

The undersigned is counsel of record in that case and represents that he is authorized to act in a representative capacity for Fairchild Semiconductor, Inc. Requester provides the fee for reexamination herewith in the amount of $2,520.00 and the fee for submitting an Information Disclosure Statement of $180.00.

A complete and entire copy of this Request for *ex parte* Reexamination and all supporting documents have been provided to the patent owner, Power Integrations, by serving Power Integrations' counsel of record in the litigation at 225 Franklin Street, Boston, MA 02110-2804. An additional copy was served on BLAKELEY, SOKOLOFF, TAYLOR, ZAFMAN LLP., attorney of record for the '876 patent, at 12400 Wilshire Boulevard, Seventh Floor, Los Angeles, CA 90025.

II. SUBSTANTIAL NEW QUESTION OF PATENTABILITY PURSUANT TO 37 C.F.R. § 1.510(b)(1)

This Reexamination Request is based upon the following prior art references.

1. U.S. Patent No. 4,638,417 ("Martin"). Attached to PTO Form 1449 as **Reference AA.**

2. "Acoustic Noise Reduction In Sinusoidal PWM Drives Using A Randomly Modulated Carrier", IEEE Transactions on Power Electronics, Vol. 6, No. 3, p. 356 (published July 1991) by T.G. Habetler and D.M. Divan ("Habetler"). Attached to PTO Form 1449 as **Reference CB.**

3. "Programmed Pulsewidth Modulated Waveforms For Electromagnetic Interference Mitigation In DC-DC Converters", IEEE Transactions on Power Electronics, Vol. 8, No. 4 (October 1993) by A.C. Wang and S. R. Sanders ("Wang"). Attached to PTO Form 1449 as **Reference CA.**

The Martin patent issued on January 20, 1987 and has a filing date of August 16, 1985. Martin is prior art to the '876 patent under 35 U.S.C. § 102(a), § 102(b), and § 102(e). Martin describes a digital frequency jittering circuit for use in power converters which varies the frequency of a voltage-controlled oscillator to reduce or eliminate EMI, as recited in claim 1 of the '876 patent. **Ref. AA**, 1:66-68. This teaching was not present during the prior examination of the '876 patent. Requestor believes that a reasonable examiner would consider this teaching important in determining whether or not the claims are patentable. Requestor respectfully submits that the Martin patent anticipates Claim 1 of the '876 patent. Requestor also submits that Claim 1 of the '876 patent is invalid as being obvious under 35 U.S.C. § 103 over Martin in view of one of ordinary skill in the art at the time the invention was made. For these reasons, Martin raises a substantial new question of patentability with respect to at least Claim 1 of the '876 patent.

Habetler was published in IEEE Transactions on Power Electronics Journal in July of 1991. Habetler qualifies as prior art to the '876 patent under § 102(a) and § 102(b). Habetler describes varying the switching frequency in a sinusoidal power converter in order to reduce acoustic noise. This teaching was not present during the prior examination of the '876 patent. Requestor believes that a reasonable examiner would consider this teaching important in determining whether or not the claims are patentable. Requestor respectfully submits that Habetler anticipates Claims 1, 17, 18, and 19 of the '876 patent. Requestor also submits that Claim 1 of the '876 patent is invalid as being obvious under 35 U.S.C. § 103 over Habetler in view of one of ordinary skill in the art at the time the invention was made. For these reasons, Habetler raises a substantial new question of patentability with respect to at least Claims 1, 17, 18, and 19 of the '876 patent.

Wang was published in October of 1993 in the IEEE Transactions on Power Electronics Journal, and so is a prior art reference under § 102(a) and § 102(b). This article describes the use of frequency variation via a digitally controlled analog waveform for EMI reduction in DC-DC power converters. Requestor believes that a reasonable examiner would consider this teaching

important in determining whether or not the claims are patentable. Requestor respectfully submits that Wang anticipates Claim 1 of the '876 patent. Requestor also submits that Claim 1 of the '876 patent is invalid as being obvious under 35 U.S.C. § 103 over Wang in view of one of ordinary skill in the art at the time the invention was made. For these reasons, Wang raises a substantial new question of patentability with respect to at least Claim 1 of the '876 patent.

III. CLAIMS FOR WHICH REEXAMINATION IS REQUESTED

Reexamination is requested of Claims 1, 17, 18, and 19 of the '876 patent in view of Martin, Habetler, and Wang. For the Examiner's convenience, Requestor includes copies of the cited art, which are attached to PTO Form 1449.

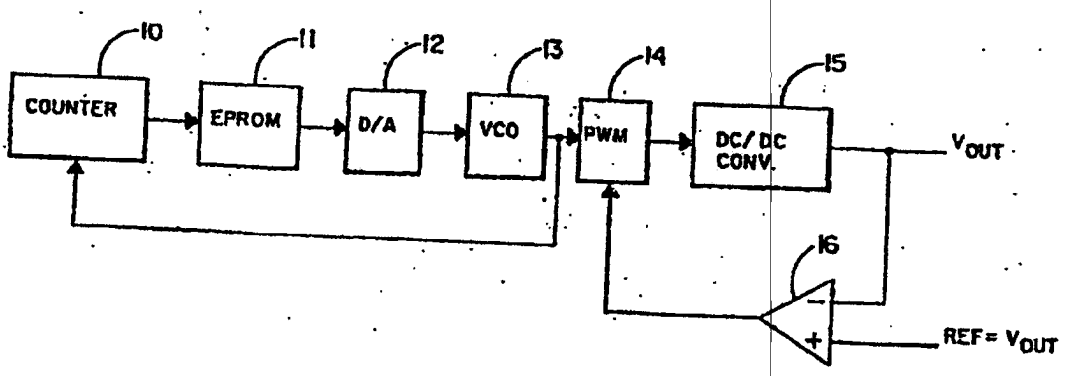
Requestor sets forth below a chart comparing each element of Claim 1 of the '876 patent with a corresponding disclosure from Martin that demonstrates that Martin anticipates Claim 1 of the '876 patent. Requestor further sets forth below a chart comparing each element of Claims 1, 17, 18, and 19 of the '876 patent with a corresponding disclosure from Habetler that demonstrates that Habetler anticipates Claims 1, 17, 18, and 19 of the '876 patent. Finally, Requestor sets forth below a chart comparing each element of Claim 1 of the '876 patent with a corresponding disclosure from Wang that demonstrates that Wang anticipates Claim 1 of the '876 patent.

IV. EXPLANATION OF PERTINENCE AND MANNER OF APPLYING MARTIN, HABETLER, AND WANG TO CLAIMS 1, 17, 18, AND 19 OF THE '876 PATENT

Claims 1, 17, 18, and 19 of the '876 patent disclose a frequency jittering circuit for use in power supplies in electronic devices. The concept of jittering the frequency of a power supply in order to reduce EMI has been around for almost 20 years. Furthermore, the very same circuit configuration described by the '876 patent to jitter the frequency (a digital to analog converter, connected to a counter, connected to an oscillator) was used for precisely that purpose. All the limitations of Claims 1, 17, 18, and 19 are found in at least one of the three references discussed below.

A. Martin Anticipates Claim 1 of the '876 Patent

Martin's frequency jittering circuit is illustrated in the sole figure of the Martin patent.



Claim 1 of the '876 patent recites "*an oscillator for generating a signal having a switching frequency, the oscillator having a control input for varying the switching frequency.*" **Ex. A**, Claim 1. The Martin circuit includes voltage-controlled oscillator (VCO) 13. VCO 13 generates a signal with a switching frequency that varies according to a control input. **Ref. AA**, 2:46-49 ("This analog signal is then applied to VCO 13 which produces an oscillating signal which has a frequency which is representative of the amplitude of the analog signal."); 2:39-40 ("the output signal produced by VCO 13 varies in frequency"). In other words, as the amplitude of the analog signal applied to the control input of VCO 13 changes, so does the frequency of the signal generated by the oscillator.

Claim 1 also includes the limitation of "*a digital to analog converter coupled to the control input for varying the switching frequency.*" **Ex. A**, Claim 1. The Martin circuit includes a digital to analog converter (D/A) 12. See **Ref. AA**, 2:34-35. As described in Martin and illustrated in the figure, D/A converter 12 is connected directly to the control input of the oscillator. **Ref. AA**, 2:35-49 (The D/A converter 12 supplies an analog signal to the VCO 13). The analog signal is used to vary the switching frequency of the signal generated by the

oscillator in the manner described in the preceding paragraph.

Claim 1 recites "*a counter coupled to the output of the oscillator and to the digital to analog converter, the counter causing the digital to analog converter to adjust the control input and to vary the switching frequency.*" **Ex. A**, Claim 1. The Martin circuit includes COUNTER 10. As shown in the above figure, the output of VCO 13 is directly connected to COUNTER 10. COUNTER 10 is also coupled to D/A converter 12 through EPROM 11. The Martin patent describes how COUNTER 10 causes D/A converter 12 to adjust the control input to the oscillator and to vary the switching frequency of the oscillator:

> Thus, as the output signal produced by VCO 13 varies in frequency, the counter 10 is caused to count at different rates. **With counter 10 counting at different rates the EPROM 11 is stepped or addressed at different rates.** The content of the PROM are... a pseudo random code in digital form. The digital signal from the PROM 11 is converted to an analog signal by D/A converter 12. **This analog signal is then applied to VCO 13 which produces an oscillating signal which has a frequency which is representative of the amplitude of the analog signal.**

Ref. AA, 2:39-49 (emphasis added); *see also* 4:8-11. Accordingly, Martin teaches each and every element of Claim 1 of the '876 patent.

Martin teaches that as COUNTER 10 is incremented it provides signals to EPROM 11, which uses those signals to look up digital signals stored at addresses in the EPROM which are identified by the counter signals. **Ref. AA**, 2:39-49. The digital signal stored in the EPROM at the particular addresses identified by the counter signals are then passed to the digital to analog converter, which converts the digital signal to an analog form and provides it to the control input of the oscillator:

> Consequently, when counter 10 produces an output signal, it selectively steps the PROM [11] (or ROM) through its addressing routine in order to select the contents of a particular address. **The contents of PROM 11 are stored in digital form.** These digital signals are supplied to **the digital-to-analog converter 12 [which] supplies an analog signal to the VCO 13.**

Ref. AA, 2:29-36 (emphasis added).

COUNTER 10 controls D/A converter 12 and causes it to adjust the control input of

oscillator VCO 13 and thus to vary the switching frequency of the oscillator. **Ref. AA**, 2:39-49. Even considering the additional feature of EPROM 11, Martin teaches each and every element of claim 1 of the '876 patent.

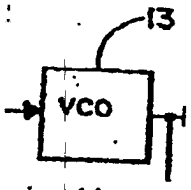
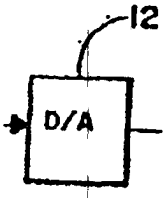
In fact, the only difference between Claim 1 of the '876 patent and the circuit shown in Martin is that Martin adds an EPROM or other storage means between the counter and the D/A converter. The fact that Martin includes an additional component should be irrelevant to anticipate, as Martin nonetheless discloses each and every element of Claim 1.

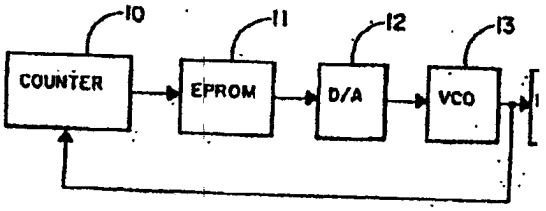
In any event, it would be obvious to one skilled in the art to remove the storage means from Martin, so that the counter would be directly connected to the D/A converter. It would be obvious to do this because the storage means is not necessary to vary the frequency of the circuit. The storage means merely adds a level of complexity to the circuit claimed in Claim 1 of the '876 patent by enabling storage of a prescribed signal pattern. **Ref. AA**, 4:5-7 ("including storage means for storing a prescribed signal pattern which is selectively supplied to said VCO means"). While removing the EPROM element would simplify the circuit, Martin still teaches each and every element of Claim 1 of the '876 patent.

1. Claim 1

Claim 1 is an independent claim that Martin anticipates. As detailed in the table below, Martin discloses each and every limitation of Claim 1. Accordingly, Requestor expressly proposes the rejection of at least Claim 1 under 35 U.S.C. §§ 102 (a), (b), and (e) as being anticipated by Martin. Requestor also proposes the rejection of at least Claim 1 as being obvious under 35 U.S.C. § 103 over Martin in view of one of ordinary skill in the art at the time the invention was made.

'876 Patent Claim 1	**Anticipated or Rendered Obvious by U.S. Patent No. 4,638,417 ("Martin")**
1. A digital frequency jittering circuit for varying the switching frequency of a power supply, comprising:	Martin describes a digital frequency jittering circuit for varying the switching frequency of a power supply. "Referring now to the sole FIGURE, there is

'876 Patent Claim 1	Anticipated or Rendered Obvious by U.S. Patent No. 4,638,417 ("Martin")
	shown a **circuit which reduces electromagnetic interference (EMI) by frequency modulation of power converters."** **Ref. AA**, 1:66-68 (emphasis added).
an oscillator for generating a signal having a switching frequency, the oscillator having a control input for varying the switching frequency;	As shown in the Figure, there is an oscillator (VCO 13) for generating a signal having a switching frequency, the oscillator having a control input for varying the switching frequency.  "This analog signal is then applied to **VCO 13 which produces an oscillating signal which has a frequency** which is representative of the amplitude of the analog signal. The VCO output signal is supplied to the pulse width modulator 14 which **varies the chopping rate of the signal from the VCO 13** while maintaining a constant duty ratio." **Ref. AA**, 2:46-52 (emphasis added). "Thus, as the output signal produced by VCO 13 **varies in frequency**, the counter 10 is caused to count at different rates." **Ref. AA**, 2:39-41 (emphasis added).
a digital to analog converter coupled to the control input for varying the switching frequency; and	As shown in the Figure, there is a digital to analog converter (D/A 12) coupled to the control input of the oscillator (VCO 13) for varying the switching frequency.  "The digital signal from the PROM 11 is converted to an analog signal by **D/A converter 12. This analog signal is then applied to VCO 13** which produces an oscillating signal which has a frequency which is representative of the amplitude of the analog signal." **Ref. AA**, 2:44-49 (emphasis added).

'876 Patent Claim 1	Anticipated or Rendered Obvious by U.S. Patent No. 4,638,417 ("Martin")
a counter coupled to the output of the oscillator and to the digital to analog converter, the counter causing the digital to analog converter to adjust the control input and to vary the switching frequency.	As shown in the Figure, there is a counter (COUNTER 10) coupled to the output of the oscillator (VCO 13) and to the digital to analog converter (D/A 12, coupled to the oscillator through the ROM element EPROM 11), the counter causing the digital to analog converter to adjust the control input and to vary the switching frequency.  "The **output signal from the VCO 13 is also fed back to counter 10** which can be any suitable counter of any prescribed length." **Ref. AA**, 2:20-22 (emphasis added). "The output of the counter 10 is connected to the input of EPROM 11 which can be any suitable kind of storage device.... The contents of the PROM 11 are stored in digital form. These digital signals are supplied to the digital-to-analog converter 12. The D/A converter 12 supplies an analog signal to the VCO 13." **Ref. AA**, 2:22-36. "Thus, as the output signal produced by VCO 13 varies in frequency, the counter 10 is caused to count at different rates. **With counter 10 counting at different rates** the EPROM 11 is stepped or addressed at different rates. The content of the PROM are ... a pseudo random code in digital form. **The digital signal from the PROM 11 is converted to an analog signal by D/A converter 12. This analog signal is then applied to VCO 13** which produces an oscillating signal which has a frequency which is representative of the amplitude of the analog signal." **Ref. AA**, 2:39-49 (emphasis added). Martin's use of the EPROM element does not prevent it from anticipating claim 1, because the COUNTER 10 is still coupled to the digital to analog converter (D/A 12). The EPROM 11 uses the signal from the COUNTER 10 to look up stored digital

'876 Patent Claim 1	Anticipated or Rendered Obvious by U.S. Patent No. 4,638,417 ("Martin")
	signals. "Consequently, when counter 10 produces an output signal, it selectively steps the PROM [11] (or ROM) through its addressing routine in order to select the contents of a particular address." 2:29-32. The EPROM has a one-to-one correspondence from input to output. Every time the EPROM element receives a given input value, it will produce the same given output value. In any event, it would be obvious to one skilled in the art to remove the EPROM or other storage means from Martin, so that the counter would be directly connected to the D/A converter. It would be obvious to do this because the storage means is not necessary to vary the frequency of the circuit. The storage means merely adds a level of complexity to the circuit claimed in Claim 1 of the '876 patent by enabling storage of a prescribed signal pattern. **Ref. AA**, 4:5-7 ("including storage means for storing a prescribed signal pattern which is selectively supplied to said VCO means"). While removing the EPROM element would simplify the circuit, Martin still teaches each and every element of Claim 1 of the '876 patent.

B. Habetler Anticipates Claims 1, 17, 18, and 19 of the '876 Patent

Habetler describes varying the switching frequency of a sinusoidal power converter in order to reduce acoustic noise:

> Acoustic noise in an inverter-driven electric machine can be reduced by avoiding the concentration of harmonic energy in distinct tones. **One method to spread out the harmonic spectrum without the use of programmed PWM is to cause the switching pattern to be random.** It is proposed that the switching pattern can be randomized by modulating the triangle carrier in sinusoidal PWM with band-limited white noise.
> * * *
> It is proposed that an effective method of spreading the spectral content of the applied voltage is by randomly modulating the triangle carrier in sinusoidal PWM. **In this way, the energy in the tones around the switching frequency is spread out with subsequent reduction in peak values.** The random modulator

maintains the advantages of sinusoidal PWM including constant average switching frequency, linear amplification, and real-time control. **The instantaneous switching frequency variation is small and can be predetermined.**

Id., pp. 356, 361-62. Figure 5 of Habetler shows an oscillator (labeled "Triangle Generator" in the figure) that generates a signal having a switching frequency, and that has a control input for varying the switching frequency.

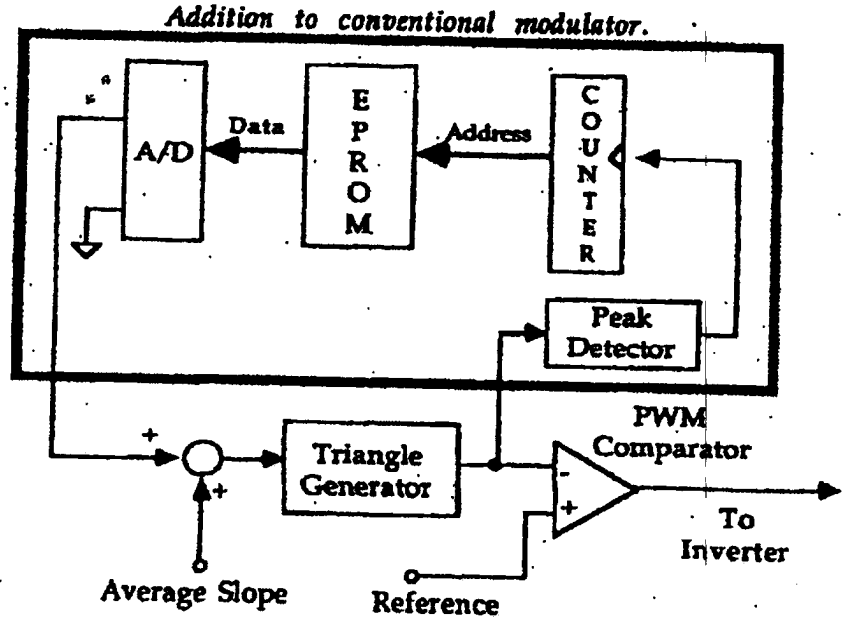


Fig. 5. Block diagram illustrating implementation of random carrier sinusoidal PWM regulator where noise source is generated digitally and stored in look-up table.

Figure 5 of Habetler also shows a digital to analog converter (labeled "A/D" because the signals are drawn moving right to left in the figure rather than left to right) coupled to the control input for varying the switching frequency by varying the slope of the triangle wave. **Ref. CB,** pp. 359 ("[t]he output of the ROM is then sent through a digital to analog converter to get the slope of the triangle wave.") Figure 5 illustrates a counter coupled to the output of the Triangle Generator and to the digital to analog converter, the counter causing the digital to analog converter to adjust the control input and to vary the switching frequency. Habetler thus teaches

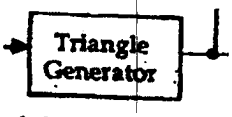
each element of Claim 1 of the '876 patent. As discussed above, the EPROM does not prevent the counter from being "coupled" to the digital to analog converter, as recited in Claim 1 of the '876 patent.

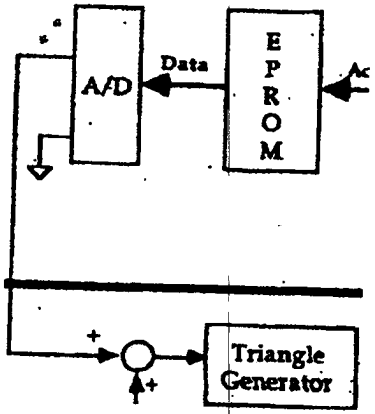
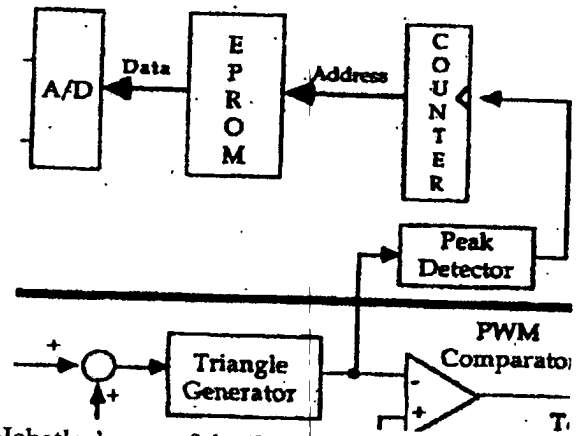
Alternatively, it would be obvious to one skilled in the art to remove the EPROM element from Habetler, so that the COUNTER would be directly connected to digital to analog converter (A/D). It would be obvious to do this because the EPROM element is not necessary to vary the frequency of the circuit. The EPROM element merely introduces a greater degree of complexity. While removing the EPROM element would eliminate this greater degree of complexity, such a simplified circuit would still vary the frequency.

1. Claim 1

Claim 1 is an independent claim that Habetler anticipates. As detailed in the table below, Habetler discloses each and every limitation of Claim 1. Accordingly, Requestor expressly proposes the rejection of at least Claim 1 under 35 U.S.C. § 102 (a) and (b) as being anticipated by Habetler. Requestor also proposes the rejection of at least Claim 1 as being obvious under 35 U.S.C. § 103 over Habetler in view of one of ordinary skill in the art at the time the invention was made.

'876 Patent Claim 1	**Anticipated or Rendered Obvious by Habetler**
1. A digital frequency jittering circuit for varying the switching frequency of a power supply, comprising:	Habetler teaches a digital frequency jittering circuit for varying the switching frequency of a power supply. "Acoustic noise in an inverter-driven electric machine can be reduced by avoiding the concentration of harmonic energy in distinct tones. One method to spread out the harmonic spectrum without the use of programmed PWM is to cause the switching pattern to be random. It is proposed that the switching pattern can be randomized by modulating the triangle carrier in sinusoidal PWM with band-limited white noise." **Ref. CB**, pp. 356. "It is proposed that **an effective method of**

'876 Patent Claim 1	Anticipated or Rendered Obvious by Habetler
	spreading the spectral content of the applied voltage is by randomly modulating the triangle carrier in sinusoidal PWM. In this way, the energy in the tones around **the switching frequency is spread out with subsequent reduction in peak values.** The random modulator maintains the advantages of sinusoidal PWM including constant average switching frequency, linear amplification, and real-time control." **Ref. CB**, pp. 361-362 (emphasis added).
an oscillator for generating a signal having a switching frequency, the oscillator having a control input for varying the switching frequency;	Figure 5 shows an oscillator that is a "Triangle Generator." The Triangle Generator generates a signal with a switching frequency. An input to the Triangle Generator varies the switching frequency.  "It is proposed that **an effective method of spreading the spectral content of the applied voltage is by randomly modulating the triangle carrier in sinusoidal PWM.** In this way, the energy in the tones around **the switching frequency is spread out with subsequent reduction in peak values.** The random modulator maintains the advantages of sinusoidal PWM including constant average switching frequency, linear amplification, and real-time control." **Ref. CB**, pp. 361-362 (emphasis added). "Fig. 5 shows another method for implementing the random carrier PWM regulator. In this approach the band limited noise generator is implemented using a lookup table, whose contents have been generated apriori, off line. That is, a large quantity of periodic random numbers can be computer generated and stored in some type of ROM. If the quantity of numbers is large, the repetition rate of the random numbers can be made large say, greater than one second, and will have no effect on the resulting voltage spectra. The output of the ROM is then sent through a digital to analog converter to get the slope of the triangle wave." **Ref. CB**, pp. 359.

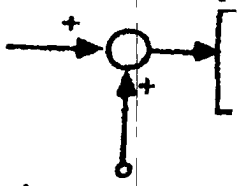
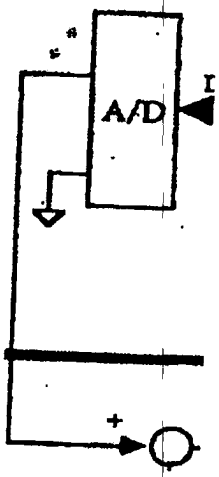
'876 Patent Claim 1	Anticipated or Rendered Obvious by Habetler
a digital to analog converter coupled to the control input for varying the switching frequency; and	Figure 5 shows a block labeled "A/D" coupled to the input of the triangle generator for varying the switching frequency of the triangle wave by varying the slope of the triangle wave. This "A/D" block is a digital to analog converter that converts a digital signal received from the EPROM into an analog signal.  "The output of the ROM is then sent through a digital to analog converter to get the slope of the triangle wave." **Ref. CB**, pp. 359.
a counter coupled to the output of the oscillator and to the digital to analog converter, the counter causing the digital to analog converter to adjust the control input and to vary the switching frequency.	Figure 5 illustrates a counter coupled to the output of the triangle generator and to the block labeled "A/D", which is a digital to analog converter. The counter causes the digital to analog converter to adjust the control input and vary the switching frequency.  Habetler's use of the EPROM element does not prevent it from anticipating claim 1, because the COUNTER is still "coupled" to the digital to analog converter (A/D). The EPROM uses the

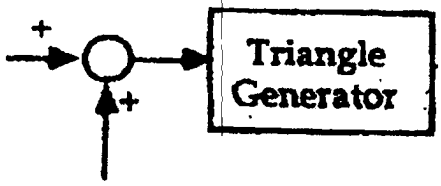
'876 Patent Claim 1	Anticipated or Rendered Obvious by Habetler
	signal from the COUNTER to look up a stored digital signal. The EPROM has a one-to-one correspondence from input to output. Every time the ROM element receives a given input value, it will produce the same given output value. Alternatively, it would be obvious to one skilled in the art to remove the EPROM element from Habetler, so that the COUNTER would be directly connected to digital to analog converter (A/D). It would be obvious to do this because the EPROM element is not necessary to vary the frequency of the circuit. The EPROM element merely adds a level of complexity to the circuit claimed in claim 1 of the '876 patent. While removing the EPROM element would simplify the circuit, such a simplified circuit would still vary the frequency.

2. Claim 17

Claim 17 is an independent claim that Habetler anticipates. As detailed in the table below, Habetler discloses each and every limitation of Claim 17. Accordingly, Requestor expressly proposes the rejection of at least Claim 17 under 35 U.S.C. § 102 (a) and (b) as being anticipated by Habetler.

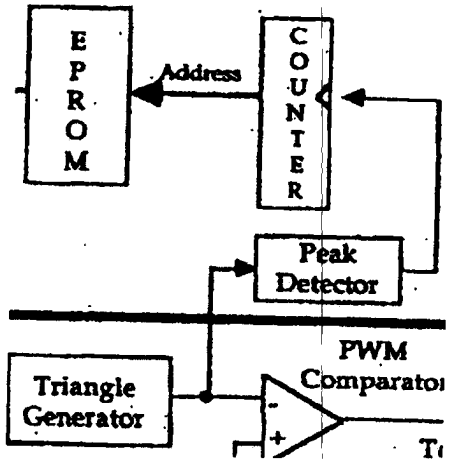
'876 Patent Claim 17	Anticipated by Habetler
17. A method for generating a switching frequency in a power conversion system, comprising:	Habetler teaches a method for generating a switching frequency in a power conversion system. "Acoustic noise in an inverter-driven electric machine can be reduced by avoiding the concentration of harmonic energy in distinct tones. **One method to spread out the harmonic spectrum without the use of programmed PWM is to cause the switching pattern to be random. It is proposed that the switching pattern can be randomized by modulating the triangle carrier in sinusoidal PWM with band-limited white noise." Ref. CB**, pp. 356 (emphasis added). "It is proposed that **an effective method of spreading the spectral content of the applied**

'876 Patent Claim 17	Anticipated by Habetler
	voltage is by randomly modulating the triangle carrier in sinusoidal PWM. In this way, the energy in the tones around **the switching frequency is spread out with subsequent reduction in peak values.** The random modulator maintains the advantages of sinusoidal PWM including constant average switching frequency, linear amplification, and real-time control." **Ref. CB**, pp. 361-362 (emphasis added).
generating a primary voltage;	Habetler teaches generating a primary voltage, which is labeled "average slope" in Figure 5. 
cycling one or more secondary voltage sources to generate a secondary voltage which varies over time; and	Habetler teaches cycling one or more secondary voltage sources to generate a secondary voltage, which is the output of the "A/D" block.  This secondary voltage varies over time.
combining the secondary voltage with the primary voltage to be received at a control input of a voltage-controlled oscillator for generating a switching frequency which is varied over time.	As shown in Figure 5, Habetler teaches that the secondary voltage is combined with the primary voltage at a voltage summer at the control input of the voltage controlled oscillator (Triangle Generator) to generate a switching frequency that is varied over time.

'876 Patent Claim 17	Anticipated by Habetler
	

3. Claim 18

Dependent Claim 18 adds to Claim 17 the limitation that the device of Claim 17 has a counter clocked with the output of the oscillator. Because Claim 18 depends on Claim 17, all limitations of Claim 17 incorporated into Claim 18 are anticipated. As detailed in the table below, Habetler discloses each and every limitation of Claim 18. Accordingly, Requestor expressly proposes the rejection of at least Claim 18 under 35 U.S.C. § 102 (a) and (b) as being anticipated by Habetler.

'876 Patent Claim 18	Anticipated by Habetler
18. The method of claim 17 further comprising clocking a counter with the output of the oscillator.	As shown in Figure 5, Habetler teaches clocking a counter (COUNTER) with the output of the oscillator (Triangle Generator). 

4. Claim 19

Dependent Claim 19 adds to Claim 17 the limitation that the primary voltage is V and each of the secondary voltage sources generates a supplemental voltage lower than V, further comprising passing the supplemental voltage to the voltage-controlled oscillator. Because Claim 19 depends on Claim 17, all limitations of Claim 17 incorporated into Claim 19 are anticipated. As detailed in the table below, Habetler discloses each and every limitation of Claim 19. Accordingly, Requestor expressly proposes the rejection of at least Claim 19 under 35 U.S.C. § 102 (a) and (b) as being anticipated by Habetler.

'876 Patent Claim 19	Anticipated by Habetler
19. The method of claim 17 wherein the primary voltage is V and each of the secondary voltage sources generates a supplemental voltage lower than V, further comprising passing the supplemental voltage to the voltage-controlled oscillator.	Habetler teaches that the supplemental voltages generated by the secondary voltage sources are lower than the primary voltage. "The triangle carrier and the line switching function are shown in Fig. 6. Note that there is very little perceivable difference in the triangle wave with and without random modulation, since the instantaneous frequency is varying only slightly." **Ref. CB** pp. 359. The supplemental voltage is passed to the voltage-controlled oscillator.

C. **Wang Anticipates Claim 1 of the '876 Patent**

This article describes the use of frequency variation via a digitally controlled analog waveform for EMI reduction in DC-DC power converters. Wang by itself anticipates all of the elements listed in Claim 1.

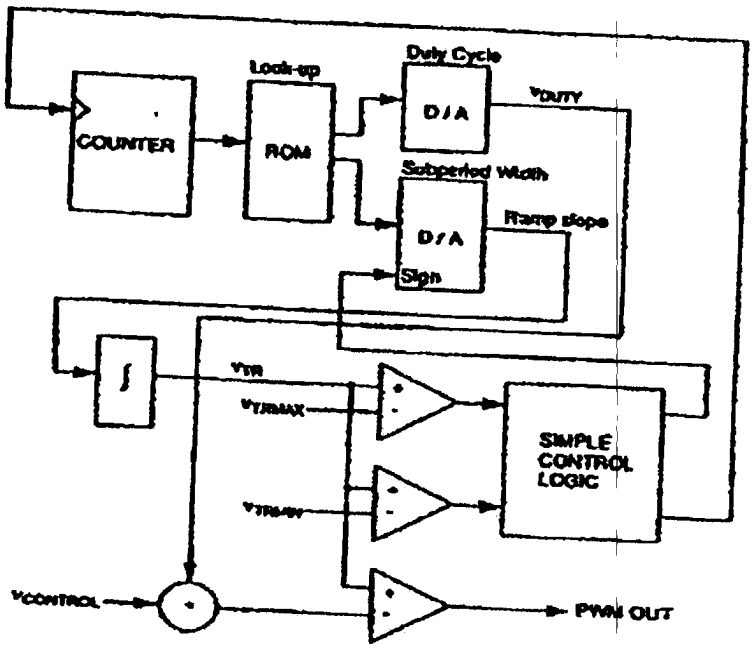
Wang discloses a circuit for reducing the EMI of a power converter by varying the switching frequency of the device:

> In this paper, a method to generate an optimal programmed switching waveform for a dc-dc converter is presented. **This switching waveform is optimized to reduce the amplitude of harmonic peaks in the EMI generated by the converter.**

. . .

The main approaches considered in this paper rely on the fact that it is possible to operate a PWM type **power circuit with a time-varying switching frequency** provided the average duty cycle is not disturbed. We employ a programmed waveform that repeats itself after K cycles. A typical programmed PWM waveform and its spectrum is illustrated in Fig. 1(b). Compared to regular PWM, the programmed PWM has a harmonic spacing that is smaller by a factor of K. The extra available harmonic frequencies are used to spread out the spectral energy of a given circuit waveform.

Ref. CA, pp. 596.



Ref. CA, pp. 604, figure 20.

As demonstrated in figure 20 above, Wang contains each and every limitation of Claim 1 of the '876 patent. Figure 20 illustrates an oscillator for generating a signal having a switching frequency ("V_{TR}") and having a control input ("Ramp slope") for varying the switching frequency. It shows a digital to analog converter ("D/A, subperiod width") coupled to the control input ("Ramp slope") for varying the switching frequency. And, it shows a counter (COUNTER) coupled to the output of the oscillator and (through the ROM element) to the digital to analog converter (D/A), the counter causing the digital to analog converter to adjust the control input and to vary the switching frequency. Wang describes the oscillator element

(referred to as a waveform generator) in detail:

> **A full implementation of the programmed waveform generator with a continuous control input can be based on a programmable triangle waveform generator.** Two numbers are stored for every subperiod. One controls the slope of the triangle waveform, and therefore, the length of the subperiod. The other is added to the control signal, and therefore changes the duty ratio of a given subperiod from the average. **The important waveforms and the resulting programmed PWM output are shown in Fig. 19. A block diagram implementation is shown in Fig. 20.**

Ref. CA, pp. 603-04 (emphasis added).

As with Martin, described above, the ROM element between the counter and the digital to analog converter does not prevent the described circuit from anticipating the '876 patent. The ROM merely functions as a lookup table to add a degree of complexity to the variation of the control input provided by the counter. **Ref. CA**, pp. 604. Again it is the counter that enables the selection of different signals stored in the ROM and thus that causes the digital to analog converter to adjust the control input and vary the switching frequency.

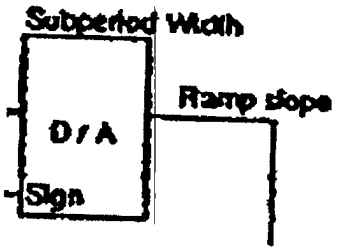
Alternatively, it would be obvious to one skilled in the art to remove the ROM element from Wang, so that the COUNTER would be directly connected to digital to analog converter (D/A). It would be obvious to do this because the ROM element is not necessary for the Wang circuit vary the frequency. The ROM element merely adds a level of complexity to the circuit claimed in claim 1 of the '876 patent. While removing the ROM element would simplify the circuit, the simplified circuit would still vary the frequency.

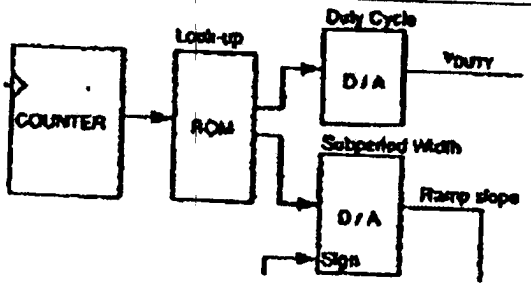
1. Claim 1

Claim 1 is an independent claim that Wang anticipates. As detailed in the table below, Wang discloses each and every limitation of Claim 1. Accordingly, Requestor expressly proposes the rejection of at least Claim 1 under 35 U.S.C. § 102 (a) and (b) as being anticipated by Wang. Requestor also proposes the rejection of at least Claim 1 as being obvious under 35 U.S.C. § 103 over Wang in view of one of ordinary skill in the art at the time the invention was

made.

'876 Patent Claim 1	Anticipated or Rendered Obvious by Wang
1. A digital frequency jittering circuit for varying the switching frequency of a power supply, comprising:	Wang teaches a digital frequency jittering circuit for varying the switching frequency of a power supply. "In this paper, a method to generate an optimal programmed switching waveform for a dc-dc converter is presented. This switching waveform is optimized to reduce the amplitude of harmonic peaks in the EMI generated by the converter." Abstract. "The main approaches considered in this paper rely on the fact that **it is possible to operate a PWM type power circuit with a time-varying switching frequency** provided the average duty cycle is not disturbed. We employ a programmed waveform that repeats itself after *K* cycles. A typical programmed PWM waveform and its spectrum is illustrated in Fig. 1(b). Compared to regular PWM, the programmed PWM has a harmonic spacing that is smaller by a factor of *K*. The extra available harmonic frequencies are used to spread out the spectral energy of a given circuit waveform. (emphasis added) Section II of the paper reviews the main techniques considered in the literature. **Sections III and IV illustrate the application of these methods in the context of a dc-dc converter." Ref. CA**, pp. 596 (emphasis added).
an oscillator for generating a signal having a switching frequency, the oscillator having a control input for varying the switching frequency;	Wang teaches an oscillator for generating a signal having a switching frequency (V_{TR}), the oscillator having a control input (Ramp slope) for varying the switching frequency. "**A full implementation of the programmed waveform generator with a continuous control input can be based on a programmable triangle waveform generator.** Two numbers are stored for every subperiod. One controls the slope of the

'876 Patent Claim 1	Anticipated or Rendered Obvious by Wang
	triangle waveform, and therefore, the length of the subperiod. The other is added to the control signal, and therefore changes the duty ratio of a given subperiod from the average. The important waveforms and the resulting programmed PWM output are shown in Fig. 19. A block diagram implementation is shown in Fig. 20. **Note that the average duty cycle can be varied linearly with the standard duty ratio control signal, marked $V_{CONTROL}$ in Fig. 19.** However, the linear range is smaller than with regular PWM in this implementation because of the variation in the D_k's." **Ref. CA**, pp. 603-604 (emphasis added).
a digital to analog converter coupled to the control input for varying the switching frequency; and	Figure 20 teaches a digital to analog converter (D/A) coupled to the control input (Ramp slope) for varying the switching frequency. 
a counter coupled to the output of the oscillator and to the digital to analog converter, the counter causing the digital to analog converter to adjust the control input and to vary the switching frequency.	Figure 20 teaches a counter (COUNTER) coupled to the output of the oscillator (SIMPLE CONTROL LOGIC) and to the digital to analog converter (D/A), the counter causing the digital to analog converter to adjust the control input (Ramp slope) and to vary the switching frequency (V_{TR}). Figure 19 shows the change in switching frequency.

'876 Patent Claim 1	Anticipated or Rendered Obvious by Wang
	 Wang's use of the ROM element does not prevent it from anticipating claim 1, because the COUNTER is still coupled to the digital to analog converter (D/A, Subperiod Width). The ROM uses the signal from the COUNTER to look up stored digital signal. The ROM has a one-to-one correspondence from input to output. Every time the ROM element receives a given input value, it will produce the same given output value. Alternatively, it would be obvious to one skilled in the art to remove the ROM element from Wang, so that the COUNTER would be directly connected to digital to analog converter (D/A). It would be obvious to do this because the ROM element is not necessary for the Wang circuit to vary the frequency. The ROM element merely adds a level of complexity to the circuit claimed in claim 1 of the '876 patent. While removing the ROM element would simplify the circuit, the simplified circuit would still vary the frequency.

V. CONSTRUCTION OF CLAIM TERMS IN THE '876 PATENT

The '876 patent and three other patents are currently the subject of litigation in the United States District Court for the District of Delaware (Civil Action No. 04-1371-JJF). This action was filed by the assignee of the '876 patent, Power Integrations, Inc., against Fairchild. The parties have set forth their respective positions as to how certain limitations of the referenced

claims of the '876 patent should be construed in claim construction briefs. The Court has considered those positions and issued a Claim Construction Order. A copy of the Claim Construction Order is attached at **Exhibit C**. A copy of the Court's associated Memorandum Opinion is attached at **Exhibit D**.

A. The Court's Constructions are not Binding on the Patent Office

For purposes of examination, including reexamination, the terms of the patent claims must be interpreted. During examination, claims are to be given their "broadest reasonable interpretation." MPEP §2111 (citing *In re Hyatt*, 211 F.3d 1367, 1372 (Fed. Cir. 2000)). The interpretation must be consistent with the understanding of those of ordinary skill in the relevant art. MPEP, §2111 (citing *In re Cortright*, 165 F.3d 1353, 1359 (Fed. Cir. 1999)).

Because of the different standards employed by the district courts and the Patent Office in construing claims, the Delaware District Court's constructions are in no way binding on the Patent Office. *See* MPEP §2286 and *In re Zletz*, 893 F.2d 319, 322 (Fed. Cir. 1989) (manner of claim interpretation that is used by courts in litigation is not the manner of claim interpretation that is applicable during prosecution of a pending application before the PTO). Accordingly, the Examiner is not bound by the Court's Claim Construction Order.

B. Construction of Specific Terms From the Claims of the '876 Patent

The construction of six limitations of the referenced claims of the '876 patent are important in evaluating the invalidity of the '876 patent: "frequency jittering"; "coupled"; "primary voltage"; "secondary voltage"; "combining"; and "supplemental voltage". The construction of each of these six limitations is considered below.

1. "frequency jittering"

In Claim 1 of the '876 Patent, the term "frequency jittering" appears only in the

preamble, and therefore should not be considered a claim limitation. "The preamble of a claim does not limit the scope of the claim when it merely states a purpose or intended use of the invention." *In re Paulsen*, 30 F.3d 1475, 1479 (Fed. Cir. 1994). Here, Claim 1 of the '876 Patent recites "a digital **frequency jittering** circuit for varying the switching frequency of the power supply...." After stating this intended use, the claim describes the required elements (an oscillator, a digital to analog converter, and a counter). *See* '876 Patent, Claim 1. At no time, however, does the body of the claim refer to the "frequency jitter circuit" mentioned in the preamble. Since the preamble does not give "life, meaning or vitality" to the claim, it is not a limitation and need not be construed. *See Intirtool, Ltd. v. Texar Corp.*, 369 F.3d 1289, 1296 (Fed. Cir. 2004).

If "frequency jittering" does need to be construed, however, it should be construed as "varying the frequency of operation of the pulse width modulated switch by varying the oscillation frequency of the oscillator." The '876 specification incorporates by reference the specification of Power Integrations' U.S. Patent No. 6,107,851 ("the '851 patent"). **Exhibit F**, 6:6-12. The term "frequency jitter" is expressly defined in the specification of the '851 Patent:

> Varying the frequency of operation of the pulse width modulated switch by varying the oscillation frequency of the oscillator is referred to as frequency jitter.

'851 Patent, 3:28-30. Because the specification of the '851 patent is incorporated by reference into the specification of the '876 patent, the definition of "frequency jitter" is part of the intrinsic evidence. *Telemac Cellular Corp. v. Topp Telecom, Inc.*, 247 F.3d 1316 (Fed. Cir. 2001) ("When a document is 'incorporated by reference' into a host document, such as a patent, the referenced document becomes effectively part of the host document as if it were explicitly contained therein."). Thus, "frequency jittering" should mean "varying the frequency of operation of the pulse width modulated switch by varying the oscillation frequency of the oscillator."

The Court construed "frequency jittering" to mean "varying the switching frequency of a switch mode power supply about a target frequency in order to reduce electromagnetic

interference." **Ex. C.** While varying the switching frequency around a target frequency may be a characteristic of the preferred embodiment, the Court's definition of "frequency jittering" is narrower than what is required by MPEP §2111.

2. "coupled"

The term "coupled" is found in Claims 1, 3, 5, 7, 21-24, 26-28, 30-32. Two circuits are "coupled" when they are configured such that "signals pass from one to the other." This is the ordinary meaning of the term and is supported by the intrinsic evidence. The '876 patent refers to elements that are "magnetically coupled" and does not require a direct connection between circuit elements. **Ex. A,** 8:5-7 ("A secondary winding 922 is **magnetically coupled** in series **across a primary winding of a transformer 920**."). Thus, circuit elements can be coupled together even if there are additional, intermediary elements so long as signals pass from one to the other.

The Court construed "coupled" as follows: "two circuits are coupled when they are connected such that voltage, current or control signals pass from one to another." **Ex. C.** This definition adds limitations from the preferred embodiment that make the Court's construction narrower than what is required by MPEP §2111. Importantly, the Court noted that its construction of "coupled" does not require that two circuit elements be directly connected. "However, the Court's construction of the term 'coupled' should not be read to imply or necessitate a direct connection, as ***the Court does not read the patent to require a direct connection or to preclude the use of intermediate circuit elements***." **Ex. D.** Thus, even under the Court's construction, circuit elements can be coupled together even if there are additional, intermediary circuit elements.

3. "primary voltage"

The Court's construction of "primary voltage" is "base or initial voltage." **Ex. C.**

4. **"secondary voltage"**

The Court construed "secondary voltage" as "a subsequent or additional voltage". **Ex. C.**

5. **"combining"**

The Court construed "combining" to mean "adding together." **Ex. C.**

6. **"supplemental voltage"**

The Court construed "supplemental voltage" to mean "a voltage in addition to the primary voltage." **Ex. C.**

VI. STATEMENT OF COMPLIANCE WITH 37 C.F.R. § 1.510(b)(5)

Fairchild certifies that, pursuant to 37 C.F.R. 1.510(b)(5), it has served a copy of this request by mailing such copy Express Mail postage prepaid to the attorney of record for the patentee at the following address, which is the current address obtained from the PTO attorney database:

BLAKELEY, SOKOLOFF, TAYLOR, ZAFMAN LLP.
12400 Wilshire Boulevard, Seventh Floor
Los Angeles, CA 90025

A courtesy copy of this request was also served on litigation counsel for Power Integrations by mailing such copy Express Mail postage prepaid to the following address:

Frank E. Scherkenbach
FISH & RICHARDSON, P.C.
225 Franklin Street
Boston, MA 02110-2804

VII. CONCLUSION

The Requestor believes that the above analysis indicates that the prior art attached hereto which was not considered previously by the Examiner, invalidates Claims 1, 17, 18, and 19 of

the '876 patent under 35 U.S.C. § 102 or § 103. At a minimum, it is believed that Martin, Habetler, and Wang raise a substantial new question of patentability, thereby justifying commencement of an *ex parte* reexamination proceeding. Accordingly, the Requestor respectfully requests that the Commissioner establish a reexamination proceeding and give due consideration to the prior art and admissions discussed above.

Dated: November 9, 2006

Respectfully submitted,

Sanjeet K. Dutta
Reg. No. 46,145

OHS West:260080321.10

71338 U.S. PTO
11/09/06

IN THE UNITED STATES DISTRICT COURT
FOR THE DISTRICT OF DELAWARE

71338 U.S. PTO
90008326
11/09/06

POWER INTEGRATIONS, INC., a Delaware corporation,

Plaintiff,

v.

FAIRCHILD SEMICONDUCTOR INTERNATIONAL, INC., a Delaware corporation, and FAIRCHILD SEMICONDUCTOR CORPORATION, a Delaware corporation,

Defendants.

C.A. No. 04-1371

CERTIFICATE OF SERVICE

I, Rita Hernandez, hereby certify that on November 9, 2006, true and correct copies of the following document were served on the following counsel of record at the addresses and in the manner indicated:

1. **REQUEST FOR EX PARTE REEXAMINATION TRANSMITTAL FORM 1465**
2. **PTO-1449 AND REFERENCES CITED THEREON**
3. **REQUEST FOR EX PARTE REEXAMINATION OF U.S. PATENT NO. 6,249,876 ATTACHMENT TO FORM 1465**
4. **CERTIFICATE OF SERVICE**

I hereby certify that the attached associated documents are being deposited with the United States Postal Service on this date in an envelope as "Express Mail Post Office to Addressee" addressed to the following:

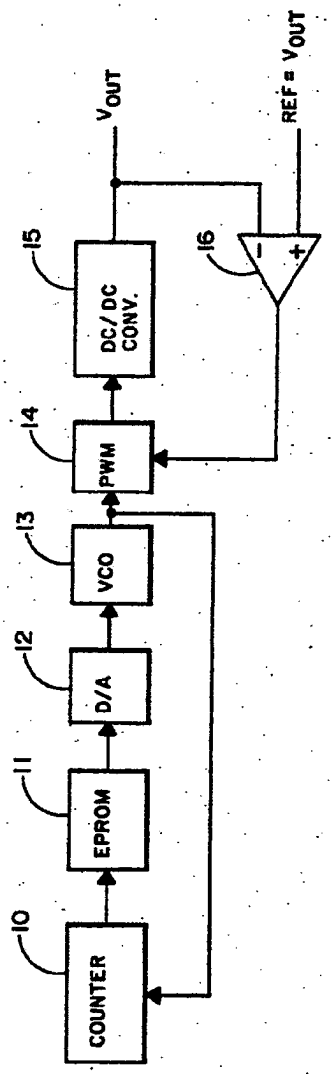
Blakeley, Sokoloff, Taylor, Zafman LLP
12400 Wilshire Boulevard,
Seventh Floor
Los Angeles, CA 90025

Frank E. Scherkenbach
Fish & Richardson P.C.
225 Franklin Street
Boston, MA 02110-2804

Date of Mailing: November 9, 2006

Rita Hernandez

EXHIBIT 11
(USP 4,638,417)


V_{OUT}
REF = V_{OUT}
15
16
DC/DC CONV.
14
PWM
13
VCO
12
D/A
11
EPROM
10
COUNTER
-
+

United States Patent [19]

Martin, Jr. et al.

[11] **Patent Number: 4,638,417**

[45] **Date of Patent: Jan. 20, 1987**

[54] **POWER DENSITY SPECTRUM CONTROLLER**

[75] Inventors: **Hubert C. Martin, Jr., Sandy; Gene D. Hitler; David W. Parsley, both of Salt Lake City, all of Utah**

[73] Assignee: **Sperry Corporation, Blue Bell, Pa.**

[21] Appl. No.: **766,186**

[22] Filed: **Aug. 16, 1985**

[51] **Int. Cl.**[4] **H02M 1/12**

[52] **U.S. Cl.** **363/41; 375/1**

[58] **Field of Search** 363/41, 97; 375/1

[56] **References Cited**

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4,383,323	5/1983	Timor	375/1
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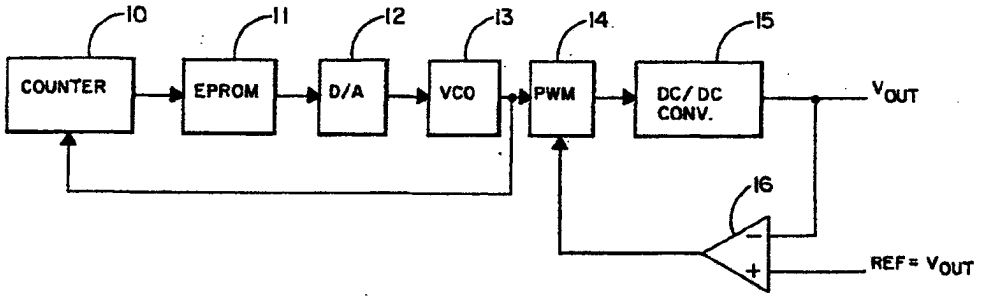
[57] **ABSTRACT**

A power density spectrum controller circuit which incorporates a programming element in conjunction with a voltage controlled oscillator and which uses spread spectrum techniques to provide a relatively clean output signal having little or no ripple, little or no noise and little or no signature while having a minimum output filtering requirement.

11 Claims, 1 Drawing Figure



POWER DENSITY SPECTRUM CONTROLLER

BACKGROUND

1. Field of the Invention

This invention is directed to power supplies, in general, and to a power supply or power conditioner which is used to drive a frequency source and which has little or no adverse effect on the output signal produced by the frequency source, in particular.

2. Prior Art

There are many circuits known in the art which are used for providing power and/or frequency signals. These circuits are usually referred to as power sources, power supplies, frequency sources and the like. Unfortunately, most of these circuits produce an output signal which has ripple, noise, a signature, or some combination thereof thereon. Ripple and noise as well known signal characteristics which are usually addressed by applying further filtration to the output of the circuit. However, the additional filtration usually results in attenuation of the signal, additional cost of the circuit and other well known shortcomings.

In a similar fashion, many power supplies generate a "signature" which is a signal pattern which is unique to the power supply and identifies same much in the nature of a fingerprint. This is not a significant problem in most ordinary usages (except for the fact that it creates ripple and noise). However, in the case of many secure usages, this signature signal can be used to identify a particular source. For example, in military applications or other applications which use encrypted signals or secure operations, it frequently occurs that a source of signals seek to remain anonymous or unidentifiable. However, in many instances, the source can be identified and located by means of appropriate spectrum analyzing which interprets the signal and discovers the signature for the power supply. By thus identifying the signature, the source can be identified despite any covert activities which are otherwise undertaken.

Thus, it is highly desirable to provide a suitable electronic circuit which can be used for removing various undesirable signals at the output of a power supply circuit without the necessity for the large scale filtration devices.

SUMMARY OF THE INVENTION

This invention relates to a circuit which, by programming the input to a voltage controlled oscillator, maintains the average power of a large number of operating frequencies of the circuit within the dynamic range of the switching mode of the power supply. The programming includes a psuedo-random code in a storage medium. The circuit uses spread spectrum techniques to reduce noise, ripple and signature on the output signal. The technique herein reduces the amount of filtering requirements at the output of the circuit.

BRIEF DESCRIPTION OF THE DRAWINGS

The sole FIGURE is a schematic block diagram of the circuit of the instant invention.

DESCRIPTION OF THE PREFERRED EMBODIMENT

Referring now to the sole FIGURE, there is shown a circuit which reduces electromagnetic interference (EMI) by frequency modulation of power converters.

In the instant circuit, the DC-to-DC converter 15 is provided. This converter produces the output signal V_{OUT} which is, of course, the output signal produced by the power conditioner.

A portion of the output signal is also returned to the comparator 16 where it is compared against the reference signal REF. The reference signal is applied to the positive (+) terminal of the comparator 16 from any suitable reference source such as 5 V DC or the like. The output of the comparator 16, viz., the comparison of the output signal V_{OUT} and the reference signal REF is supplied to the pulse width modulator 14. The signal supplied to the pulse width modulator controls the duty ratio of the PWM 14 to regulate the DC/DC converter 15 output voltage V_{OUT}.

The modulator 14 is connected to receive a signal from the voltage controlled oscillator 13. The modulator 14 is operative to vary the duty ratio of the signal which is produced by the VCO 13.

The output signal from the VCO 13 is also fed back to counter 10 which can be any suitable counter of any prescribed length. The output of the counter 10 is connected to the input of EPROM 11 which can be any suitable kind of storage device. In the preferred embodiment, the EPROM is suggested as a preferred method and apparatus for storing information. However, any suitable kind of ROM is believed to be appropriate. The storage mechanism or ROM 11 is used to store a pseudo-random (PR) code therein. Consequently, when counter 10 produces an output signal, it selectively steps the PROM (or ROM) through its addressing routine in order to select the contents of a particular address.

The contents of the PROM 11 are stored in digital form. These digital signals are supplied to the digital-to-analog converter 12. The D/A converter 12 supplies an analog signal to the VCO 13. The output of the VCO 13 is supplied to the modulator 14 as described above and returned to counter 10.

Thus, as the output signal produced by VCO 13 varies in frequency, the counter 10 is caused to count at different rates. With counter 10 counting at different rates the EPROM 11 is stepped or addressed at different rates. The content of the PROM are, a noted, a pseudo random code in digital form. The digital signal from the PROM 11 is converted to an analog signal by D/A converter 12. This analog signal is then applied to VCO 13 which produces an oscillating signal which has a frequency which is representative of the amplitude of the analog signal. The VCO output signal is supplied to the pulse width modulator 14 which varies the chopping rate of the signal from the VCO 13 while maintaining a constant duty ratio. In particular, the modulator 14 operates to provide a fixed duty ratio over a wide range of operating frequencies of the VCO 13.

The DC-to-DC converter provides an output which is a function of duty ratio and not frequency. This technique produces independent means of varying the operating frequency in a psuedo random pattern without changing the output voltage and so forth.

In the preferred embodiment, the circuit involved uses a chopping power supply with a DC-to-DC converter 15 which chops at a rate of greater than 1 MHz. This circuit then operates as a generator with pseudo random chopping frequency to provide a spread spectrum operation in order to spread the ripple over a relatively large bandwidth from 750 KHz to 1.5 MHz.

As the output signal V_{OUT} varies, it is mixed with the reference signal REF which alters the operation of the

pulsewidth modulator. The signal supplied to the pulsewidth modulator 14 by the VCO 13 is also varying on a pseudo random basis, as described above. The pseudo-randon operation of the circuit which supplies the analog signal to the pulsewidth modulator 14 is also described. Consequently, a pseudo-random frequency signal with a constant amplitude is supplied to the modulator which then produces a randomly varying ripple signal from the circuit. As a consequence, the output signal has been spread over a very wide spectrum.

Thus, there has been shown and described a unique power conditioning circuit which uses spread spectrum techniques as well as frequency hopping techniques to reduce ripple, noise and signature from an output signal. This is accomplished by preventing periodic noise from appearing in the output signal. More importantly, this operation is achieved without the addition of extensive filtration circuits at the output of the circuit involved. Thus, electromagnetic interference is greatly reduced at the output signal of this system.

This operation is especially useful in communication systems and permits smaller, lighter, more efficient power supplies at high frequencies. It is especially useful in areas where advantages are obtained when output filtration is minimized.

In addition to communication systems, this type of power supply system can be very useful in many semiconductor applications wherein the semiconductor devices use lower and lower voltage and/or power. That is, by reducing the noise and ripple on the input signals, the operation of such semiconductor devices which have low voltage requirements, (e.g. 2.5 volts) is highly advantageous.

This circuit is highly advantageous in removal of unwanted signals at the output. Moreover, there is a decided improvement on the upper limits of the frequencies at which circuits of this type can operate without the unwanted signals at the output.

In the preferred embodiment, specific components and arrangements are shown and described. However, those skilled in the art may conceive of different components in the overall circuit scheme or a different arrangement of the components as shown. However, any such modifications to the circuit which fall within the purview of this description are intended to be included therein as well. Clearly, the description is not intended to be limitative of the invention but is, rather, illustrative only. The scope of the invention is not limited by this description but is limited only by the claims appended hereto.

We claim:

1. A signal control circuit which produces an output signal having little or no ripple, noise or signature, comprising,

pulse width modulator means,

voltage controlled oscillator (VCO) means connected to supply signals to the input of said pulse width modulator means,

coded means connected to supply signals to said VCO means and including storage means for storing a prescribed signal pattern which is selectively supplied to said VCO means,

control means comprising counter means for supplying signals to said storage means thereby to selectively address said storage means to supply said signal pattern to said VCO means,

signal converter means connected to the output of said pulse width modulator means and operative to produce an output signal which is a function of the duty ratio of the pulse width modulator, and

comparator means connected to the output of said signal converter means and operative to compare said output signal with a reference signal and to supply a control signal to said pulse width modulator to control the duty ratio thereof.

2. The circuit recited in claim 1 wherein,

said coded means comprises ROM means connected to said counter means such that the output signal from said counter means comprises an address signal for said ROM means.

3. The circuit recited in claim 1 including,

second signal converter means connected between said coded means and said VCO means.

4. The circuit recited in claim 3 wherein,

said coded means provides digital signals, and

said second signal converter means comprises digital-to-analog (D/A) converter means.

5. The circuit recited in claim 1 wherein,

feedback means connected around said signal producing means whereby the output of said signal producing means is fed back to the input thereof.

6. The circuit recited in claim 1 including,

reference signal source means connected to an input of said comparator means to provide a reference signal to compare with said output signal.

7. The circuit recited in claim 2 wherein,

said ROM means comprises an EPROM.

8. The circuit recited in claim 1 wherein,

said signal pattern comprises a pseudo-random code.

9. The circuit recited in claim 1 wherein,

said signal control circuit comprises a power amplifier.

10. The circuit recited in claim 1 wherein,

said signal converter means produces an output signal which is a function of the input signal supplied thereto.

11. The circuit recited in claim 10 wherein,

said signal converter comprises a DC-to-DC converter.

* * * * *

EXHIBIT 12
(Programmed Pulsewidth Modulated Waveforms for Electromagnetic Interference Mitigation in DC-DC Converters)

Programmed Pulsewidth Modulated Waveforms for Electromagnetic Interference Mitigation in DC–DC Converters

Andrew C. Wang and Seth R. Sanders

Abstract—**The regular switching action of a pulsewidth modulated (PWM) circuit generates conducted and radiated electromagnetic interference (EMI), and may also generate acoustical disturbances. Programmed pulsewidth modulation techniques have been applied using various methods to control harmonics inherent in switched power circuits. In this paper, a method to generate an optimal programmed switching waveform for a dc–dc converter is presented. This switching waveform is optimized to reduce the amplitude of harmonic peaks in the EMI generated by the converter. Experimental results, a brief discussion of sensitivity, and a practical implementation of a circuit to generate the PWM waveform are given.**

I. Introduction

THIS paper investigates methods for reducing unwanted spectral components of circuit waveforms in PWM power conversion circuits. Fig. 1(a) shows a portion of a 50% duty cycle square wave and its spectral components. In many applications, the concentration of power at discrete frequencies is undesirable. For instance, it may be necessary to reduce an annoying audible tone, or an electromagnetic interference (EMI) specification may be satisfied by reducing peak harmonic components, or one might be able to reduce the size and weight of filter elements by reducing peak spectral components.

The main approaches considered in this paper rely on the fact that it is possible to operate a PWM type power circuit with a time-varying switching frequency provided the average duty cycle is not disturbed. We employ a programmed waveform that repeats itself after K cycles. A typical programmed PWM waveform and its spectrum is illustrated in Fig. 1(b). Compared to regular PWM, the programmed PWM has a harmonic spacing that is smaller by a factor of K. The extra available harmonic frequencies are used to spread out the spectral energy of a given circuit waveform.

Section II of the paper reviews the main techniques considered in the literature. Sections III and IV illustrate the application of these methods in the context of a dc-dc converter. Experimental results are presented in Section V, and their sensitivity to parameter variation is discussed in Section VI. An implementation is given in Section VII.

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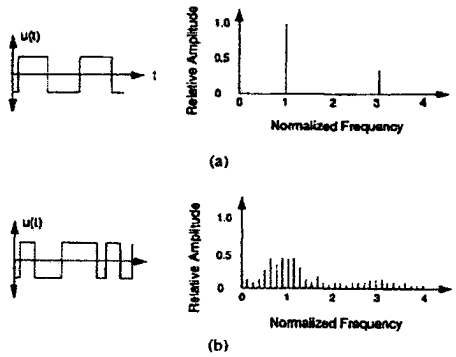

Fig. 1. Typical PWM waveforms and associated spectra. (a) Regular PWM. (b) Programmed PWM.

II. Review of Existing Techniques for Harmonic Control

The first method of harmonic control to be discussed can be termed programmed pulsewidth modulation. In programmed PWM, a precomputed set of turn-on and turn-off times (or angles) is stored in a memory or look-up table, and then accessed periodically by a control circuit. This method can be used to generate steady state waveforms and therefore has found applications in inverters and dc-dc converters. Some of the earliest work in harmonic control is due to Turnbull [1]. In the context of an inverter, Turnbull calculated the necessary turn-on and turn-off angles to generate a modified square-wave that had no third or fifth harmonic components. Waveform symmetry properties, namely quarter-cycle even symmetry and half-cycle odd symmetry, were maintained to assure that no even harmonics were generated. Reference [1] also noted that certain three-phase connections blocked triple-n (i.e., third, sixth, etc.) harmonic components, and that it was advantageous in these three-phase connections to select the switching angles to null the fifth and seventh harmonics. The later work of Patel and Hoft [2],[3] generalized the results of Turnbull by allowing, in principle, an arbitrary number of turn-on and turn-off transitions per cycle. The waveforms in [2],[3] contained the necessary quarter- and half-cycle symmetries to avoid the introduction of even harmonics. Reference [2] applied a Newton-type numerical algorithm to

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determine the switching angles that resulted in a prescribed set of harmonics being nulled. Reference [3] extended the method of [2] to specify the amplitude of the fundamental as well as nulling a given set of harmonic components. The paper [5] of Goodarzi and Hoft took a similar approach to the harmonic control problem, but minimized a weighted square sum of certain harmonic components with the constraint that the amplitude of the fundamental attained a constant value. This method also relied on a Newton-type numerical scheme for determining the optimal switching angles. A summary of the programmed PWM methods is given in the paper [4] of Enjeti *et al.*

A second approach to harmonic control involves randomized switching, and has been quite successfully applied by a number of researchers. It is of interest that with the randomized type switching, one is not restricted to a set of precomputed waveforms. An example of this is the recent work of Tanaka *et al.* [6]. The focus in [6] was not on the lower harmonics of the fundamental switching frequency, but on much higher frequency noise generated by the turn-on and turn-off process in a given dc-dc converter. This work relied on the spectral characterization of the noise generated by each type of transition (turn-on or turn-off), as studied in the authors' earlier papers [7],[8]. Using characterizations of the relevant transitions as impulse responses, the authors were able to deduce the form of the spectrum of a periodic sequence of turn-on and turn-off transitions. Reference [6] then added a random timing component to the switching sequence in an attempt to spread high frequency harmonic components. The random timing component introduced in [6] evidently corresponds to a frequency (or phase) modulation with white noise. The experimental results reported in [6] state that high frequency spectral components are reduced in magnitude by a factor of approximately two or three via the spectral spreading.

A very effective use of randomized switching has been reported in [9]. Reference [9] used a scheme very similar to that of [6] to reduce acoustical and electrical noise harmonics in a PWM induction motor drive. The main difference in [9] with respect to [6] is the use of band-limited modulation. In particular, reference [9] relied on Carson's rule for the estimation of spectral bandwidths in wideband frequency modulation. The result was an effective shaping of the spectrum to reduce harmonic peaks. A reduction of the peak spectral components by a factor of approximately five was obtained. The paper [9] noted that the randomized switching could be implemented by generating the switch times in an on-line manner using a random number generator and shaping filter or by storing a long sequence (a few seconds in length) of switching periods.

Another implementation of randomized switching is in the paper of Legowski *et al.* [10] where a random PWM technique is used to generate a high-quality sine wave inverter output. One apparent drawback of the scheme of [10] is the necessity of increasing the average switching frequency by a large factor. In [14], formulas are presented for estimating the power spectra of several randomized switching schemes. The formulas are verified using Monte-Carlo simulations.

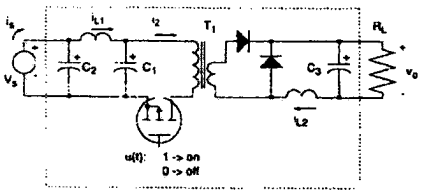

Fig. 2. Forward converter power path frequency, kHz

III. Background

As an example of a circuit where the use of programmed PWM can be compared with regular PWM, we consider the forward converter of Fig. 2. To design a programmed switching sequence for this converter, it is first necessary to choose a circuit waveform that we wish to optimize using the programmed PWM. For example, we may wish to modify the spectrum of the input current $i_s(t)$. Possible criteria can be based on the FCC conducted EMI regulations. Our approach for meeting the FCC regulations is to spread out the spectral energy in $i_s(t)$ to reduce the overall peak amplitude in the spectrum. We accomplish this by first defining a desired spectral envelope for the selected waveform. Then, we apply a constrained min-max optimization algorithm on the switching instants to make the spectrum of the waveform fit under this envelope.

A. Circuit Waveforms

We need to define the programmed PWM waveform, and determine how it affects the waveforms occurring in the converter. For steady-state operation, most of the voltage and current waveforms occurring in the converter can be approximated as filtered versions of the PWM waveform which drives the switch. Some of the waveforms may also contain significant switching transients, which we also consider. Equations for circuit waveforms are given in Section IV.

The programmed PWM waveform is similar to the regular PWM waveform except that the turn-on and turn-off times are varied. Two possible parameterizations for the programmed PWM are given in Fig. 3. In each case, the overall period is multiplied by an integer K so that it contains K subperiods. Subperiod k has length T_k and duty cycle D_k. For the "triangle" parameterization shown in Fig. 3, we require that the "on" time of duration $T_k D_k$ within subperiod k must be centered within this subperiod. Although this restricts the range of admissable PWM waveforms, it is easier to implement in practice using a programmable triangle wave, as will be explained in Section VII. The "sawtooth" parameterization can be used to generate arbitrary PWM waveforms, but requires a programmable sawtooth wave. We have found from optimizations with both parameterizations that the differences in numerical results are not very significant. Therefore, we will limit our discussion below to the triangle parameterization waveform, noting that results obtained with the sawtooth parameterization are similar.

B. Optimization Criteria

The design goal in our experimental work is the suppression of conducted EMI. Conducted EMI onto distribution lines is

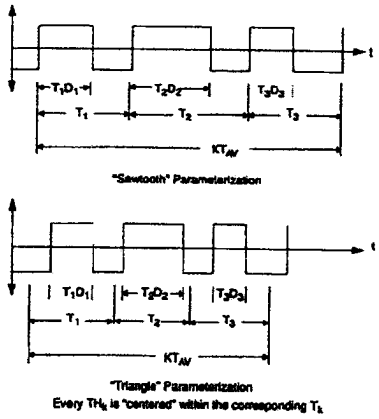

Fig. 3. Possible parameterizations of PWM waveform (for $K = 3$).

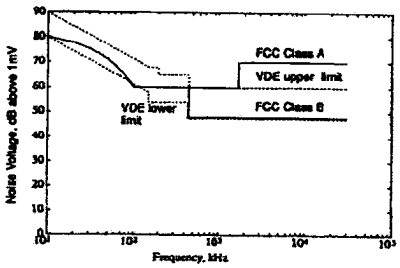

Fig. 4. FCC and VDE conducted EMI limits.

detrimental and therefore regulated by various agencies, such as the FCC and VDE. The noise is generally measured with the use of a line impedance stabilization network (LISN) which presents a specified impedance to the device under test and has a voltage output for noise level measurement. The FCC specified LISN presents an impedance that is almost constant above 1 MHz and that drops off slightly below 1 MHz, as given in [12]. With this LISN, typical FCC conducted noise limits [13] are shown in Fig. 4. Similar VDE regulations are also shown. A reasonable optimization goal in light of these regulations is to reduce the peak harmonic amplitude, weighted by the applicable curve in Fig. 4.

Another possible goal is the reduction of radiated EMI, which is caused by high frequency components ofswitching transients. After implementing appropriate physical layout by elimination of large area current loops, and the use of shielding, a programmed PWM waveform can help spread the spectrum to reduce peak harmonics in the electromagnetic radiation. We could attempt to make the reshaped radiation spectrum fit under the curve of the FCC limits on electromagnetic radiation, shown in Fig. 5.

C. Programmed Waveform Constraints

For our purposes, the programmed PWM waveform must meet several constraints, both in the time and frequency domains.

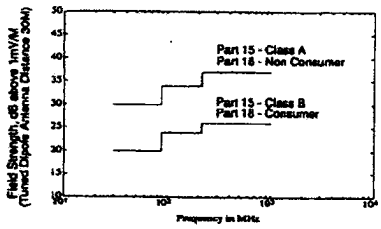

Fig. 5. FCC radiation limits, U.S. code Parts 15 and 18, Title 47.

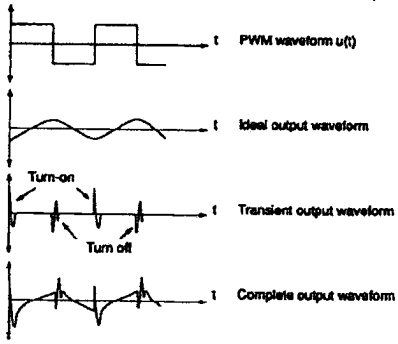

Fig. 6. Output waveform composition.

C1) The programmed PWM waveform must have the same average period and the same average duty cycle as the original PWM waveform.

C2) Every pulse must be longer than some minimal width, due to semiconductor switch constraints.

C3) For control purposes, the average duty cycle of the programmed waveform must be continuously variable via a control signal.

C4) The lowest frequency harmonic in the programmed PWM waveform must be well above the bandwidth f_p of the control loop. Otherwise, the control loop will modify the programmed PWM waveform, even in the steady state.

Constraint ($C4$) limits the maximum number of subperiods in the programmed waveform before it repeats. Let f_o be the original switching frequency, and K be the (integral) number of subperiods in the programmed waveform. Then, K must be less than (f_o/f_p).

IV. Generation of a Programmed Switching Waveform

In this section, we formulate equations necessary for the optimization procedure. We call the waveform that we are trying to optimize (such as the current $i_s(t)$ drawn from the source) the "output waveform" of our optimization. It is the sum of an "ideal" waveform and a "transient" waveform as shown in Fig. 6. The ideal portion of the output waveform is generated by assuming there are no parasitics so that the circuit behaves as if it were ideal. The transient waveform contains only the turn-on and turn-off transient components, which are due to circuit parasitics.

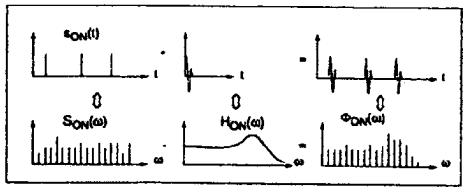

Fig. 7. Calculation of turn-on noise portion of output waveform, and corresponding spectra.

The Fourier series coefficients of the output waveform are denoted $\phi[n]$. In the optimization, we first generate an equation for the relationship between the programmed waveform parameters $(T_1, T_2, \ldots, T_{K-1}, D_1, \ldots, D_{K-1})$ and $\phi[n]$. Next, we weight $\phi[n]$ with a simple function to specify an optimization target for the relative harmonic amplitudes. Finally, the constraints are implemented, and then the optimization performed.

We denote the average length of the subperiods in the programmed PWM by T_{AV}, which must be equal to the period of the original PWM waveform, due to constraint $(C1)$. Similarly, again by $(C1)$, the average duty cycle D_o of the programmed PWM must be the same as that of the regular PWM. In the additional definitions below, functions of time are noted in lower case. Their Fourier series representations are also in lower case, as bracketed functions of n. Fourier transforms are in upper case.

$s_{ON}(t)$	Function containing a unit impulse at each turn-on instant
$s_{OFF}(t)$	Function containing a unit impulse at each turn-on instant
$u(t)$	PWM switching waveform
$H_{ON}(\omega)$	Fourier transform of turn-on transient
$H_{OFF}(\omega)$	Fourier transform of turn-off transient
$\zeta(t)$	Signum function
$H_1(\omega)$	Transfer function from PWM switching waveform to output waveform
$\phi_{ID}[n]$	Fourier series coefficients of ideal output waveform
$\phi_{TR}[n]$	Fourier series coefficients of turn-on and turn-off transient portion of output waveform
$\phi[n]$	Fourier series coefficients of complete output waveform

The period of the programmed PWM waveform is KT_{AV}, therefore, the lowest programmed PWM harmonic occurs at $\omega_0 = (2\pi)/(KT_{AV})$. Due to constraint $(C1)$, the last subperiod and its duty cycle are given by:

$$T_K = KT_{AV} - \sum_{k=1}^{K-1} T_k \tag{1}$$

$$D_L = \frac{KT_{AV}D_0 - \sum_{k=1}^{K-1} T_k D_k}{T_k} \tag{2}$$

We use the functions $s_{ON}(t)$ and $s_{OFF}(t)$ as a starting point for our calculation of the output waveform's Fourier series representation. The functions $s_{ON}(t)$ and $s_{OFF}(t)$ are

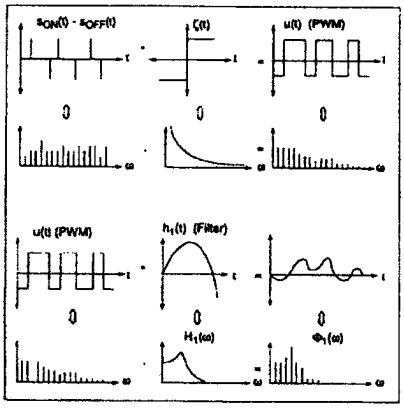

Fig. 8. Calculation of ideal portion of output waveform and corresponding spectra.

defined as waveforms with impulses at the PWM waveform turn-on times and turn-off times, respectively. Hence, they and their corresponding Fourier series representations $s_{ON}[n]$ and $s_{OFF}[n]$ are functions of $T_1, T_2, \ldots, T_K$ and $D_1, D_2, \ldots, D_K$:

$$s_{ON}(t) = \sum_{m=-\infty}^{\infty} \sum_{k=1}^{K} \delta\left(t - \left(T_1 + T_2 + \ldots + \frac{T_k}{2} - \frac{D_k}{2} - mKT_{AV}\right)\right) \tag{3}$$

$$s_{OFF}(t) = \sum_{m=-\infty}^{\infty} \sum_{k=1}^{K} \delta\left(t - \left(T_1 + T_2 + \ldots + \frac{T_k}{2} + \frac{D_k}{2} - mKT_{AV}\right)\right) \tag{4}$$

$$s_{ON}[n] = \sum_{k=1}^{K} e^{(-jn\omega_0)\left(T_1+T_2+\ldots+\frac{T_k}{2}-\frac{D_k}{2}\right)} \tag{5}$$

$$s_{OFF}[n] = \sum_{k=1}^{K} e^{(-jn\omega_0)\left(T_1+T_2+\ldots+\frac{T_k}{2}+\frac{D_k}{2}\right)} \tag{6}$$

Now, the Fourier series coefficients $\phi_{TR}[n]$ of a waveform that consists only of the output waveform's turn-on and turn-off transients are easily calculated. We utilize the Fourier transforms of the switching transients in the equations below. An illustration of the calculation for (7) is shown in Fig. 7.

$$\phi_{ON}[n] = s_{ON}[n] \cdot H_{ON}(n\omega_0) \tag{7}$$

$$\phi_{OFF}[n] = s_{OFF}[n] \cdot H_{OFF}(n\omega_0) \tag{8}$$

$$\phi_{TR}[n] = \phi_{ON}[n] + \phi_{OFF}[n] \tag{9}$$

Next, to calculate the Fourier series coefficients $\phi_{ID}[n]$ of the "ideal" portion of the output waveform (without turn-on and turn-off noise), we first generate the PWM waveform $u(t)$ driving the switching element. The ideal output waveform is related to $u(t)$ through a linear, time-invariant (LTI) system, which we characterize by the transfer function $H_1(s)$. The calculation of $\phi_{ID}[n]$ is illustrated in Fig. 8, and equations are

given below:

$$u(t) = (s_{ON}(t) - s_{OFF}(t)) * \zeta(t) \quad (10)$$

$$\phi_{ID}[n] = (s_{ON}[n] - s_{OFF}[n]) \cdot \zeta(nw_0) \cdot H_1(nw_0) \quad n \in \{1, 2, \ldots, \infty\} \quad (11)$$

The Fourier series coefficients of the complete output waveform are obtained in (12), by summing the coefficients of the ideal waveform and the transient waveform. An equivalent form is (13), as required for our optimization algorithm.

$$\phi[n] = \phi_{ID}[n] + \phi_{TR}[n] \quad (12)$$

$$\phi[n] = f_n(T_1, T_2, \ldots, T_{k-1}, D_1, D_2, \ldots, D_{k-1}) \quad (13)$$

To allow for a target spectral envelope that is not flat, we define a weighting function $\Psi[n], n \in \{1, 2, \ldots \infty\}$, where $\Psi[n]$ represents the desired relative amplitude of harmonic n. Then the cost function that we attempt to minimize is (14).

$$J = \max_n \left(\frac{|\phi[n]|}{\Psi[n]}\right) \qquad n \in \{1, 2, \ldots \infty\} \quad (14)$$

Thus, the optimization will attempt to make the amplitudes of the harmonicsfit under an "envelope" in the shape described by $\Psi[n]$.

There are some constraints on the domain of the optimization. From constraint $(C3)$, we have the constraint (15), and from constraint $(C2)$, we obtain (16):

$$\begin{matrix} D_k > D_{\min} \\ D_k < D_{\max} \end{matrix} \qquad k \in \{1, 2, \ldots, K\} \quad (15)$$

$$T_k D_k > T_{\min} \qquad k \in \{1, 2, \ldots, K\} \quad (16)$$

A. Optimization Method

A suitable algorithm for solving the above constrained min-max problem is available in [11]. It is based on the method of steepest descent, but allows us to find minima of the "max" function given in (14), which is nondifferentiable. The main requirement of the algorithm in [11] is that all the component functions which the maximum is taken over be continuously differentiable over the domain of optimization. This requirement is satisfied except at points where at least one of the harmonic amplitudes is equal to zero. If we start at a point where none of the harmonic amplitudes is equal to zero, the optimization proceeds with no difficulties.

Note that J in (14) is computed on each iteration of the optimization algorithm. We need to limit the number of Fourier coefficients used in the computation of J to make the computation tractable. It has been found that for our conducted EMI calculations, where the lowest frequency harmonics were the largest, using $n \in \{1.2, \ldots, 1.25K\}$ allowed the minimization algorithm to converge in a reasonable amount of time for a variety of parameters. All of the results were verified by substituting the resulting optimized T_k and D_k in (14), and checking that the calculated value of J was still valid for large values of n.

Although the min-max algorithm is not guaranteed to find a global minimum, we were able to use it to find useful PWM waveforms. Some optimization weightings gave better results than others in terms of minimizing J, depending on the shape of the weighting. Results are reported in Section V.

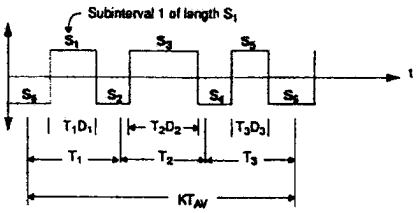

Fig. 9. Definition of subintervals (for K=3).

B. Quantization

In a digital PWM waveform generator, the switching instants of the PWM waveform must be quantized. The step size is equal to the period of the waveform generator's internal clock. For the results in Section V, we used the quantization method described below, which minimizes the largest percentage error in the length of any one "subinterval" of the PWM waveform. A subinterval is defined as the time between two neighboring transitions and is depicted in Fig. 9.

Let $S_m, m \in \{1, 2, \ldots, (2K)\}$ be the calculated subinterval lengths and $\bar{S}_m, m \in \{1, 2, \ldots, (2K)\}$be the quantized subinterval lengths. Quantization requires that:

$$\bar{S}_m = \frac{P_m}{f_i} \quad (17)$$

where P_m is an integer for $m \in \{1, 2, \ldots, (2K)\}$ and f_i is the internal clock frequency of the PWM waveform generator. In our implementation, the constraint on the quantization

$$\sum_{m=1}^{2K} \bar{S}_m = \sum_{m=1}^{2K} S_m \quad (18)$$

was imposed, and the quantization error

$$e = \max_n \left(\left| \frac{\bar{S}_m - S_m}{S_m} \right| \right) \qquad m = \{1, 2, \ldots, 2K\} \quad (19)$$

(19) was minimized. Thus, the largest percentage error in the quantized length of any subinterval was minimized by (19). At the same time, the accuracy of the overall period of the quantized waveform was ensured by (18).

V. Results

For an experimental verification, we used an AT&T model 950A dc-dc forward converter, which is designed for a 48 Vdc input and 5 Vdc output. With a 2.5Ω load, the PWM waveform was a rectangular wave with a 39% duty cycle. To test the programmed PWM, we replaced the gate drive signal in the forward converter with an EPROM based programmable waveform generator. The waveform generator was clocked at 16 MHz, and the programmed PWM transitions occurred only on rising clock edges. In this experiment our interest was in steady-state measurements, and hence the circuit was run open-loop.

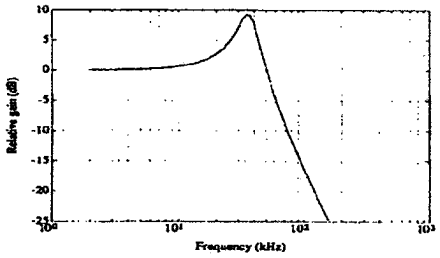

Fig. 10. Transfer function (magnitude) from PWM signal to input current.

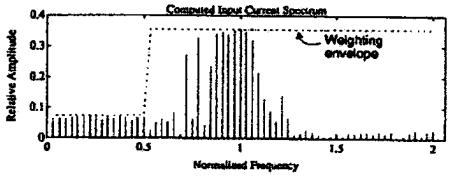

Fig. 11. Optimization result - input current spectrum.

The optimization target was chosen to be the reduction of the amplitude of the largest harmonic in the current waveform drawn by the converter. The essential configuration of the commercial converter's power path, for study of the lower frequency harmonics, is shown in Fig. 2. The relationship between the switching waveform $u(t)$ and the input current $i_1(t)$ in this circuit topology is nonlinear. However, in order to generate the programmed PWM waveform using the process in Section IV, we make the approximation that i_{L2} is constant within each phase of the switch cycle. Then we have:

$$\Phi_1(\omega) = \frac{I_1(\omega)}{U(\omega)} \simeq \frac{I_0}{1 + j\omega R_{L1} C_1 - \omega^2 L_1 C_1} \qquad (20)$$

where R_{L1} is the ac parasitic series resistance associated with L_1 and I_o is a scaling constant. With $L_1 = 6.2uH$, $C_1 = 3.0uF$, and $R_{L1} = 0.1\Omega$ (which is extrapolated from an LC bridge measurement), the magnitude of the transfer function (20) is graphed in Fig. 10.

We found that the input current waveform did not have appreciable switching transients. Therefore, we omitted switching transients from the model used for the optimization.

A. Optimization

The number of subperiods in the programmed PWM waveform to be generated was chosen to be $K = 32$. We set $T_{\min} = 0.1T_{AV}$, $D_{\min} = 0.3$ and $D_{\max} = 0.5$. The spectral weighting was chosen to spread the power of the original first harmonic in the regular PWM to nearby "new" harmonic frequencies in the programmed PWM, and also to minimize the low frequency harmonics in the programmed PWM. It is shown as a dotted line in Fig. 11.

The results of the optimization are also shown in Fig. 11, as vertical bars. Many optimizations were performed with different spectral weightings. In general, attempts at greater suppression of low frequency harmonics caused most of the optimization "effort" to be focused there, and not on making the higher frequency harmonics fit the envelope. It was found that relaxing the requirements on the lower harmonics made the upper harmonics fit the target envelope much more closely.

TABLE I
OPTIMIZATION RESULT — PWM WAVEFORM

k	T	D	k	T	D	k	T	D	k	T	D
1	0.885	0.391	9	0.756	0.413	17	0.865	0.401	25	1.031	0.398
2	0.876	0.389	10	0.848	0.381	18	1.022	0.390	26	0.922	0.389
3	0.842	0.400	11	0.865	0.403	19	1.121	0.382	27	1.005	0.388
4	1.000	0.392	12	1.010	0.386	20	1.024	0.391	28	1.001	0.388
5	1.200	0.386	13	1.065	0.392	21	0.946	0.390	29	1.003	0.389
6	1.260	0.387	14	1.051	0.382	22	0.982	0.398	30	1.021	0.392
7	1.186	0.388	15	0.903	0.400	23	1.203	0.384	31	1.037	0.384
8	0.984	0.383	16	0.904	0.385	24	1.227	0.382	32	0.883	0.400

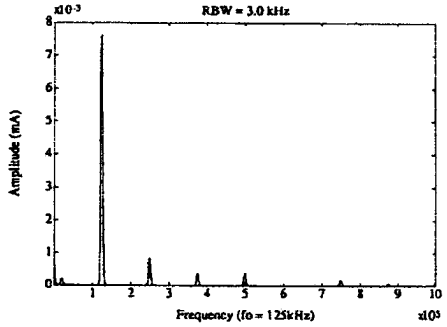

Fig. 12. Measured spectrum of input current, with regular PWM drive (0.001 Hz -1 MHz).

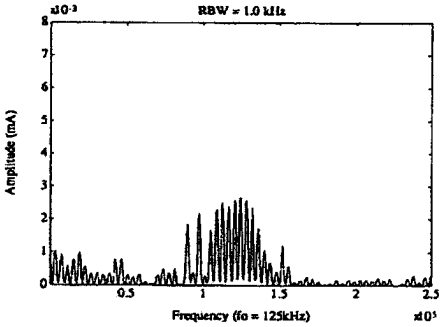

Fig. 13. Measured spectrum of input current, with programmed PWM (0.001 Hz -250 kHz)

B. Experimental measurements

The target envelope in Fig. 11 produced a good compromise between reduction in size of the largest harmonic and the peak-to-peak amplitude of the ripple, which is larger with programmed PWM than with regular PWM. The waveform generated by the optimization with this target envelope is listed in Table I. Before use in our experiment, the waveform was quantized as described in Section IV-B.

Measurements with the converter began with a regular 39% duty cycle PWM waveform driving the switch at the original switching frequency, $f_o = 125$ kHz. The spectrum of the resulting input current waveform (as measured by an HP 4195A network/spectrum analyzer) is shown in Fig. 12. With the programmed PWM waveform, the measured spectrum of

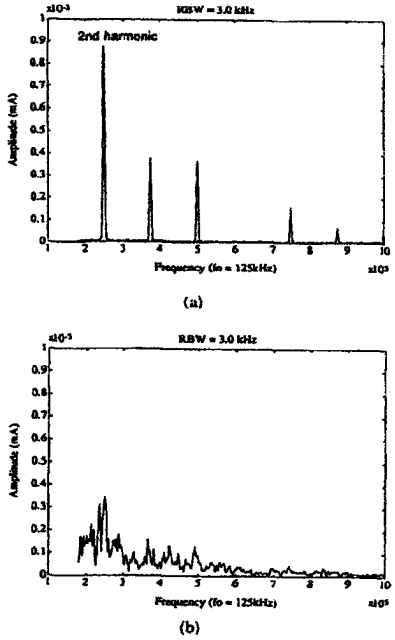

Fig. 14. Measured spectrum of input current, 180 kHz – 1 MHz: (a) Regular PWM. (b) Programmed PWM.

the input current around the original first harmonic became that shown in Fig. 13. Note that the important largest harmonics are very close to those predicted in Fig. 11. Although the lower harmonics are not as well predicted, the power in them is kept very low. The measured peak harmonic amplitude has been reduced from 7.6 to 2.7 mA, or 35% of the original level.

Although the higher frequency harmonics were not considered in the optimization procedure, it is observed that their amplitudes are also reduced by varying degrees and could fit under a smaller envelope. For instance, the amplitude of the second harmonic for regular PWM was 0.85 mA. With programmed PWM, the largest harmonic above 180 kHz is still at 250 kHz, but its amplitude is reduced by 59% to 0.35 mA. Measurements are shown in Fig. 14.

The cost of reducing the size of the peak harmonic includes an increase by 17% of the total power in the harmonics from 1 KHz to 1 MHz. Also, peak-to-peak input current ripple is increased from 28 to 38 mA. In addition, low frequency harmonics are now present, but must be kept above the control circuit's bandwidth for the "optimized" PWM to work.

The results obtained with programmed PWM compare favorably with those reported in [6] for randomized PWM. In [6], it was found that a 15% random deviation in the switching frequency approximately halved the peak level in a converter's switching noise amplitude spectrum (as measured by a spectrum analyzer).

C. Additional optimization results

We have also found that fixing all the D_k's to be equal to the average duty cycle and allowing the optimization algorithm

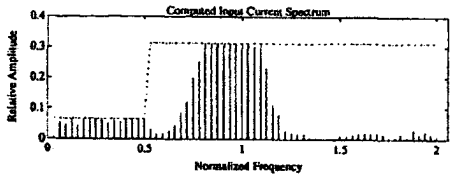

Fig. 15. Optimization result for Dk=0.39, $k \in \{1,2,\ldots,K\}$.

to vary only the T_k's still gave good results, at least in our setup. In fact, with the same parameters as in Section 5.1, but with all of the D_k's fixed at 0.39, the optimization generated a slightly *lower* value of J in (14). The result is shown in Fig. 15, and can be compared to Fig. 11.

This improved result occurred in spite of the additional constraints becausethe optimization algorithm finds local, but not necessarily global minima. Obviously, in Section V-A, a local minima was found. Therefore, it could be useful to try other starting points for the optimization algorithm in order to find better local minima. One might also try other optimization algorithms such as simulated annealing [15].

VI. Sensitivity

Variations in the switching instants of the actual programmed PWM waveform can cause the spectrum of the output waveform to deviate from the design. The effect of variations on an optimized programmed PWM system are more difficult to analyze than on a circuit using regular PWM. This is mainly due to the fact that the cost index in the optimization is described by a nonlinear "max" function, as seen in (14). A particular harmonic's sensitivity to parameter variations at any point can be found from the partial derivative matrix. However, a highly sensitive harmonic may not be a problem, if the weighted amplitude of the harmonic is much lower than that of the largest harmonic. To get some idea of the sensitivity in light of this difficulty, we consider specific types of parameter variations.

A. Sensitivity to quantization

One type of PWM waveform error may be caused by quantization of the switching instants, or imprecision in the actual circuit. As an example to study, we use the numerical results of Section V. Let the actual values generated by the implementation be called $\overline{D}_k, \overline{T}_k, k \in \{1,2,\ldots,K\}$. Assume each of the $\overline{D}_k$ and $\overline{T}_k$are perturbed from their calculated values by a small percentage:

$$\overline{D}_k = D_k(1+\zeta_k) \quad \overline{T}_k = T_k(1+\eta_k) \qquad k \in \{1,2,\ldots,K\} \tag{21}$$

where the ζ_k's and the η_k's are uniformly distributed random variables between -0.01 and +0.01. It was found that this type of perturbation in the PWM waveform increased one of more of the lower frequency harmonics by a large amount. Fig. 16

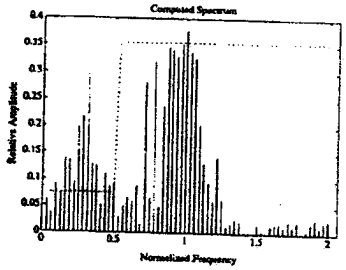

Fig. 16. Programmed PWM spectrum after random perturbation of switching instants.

shows a typical spectrum created by perturbing the results of Section V.

The lower frequency harmonics are affected relatively more than the higher frequency harmonics, mainly due to their nominally small amplitudes. The lower frequency harmonics are nominally small because the target shape of output waveform spectrum was chosen to suppress lower order harmonics. The PWM waveform must have very small low frequency harmonics because it passes through a low pass filter to generate the output waveform, and the low pass filter does little to attenuate these harmonics.

B. Sensitivity to steady-state variations in duty cycle

Another possible deviation in the steady state PWM waveform can be a steady-state deviation in the average duty cycle. An analog control input, which is required for proper regulation, can cause such a deviation. It is impractical to store digital waveform data for all possible average duty cycles. Therefore, Section VII describes an implementation that allows the PWM waveform's average duty cycle to be linearly controlled via an analog control signal. This control signal can cause a change in the output waveform's steady-state spectral distribution.

Control of the average duty cycle with the implementation of Section VII is achieved by adding a fixed amount to each D_k. Let ΔD_{AV} be the change in the average duty cycle that is commanded by the analog control input. Let $\overline{D}_k, k \in \{1, 2, \ldots, K\}$ be the perturbed values of the $D_k, k \in 1, 2 \ldots, k$ generated by the implementation. The PWM waveform generated by the implementation in Section VII is then described by

$$\overline{D}_k = D_k + \Delta D_{AV}. \tag{22}$$

and the previously computed T_k's.

Again, we look at how the results from Section V would be affected. For reference, the spectrum of the original 39% average duty cycle waveform is shown in Fig. 17(b). Fig. 17(a) shows the result of perturbing the calculated 39% duty cycle waveform to a 29% average duty cycle, while Fig. 17(c) is for a perturbation to a 49% duty cycle. Note that the perturbation in the PWM waveform is much greater here than in Section VI-A, but the shape of the spectrum is not affected very much at all.

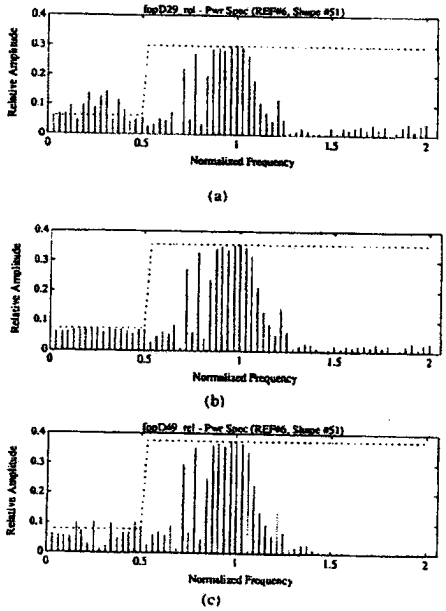

Fig. 17. Computed spectrum of output waveform when (a) average duty cycle is perturbed to 29%. (b) Average duty cycle is not perturbed (39%). (c) Average duty cycle is perturbed to 49%.

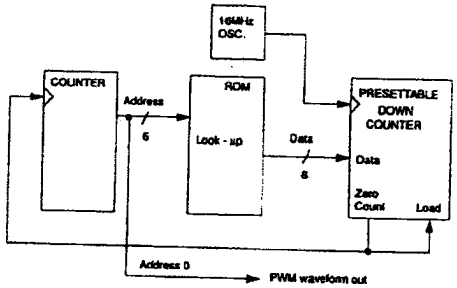

Fig. 18. Simplified PWM generator used in Section V for open-loop measurements.

VII. Implementation

The experimental circuit of Section V was run for open-loop testing only, with the PWM waveform generator depicted in Fig. 18. It lacks an analog section and therefore the duty cycle control input required for feedback control. For a 32 subperiod sequence, 64 bytes of EPROM are required.

A full implementation of the programmed waveform generator with a continuous control input can be based on a programmable triangle waveform generator. Two numbers are stored for every subperiod. One controls the slope of the triangle waveform, and therefore, the length of the subperiod. The other is added to the control signal, and therefore changes the duty ratio of a given subperiod from the average. The

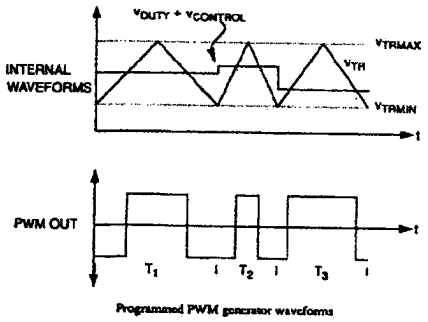

Fig. 19. Programmed PWM generator waveforms

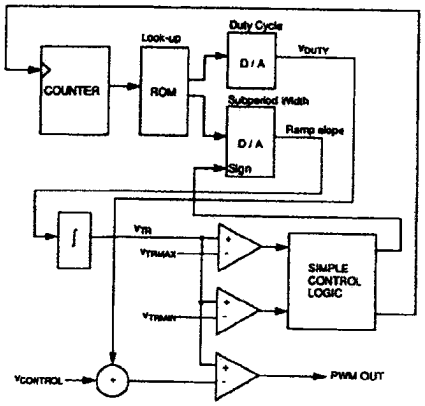

Fig. 20. Programmed PWM generator implementation with control input.

important waveforms and the resulting programmed PWM output are shown in Fig. 19. A block diagram implementation is shown in Fig. 20. Note that the average duty cycle can be varied linearly with the standard duty ratio control signal, marked $v_{CONTROL}$ in Fig. 19. However, the linear range is smaller than with regular PWM in this implementation because of the variation in the D_k's. For the experimental result in Section V, the D_k's only varied from 0.38 to 0.41, so this limitation is not necessarily significant.

VIII. Conclusion

The use of programmed PWM to reduce the magnitude of the peak harmonic in various dc-dc converter circuit waveforms was investigated. A set of equations for the power supply waveforms was presented, along with an optimization method. We found significant reduction possible with a variety of spectral weightings. In the experimental set-up, a reduction in the power of the peak harmonic to approximately one-ninth was achieved in a commercial power converter's input current waveform. Even better results may be possible with other optimization methods, such as simulated annealing.

We also noted that even if we did not allow the D_k's to vary, a reasonable output waveform spectrum could still be achieved, at least in our experimental case. Fixing the D_k's can have additional benefits: the implementation would be simpler and cheaper. Also, the implementation could almost definitely produce a more precise PWM waveform. This would lead to smaller perturbations due to round-off in the switching instants, which cause the output waveform spectrum to change.

Additionally, we found that the spectrum of the input current waveform did not change much when the average duty cycle of the PWM waveform was altered by an analog control input. This is a very useful result for implementation since it implies that only a few optimized waveforms with different average duty cycles need to be stored in ROM.

The relatively large sensitivity of the spectrum to random perturbations (such as round-off) in the switching instants can cause difficulties. However, the quantization technique used in Section V produced experimental results that were very close to the predicted results. Also, choosing the target spectral shape to suppress lower order harmonics can help to prevent them from becoming too large when the PWM waveform is perturbed.

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EXHIBIT 13
(IEEE Standard Dictionary of Electrical and Electronic Terms (1984), p. 204)

An American National Standard

Approved July 20, 1984

IEEE Standard Dictionary of Electrical and Electronics Terms

Third Edition

Library of Congress Catalog Number 84-081283

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August 10, 1984

conductor in one second when the current is maintained constant at one ampere. 210

Coulomb friction (1) (general). A constant velocity-independent force that opposes the relative motion of two surfaces in contact. *See:* **control system, feedback.** 329

(2) (control systems). That occurring between dry (that is unlubricated) surfaces. *Note:* It is usually idealized as a constant force whose sign is such as to cause the force to oppose the relative motion of the rubbing elements. *Syn.:* **dry friction.** *See:* **stiction.** 56

Coulomb's law (electrostatic attraction). The force of repulsion between two like charges of electricity concentrated at two points in an isotropic medium is proportional to the product of their magnitudes and inversely proportional to the square of the distance between them and to the dielectric constant of the medium. *Note:* The force between unlike charges is an attraction. 210

coulometer (voltameter). An electrolytic cell arranged for the measurement of a quantity of electricity by the chemical action produced. *See:* **electricity meter (meter).** 328

count (radiation counters). A single response of the counting system. *See:* **gas-filled radiation-counter tubes; scintillation counter; tube count.** 125, 190, 117, 96

count-down (transponder). The ratio of the number of interrogation pulses not answered to the total number of interrogation pulses received. *see also:* **navigation.** 13, 187

counter (1) (electronic computation). (A) A device, capable of changing from one to the next of a sequence of distinguishable states upon each receipt of an input signal. *Note:* One specific type is a circuit that produces one output pulse each time it receives some predetermined number of input pulses. The same term may also be applied to several such circuits connected in cascade to provide digital counting. (B) Less frequently, a counter is an accumulator. (C) (ring). A loop of interconnected bistable elements such that one and only one is in a specified state at any given time and such that, as input signals are counted, the position of the one specified state moves in an ordered sequence around the loop. *See:* **trigger circuit.** 210

(2) (test, measurement and diagnostic equipment). (A) A device such as a register or storage location used to represent the number of occurrences of an event: and (B) An instrument for storing integers, permitting these integers to be increased or decreased sequentially by unity or by an arbitrary integer, and capable of being reset to zero or to an arbitrary integer. 54

counter cells. *See:* **counter-electromotive-force cells.**

counterclockwise polarized wave (radio wave propagation). *See:* **left-handed polarized wave.**

counter electromotive force (any system). The effective electromotive force within the system that opposes the passage of current in a specified direction. 328

counter-electromotive-force cells (counter cells). Cells of practically no ampere-hour capability used to oppose the battery voltage. *See:* **battery (primary or secondary).** 328

counter-mounted cooking unit (National Electrical Code). A cooking appliance designed for mounting in or on a counter and consisting of one or more heating elements, internal wiring, and build-in or separately mountable controls. *See:* **wall-mounted oven.** 256

counterpoise (1) (antenna). A system of conductors, elevated above and insulated from the ground, forming a lower system of conductors of an antenna. *Note:* The purpose of a counterpoise is to provide a relatively high capacitance and thus a relatively low impedance path to earth. The counterpoise is sometimes used in medium- and low-frequency applications where it would be more difficult to provide an effective ground connection. 111

(2) (overhead line) (lightning protection). A conductor or system of conductors, arranged beneath the line, located on, above, or most frequently below the surface of the earth, and connected to the footings of the towers or poles supporting the line. *See:* **antenna; ground.** 64

counter, radiation. *See:* **radiation counter.**

counter tube (radiation counters). A device that reacts to individual ionizing events, thus enabling them to be counted. (1) (externally quenched). A radiation-counter tube that requires the use of an external quenching circuit to inhibit reignition. (2) (gas-filled, radiation). A gas tube used for detection of radiation by means of gas ionization. (3) (gas-flow). A radiation-counter tube in which an appropriate atmosphere is maintained by a flow of gas through the tube. (4) (Geiger-Mueller). A radiation-counter tube operated in the Geiger-Mueller region. (5) (proportional). A radiation-counter tube operated in the proportional region. (6) (self-quenched) A radiation-counter tube in which reignition of the discharge is inhibited by internal processes. *See:* **anticoincidence (radiation counters).** *See:* **gas-filled radiation-counter tube.** 96,125,190

counting channel (liquid-scintillation counting). A region of the pulse-height spectrum which is defined by upper and lower boundaries set by discriminators. 422

counting efficiency (1) (radiation-counter tubes). The average fraction of the number of ionizing particles or quanta incident on the sensitive area that produce tube counts. *Note:* The operating conditions of the counter and the condition of irradiation must be specified. *See:* **gas-filled radiation-counter tubes.** 125, 190

(2) (sciatillation counters). The ratio of (A) the average number of photons or particles of ionizing radiation that produce counts to (B) the average number incident on the sensitive area. *Note:* The operating conditions of the counter and the conditions of irradiation must be specified. *See:* **scintillation counter.** 117

(3) (liquid-scintillation counting). The ratio of the

which is not the same for all of the source emitters. 363

initial condition (analog computers). The value of a variable at the start of computation. A more restricted definition refers solely to the initial value of an integrator. Also used as a synonym for the computer-control state "reset." *See:* **reset.** 9

initial luminous exitance (illuminating engineering). The density of luminous flux leaving a surface within an enclosure before interreflections occur. *Note:* For light sources this is the luminous exitance as defined herein. For nonself-luminous surfaces it is the reflected luminous exitance of the flux received directly from sources within the enclosure or from daylight. *See:* **luminous exitance.** 167

initiating relay (power switchgear). A programming relay whose function is to constrain the action of dependent relays until after it has operated. 103

injected current (ac high-voltage circuit breakers). The current which flows through the test circuit breaker from the voltage source of a current injection circuit when this circuit is applied to the test circuit breaker. 426

injected-current frequency (ac high-voltage circuit breaker). The frequency of the injected current. 426

injection fiber. *See:* **launching fiber.** 433

injection laser diode (ILD) (fiber optics). A laser employing a forward-biased semiconductor junction as the active medium. *Syn:* **diode laser; semiconductor laser.** *See:* **active laser medium; chirping; laser; superradiance.** 433

injection time (ac high-voltage circuit breaker). The time with respect to the power frequency current zero when the voltage circuit is applied. 426

inner product. *See:* **polarization vector, Note 2.** 111

in-phase spring rate (dynamically tuned gyro) (inertial sensor). The residual difference, in a dynamically tuned gyro, between the dynamically induced spring rate and the flexure spring rate. 46

input (1) (data transmission). (A) The data to be processed. (B) The state or sequence of states occurring on a specified input channel. (C) The device or collective set of devices used for bringing data into another device. (D) A channel for impressing a state on a device or logic element. (E) The process of transferring data from an external storage to an internal storage. 59

(2) (to a relay) (power switchgear). A physical quantity or quantities to which the relay is designed to respond. *Notes:* (A) A physical quantity that is not directly related to the prescribed response of a relay, (though necessary, to or in some way affecting the relay operation,) is not considered part of input. (B) Time is not considered a relay input, but it is a factor in performance. 103

input assertion (software). A logical expression specifying one or more conditions that program inputs must satisfy in order to be valid. *See:* **program.** 434

input-axis misalignment (gyro, accelerometer) (inertial sensor). The angle between an input axis and its associated input reference axis when the device is at a null condition. (The magnitude of this angle is unambiguous, but when components are reported, the convention should always be identified. IEEE standards use both direction cosines and right-handed Euler angles, depending on the principal field of application. Other conventions, differing both in signs and designation of axes, are sometimes used. 46

input impedance (1) (analog computers). In an analog computer, a passive network connected between the input terminal or terminals of an operational amplifier and its summing junction. 9

(2) (at a transmission line port) (waveguide). The impedance at the transverse plane of the port. *Note:* This impedance is independent of the generator impedance. 267

input limiter. *See:* **limiter circuit.** 9

input signal (hydraulic turbines). A control sign injected at any point into a control system. 8

input signal level sensitivity (spectrum analyzer). The input signal level that produces an output equal to twice the value of the average noise alone. This may be power or voltage relationship, but must be stated so. *See:* **equivalent input noise sensitivity; sensitivity.** 390

inrush current (1) (electronics power transformer). The maximum root-mean-square or average current value, determined for a specified interval, resulting from the excitation of the transformer with no connected load, and with essentially zero source impedance, and using the minimum primary turns tap available and its rated voltage. 95

(2) (packaging machinery). Of a solenoid or coil, the steady-state current taken from the line with the armature blocked in the rated maximum open position. 429

insertion loss (1) (data transmission). Resulting from the insertion of a transducer in a transmission system, the ratio of (1) the power delivered to that part of the system following the transducer, to (2) the power delivered to that same part of the system after insertion of the transducer. *Note:* If the input or output power, or both, consist of more than one component, such as multifrequency signal or noise, then the particular components used and their weighting must be specified. 59

(2) (fiber optics). The total optical power loss caused by the insertion of an optical component such as a connector, splice, or coupler. 433

insertion loss (or gain). *See:* **general insertion loss (or gain); matched insertion loss (or gain); matched generator insertion loss (or gain); matched load insertion loss (or gain).** 267

in service (power system measurement). The state in which a unit is electrically connected to the system. 432

in-service planned derated hours (IPDH) (power system measurement). The in-service hours during which a planned derating was in effect. 432

in-service test (metering). A test made during the period that the meter is in service. It may be made on the customer's premises without removing the meter from its mounting, or by removing the meter for test,

or watt-hours. 394

(2) (power and distribution transformer). The ratio of true watts or watthours to the measured watts or watthours, divided by the marked ratio. *Note:* The transformer correction factor for a current or voltage transformer is the ratio correction factor multiplied by the phase-angle correction factor for a specified primary circuit power factor. The true primary watts or watthours are equal to the watts or watthours measured, multipled by the transformer correction factor and the marked ratio. The true primary watts or watthours, when measured using both current and voltage transformers, are equal to the current transformer correction factor times the voltage transformer correction factor multiplied by the product of the marked ratios of the current and voltage transformers multiplied by the observed watts or wattshours. 53

transformer, dry-type. *See:* **dry-type transformer.**

transformer, energy-limiting. A transformer that is intended for use on an approximately constant-voltage supply circuit and that has sufficient inherent impedance to limit the output current to a thermally safe maximum value. *See:* **transformer, specialty.** 203

transformer equipment rating. A volt-ampere output together with any other characteristics, such as voltage, current, frequency, and power factor, assigned to it by the manufacturer. *Note:* It is regarded as a test rating that defines an output that can be taken from the item of transformer equipment without exceeding established temperature-rise limitations, under prescribed conditions of test and within the limitations of established standards. *See:* **duty.** 203

transformer, grounding. *See:* **grounding transformer.**

transformer grounding switch and gap (capacitance potential device). Consists of a protective gap connected across the capacitance potential device and transformer unit to limit the voltage impressed on the transformer and the auxiliary or shunt capacitor, when used; and a switch that when closed removes voltage from the potential device to permit adjustment of the potential device without interrupting high-voltage line operation and carrier-current operation when used. *See:* **outdoor coupling capacitor.** 341

transformer, group-series loop insulating. An insulating transformer whose secondary is arranged to operate a group of series lamps and/or a series group of individual-lamp transformers. *See:* **transformer, specialty.** 203

transformer, high-power-factor. A high-reactance transformer that has a power-factor-correcting device such as a capacitor, so that the input current is at a power factor of not less than 90 percent when the transformer delivers rated current to its intended load device. *See:* **transformer, specialty.** 301

transformer, high-reactance (1) (output limiting). An energy-limiting transformer that has sufficient inherent reactance to limit the output current to a maximum value. *See:* **transformer, specialty.** 203

(2) secondary short-circuit current rating. The current in the secondary winding when the primary winding is connected to a circuit of rated primary voltage and frequency and when the secondary terminals are short-circuited. *See:* **transformer, specialty.** 203

(3) (kilovolt-ampere or voltampere short-circuit input rating). The input kilovolt-amperes or volt-amperes at rated primary voltage with the secondary terminals short-circuited. *See:* **transformer, specialty.** 203

transformer, ideal. A hypothetical transformer that neither stores nor dissipates energy. *Note:* An ideal transformer has the following properties: (1) Its self and mutual impedances are equal and are pure inductances of infinitely great value. (2) Its self-inductances have a finite ratio. (3) Its coefficient of coupling is unity. (4) Its leakage inductance is zero. (5) The ratio of the primary to secondary voltage is equal to the ratio of secondary to primary current. 239,197

transformer, individual-lamp insulating. An insulating transformer used to protect the secondary circuit, casing, lamp, and associated luminaire of an individual street light from the high-voltage hazard of the primary circuit. *See:* **transformer, specialty.** 203

transformer, insulating. A transformer used to insulate one circuit from another. *See:* **transformer, specialty.** 203

transformer integrally mounted cable terminating box. A weatherproof air-filled compartment suitable for enclosing the sidewall bushings of a transformer and equipped with any one of the following entrance devices: (1) Single or multiple-conductor potheads with couplings or wiping sleeves. (2) Wiping sleeves. (3) Couplings with or without stuffing boxes for conduit-enclosed cable, metallic-sheathed cable, or rubber-covered cable. 289

transformer, interphase (thyristor power converter). An autotransformer, or a set of mutually coupled inductive reactors, used to obtain multiple operation between two or more simple converters that have ripple voltages that are out of phase. 121

transformer, isolating (1) (signal-transmission system). A transformer inserted in a system to separate one section of the system from undesired influences of the other sections. *Example:* A transformer having electrical insulation and electrostatic shielding between its windings such that it can provide isolation between parts of the system in which it is used. It may be suitable for use in a system that requires a guard for protection against common-mode interference. *See:* **signal.** 188

(2) (electroacoustics). A transformer inserted in a system to separate one section of the system from undesired influences of other sections. *Note:* Isolating transformers are commonly used to isolate system grounds and prevent the transmission of undesired currents. 239

transformer, line. *See:* **line transformer.**

transformer loss (communication). The ratio of the signal power that an ideal transformer would deliver to a load, to the power delivered to the same load by the actual transformer, both transformers having the same impedance ratio. *Note:* Transformer loss is

EXHIBIT 14
(Claims Chart)

Independent Claims for USP 6,249,876 B1	**Prior Art: US Patent No. 4,638,417 to Martin.**
1. A digital frequency jittering circuit for varying the switching frequency of a power supply, comprising:	The '417 patent teaches a digital circuit using a spread spectrum technique to reduce EMI in power supply. *See* Exhibit 11 at 1:55-56 and 66-68. *See also* the sole figure at p.2.
an oscillator for generating a signal having a switching frequency, the oscillator having a control input for varying the switching frequency;	The sole figure shows a voltage controlled oscillator (VCO) 13 that generates a signal having a switching frequency and has a control input (e.g., the place that receives the signal from D/A 12) for varying the switching frequency.
a digital to analog converter coupled to the control input for varying the switching frequency; and	The sole figure shows a digital to analog converter 12 coupled to the control input for varying the switching frequency.
a counter coupled to the output of the oscillator and to the digital to analog converter, the counter causing the digital to analog converter to adjust the control input and to vary the switching frequency.	The counter 10 together with EPROM 11 as shown in the sole figure can be considered as corresponding to the counter in the claim element.* The counter 10 is coupled to the output of the oscillator 13. *See* the sole figure. The output of the EPROM 11 is coupled to the digital to analog converter. *Id.* The counter causes the digital to analog converter to adjust the control input and to vary the switching frequency. *Id.*

* As I explain in my Declaration, a counter can include the EPROM 11, or alternatively, the EPROM 11 can be considered as part of the digital to analog converter 12.

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EXHIBIT 15
(Claims Chart)

Independent Claims for USP 6,249,876 B1	**Prior Art: Habetler "Acoustic Noise Reduction in Sinusoidal PWM Drives Using a Randomly Modulated Carrier"**
1. A digital frequency jittering circuit for varying the switching frequency of a power supply, comprising:	The Habetler article teaches a digital circuit using a spread spectrum technique to modulate the switching frequency of a PWM drive to reduce acoustic noise, which would also reduce EMI. *See* Exhibit 8 at p. 356.
an oscillator for generating a signal having a switching frequency, the oscillator having a control input for varying the switching frequency;	Habetler discloses a triangle generator (*i.e.*, an oscillator), which generates a signal having a switching frequency. *See* Fig. 5 at p. 359. The triangle generator has a control input (e.g., the place that receives the average slope signal and the signal from the D/A) for varying the switching frequency. *Id.*
a digital to analog converter coupled to the control input for varying the switching frequency; and	Fig. 5 shows a digital to analog converter (D/A) that is coupled to the control input for varying the switching frequency. *Id.* at p. 359.
a counter coupled to the output of the oscillator and to the digital to analog converter, the counter causing the digital to analog converter to adjust the control input and to vary the switching frequency.	Habetler discloses a counter together with a EPROM as shown in Fig. 5. *Id.* The output of the EPROM is coupled to the digital to analog converter and the output of the oscillator is coupled to the counter.* *Id.*

* As I explain in my Declaration, the EPROM can be considered part of either the counter or the digital to analog converter.

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EXHIBIT 16
(Claims Chart)

Independent Claims for USP 6,249,876 B1	**Prior Art: Wang et al. "Programmed Pulsewidth Modulated Waveforms for Electromagnetic Mitigation in DC-DC Converters"**
1. A digital frequency jittering circuit for varying the switching frequency of a power supply, comprising:	The Wang article teaches a digital circuit using a spread spectrum technique to modulate the switching frequency of a PWM power circuit to reduce acoustic noise or EMI. *See* Exhibit 12 at p. 596.
an oscillator for generating a signal having a switching frequency, the oscillator having a control input for varying the switching frequency;	Wang discloses a programmable triangle waveform generator (*i.e.*, an oscillator), which generates a signal having a switching frequency. *See* p. 603. The triangle waveform generator has a control input (e.g., the place that receives the ramp slope signal) for varying the switching frequency. *Id.*
a digital to analog converter coupled to the control input for varying the switching frequency; and	Fig. 20 shows a digital to analog converter (Subperiod Width D/A) that is coupled to the control input for varying the switching frequency. *See* p. 604.
a counter coupled to the output of the oscillator and to the digital to analog converter, the counter causing the digital to analog converter to adjust the control input and to vary the switching frequency.	Wang discloses a counter together with a ROM as shown in Fig. 20. *Id.* The output of the ROM is coupled to the digital to analog converter and the output of the oscillator is coupled to the counter.* *See*, Fig. 20 at p.604.

* As explained in my Declaration, the ROM can be considered part of either the counter or the digital to analog converter.

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EXHIBIT 17
(Random-Switching Control in DC-to-DC Converters)

PESC '89 RECORD

Volume I

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RANDOM-SWITCHING CONTROL IN DC-TO-DC CONVERTERS

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ABSTRACT

The concept of random-switching control, by which the switching-noise spectrum is smoothed and its level is reduced, is proposed. Two types of control circuits realizing the random switching are introduced, and its effectiveness is confirmed by the experimental results of switching-noise spectrum.

1.INTRODUCTION

The switching-mode power converter has been widely used because of its features of high efficiency and small weight and size. These features are brought by the ON-OFF operation of semiconductor switches. However, this switching operation causes the surge and noise which deteriorate the reliability of the converters themselves and the entire electronic systems. This problem on the surge and noise is one of the most serious difficulties in DC-to-DC converters. For some converters the generation mechanism of the surge and noise has been already made clear [1,2], and various techniques to suppress the surge and noise have been developed. In the previous papers, the quantitative discussions have been based on the surge and noise voltage waveforms. In many cases, on the other hand, the regulation of noise interference in electronic systems is described by using its power spectrum, and so the frequency domain characteristics of surge and noise have to be discussed.

In this paper, we first discuss the properties of switching noise in power converters from the viewpoint of the frequency domain. Second, the concept of random-switching control is proposed, by which the switching-noise spectrum is smoothed and its level is reduced. Third, two types of control circuits realizing the random switching are introduced for a buck converter, and their basic operations are explained and experimentally examined. Finally, we report the experimental results of switching-noise spectrum by two kinds of control techniques, namely the random-switching control and the conventional PWM control. From the comparison between these control schemes, it is confirmed that the random-switching control is effective for suppressing the peak level of switching-noise spectrum.

2.SWITCHING-NOISE SPECTRUM

In this section, we examine the characteristics of switching-noise spectrum in DC-to-DC converters. And the novel concept of random switching is proposed, by which the noise spectrum is smoothed and its level is reduced. Furthermore the effectiveness of random switching on switching-noise spectrum is theoretically discussed for a simple case.

In the DC-to-DC converter, the output voltage is generally controlled by varying the ON-OFF interval ratio of main switch. When a converter operates in steady state, the ON-OFF interval ratio of the converter is kept constant. So the turn-on and turn-off noises are generated at regular intervals and their repetition intervals are equal to the switching period of the converter, as shown in Fig.1-(a). From the viewpoint of the frequency domain, the switching-noise spectrum is observed as the harmonics of switching frequency as shown in Fig.1-(b). The switching-noise spectrum is a series of line components, and this fact indicates that the power of switching noise is concentrated in the specific fre-

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quencies, i.e. the multiple frequencies of switching frequency. If the power of switching noise is dispersed in the frequency domain, it is expected that the peak level of the switching-noise spectrum can be reduced.

Based on the above-mentioned expectation, a new technique is introduced into the switching timing of transistor switch. As shown in Fig.2-(a), this is performed by adding a random perturbation to switching instant while the output-voltage regulation of converter is sufficiently performed. The switching-noise spectrum is then turned into a dispersed one because of the irregular switching, and its peak level becomes smaller than that by the conventional technique as shown in Fig.2-(b). This power dispersion of switching noise in the frequency domain comes from the random operation of switching instant, which is called random-switching control.

To show the advantage of the random-switching control over the conventional one, we theoretically compare the effects of the two control schemes on the switching-noise spectrum. The following symbols are introduced for the convenience of description.

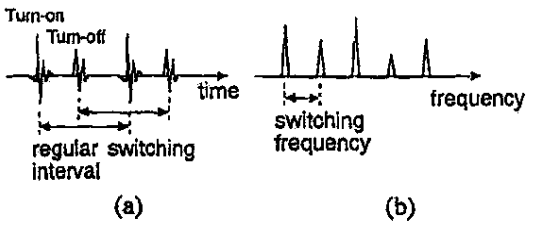

Fig.1. Schematic waveform and spectrum of switching noise, (a) waveform and (b) spectrum.

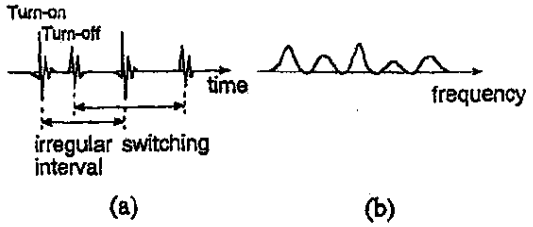

Fig.2. Schematic waveform and spectrum of switching noise with random perturbation, (a) waveform and (b) spectrum.

$\delta(t)$: unit impulse function.
$N(t)$: single switching noise at turn-on or turn-off instant.
T_{CI} : switching interval by constant-interval switching control.
t_k : switching instant by random-switching control.
$U_{CI}(t)$: switching function by constant-interval switching control.
$U_{RS}(t)$: switching function by random-switching control.
$\Phi_{CI}(\omega)$: power spectral density of $U_{CI}(t)$.
$\Phi_{RS}(\omega)$: power spectral density of $U_{RS}(t)$.
$\Phi_{NCI}(\omega)$: power spectral density of switching noise by constant-interval switching control.
$\Phi_{NRS}(\omega)$: power spectral density of switching noise by random-switching control.
$W_N(j\omega)$: frequency response of $N(t)$.
f_{CI} : switching frequency by constant-interval switching control.
f_{RS} : instantaneous switching frequency by random-switching control.

On the comparison of power spectrum, the total power of spectrum should be equal to each other. Hence the following equation is also introduced.

$$f_{CI} = \overline{f_{RS}} \quad , \qquad (1)$$

where $\overline{f_{RS}}$ is mean value of f_{RS}. The theoretical discussions on switching-noise spectrum are illustrated in Fig.3.

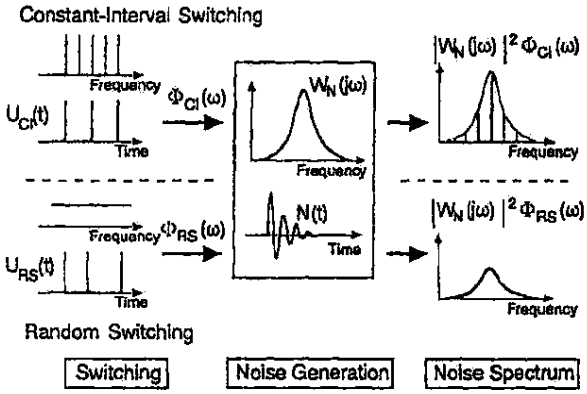

Fig.3. Theoretical comparison of switching-noise spectrums.

First, we take one group of the switching noises, e.g. turn-on noise, for the simplicity of description. It is expressed using single switching noise N(t) as

$$\sum_k N(kT_{CI}) \quad \text{for constant-interval switching,} \qquad (2)$$

$$\sum_k N(t_k) \quad \text{for random switching,}$$

where $k = -\infty, \cdots, -1, 0, 1, \cdots, +\infty$. Next, we consider the single switching noise N(t) to be the output of the fictitious noise generator, whose impulse response is equal to N(t). The switching noise is regarded as the output of fictitious noise generator with the input represented by a switching function, i.e. a series of unit impulses. These switching functions are expressed as

$$U_{CI} = \sum_k \delta(kT_{CI})$$

for constant-interval switching, (3)

$$U_{RS} = \sum_k \delta(t_k) \quad \text{for random switching.} \qquad (4)$$

Now changing a standpoint from the time domain to the frequency domain. The power spectrum $\Phi_{CI}(\omega)$ of switching function $U_{CI}(t)$ is a series of line components, because the interval of impulses is constant. On the other hand, for the switching function $U_{RS}(t)$ which consists of random-interval impulses, its power spectrum $\Phi_{RS}(\omega)$ is a continuous spectrum. And it can be assumed as a band-limited white noise, as examined experimentally in a later section. Hence, comparing power spectrums $\Phi_{CI}(\omega)$ and $\Phi_{RS}(\omega)$, the peak level of $\Phi_{RS}(\omega)$ is smaller than that of $\Phi_{CI}(\omega)$.

Next, using the power spectrums $\Phi_{CI}(\omega)$, $\Phi_{RS}(\omega)$ and the frequency response of fictitious noise generator $W_N(j\omega)$, the power spectrums of switching noise are represented as follows:

$$\Phi_{NCI}(\omega) = |W_N(j\omega)|^2 \Phi_{CI}(\omega)$$

for constant-interval switching, (5)

$$\Phi_{NRS}(\omega) = |W_N(j\omega)|^2 \Phi_{RS}(\omega)$$

for random switching. (6)

From these equations, it is obtained that the peak level of switching-noise spectrum by random-switching control is smaller than one by constant-interval control. And these two spectrums are similar in shapes, since the envelopes of these spectrums are determined by the frequency response $W_N(j\omega)$. The above discussions on switching-noise spectrum are also valid for the other group of turn-off noises.

3. REALIZATION OF RANDOM SWITCHING

In the case of applying the random-switching control technique to DC-to-DC converters, the following requirements must be satisfied:

(i) The output voltage is sufficiently regulated.

(ii) A frequency component of noise spectrum is not generated within the pass-band of low-pass filter in the converter.

In this section, two types of control circuits approximately realizing the random switching are proposed for a buck converter. One is the circuit which controls the output voltage by switching the ON-OFF interval ratio between two fixed values according to the instantaneous value of output voltage. This is called Control Circuit-I. The other is a modified PWM circuit, in which the sawtooth wave is modulated by the additional white noise. This is called Control Circuit-II. The basic operations of these two control circuits are explained and experimentally examined.

3.1 Control Circuit-I

The block diagram of approximate random-switching Control Circuit-I and its switching timing chart are shown in Figs.4 and 5 respectively. In Fig.4, the part encircled by dashed line is the control block, and its detailed operations are as follows: (i) The output voltage E_o of buck converter is compared with the reference voltage by the comparator. (ii) Because of the output ripple voltage of converter, the output voltage of comparator oscillates. (iii) The output of comparator is sampled with the constant-interval clock clock signal. (iv) According to the sampled value, one of two fixed duty ratios, D_1 and D_2, is selected and sent to the main switch.

By applying this control method, the switching converter takes no steady state, and this feature of Control Circuit-I realizes the random-switching operation approximately. For the buck converter with Control Circuit-I, the ratio of output voltage E_o to input voltage E_i is expressed as

$$\frac{E_o}{E_i} = P_1D_1 + P_2D_2 , \qquad (7)$$

$$(0 \le P_1 \le 1,\ 0 \le P_2 \le 1,\ P_1 + P_2 = 1)$$

where P_1 and P_2 are the ratios of the appearance frequencies of D_1 and D_2 to the switching frequency f_s, respectively, and the internal power loss in converter are neglected.

Now, we experimentally check whether the random-switching Control Circuit-I satisfies the above-mentioned requirements. The load characteristics of buck converter with Control Circuit-I is shown in Fig.6. This result experimentally indicates that the output-voltage regulation is sufficiently performed by Control Circuit-I. Next, the loci of converter state variables, i.e. reactor current i_L and output voltage v_o, are shown in Fig.7, where (a) is a locus by the conventional PWM control, and (b) is one by the random-switching Control Circuit-I. From the comparison these loci, the increase in output-voltage ripple by employing Control Circuit-I is sufficiently small.

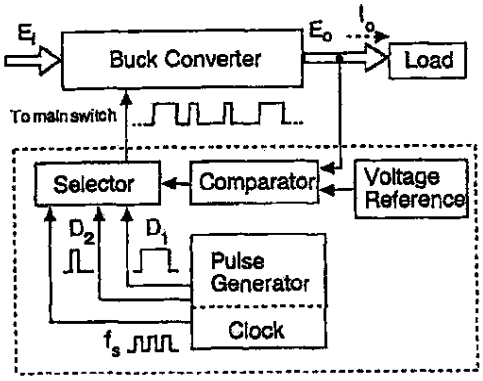

Fig.4. Block diagram of random-switching Control Circuit-I.

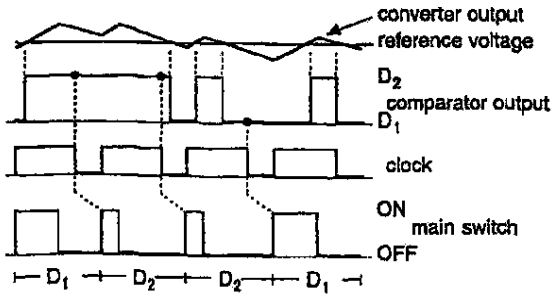

Fig.5. Timing chart of random-switching Control Circuit-I.

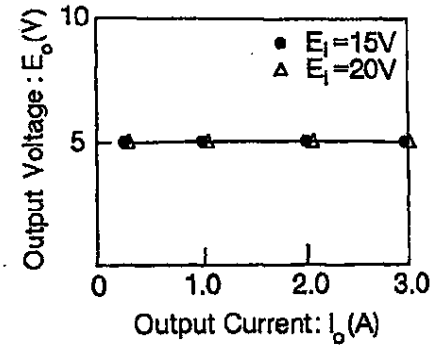

Fig.6. Load characteristics of buck converter with random-switching Control Circuit-I. (D_1=0.5, D_2=0.2, f_s=100kHz)

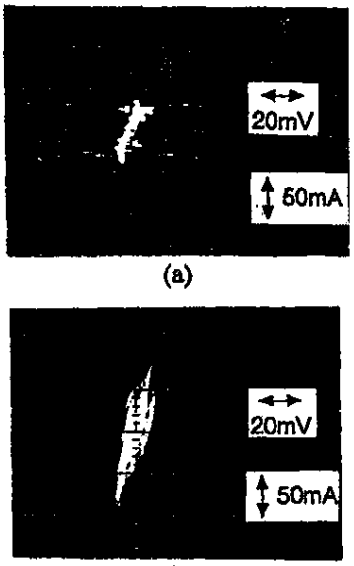

Fig.7. Loci of buck-converter state variables with (a) conventional PWM control and (b) random-switching Control Circuit-I. (vertical: reactor current, horizontal: output voltage; E_i=15V, E_o=5.0V, I_o=1.0A, D_1=0.5, D_2=0.2, f_s=100kHz)

3.2 Control Circuit-II

The block diagram of approximate random-switching Control Circuit-II and its timing diagram are shown in Figs.8 and 9 respectively. In Fig.8, the part encircled by dashed line is the control block, and its detailed operations are as follows: (i) The output of white-noise generator is sampled and held with the signal from the sawtooth-wave generator.

(ii) According to the value of the sampled white noise, the rising rate of sawtooth wave is modulated, but the peak value of sawtooth wave is kept constant. (iii) The modulated sawtooth wave and the reference voltage are converted to a PWM signal with the comparator.

As stated above, Control Circuit-II is a modified PWM control circuit, and it has the following advantages: (a) The switching interval changes with the white noise, but the duty ratio of main switch is kept a constant value. (b) As the peak-to peak value of sawtooth wave is kept constant, the transfer function of Control Circuit-II is also constant regardless of the changing of switching interval. From the advantage (a), it is easily obtained that two requirements on random-switching control are satisfied with Control Circuit-II.

The experimental results of sawtooth waves by the conventional PWM control and by Control Circuit-II are shown in Fig.10. In the experiment, the conventional PWM control is also performed with Control Circuit-II by making the output of white-noise generator zero. In Fig.10-(b), the switching frequency $\overline{f_s}$ is the mean value of instantaneous switching frequency f_s, and the frequency deviation Δf_s is the frequency bandwidth between minimum and maximum value of f_s.

4.EXPERIMENTAL CONFIRMATION

To confirm the effectiveness of random-switching, we compare the experimental results of noise spectrum by two kinds of control techniques, namely the conventional PWM control and the random-switching control by Control Circuit-I and Control Circuit-II. The comparisons are made on the switching-noise spectrum across the input terminals of a buck converter.

4.1 Comparison of Control Circuit-I and PWM

The spectrums of switching noise with the PWM control and the random-switching control by Control Circuit-I are shown in Fig.11 and Fig.12, respectively. In these figures, the labels "Turn-on" and "Turn-off" indicate the frequency components of the switching-noise generated in the instants of main-switch turn-on and turn-off. Here the input-output conditions of buck converter are the same as each other. And the random-switching Control Circuit-I is adjusted so as to generate the irregular turn-off and the regular turn-on. From Fig.11-(a) and Fig.12-(a),

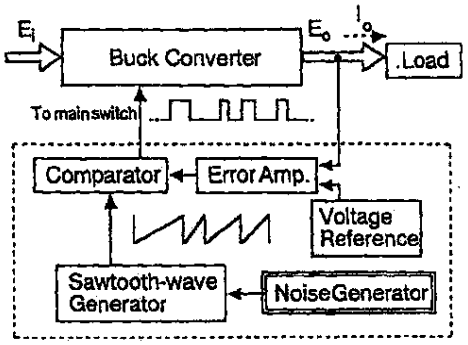

Fig.8. Block diagram of random-switching Control Circuit-II.

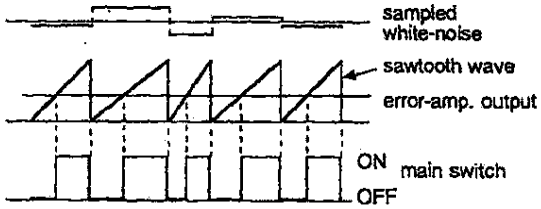

Fig.9. Timing chart of random-switching Control Circuit-II.

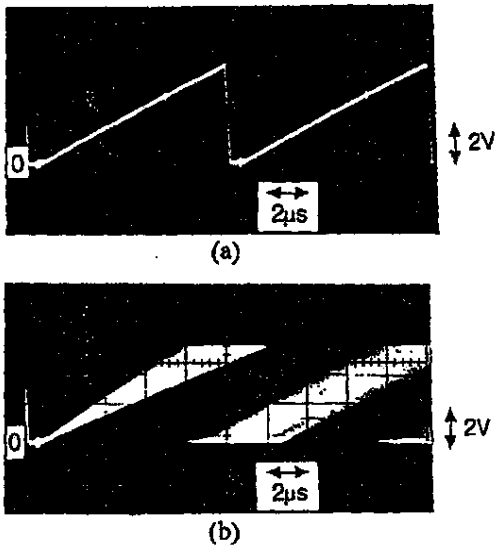

Fig.10. Sawtooth waveforms for (a) conventional PWM control and (b) random-switching control by Control Circuit-II.

the turn-off peak level of switching-noise spectrum by the random-switching Control Circuit-I is surely small compared with that of PWM control. However, the difference between the two spectrums on turn-off noise is not so large, because the turn-off switching is not sufficiently random and the power dispersion of switching noise in the frequency domain is not enough, as shown in Fig.12-(b). As to the turn-on noise, the power dispersion of turn-on noise dose not occur because of its regular switching, as shown in Fig.11-(c) and Fig.12-(c).

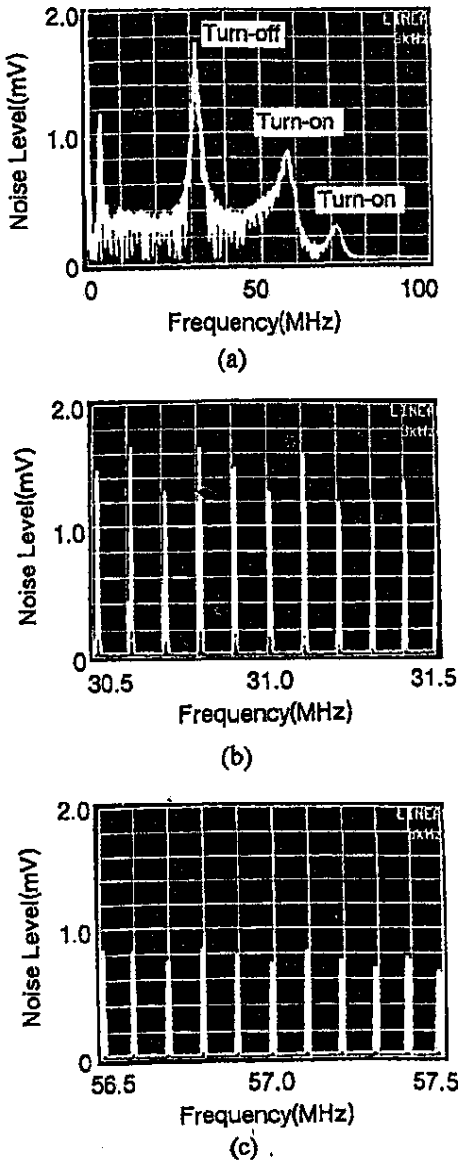

Fig.11. Switching-noise spectrums by PWM control, (a) DC-100MHz, (b) magnified around turn-off noise, (c) magnified around turn-on noise. (E_i=15V, E_o=5.0V, I_o=1.0A, f_s=100kHz; resolution bandwidth: 3kHz)

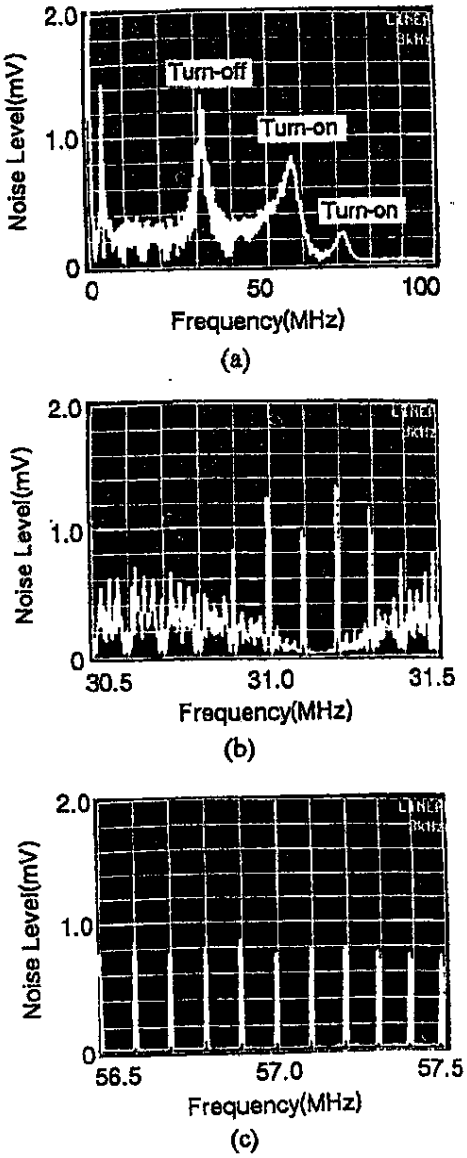

Fig.12. Switching-noise spectrums by random-switching Control Circuit-I, (a) DC-100MHz, (b) magnified around turn-off noise, (c) magnified around turn-on noise. (E_i=15V, E_o=5.0V, I_o=1.0A, f_s=100kHz, D_1=0.4, D_2=0.3; resolution bandwidth: 3kHz)

4.2 Comparison of Control Circuit-II and PWM

The spectrums of switching noise with the PWM control and the random-switching control by Control Circuit-II are shown in Fig.13 and Fig.14. In both controls, Control Circuit-II is adjusted so as to satisfy the condition on switching frequency expressed by equation (6). From Fig.13-(a) and Fig.14-(a), the peak level of switching-noise spectrum by the random-switching Control Circuit-II is approximately halved compared with that of PWM control, while these spectrums are similar in shape. On both the turn-on and the turn-off noises, Control Circuit-II have the sufficient effect of power dispersion in the frequency domain as shown in Fig.14-(b) and Fig.14-(c), and these spectrums with random-switching Control Circuit-II look like white noise. From these experimental results, it is derived that the randomness of the switching function described in the section 2 is sufficient for the random-switching Control Circuit-II.

Next, the influence of frequency deviation Δf_s on reducing the peak level of noise spectrum is shown in Fig.15. In this case, 15% deviation of switching frequency $\overline{f_s}$ is enough.

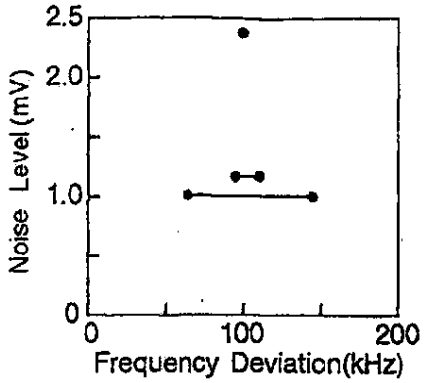

Fig.15. Effect of frequency deviation on peak level of turn-off noise spectrum. (E_i=15V, E_O=5.0V, I_O=1.0A, $\overline{f_s}$=100kHz; resolution bandwidth: 3kHz)

4.3 Control Circuit-I and Control Circuit-II

Comparing the spectrums by two types of random-switching controls, Control Circuit-II is more effective on smoothing and reducing the switching- noise spectrum than Control Circuit-I. In addition, the basic characteristics of switching converter is not changed by employing Control Circuit-II. From the two reasons stated above, Control Circuit-II is better than Control Circuit-I in applying the random-switching control to DC-to-DC converters.

5.CONCLUSION

From the viewpoint of the frequency domain, the properties of switching noise in power converters have been examined, and the proposal of random-switching control and the report of its experimental results have been made. The discussions are summarized as follows:

(i) The concept of random-switching control is proposed, by which the noise spectrum is smoothed and its level is reduced.

(ii) Two types of control circuits approximately realizing the random-switching control are introduced, and the usefulness of the random-switching control is experimentally confirmed.

(iii) It is clarified that Control Circuit-II is more effective on reducing the level of switching-noise spectrum than the other.

The analysis of switching-noise spectrum variation by the random-switching control is our future study.

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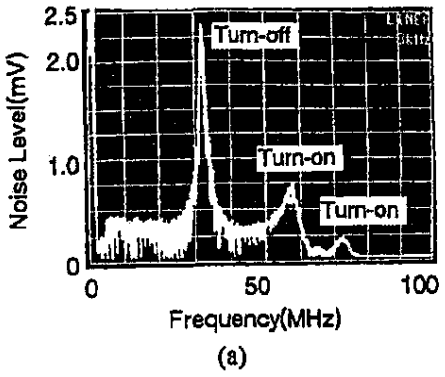
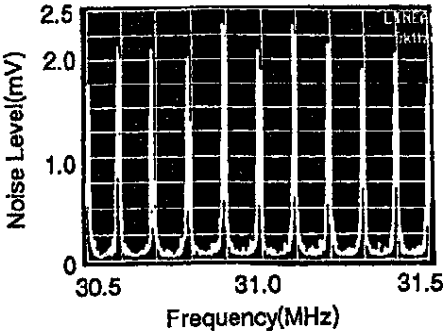
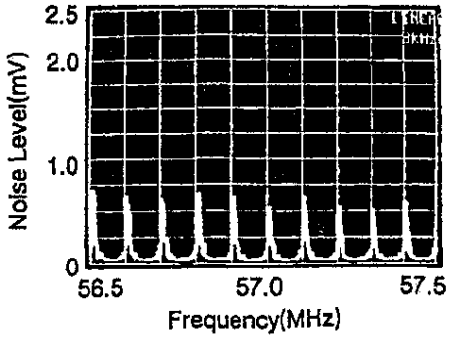
[2] T. NINOMIYA et al., "Backward-Noise Generation in Forward DC-to-DC Converters," *IEEE Trans. Power Electron.*, vol. PE-2, pp. 208-216, Jul. 1987.



(a)

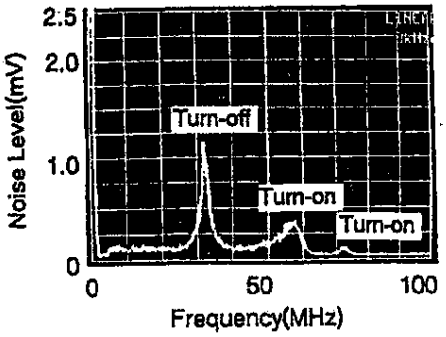


(b)

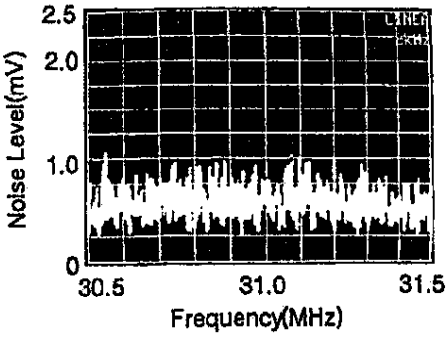


(c)

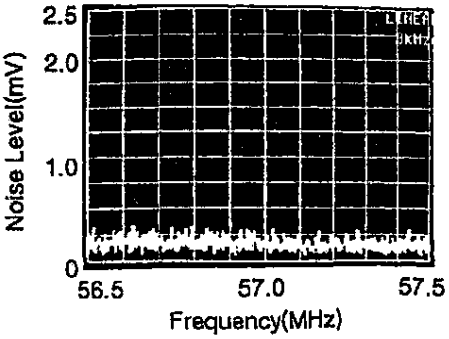
Fig.13. Switching-noise spectrums by PWM control, (a) DC-100MHz, (b) magnified around turn-off noise, (c) magnified around turn-on noise. (E_i=15V, E_o=5.0V, I_o=1.0A, f_s=100kHz; resolution bandwidth: 3kHz)



(a)



(b)



(c)

Fig.14. Switching-noise spectrums by random-switching Control Circuit-II, (a) DC-100MHz, (b) magnified around turn-off noise, (c) magnified around turn-on noise. (E_i=15V, E_o=5.0V, I_o=1.0A, $\overline{f_s}$=100kHz, Δf_s=95-110kHz; resolution bandwidth: 3kHz)

EXHIBIT 18
(Reduction of Power Supply EM1 Emission by Switching Frequency Modulation)

Reduction of Power Supply EMI Emission by Switching Frequency Modulation

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Abstract

The effect of PWM frequency modulation on power supply EMI noise emission is investigated. Significant reduction of emission is possible with this scheme.

I. Introduction

Electro-Magnetic Interference (EMI) emission is always of grave concern for power electronic circuit designers. Due to rapid switching of high current and high voltage, interference emission is a serious problem in switching power circuits. Many products fail to make it to the market because of their failure to comply with the government EMI regulations. Numerous companies have cited EMI problems as the culprit in the delay of their product introduction.

EMI noise reduction is generally accomplished by three means: suppression of noise source, isolation of noise coupling path, and filter/shielding. In this paper, another means of EMI noise reduction is proposed. By modulating the PWM frequency of power supply, it is possible to modify noise emission spectrum so that it can pass government EMI regulations.

In the paper, measurement of EMI noise is first reviewed. Noise sources of a power switching circuit will then be described. The theoretical and the experimental results using the proposed EMI reduction means will be discussed.

This work was partly supported by Industry Partnership Program to Virginia Power Electronics Center.

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II. Conducted EMI Test

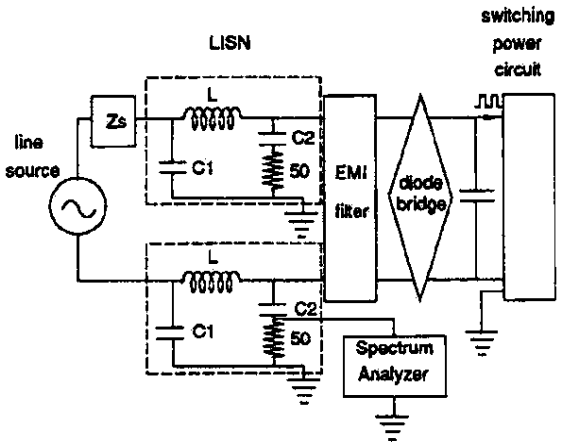


Figure 1 Conducted EMI Test Circuit

Figure 1 shows the circuit diagram of conducted EMI emission test for a switching power circuit. The dotted box (LISN) shows a line impedance stabilizing network. The noise voltage measured across the 50 Ω resistor, usually displayed in frequency domain, is by definition the conducted EMI emission of the switching power circuit. The purpose of a LISN is to prevent the line impedance Zs from affecting the measurement result, so that the result is repeatable. The values of the reactive components inside LISN are such that for line frequency, L is essentially shorted, and C1 and C2 are essentially open. For EMI noise frequency, however, L is essentially an open circuit, and C2 is essentially shorted. In other words, line frequency power goes through LISN unaffected, and noise

generated by the switching circuit sees a 50 Ω impedance from each phase to ground. The 50 Ω resistance is normally the input impedance of the measuring spectrum analyzer.

Resolution Bandwidth (RBW) of Spectrum Analyzer

The emission compliance limit is set by FCC in the United States and by VDE in the Common European Market. FCC specifications call for compliance for frequency range from 450 kHz to 30 MHz. VDE specifies a larger frequency range, from 10 kHz to 30 MHz. It is to be noted that the spectrum measured depends, among the other parameters, on the resolution bandwidth set by the spectrum analyzer. The larger the set RBW, the higher the measured emission floor and the less pronounced the switching-frequency harmonic peaking in the spectrum. According to regulations, RBW should be set at 200 Hz for noise frequency less than 150 kHz, and at 9 kHz for noise frequency between 150 kHz and 30 MHz.

III. EMI Noise Sources and Coupling Paths

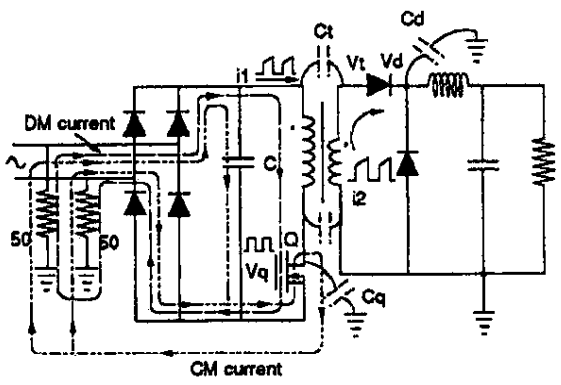


Figure 2 Conducted Noise Emission Sources In A Forward Converter Circuit

Figure 2 shows a circuit diagram depicting noise sources, noise coupling paths, and the noise-frequency equivalent circuit of the LISN [1]. A forward converter circuit topology is used for illustration. As stated earlier, the voltage measured across the 50 Ω LISN resistor is by definition the measured conducted EMI. Therefore, any current coupled to the 50 Ω resistor causes EMI conducted emission.

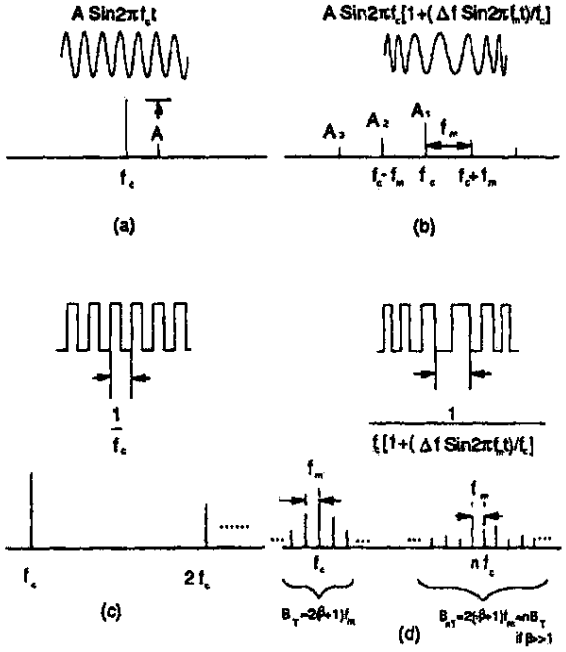
There are two modes of current coupling to the 50 Ω resistor: the differential-mode (DM) and the common-mode (CM). DM noise is caused by the pulsating transistor current. Part of the pulsating current is shunted by the bulk capacitor, and the rest flows through the two 50 Ω resistors via the rectifying diodes. If the impedance of the capacitor C is very small compared to 100Ω(= 50Ω + 50Ω), then the DM noise coupling is small. The parasitic inductance of C must be kept low to avoid DM coupling at very high frequency. The CM noise is caused by the current coupled through parasitic capacitors Cd, Cq and Ct. Cd, and Cq are the parasitic capacitances between semiconductor and chassis, and Ct is the transformer winding capacitance. The voltages across the three parasitic capacitors are high-voltage high-frequency waveforms. Displacement current generated by these voltage waveforms flows through the 50 Ω resistors and causes the measured EMI emission. If the heat sinks used for the semiconductor devices are physically tied to the chassis, then the values of Cq and Cd will be increased and so will the measured EMI. If the winging arrangement of the transformer is altered, Ct will be affected, and so will the measured EMI. From the discussion given above, it is clear why the circuit layout and component packaging affect the EMI performance of a circuit.

IV. EMI Reduction by Modulation of Power Supply Switching Frequency

From the discussion given in the last section, it is clear that the measured emission is periodical with respect to switching frequency. The emission, therefore, centers at the switching frequency and the harmonic frequencies. Concentration of emission power at these discrete frequencies makes it harder to meet EMI regulations. By modulating the switching frequency, side-bands are created, and the emission spectrum is smeared. The power

is shattered into smaller pieces scattered around many side-band frequencies. This effect makes it easier for the resultant emission spectrum to pass EMI regulations. The details are explained below.

Spectrum of a Frequency-Modulated Sine Wave (FM)



(a) Sinsoidal Waveform
(b) Frequency-Modulated Sinusoidal Waveform
(c) Square Waveform
(d) Frequency-Modulated Square Waveform

Figure 3 Spectra Of Waveforms

Figure 3 shows the effect of frequency modulation on the frequency spectrum, where f_c is the carrier frequency, f_m is the modulating frequency, and Δf is the amplitude of frequency change. As can be seen from Figure 3(b), side-band harmonics are generated, and the magnitude at $f=f_c$ is reduced compared to the unmodulated signal. It looks as if the bar in Figure 3(a) is shattered and scattered around the side-band frequencies shown in figure 3(b). Notice that the frequency difference between each two adjacent side-band harmonics is f_m.

The extent of shattering and the magnitude of the resultant spectrum depend on the modulation index $\beta = \Delta f / f_m$ [2]. Figure 4 shows the actual spectra for several β values. The larger the β value, the more evenly distributed is the spectrum.

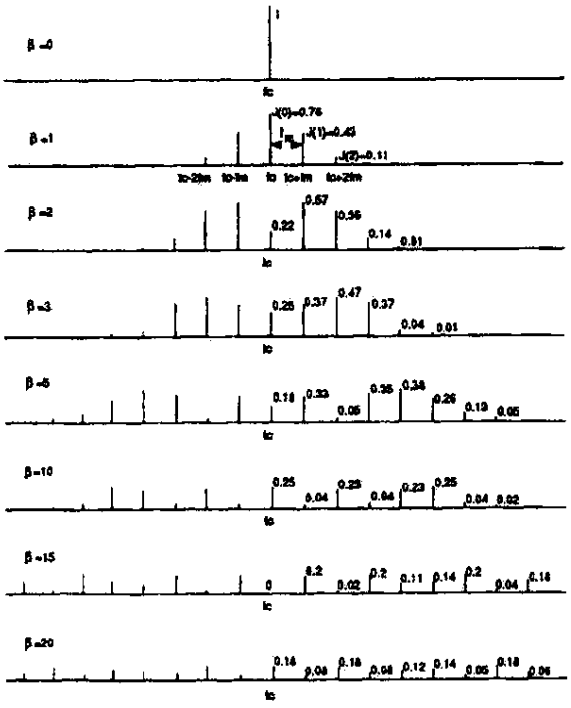


Figure 4 Spectra of Frequency-Modulated Sine wave

Carson's Rule

There are two important characteristics of an FM signal according to Carson's Rule:

(a) Total power of a signal is unaffected by the frequency modulation. The total power of a signal is equal to the summation of the square of each harmonic amplitude. Referring to Figure 3, this means $A^2 = A_1^2 + 2(A_2^2 + A_3^2 + \ldots)$

(b) 98% of the total power of a frequency-modulated signal is contained inside the bandwidth B_T, where $B_T = 2(\beta+1)f_m$. Practically speaking, this means the side-

band harmonic frequency ranges from (f_c-B_T/2) to (f_c+B_T/2). $\beta=\Delta f/f_m$, $B_T=2\Delta f/(\beta+1)/\beta$. If $\beta>>1$, then $B_T=2\Delta f$.

Spectrum of Frequency-Modulated Pulse Train

If the unmodulated waveform is a pulse train, then it itself contains harmonics. To avoid confusion, these harmonics are referred to as switching-frequency harmonics. Frequency modulation of the pulse-train waveform shatters each of the switching harmonic components into side-band harmonics as shown in Figure 3(d). Notice, however, that the frequency difference between each two adjacent side-band harmonics is still f_m, but the modulation index of each switching harmonics β_n is different, where n is the number of switching harmonics of the unmodulated pulse train (e.g. n=2 for second switching-frequency harmonics). $\beta_n=n\beta$. Since the modulation index changes with each switching harmonic, the scattering effect of each switching harmonics is different. For example, if $\beta=5$, then the third switching harmonic is scattered with modulation index of 15. Carson's rule applies to each harmonic, i.e., $B_{nT}=2(n\beta+1)f_m$. If $\beta>>1$, then $B_{nT}=nB_T$. It is possible that the side-band harmonics of different switching-frequency harmonics overlap. The general tendency of frequency modulation is to spread out the power of each switching harmonic. The higher the harmonic number, the more even is the spread-out power.

It is described in Section II that the noise generated by the power supply, either DM noise or CM noise, is a pulse-train waveform. The effect of FM on the power supply noise spectrum is similar to that depicted by Figure 3(d).

V. Experimental Verification

A frequency-modulated forward converter is designed and built to test the theory described above. A description of the converter is given below:

Switching Frequency: 90 kHz nominal

Modulating Frequency (f_m): adjustable

Frequency Variation (Δf): Adjustable but limited to 10 kHz

Output Voltage: 3 V

Output Current: 5 A

Input Line Voltage: 120 Vrms, 60 Hz

Control Strategy: Single loop feedback with 3 kHz band-width

PWM Frequency Modulation Circuit:

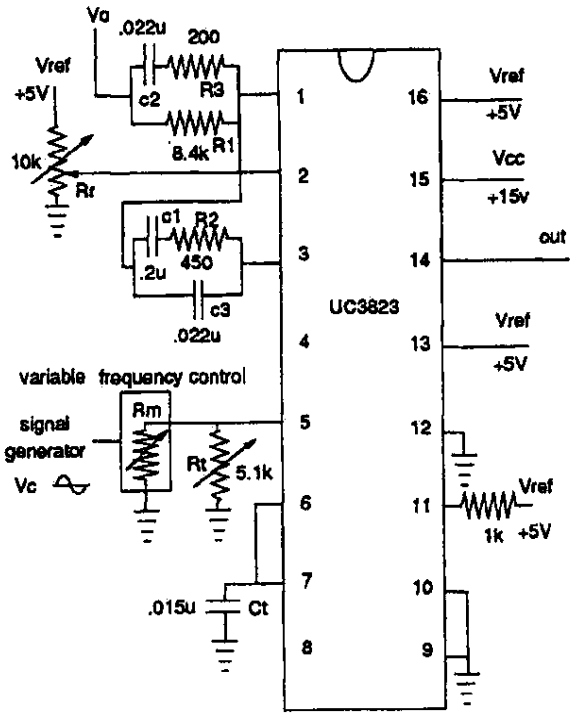


Figure 5 (a) Drive Circuit

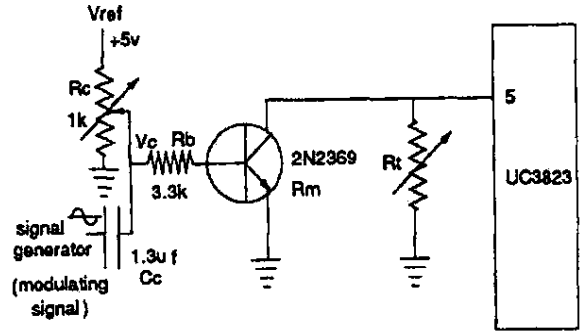


Figure 5 (b) Variable Switching Frequency Circuit

Figure 5(a) shows the control circuit that employs a conventional control chip UC3823. Pin 5 is connected with an equivalent transistor resistor Rm and an adjustable Rt. The paralleled value of Rm and Rt and the capacitor value C determine the PWM frequency. Modulation of Rm value is accomplished by the circuit shown in Figure

5(b). The effective collector-to-emitter resistance of the transistor (Rm) is modulated by a sinusoidal signal from a signal generator. The frequency and the amplitude of signal generator output control f_m and Δf, respectively. The variable resistor R_c controls the carrier frequency f_c.

Conducted EMI Test

A Hewlett-Packard 8568 spectrum analyzer is used for EMI measurement. Peak detector is used for all the tests, since quasi-peak is not available from this model. Figure 6 shows the measured conducted EMI of the forward converter described above. It is to be noticed that the spectrum analyzer RBW is not exactly set according to regulations as summarized in section II, that is, RBW = 200 Hz for f<150 kHz and RBW = 9 kHz for 150 kHz < f <30 MHz. This is done purposely, to avoid a step change in spectrum at 150 kHz and to show higher order switching frequency harmonics clearly.

For the unmodulated case, the amplitude of the harmonics is clearly shown in Figure 6(a). Figure 6(b) shows the spectrum for the case when the PWM frequency is modulated by a signal with f_m = 400 Hz and Δf = 15 kHz. It can be seen from Figure 6(b) that the switching frequency harmonics are shattered by the modulation, and the overall spectrum improves. The dotted line indicates the envelope of the unmodulated case. Figure 7 shows the same result as Figure 6, but with proper RBW. Figure 7(a) shows the noise spectrum between 50 kHz and 150 kHz, and Figure 7(b) shows the spectrum between 150 kHz and 30 MHz. Figures 7(c) and 7(d) show the results when frequency modulation is used. Notice from the figure that RBW's of 300 Hz and 10 kHz were used, because 200 Hz setting and 9 kHz setting, required by the regulations, are not available from the analyzer model used. Also, f_m of 400 Hz and Δf of 15 kHz were used. It is evident from Figure 7(b) that side-band harmonics of the fundamental switching frequency are created. Due to the nonlinearity of the variable switching frequency circuit shown in Figure 5, the side band is not symmetrical with respect to the fundamental frequency (90 kHz). The amplitude envelope of the unmodulated test is indicated by the dotted line, and VDE Class A specification is indicated by the solid line. Improvement due to FM is clearly shown. The improvement is particularly evident at fundamental switching frequency. This is practically significant, because the fundamental-frequency EMI dictates the size of the EMI filter. From 150 kHz to 30 MHz, the improvement is not as pronounced. The explanation is given in the following discussion.

Parameters Affecting the Performance

There are several parameters that affect the modulating effect as described in Section IV. Mathematically speaking, $\beta(=\Delta f/f_m)$ value alone determines the resultant frequency spectrum. In practice, however, the measurement requirement dictated by FCC or VDE rules also affects the result.

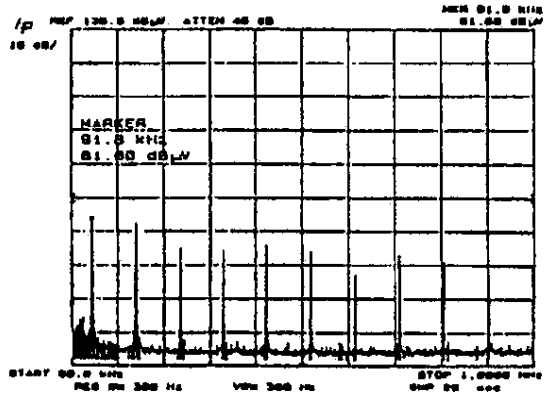
β Value

In theory, the larger the β value, the more even is the resultant spectrum. This is evident from Figure 4. However, because of measurement bandwidth requirements, increasing β may not result in any significant reduction in the measured EMI. For example, if f_m is significantly smaller than the measurement bandwidth requirements (200 Hz for 10k Hz< f <150k Hz, and 9k Hz for f >150 Hz), the measured result will not show any significant improvement by using FM, even though mathematically it should. To the spectrum analyzer set at relatively large RBW, the side-band harmonics are indistinguishable, and the measurement result shows the total as one large harmonic.

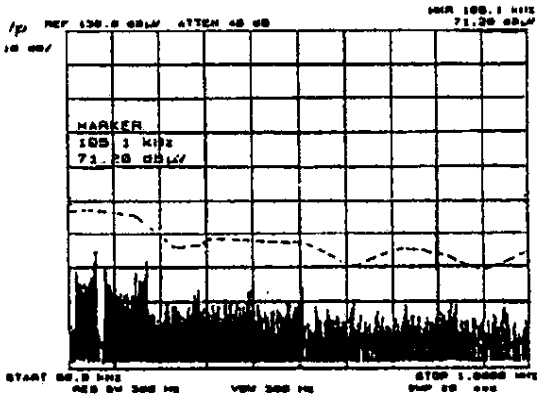
To be effective in EMI reduction, therefore, f_m should be close to or larger than the required RBW. Take Figure 7(c) as an example; f_m is 400 Hz, and the effect of the shattering of the fundamental frequency harmonics is very evident, because RBW is only 300 Hz. For measurement frequency higher than 150 kHz, RBW is set at 10 kHz, and the effect of FM shattering could be insignificant. At a much higher frequency, however, the side-band harmonic frequencies are more evenly separated, and the FM could become effective again in noise reduction.

Δf Value

From the EMI reduction point of view, a larger Δf value should be selected, because it leads to a larger β value. Since there are side-band harmonic frequency created in FM operation, it is required that the side-band frequencies do not fall into audible range. This requirement implies that $(f_c-\Delta f)$ should be above audible fre-



(a) Without FM

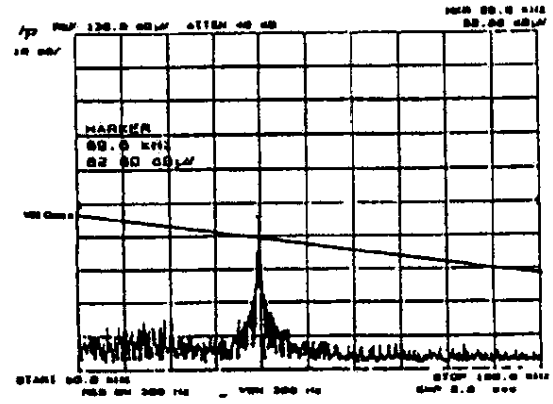


(b) With FM

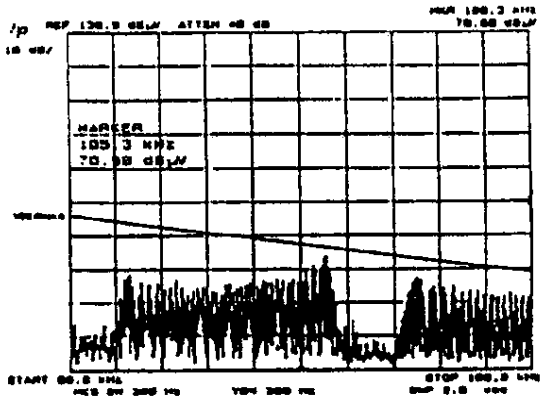
Frequency range: 50 kHz to 1 MHz

Resolution Bandwidth: 300 Hz

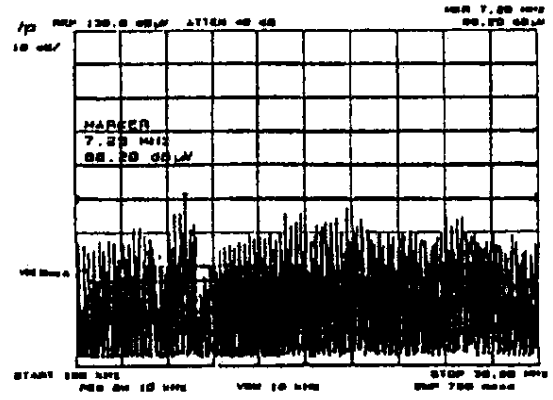
Figure 6 Effect of Frequency Modulation on Spectrum



(a)

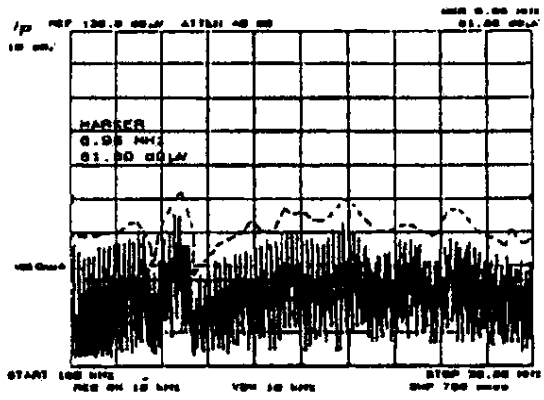


(c)



(b)

(a) and (b): Without FM



(d)

(c) and (d): With FM

For (a) and (c): Frequency Range: 50 kHz - 150 kHz
Resolution Bandwidth: 300 Hz

For (b) and (d): Frequency Range: 150 kHz - 30 MHz
Resolution Bandwidth: 10 kHz

Figure 7 Comparison of EMI Conducted Noises

quency range. Another consideration is the effect of FM on power supply component selection, particularly on magnetic and capacitive components. Therefore, practical limit would normally be set for $\Delta f/f_c$ value.

High Δf has another effect on the measured EMI. According to Carson's rule, the side-band bandwidth $B_{nT} = nB_T$ for each switching harmonic. For higher order switching harmonics (large n) and large Δf, the side-band bandwidth is large. Therefore, side-band harmonics of different switching-frequency harmonics may overlap. This possibility makes it difficult to predict the FM effect according to Carson's rule.

f_m Value

The effect of f_m value on EMI is two fold. On the one hand, f_m should be small to have large β value. On the other hand, f_m should be large compared to spectrum analyzer RBW, in order to have significant reduction effect. Also, f_m value should be small to avoid disturbing the power supply output voltage regulation. Thus, f_m should be significantly less than the control loop gain crossover frequency.

VI. Conclusions

There are several conclusions drawn from the investigation:

(1) Conducted EMI of a switching power circuit can be reduced by modulation of the PWM switching frequency. This possibility bas been verified experimentally.

(2) The modulating parameters must be properly chosen to have effective EMI reduction without causing significant side effects, such as audible noise due to frequency variation, and poor converter output voltage regulation. Reduction of more than 10 dB is practical.

(3) Frequency modulation is particularly effective in reducing the fundamental harmonic, if the switching frequency is less than 150 kHz. Modulating frequency f_m should be chosen to be somewhat greater than 200 Hz. This choice is effective in reducing EMI fundamental harmonic without causing many adverse side effects mentioned in [2]. If the switching is above 150 kHz, then a much larger modulating frequency should be chosen (9 kHz) to reduce the fundamental component. Such a choice in some cases may cause significant adverse side effects. A compromise of using lower modulating frequency may be necessary.

(4) Both the common-mode emission and the differential-mode emission can be reduced by frequency modulation. However, the emission generated by ringing can not be reduced by this approach. Snubber circuit and use of soft diodes alleviate this problem.

(5) Since the side-band harmonics generated by frequency modulation are scattered over a wide frequency range, the EMI filter must be properly damped to avoid possible amplification of emission at the filter pole frequencies.

(6) The resonant class of converters, in general, are operated with variable switching frequency over the input voltage and the output power range. However, if the input voltage and the load power are fixed during EMI measurement, then the switching frequency is constant, and there is no modulation effect. If the resonant converter is operated off-line, then the DC input voltage contains 120 Hz ripple, which causes modulation of switching frequency; EMI emission reduction is then possible.

(7) The effect of frequency modulation on the radiated EMI should be similar to on the conducted EMI, even though this possibility is not experimentally verified. Radiated EMI specification ranges from 30 MHz to 1 GHz, and the measurement resolution bandwidth (RBW) is 120 kHz. However, the side-band harmonics of the very high order switching-frequency harmonics (30 MHz--1 GHz) are widely separated, and the emission can be effectively reduced even with moderate modulating signal frequency.

(8) Single-frequency modulating signal is used in the analysis of spectrum and in the experiment. Other forms of modulating signal are possible, including a randomly modulated carrier frequency.

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[2] L.W.Couch II "Digital and Analog Communication Systems" Macmillan, 1987

EXHIBIT 19
(Easing EMC Problems In Switched Mode Power Converters By Random Modulation Of The PWM Carrier Frequency)

Easing EMC problems in switched mode power converters by random modulation of the PWM carrier frequency.

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Abstract -**This paper presents a method of reducing the measured amplitude of the high frequency harmonics, contained in standard fixed frequency PWM, by the use of a pseudo-random binary sequence to modulate the PWM carrier frequency, achieving a spread spectrum effect on the EMC spectrum of the system.**

I. INTRODUCTION

Increasing awareness of electromagnetic compatibility (EMC) issues in equipment design, spurred on by the recent introduction of the European Community (EC) EMC directive [1], has highlighted the problems of interference generation by both motor drive systems and switch-mode power converters (SMPC's). Active power conditioning may be used to ease the problems caused by high amplitude / low frequency current pulses drawn from the utility supplies by systems employing standard rectifier / filter arrangements [2][3][4]. Also, resonant switching techniques [5][6][7] help to shape the voltage and/or current switching edges in high frequency circuits, thus reducing both dv/dt or di/dt induced EMC problems. However, increasing use of higher frequency switching in systems employing pulse width modulation (PWM) techniques, leads to higher levels of conducted and radiated interference, caused by high order harmonics of the periodic PWM carrier frequency signal. These high harmonic order signals needs to be filtered out of the system, in order to prevent their entry into the utility supply as conducted interference, or their radiation into free-space as electromagnetic interference.

As standard PWM techniques rely on varying the pulse width of a signal within a fixed time period, the individual amplitude of each high frequency harmonic may change as a function of the pulse width. However as the period of the signal is fixed, there will always be some energy present at the harmonic frequencies, giving rise to corresponding peaks in the power density spectrum which may lie above the limits set in EMC standards relevant to the equipment under test. Traditionally, filters are used in the power line input to prevent the harmonic energy entering the power utility system as conducted interference, and shielding is used to remove the radiated emissions. The effectiveness of the mains input filter required for any given piece of equipment is dependant on both the power density of the interference signal at the input, and the choice of filter corner frequency. As the level of attenuation of a filter at a given frequency is given by

$$Attenuation_{dB} = 40\log_{10}\left(\frac{f}{f_c}\right) \quad \text{.....(i)}$$

Where Attenuation = Attenuation of filter at freq. f in dB

f = Frequency of interest.

f_c = Corner frequency of filter.

In order to minimise the physical size of filter, the power density of any given harmonic should be kept as low as possible, allowing the use of a high filter corner frequency whilst still giving acceptable attenuation at any given frequency.

This paper describes the effect of a spread-spectrum technique on the conducted EMC produced by a switched-mode power converter. The spectral spreading is achieved by using a pseudo random binary sequencer (PRBS) to modulate the period of the PWM signal.

II. SPREAD-SPECTRUM

Spectral spreading is a well known communications system technique, which may be applied to switched mode power converters to reduce the amplitude of the peak unwanted spectral energy present in high order harmonics of a PWM waveform, whilst distributing the energy to additional harmonics. One technique uses the pre-programming of turn-on and turn-off times for a PWM waveform into a memory, which may then be periodically accessed by a control circuit [8]. A different method involves the use of a random timing component to modulate the switching sequence to achieve spectral spreading of the high frequency harmonic components [9]. The method used in this paper is a direct application of a frequency-hopping spread-spectrum (FHSS) technique to the PWM carrier frequency. This implementation achieves spectral spreading by sequentially hopping between a

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number of discrete PWM carrier frequencies, remaining at any given frequency for only a short period of time. In order to ensure the pulse width is unaffected by the change in frequency, this change should only occur at the end of a given PWM period. This leads to a dwell time at each frequency being a function of the frequency and the number of cycles at this frequency. This leads to a maximum reduction of the spectral energy for 1 cycle at a given frequency of

$$P_m = P_{om} \cdot \left(\frac{1/f_m}{\sum_1^n 1/f_n} \right) \quad \text{...(ii)}$$

where m = 1....n

This technique concentrates the energy towards the lower frequencies in the modulation range, however EC EMC test standards tend to set higher thresholds at lower frequencies. The extent to which the energy is spread around the spectrum with frequency hopping is dependant on the dispersion index β, The larger the dispersion index, the more evenly spread the spectrum. Now:-

$$\beta = T.\Delta f \quad \text{.....(v)}$$

here Δf = Peak frequency deviation of the carrier wave,

and T = period of repetition of modulating waveform.

From this it may be seen that a high dispersion index, and hence good spectral spreading may be achieved with either a high peak frequency deviation (Δf large), or a long modulating sequence (T large).

III. MODULATING SEQUENCE TYPE

As spread-spectrum modulation is a form of wideband modulation, consideration of this technique should lead to an analytical expression for the spectral density envelope. The effect is easiest to predict for sinusoidal modulation of a sinusoidal carrier frequency. As this simple case results in a series of Bessel functions [10], the study of the effect of the modulating sequences used in this paper on the resultant spectral power density of the square edged PWM waveform, may best be evaluated by taking the spectrum of computer generated switching signals modulated with the various sequences used. The data files generated form idealised sequences, as the generation of data to include sufficient detail to accurately model switching transients and circuit parasitic effects leads to data files too large to be analysed for practical sequence lengths. Fig. 1 shows the effect of modulating a 25kHz 50% duty cycle PWM waveform with a ramp based sequence and various frequency deviations (Δf's).

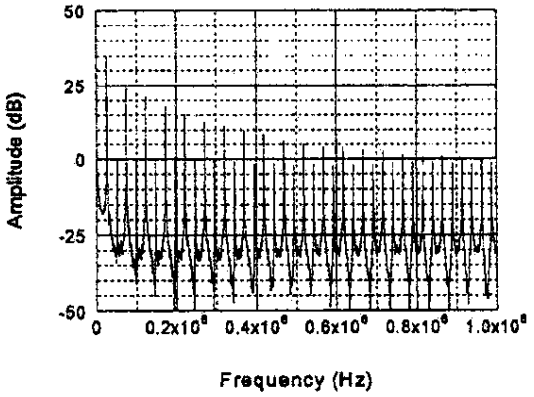

Fig 1a. Constant 25kHz PWM

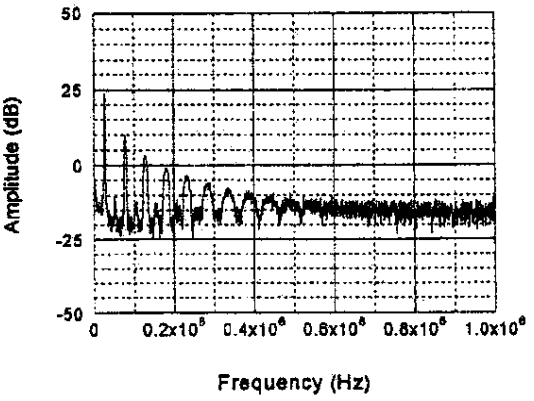

Fig 1b. Δf=2kHz (frequency varied form 25kHz to 27kHz), n=256

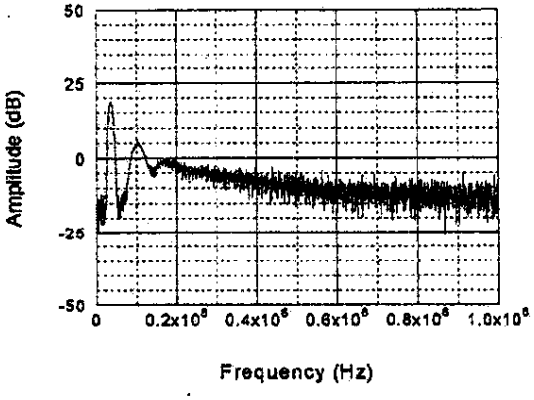

Fig 1c. Δf=20kHz (frequency varied from 25kHz to 45kHz), n=256.

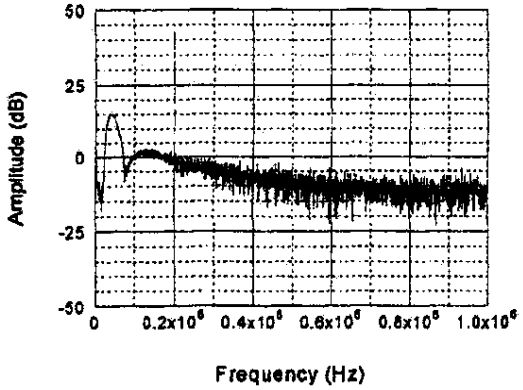

Fig 1d. Δf=40kHz (frequency varied form 25kHz to 65kHz), n=256

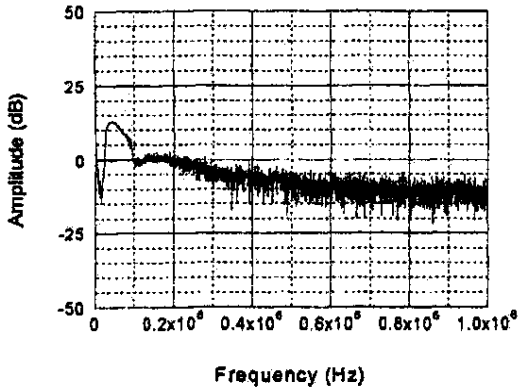

Fig 1e. Δf=60kHz (frequency varied form 25kHz to 85kHz), n=256

Fig 1. Graphs showing effect of peak frequency deviation on spectral spreading of PWM signals

Increasing frequency deviation from the unmodulated 25kHz signal results in the merging of ever lower harmonic numbers of the original spectrum as by Carson's rule

$$BW_n = n.BW_{fundamental}$$

where BW_n is the bandwidth of the nth harmonic.

Fig. 2 demonstrates the effect of different modulation sequences on the spectral spreading, the most effective sequence type being the pseudo-random based sequence (Fig 2d). The modulation shown was achieved with a sequence changing the PWM frequency to $(f + m.\Delta f / n)$ at the end of every PWM period (where f is the PWM base frequency, m is the current value in the sequence and n is the number of discrete frequencies in the sequence). With this modulation strategy the period of repetition for the sequence is $T=(\sum_{1}^{n} 1/f_n)$.

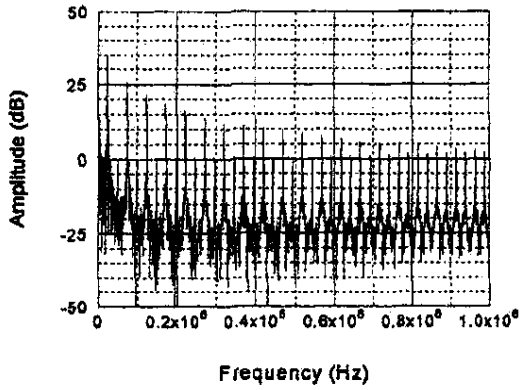

Fig 2a. Constant 25kHz PWM

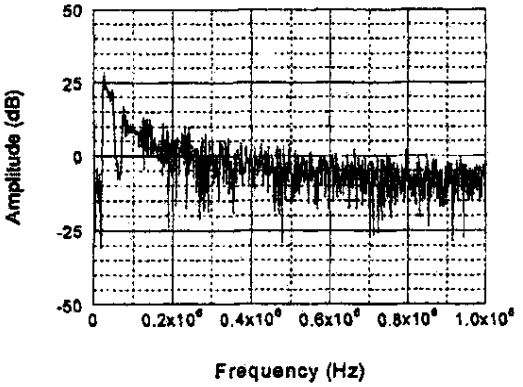

Fig 2b. Modulation with sine based sequence

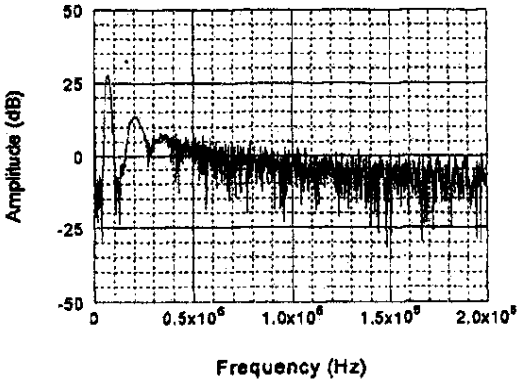

Fig 2c. Modulation with ramp based sequence

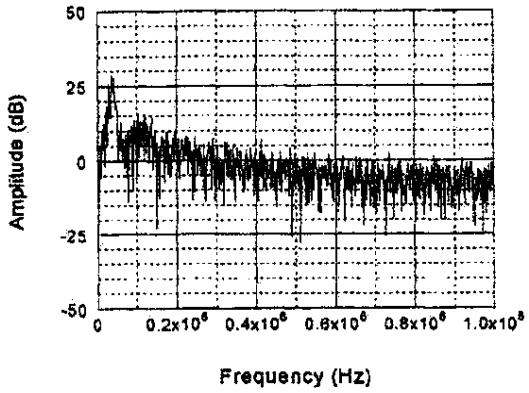

Fig 2d. Modulation with a Maximum length Pseudo-Random sequence.

Fig 2. Graphs showing effect of modulating sequence type on spectral spreading of PWM signals (Δf=20kHz, n=32)

IV. EFFECT OF PRACTICAL MEASUREMENT CONSTRAINTS ON PREDICTED SPECTRAL-SPREADING

One major constraint on the effectiveness of the FHSS technique is the resolution bandwidth (RBW) of the measurement spectrum analyser, as specified in the EC EMC standards. Whilst it is possibly in theory to spread the energy from one harmonic to an infinite number of closely spaced frequencies, if they all fall within one RBW of the measurement system, the effect of the spectral-spreading will be lost. The RBW specified in the EC EMC standards is 9kHz for the conducted interference tests within the range 150kHz to 30MHz. Other standards may differ in the RBW required for compliance measurements. The EC Standards also require that the peaks in the spectrum which lie above the prescribed limits are measured with a quasi-peak detector to ensure compliance. The charge and discharge time constants for this detector being 1ms and 160ms within the frequency span of interest. These time constants place restrictions on the time the PWM signal should spend within any given RBW of the measurement system, and the repetition period of the sequence.

V. IMPLICATIONS OF PEAK FREQUENCY DEVIATION (ΔF) AND REPETITION PERIOD (T) ON A PRACTICAL SMPC SYSTEM.

The use of a large frequency deviation (Δf) on the PWM frequency places a requirement on the design and sizing of the reactive components in the SMPC system, e.g. the transformer has to be designed to avoid saturation at the lowest frequency used without having excessive losses at the highest frequency. Ripple current and output ripple voltage has also to be considered at both ends of the frequency range to be used. The active components will also suffer from additional stresses due to the variations in losses between the various switching frequencies etc. Practically a limit will be imposed on the sequence repetition period T by the system control loop bandwidth, as to avoid output voltage ripple effects, the modulating frequency (1/T) should be small with respect to the voltage loop bandwidth. This leads to the use of long sequences, which is also consistent with the requirements of the quasi-peak detector circuit outlined above. Care should also be taken to ensure that all of the magnetic components are tightly wound and well 'potted', as loose windings may be likely to demodulating the sequence to generate electromagnetically induced audio noise, if the sequence repetition frequency falls within the audio range.

VI. MEASUREMENTS ON A PRACTICAL SYSTEM.

Validation of the technique was carried out on a 75W asymmetrical half bridge forward converter operating off-line. The specification for the system is given in Table 1. The system was operated open-loop under a constant 75W output power delivery to the load.

Table 1. SMPC System specification:
Output Voltage: 50V
Output Current: 1.5A.
Δf: Variable up to 3x Unmodulated Carrier Frequency, f_c
Frequency Range of operation: f_c to (f_c+Δf)
Sequence length: Variable from 7 to 257
Sequences used: Sine wave, ramp and maximum length pseudo-random.

The modulation sequence for the FHSS is stored in EPROM, the sequence length being variable. Adjustment of the peak frequency deviation being independent of both the sequence type and length. The conducted EMI measurements presented in this paper were carried out with a Farnell 150kHz to 30MHz line impedance stabilisation network (LISN), and a Farnell SSA1000A (150kHz to 1GHz) spectrum analyser. The system is PC controlled via a general purpose instrument bus (GPIB) and runs the EASY-1 pre-compliance testing software. Fig 3 shows the effect of modulating a SMPC PWM carrier with a maximal length pseudo-random sequence. The modulation had a peak frequency deviation of 20kHz and sequence lengths of 8 and 256. Fig 3a shows the spectrum of the unmodulated system for reference, giving a peak level of 92dBμV. This may be compared with the peak level of 88dBμV shown in the

spectrum of the PWM waveform modulated with a short sequence length (n=8), fig 3b. The use of a longer sequence (n=256) gives a further 2dBμV reduction to a peak of 86dBμV as shown by fig 3c. Fig 4 Shows the effect of the FHSS modulation on higher harmonics of the PWM waveform. Fig 4a shows the harmonics of the unmodulated waveform centred around 10MHz, the peak level may be seen to be 75dBμV.

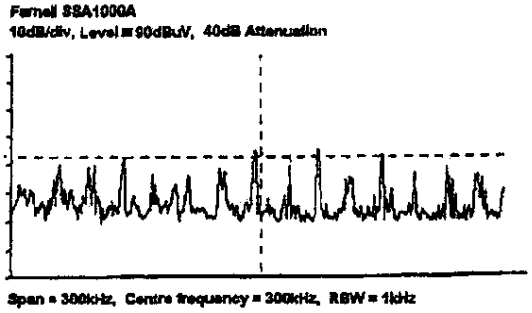

Fig 3a. Spectrum of a constant frequency 25kHz PWM waveform.

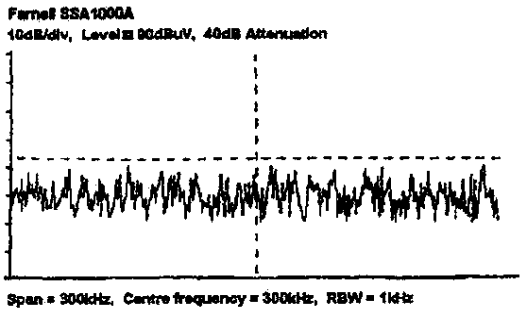

Fig 3b Pseudo-random sequence modulation (Δf=20kHz, n=8)

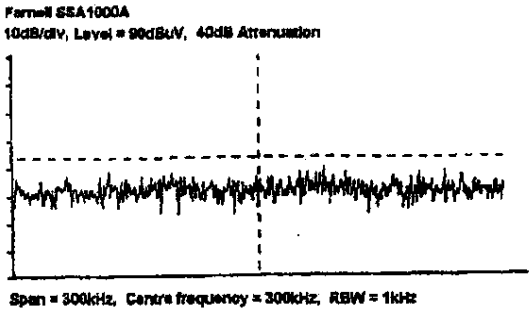

Fig 3c. Pseudo-random sequence modulation (Δf=20kHz, n=256)

Fig 3. Practical measured spectra with various sequence lengths (RBW = 1kHz, Centre frequency (c.f.) = 300kHz & Span = 300kHz)

Fig 4b shows the spectrum of the waveform modulated with a long sequence (n=256) centred at the same frequency. The peak levels are now at 67dBμV showing a 8dBμV reduction in peak levels by the modulation technique. Whilst this shows a reduction in the peak levels due to FHSS modulation, these results were taken with a measurement RBW of 1kHz, however the EC EMC regulations specify measurement RBW of 9kHz for the 150kHz to 30MHz frequency range.

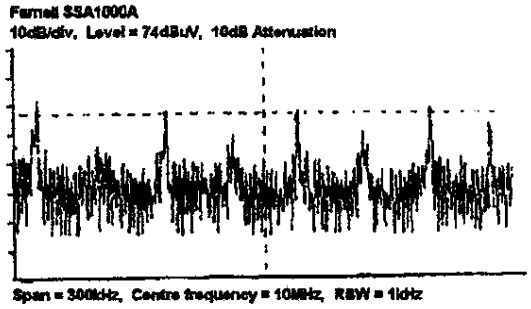

Fig 4a Spectrum of constant frequency 25kHz PWM waveform.

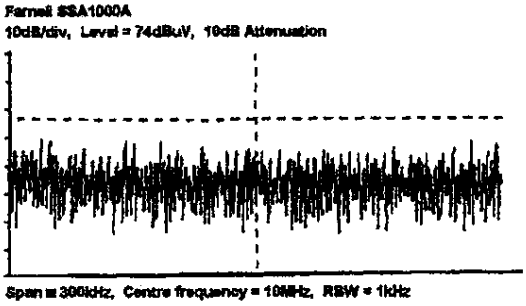

Fig 4b. Pseudo-random sequence modulation (Δf=20kHz, n=256)

Fig 4. Practical measured spectra with various sequence lengths (RBW = 1kHz, Centre frequency (c.f.) =10MHz & Span = 300kHz)

Fig 5 shows the effect on the spectrum generated by a 60kHz PWM waveform of applying a maximal length pseudo-random sequence of length 256 with a Δf of 40kHz. The measurement RBW was 9kHz. Quasi-peak measurements were taken at sample frequencies corresponding to peaks in the unmodulated spectrum. The results, given in table 2, show reductions in the measured quasi-peak amplitudes of the modulated waveform by up to 9dBμV.

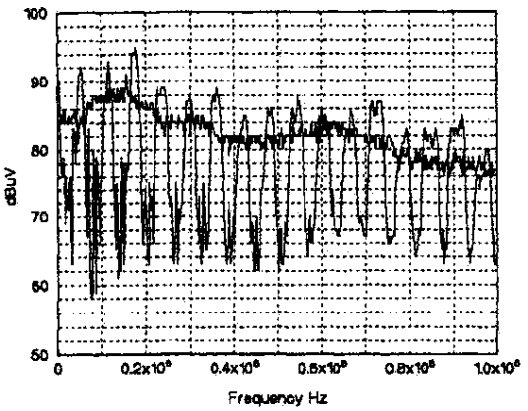

Fig 5. Spectrum of a constant frequency 60kHz PWM waveform and a FHSS waveform spread with a pseudo-random sequence (n=256, Δf=40kHz). Measurement RBW = 9kHz.

Table 2. Quasi-peak measurements on a practical 75W SMPC.

Peak Frequency	Constant frequency PWM	Spread spectrum PWM	Reduction in level
183.00kHz	94dBμV	88dBμV	6dBμV
554.20kHz	88dBμV	81dBμV	7dBμV
921.60kHz	85dBμV	76dBμV	9dBμV

VII. CONCLUSIONS

It has been shown that the measured conducted EMI generated by SMPC's may be reduced by modulation of the PWM carrier frequency using a FHSS technique. Various results have been presented showing the measured reductions in both peak and quasi-peak levels under various measurement RBW's, including the 9kHz bandwidth specified in the EC EMC regulations. Attention has also been drawn to the implications of the FHSS modulation technique on the physical characteristics of the SMPC.

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EXHIBIT 20
(The Effect of Carrier Frequency Modulation of PWM Waveforms on Conducted EMC Problems in Switched Mode Power Supplies)

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The Effect of Carrier Frequency Modulation of PWM Waveforms on Conducted EMC Problems in Switched Mode Power Supplies

David Stone & Barry Chambers, University of Sheffield, Department of Electronic and Electrical Engineering

Summary

Electromagnetic compatibility (EMC) remains an issue which can present many problems to designers of high frequency power converter circuits. Usual techniques for alleviating the problems of interference generation by power converters involve the use of screening materials and filters, however, the effectiveness of such measures depends on the frequency of the interference and the power density at each frequency of interest. As pulse width modulation (PWM) generates high frequency harmonics at multiples of the switching frequency, modulation of the switching frequency may be used to spread the spectral power density present at these harmonic frequencies. This paper presents a technique of frequency-hopping spread-spectrum modulation which may be applied to switched-mode power converters (SMPC's) to reduce the spectral power density at harmonics of the switching frequency. The influence of the peak frequency deviation, the modulation sequence length and the type of modulating sequence on the resultant spectrum are discussed. These prediction have been broadly confirmed in practice, with measurements carried out with an EMC pre-compliance test system.

Introduction

Recent increasing awareness of electromagnetic compatibility (EMC) issues in equipment design, spurred on by the introduction of the European EMC directive [1], has highlighted the problems of interference generation by system switched-mode power supplies. Active power conditioning may be used to ease the problems caused by high amplitude / low frequency current pulses drawn from the utility supplies by systems employing standard rectifier / filter arrangements [2, 3, 4]. Also, resonant switching techniques [5, 6, 7] help to shape the voltage and/or current switching edges in high frequency circuits, thus reducing both dv/dt and di/dt induced EMC problems. However, increasing use of higher frequency switching in switched mode power supplies employing pulse width modulation (PWM) techniques, leads to higher levels of conducted and radiated interference, caused by high order harmonics of the periodic PWM carrier frequency signal. These high harmonic order signals need to be filtered out of the supplies, in order to prevent their entry into the utility supply as conducted interference, or their radiation into free-space as electromagnetic interference. Inherently, standard PWM techniques rely on varying the pulse width of a signal in a fixed time period frame. Whilst the amplitude of each high frequency harmonic may change as a function of pulse width, as the period of the signal is fixed, there will always be some energy present at the harmonic frequencies, giving rise to peaks corresponding to these frequencies in the power density spectrum. It is possible that these peaks may lie above the limits set in EMC standards relevant to the equipment under test, and hence the equipment may fail the certification tests.

Traditionally, filters are used in the power line input to prevent the harmonic energy entering the power utility system as conducted interference, and shielding is used to remove the radiated emissions. As the attenuation of any filter used, at a given frequency is as given as below [8],

$$Attenuation_{dB} = 20\log_{10}\left(\frac{I_{input}}{I_{transmitted}}\right) \qquad (1)$$

Where:
Attenuation = Attenuation of the filter in dB.
I_{input} = Input current.
$I_{transmitted}$ = Transmitted Current.

and the maximum acceptable transmitted current is fixed by the relevant EMC standard, the effectiveness of the filter required for a given piece of equipment is dependant of the power density of the interference signal at the input. The filter size is also related to the choice of filter corner frequency, as the level of attenuation of a filter at a given frequency is given by.

$$Attenuation_{dB} = 40\log_{10}\left(\frac{f}{f_c}\right) \qquad (2)$$

Where
Attenuation = Attenuation of filter at freq. f in dB
f = Frequency of interest.
f_c = Corner frequency of filter.

Therefore, in order to minimise the size of filter components, the power density at any given harmonic should be kept as low as possible, therefore allowing a high filter corner frequency, for a given acceptable level of signal at a given frequency.

To this end, the peak unwanted spectral energy present in high order harmonics of a PWM waveform may be reduced by the use of spectral spreading. This allows the peak energy at a given harmonic to be lowered by distributing the energy to additional harmonics.

Spread-spectrum

The spreading of energy present at one frequency across a number of different frequencies may be carried out in various ways. One technique involves the pre-programming into a memory of the turn-on and turn-off times for a PWM waveform, and periodically accessing them by a control circuit [9]. A second method involves the use of a random timing component to modulate the switching sequence to achieve spectral spreading of the high frequency harmonic components [10]. Narrow band sinewave frequency

modulation of the switching carrier frequency has also been shown to be successful in the reduction of electromagnetic interference (EMI) [11].

Spread-spectrum techniques are common in modern r.f. communication systems, where they are used to spread energy from a single frequency transmission across a wide bandwidth to avoid unwanted interception of the signal. Whilst many methods of achieving a spread-spectrum effect exist in the field of communications, the one most applicable to switched-mode power converters (SMPC's) is "frequency hopping spread-spectrum". This technique achieves the spreading of spectral energy by sequentially hopping between a number of discrete carrier frequencies, and remaining at each frequency for only a short period of time. The frequency of the carrier returns to its original value as the sequence repeats.

There are two possible methods of implementing this frequency-hopping effect. The carrier frequency may be changed at regular intervals, T, or at the end of each period of the carrier. The latter gives a "dwell time" time at each frequency (f) equal to $1/f$.

The first method gives a reduction in spectral power density at each frequency of:

$$P_m = \frac{P_{om}}{n} \qquad (3)$$

where:
P_m = Power at frequency m,
n = number of frequencies in sequence ($m = 1 \ldots n$).
P_{om} = Power at frequency m if the carrier was always at this frequency.

The second achieves a reduction in spectral energy of:

$$P_m = P_{om} \cdot \left(\frac{1/f_m}{\sum_1^n 1/f_n}\right) \qquad (4)$$

where $m = 1 \ldots n$

Whilst changing frequencies regularly spreads the energy evenly around the spectrum, the second method is easier to implement, ensuring an integer number (1) of PWM cycles at each frequency. This technique concentrates the energy towards the low frequencies, however EMC test standards tend to set higher thresholds at lower frequencies. The extent to which the energy is spread around the spectrum with frequency hopping is dependant on the dispersion index β, The larger the dispersion index β, the more evenly spread the spectrum. Now:

$$\beta = T \cdot \Delta f \qquad (5)$$

Where
Δf = Peak frequency deviation of the carrier wave,
T = period of repetition of modulating waveform.

From this expression it may be seen that a high dispersion index may be achieved either by using a long modulating sequence (T large), or a high peak frequency deviation (Δf large).

Modulating sequence

The effect of wideband frequency modulation is easiest to predict when a sinusoidal carrier frequency is being modulated by a sinusoidal modulating signal. Even in this case, an analytical expression for the spectral density envelope results in a series of Bessel functions [12]. Study of the effect of the modulating sequences used in this paper and the lengths of the sequences, on the resultant power density spectrum of the PWM signals, may best be carried out by taking the spectrum of computer generated signals, modulated with the various sequences used (Figs 1, 2 & 3). The sequences generated form idealised sequences, as generation of data containing sufficient detail to include switching transient and circuit parasitic effects generates data files too large to be analysed easily for practical sequence lengths.

Fig 1 shows the effect of various values of T on the spectrum of a 20 kHz switching signal (duty cycle = 0.5). Frequency hopping was carried out by using a random sequence which changed the switching frequency to $(f + m \cdot \Delta f/n)$ at the end of every PWM period (where f is the base frequency, m is the value in the sequence, n is the number of discrete frequencies in the sequence, and the period of repetition:

$T = (\sum_1^n 1/f_n)$.

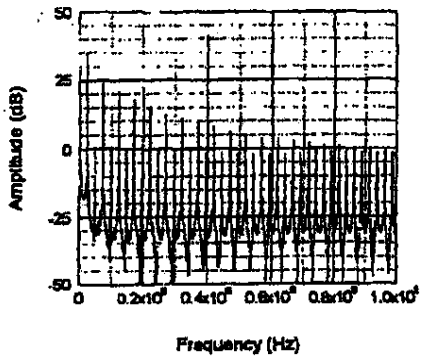

Fig. 1a: Constant 20 kHz PWM

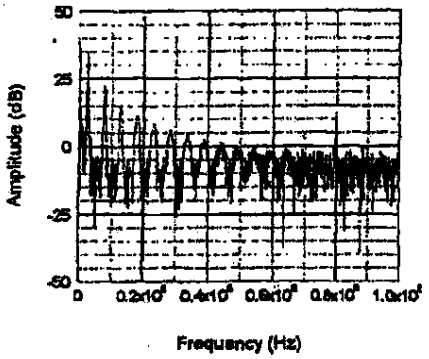

Fig. 1b: $\Delta f = 2$ kHz, $n = 16$

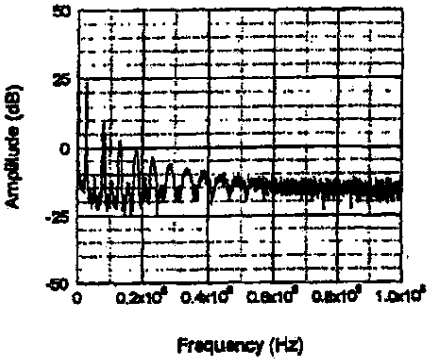

Fig. 1c: $\Delta f = 2$ kHz, $n = 256$

Fig. 1: Graphs showing effect of sequence length on spectral spreading of PWM signals

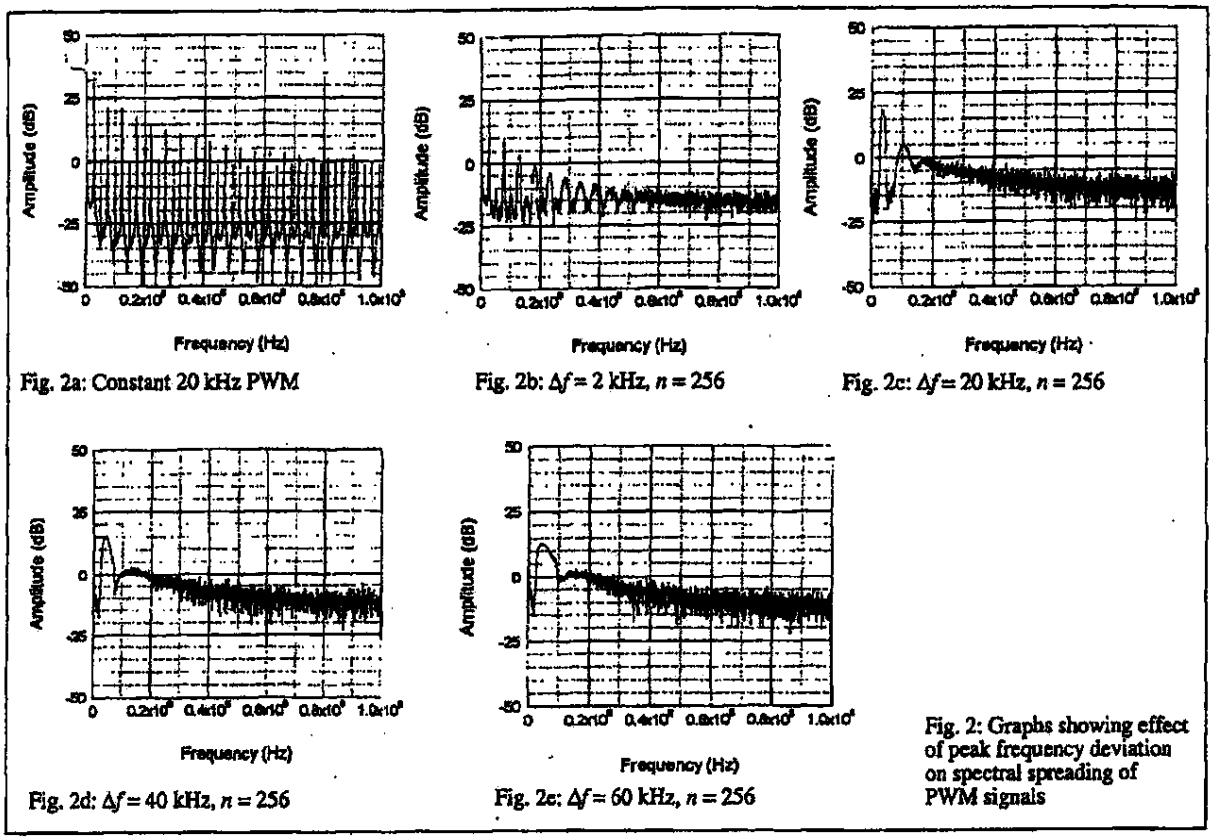

Fig. 2a: Constant 20 kHz PWM

Fig. 2b: $\Delta f = 2$ kHz, $n = 256$

Fig. 2c: $\Delta f = 20$ kHz, $n = 256$

Fig. 2d: $\Delta f = 40$ kHz, $n = 256$

Fig. 2e: $\Delta f = 60$ kHz, $n = 256$

Fig. 2: Graphs showing effect of peak frequency deviation on spectral spreading of PWM signals

Fig. 1a shows the spectrum of the unmodulated waveform, Fig. 1b shows the spectrum for $\Delta f = 2$ kHz (carrier frequency variation from 20 kHz to 22 kHz), $n = 16$. In Fig. 1c $\Delta f = 2$ kHz, $n = 256$. Fig. 2a shows the spectrum of the unmodulated waveform, Fig. 2b shows the spectrum for $\Delta f = 2$ kHz (carrier frequency variation from 20 kHz to 22 kHz), $n = 256$, Fig. 2c shows the spectrum for $\Delta f = 20$ kHz , $n = 256$. In Fig. 2d, $\Delta f = 40$ kHz, $n = 256$, in Fig. 2e $\Delta f = 60$ kHz, n = 256. The graphs in both Figures 1 and 2 clearly show the widening of the bandwidth of each harmonic with increasing sequence length and peak frequency deviation. The bandwidth of each modulated harmonic increases with harmonic number, as by Carson's rule:

$$BW_n = n \cdot BW_{fundamental} \qquad (6)$$

where BW_n is the bandwidth of the nth harmonic.

This leads to the overlapping of higher frequency harmonics, and a difficulty in predicting the spectral power density at these high frequencies.

Fig. 3a shows the spectrum of the unmodulated carrier and this may be compared to the resultant spectrum when sinusoidal, ramp, and pseudo-random sequences are used to modulate the carrier, Figs. 3b, c, d, & e respectively. (The modulation is for a 20 kHz carrier frequency with $\Delta f = 20$ kHz, and a sequence length, $n = 32$). Whilst all of the modulating sequences produce 10 dB or more reduction in the peak spectral power density at the original unmodulated carrier frequency, they differ in the way that they spread the energy around the spectrum. The most even distribution of spectral energy above the maximum modulated carrier frequency occurs with the use of pseudo-random modulating sequences.

Pseudo-random sequence generation

The generation of maximum length pseudo-random sequences may be done digitally using a number of possible algorithms. One of the simplest [13], which gives sequence lengths of 2^n, takes the form:

$$X_{t+1} = (aX_t + b) \text{ MOD } c \qquad (7)$$

where $c = 2^p$, $b = 2q + 1$, $a = 4b + 1$, and p, q are any integer.

It is also possible to generate number sequences whose length is not 2^n, based on the use of quadratic residues, or primitive roots [14]. The sequences generated using Quadratic Residues are not strictly pseudo-random, as they exhibit a symmetry about the central number in the sequence.

$$X_n = n^2 \text{ MOD } p \qquad (8)$$

where p is a prime number, and n is an integer 1 .. p.

It may be seen from the comparison of the graphs in Figs. 3d and 3e, that there is little difference between the effect of carrier frequency modulation with a maximum length pseudo-random sequence, and that obtained using a sequence generated by the quadratic residues method. Therefore the symmetry exhibited by the quadratic residues based sequence may be exploited as a method of halving the memory requirement of a spread-spectrum PWM system, without having a detrimental effect on the system performance.

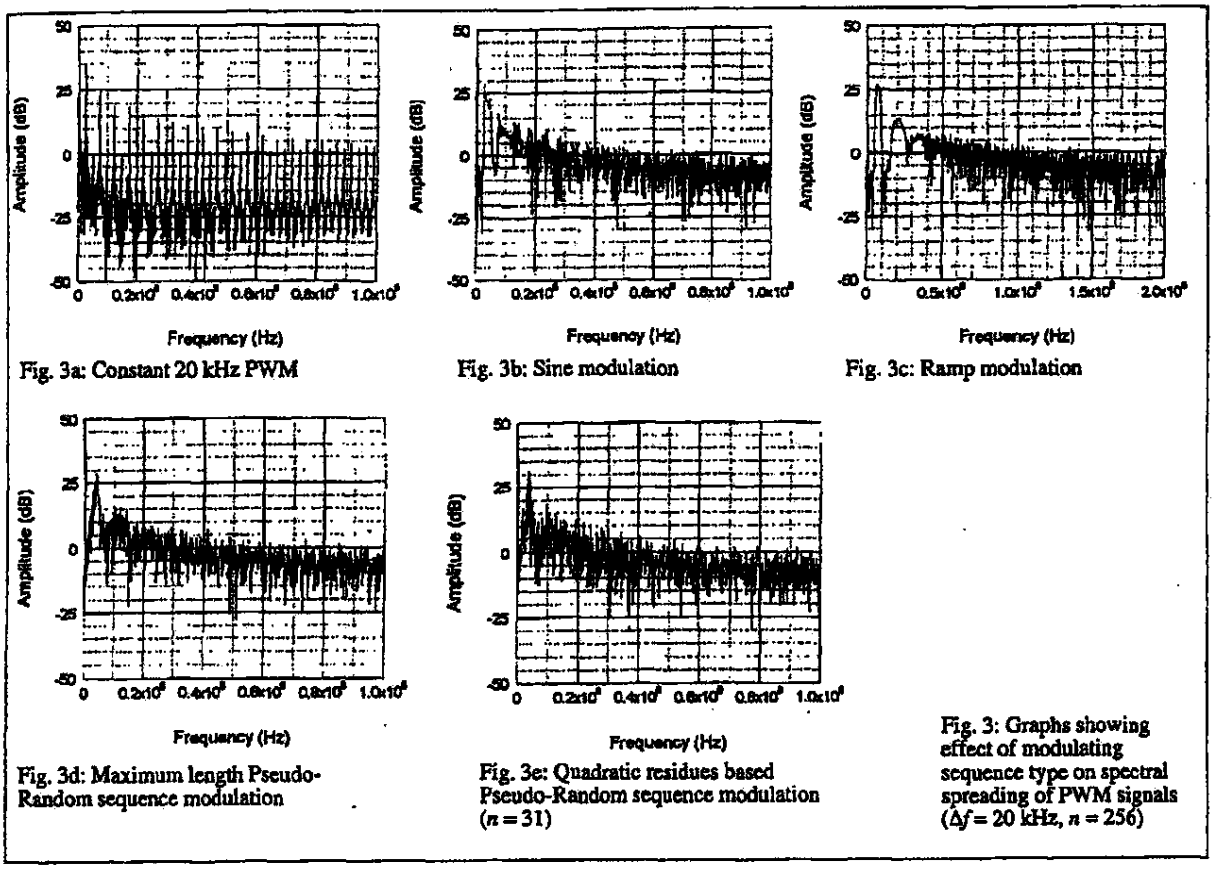

Fig. 3a: Constant 20 kHz PWM

Fig. 3b: Sine modulation

Fig. 3c: Ramp modulation

Fig. 3d: Maximum length Pseudo-Random sequence modulation

Fig. 3e: Quadratic residues based Pseudo-Random sequence modulation ($n = 31$)

Fig. 3: Graphs showing effect of modulating sequence type on spectral spreading of PWM signals ($\Delta f = 20$ kHz, $n = 256$)

EMI measurement techniques

One major factor affecting the amount of spectral spreading measured in practice due to modulation techniques, is the resolution bandwidth (RBW) of the measuring system. Whilst it is theoretically possible to spread the spectral energy from the unmodulated carrier frequency to a large number of closely spaced frequencies, if they all fall within the RBW of the measurement system they will appear at the same frequency, thus defeating the object of the spectral spreading. The European Commission (EC) EMC regulations require conducted emissions to be carried out with a RBW of 9 kHz for frequencies in the range 150 kHz $< f <$ 30 MHz. Therefore to ensure the effectiveness of the spread spectrum technique on the EMC measurements, the signal bandwidth should be greater than the bandwidth of the measurement system. Also as the EMC compliance measurements are carried out with the spectrum analyser set for quasi-peak detection, and the quasi-peak detector charge and discharge time constants are 1 ms and 160 ms respectively for a 9 kHz RBW, the effect of the modulating sequence length on the sequence repetition period needs to be considered.

Practical implications of Δf and T.

The use of a large Δf places a requirement on the design of the magnetic and output filter components in the switched-mode power converter, both in terms of the ripple current magnitude which will be maximum at low frequency, and the losses which will increase with frequency. It also puts loss constraints on the semiconductors as switching losses are proportional to frequency. Practically, a limit will be imposed on the sequence repetition period T by the system control loop bandwidth, as to avoid output voltage ripple due to the modulating sequence, $1/T$ should be small with respect to the voltage loop bandwidth This implies a long modulating sequence. Care should also be taken to ensure the magnetic components are tightly wound to avoid the generation of electromagnetically induced audio noise due to the modulation sequence repetition frequency falling within the audio range.

Practical measurements

Validation of the results was carried out on a 75 W asymmetrical half bridge off-line forward converter capable of frequency hopping spread-spectrum modulation of the PWM carrier frequency. The modulation sequence is stored in EPROM giving a variable sequence length. The peak frequency deviation can be set independently of the sequence length. The conducted EMI measurements were carried out with a 150 kHz to 30 MHz line impedance stabilisation network (LISN), and a Farnell SSA1000A (150 kHz to 1 GHz) spectrum analyser. The pre-compliance measurements were carried out using the above system under computer control, running the EASY1 EMC measurement software. The tests were carried out with the SMPC delivering a constant 75 W output power to the load. The system specifications are:

Output Voltage: 50 V, Output Current: 1.5 A,
Input Line Voltage: 240 V_{rms}, 50 Hz.
Peak Frequency Variation, Δf: Variable up to 3 × Unmodulated Carrier Frequency, f_c.

Frequency Range of operation: f_c to $(f_c + \Delta f)$,
Sequence length: Variable from 7 to 257,
Sequences used: Sine wave, ramp, random (equation (7), with $q = 2, p = 3 \ldots 8$) & quadratic residue sequences (equation (8) with $p = 7, 17, 31, 61, 127$ & 257)

Fig. 4 shows the measured effect of frequency-hopping spread-spectrum modulation on the spectrum of the switched mode power supply line current. Fig. 4a is the measured spectrum of the unmodulated 20 kHz PWM waveform, Fig. 4b is the spectrum taken when the PWM signal is modulated with $\Delta f = 20$ kHz and a sequence length of 257. The results show a lowering of the peak levels by up to 10 dB. The spectra were taken with a RBW of 1 kHz on the spectrum analyser.

Whilst Fig 4 shows a reduction in peak levels, the RBW of the spectrum analyser is not consistent with that required for an EMC test (9 kHz). The effect of spread spectrum modulation on the line current spectrum measured with the pre-requisite 9 kHz RBW is shown in Fig 5. These also show a reduction of peak levels (4 to 6 dB in this case). To accommodate the larger RBW of the test system, the measurement span was increased to 1 MHz. To fulfil the EC EMC standard tests, measurements were carried out at peak frequencies using the quasi peak detector in the pre-compliance test system. Table 1 lists representative measurements at various frequencies.

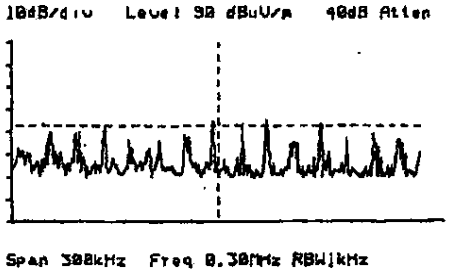

Fig. 4a: Constant 20 kHz PWM

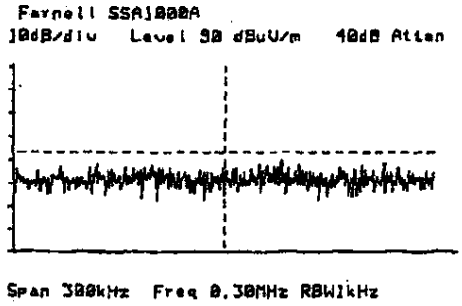

Fig. 4b: Quadratic residues based sequence modulation ($\Delta f = 20$ kHz, $n = 257$)

Fig. 4: Plots showing the effect of modulation with a quadratic residues based sequence on spectral spreading of PWM signals; RBW of spectrum analyser = 1 kHz

Conclusions

It has been shown that it is possible to reduce the peak levels in the PWM power density spectrum by the use of frequency-hopping spread spectrum modulation. Results have been presented showing the effect of both the length and the shape of modulating sequence used, and the depth to which the PWM carrier frequency is modulated. It has also been shown that the technique reduces the peak levels at the 9 kHz RBW of the measuring equipment, as specified in the EC EMC standards, and may reduce the quasi peak measured levels by at least 6 dB. Whilst it is recognised that this technique does not dissipate the generated interference energy, and does not directly address the other sources of noise generation in a SMPC, such as reverse recovery of the secondary diodes, the results show that modulation of the PWM carrier frequency may ease the filtering and shielding requirements of a switched mode power converter system by spreading the spectral energy contained in the high order harmonics of the switching frequency.

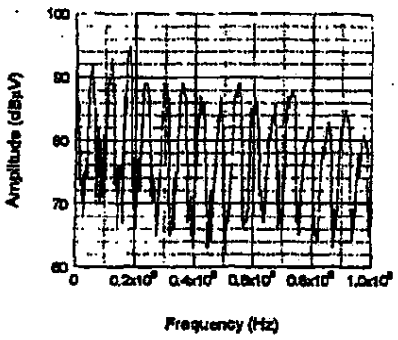

Fig. 5a: Constant 20 kHz PWM

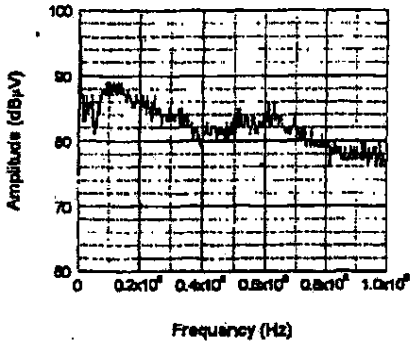

Fig. 5b: Quadratic residues based sequence modulation ($\Delta f = 20$ kHz, $n = 257$)

Fig. 5: Graphs showing effect of modulating sequence on spectral spreading of PWM signals ($\Delta f = 20$ kHz, $n = 257$), RBW of spectrum analyser - 9 kHz

Table 1: Reduction in quasi-peak measured values at various peak frequencies from Fig 5b

Quasi-Peak Measurements			
Peak Frequency	Constant frequency PWM	Spread spectrum PWM	Reduction in level
183.60kHz	94dBmV	88dBmV	6dBmV
554.20kHz	89dBmV	81dBmV	8dBmV
917.20kHz	85dBmV	76dBmV	9dBmV

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EXHIBIT 21
(Effect Of Spread-Spectrum Modulation Of Switched Mode Power Converter PWM)

Effect of spread-spectrum modulation of switched mode power converter PWM carrier frequencies on conducted EMI

D.A. Stone and B. Chambers

Indexing terms: Power electronics, Power convertors, Electromagnetic compatibility, Electromagnetic interference, Switched mode power supplies, Frequency agility

The effect on conducted interference of the application of frequency-hopping spread-spectrum modulation techniques to the PWM carrier frequency of switched mode power converters has been investigated. Preliminary results show this technique is capable of a 10dB reduction in conducted interference levels.

Introduction: Recent introduction of the European electromagnetic compatibility (EMC) legislation [1] has spurred on research into conducted and radiated electromagnetic interference (EMI). Switched mode power converters form a major source of conducted interference, and require a mains input filter to prevent the generated interference reaching the utility supply. Increased use of high frequency switching in pulse width modulated (PWM) systems leads to conducted interference generation at harmonics of the PWM carrier frequency. To pass the relevant EMC standards, it is necessary to ensure that the unwanted spectral power density of these harmonics is reduced as much as possible. The peak energy at any given harmonic may be lowered, while distributing the energy to additional harmonics, by modulating the PWM carrier frequency. Previously, this has been achieved by preprogramming, and periodic accessing of the turn-on and turn-off times of the PWM waveform [2]. However, this requires the storage of both the turn-on and turn-off times for a given period in EPROM and a requirement for more than one sequence to be stored for significantly different duty cycles, with small variations from a stored duty cycle being achieved by interpolation. A second technique invokes the narrowband sinusoidal frequency modulation of the PWM carrier [3], which is achieved by an analogue implementation. This Letter shows how the spectral spreading effect may also be achieved by utilising digital frequency-hopping (FH) spread-spectrum techniques.

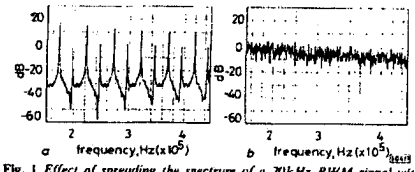

Fig. 1 *Effect of spreading the spectrum of a 20kHz PWM signal with quadratic residue based sequence (span = 150 – 450kHz)*

a Harmonics of constant frequency 20kHz PWM
b 20kHz PWM signal spread with a QR based sequence of length 263

Frequency-hopping spread-spectrum: The spreading of energy from one frequency across a number of frequencies may be carried out by spread-spectrum modulation. The FH spread-spectrum technique is the most applicable to switched mode power converters (SMPCs) as it invokes the changing of the PWM carrier frequency at regular intervals, usually at the end of each switching cycle. This gives a 'dwell-time' at each frequency of $1/f$, where f is the frequency for a particular cycle. The extent to which energy is spread around the spectrum is dependent on the dispersion factor $\beta = T\Delta f$ where Δf = peak frequency deviation of the carrier wave, and T = period of repetition of the modulating sequence. Fig. 1 shows both the spectrum of a constant frequency 20kHz PWM signal, and the predicted effect on the spectrum if the PWM signal is modulated with a quadratic residues-based sequence of length 263, and having a peak carrier frequency deviation Δf = 20kHz (frequency spread from f to $2f$). The quadratic residue (QR) sequence was generated from the equation $X_n = n^2 \bmod p$ where p is a prime number, and $n \in \{1, 2, ..., p\}$ [4]. It is also possible to generate maximal length pseudorandom sequences by using the equation $X_{n+1} = (aX_n + b) \bmod c$ where $c = 2^p$, $b = 2q + 1$, $a = 4b + 1$, and p, q are any integers. These maximal length pseudorandom sequences exhibit very similar spectral spreading characteristics to the QR based sequences, but as the QR based sequences exhibit a symmetry about the central number in the sequence, they would require just over 50% of the memory overhead required to store a maximal length pseudorandom sequence.

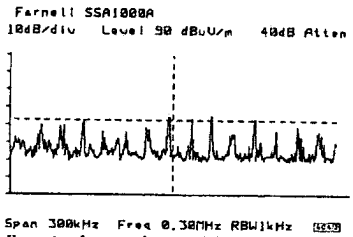

Fig. 2 *Harmonics of constant frequency 20kHz PWM*

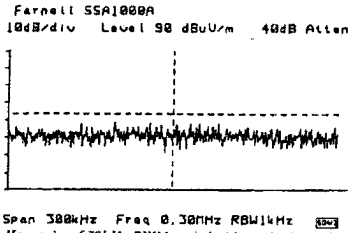

Fig. 3 *Harmonics of 20kHz PWM spread with quadratic residue based sequence (Δf = 2 kHz, n = 263)*

EMI measurements: In practice, the effect of spectral spreading is limited by the resolution bandwidth (RBW) of the measurement system. Since it is theoretically possible to spread the energy from a single frequency to a large number of closely spaced frequencies, if they all fall within the RBW of the measurement system they will appear as one signal. Therefore, care must be taken to ensure that the signal bandwidth is larger than that of the measurement system. Preliminary results, shown in Figs. 2 and 3, illustrate the measured effect of FH spread-spectrum modulation on the conducted interference generated by a 75W asymmetrical half-bridge converter. The original PWM carrier frequency was at 20kHz, and under modulation, this signal was spread from 20 to 22kHz (Δf = 2kHz) with a quadratic residues based sequence of length n = 263. The plots show a frequency span of 150 – 450kHz, taken with a spectrum analyser RBW of 1kHz. From Fig. 2 it may be seen that there is a 10dB reduction in the peak amplitudes of the harmonics, while the energy is spread across the spectrum, thus raising the background level. The measurements were taken with a Farnell SSA1000A (150kHz – 1GHz) spectrum analyser, 150kHz – 30MHz line impedance stabilisation network (LISN), and the SMPC delivering a constant 75W output power.

Conclusions: We have shown the possibility of reducing the peak levels of measured conducted EMI from SMPCs with the use of FH spread spectrum modulation of the PWM carrier frequency. This may be practically achieved with short sequence lengths based on quadratic-residues-derived sequences, which could be integrated into the SMPC control circuits without much additional memory overhead.

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Realisation of immittance functions with complex singularities by means of modified Antoniou GIC

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Indexing terms: Impedance convertors, Gyrators, Operational amplifiers

The Antoniou general immittance convertor (GIC) has been widely used in the active simulation of inductances. However, when only resistors and capacitors are used in its structure, the simulated immittance function has all singularities on the real negative axis in the complex plane. A modified version of the Antoniou GIC, to obtain immittance functions with both real and complex poles and zeros, is proposed.

Introduction: Since 1967 when Antoniou [1] proposed the opamp based structure of Fig. 1 as a gyrator, this circuit has been intensively used in active impedance simulation [2, 3] and active filter synthesis [2, 4]. Other realisations of general immittance convertors based on other electronic devices (current conveyors [5], OTAs [6] and operational mirrored amplifiers [7]) have been reported. However, at least in low frequency applications, operational amplifiers remain intensively used devices.

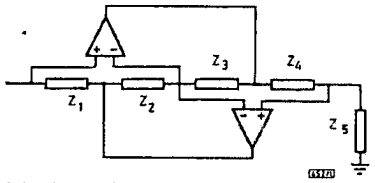

Fig. 1 *Antoniou general immittance convertor*

The input impedance presented by the circuit of Fig. 1 is

$$Z_{in}(s) = \frac{Z_1(s)Z_3(s)Z_5(s)}{Z_2(s)Z_4(s)} \quad (1)$$

When the embedded impedances $Z_i (i = 1, ..., 5)$ are RC impedances, the simulated immittance function has all its zeros and poles on the negative real axis in the s-plane. To obtain a pair of complex conjugate singularities, it is necessary to introduce inductors in the GIC structure, which is unacceptable in active realisations or IC implementations.

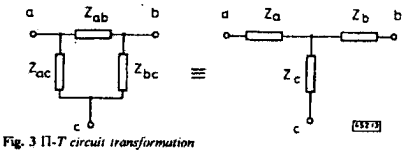

Fig. 3 Π-T *circuit transformation*

Realisation of series and parallel RLC impedances: Two particular cases of immittance functions with complex singularities are the series and parallel RLC impedances. To obtain an active impedance simulator able to provide such functions, the circuit of Fig. 1 was modified by replacing the impedances Z_1 and Z_2 with Π circuits as is shown in Fig. 2. Making use of the Π-T transformations (see Fig. 3),

$$Z_a = \frac{Z_{ab}Z_{ac}}{Z_{ab} + Z_{ac} + Z_{bc}} \quad Z_b = \frac{Z_{ab}Z_{bc}}{Z_{ab} + Z_{ac} + Z_{bc}}$$
$$Z_c = \frac{Z_{bc}Z_{ac}}{Z_{ab} + Z_{ac} + Z_{bc}} \quad (2)$$

we obtain the equivalent structures of Fig. 4, exhibiting input impedances given by

$$(i) \quad Z_{in} = \frac{Z_{1a}Z_3Z_5}{(Z_{1b} + Z_2)Z_4} = \frac{Z_{1ab}Z_{1ac}Z_3Z_5}{Z_4[Z_2(Z_{1ab} + Z_{1ac} + Z_{1bc}) + Z_{1ab}Z_{1bc}]} \quad (3)$$

$$(ii) \quad Z_{in} = \frac{(Z_1 + Z_{2a})Z_3Z_5}{Z_{2b}Z_4} = \frac{[Z_1(Z_{2ab} + Z_{2ac} + Z_{2bc}) + Z_{2ab}Z_{2ac}]Z_3Z_5}{Z_{2ab}Z_{2bc}Z_4} \quad (4)$$

respectively. Note that in the circuits of Fig. 4, the equivalent impedances Z_{1c} and Z_b do not affect the expressions of $Z_{in}(s)$.

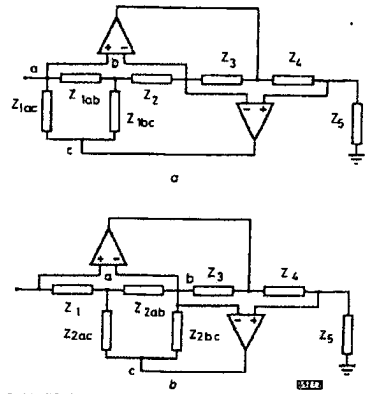

Fig. 2 *Modified structures of Antoniou GIC able to perform parallel RLC and series RLC impedance simulation*

a Parallel
b Series

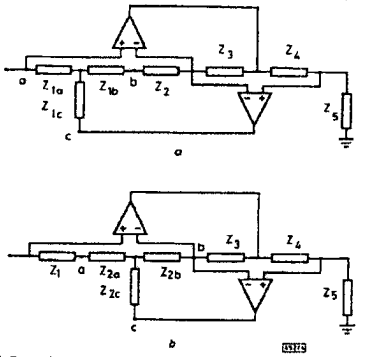

Fig. 4 *Equivalent circuits for structures of Fig. 2 obtained through Π-T transformations*

EXHIBIT 22
(Analysis and Synthesis of Randomized Modulation Schemes for Power Converters)

Analysis and Synthesis of Randomized Modulation Schemes for Power Converters

Aleksandar M. Stanković, *Member, IEEE*, George C. Verghese, *Member, IEEE*, and David J. Perreault, *Member, IEEE*

Abstract—**After establishing that the proper objects of study for randomized modulation of converters are the power spectra of signals, we classify such modulation schemes and present associated spectral formulas, several of which are new. We also discuss numerical (Monte Carlo) verification issues for power spectral formulas. A general spectral formula for stationary randomized modulation schemes is presented, and specialized to several modulation schemes of practical interest for dc/dc converters. Analytical results are then given for block-stationary randomized modulation schemes that are suitable for inverter operation. In the process, we present results for several modulation schemes that have been reported in the literature without analytical explanations. Experimental verifications of some of our analytical results are presented. We formulate narrow-band and wide-band synthesis problems in randomized modulation, and solve them numerically. Our results suggest that randomized modulation is very effective in satisfying narrow-band power constraints, but has limited effectiveness in meeting wide-band constraints.**

I. Introduction

RANDOMIZED modulation is of increasing interest in power electronics. While implementation results have been impressive, theoretical analysis has been limited so far. This paper and the thesis [39] describe the basic theoretical framework needed to address analysis and synthesis problems for a large variety of randomized switching schemes, and they also provide representative results.

Over the last three decades power converter designers have resorted to randomized switching for different reasons. The randomized switching concept apparently originated [6] at a time when the switching frequency in dc/dc converters was typically limited to the audible range. Faster devices eventually offered a simple solution to the acoustic noise problem, at least in dc/dc conversion, and randomized switching was set aside. As PWM technology and microprocessors matured during the early eighties, new methods became available to address the effects of acoustic noise and of electromagnetic interference (EMI). While most of the engineering effort was directed toward the optimization of deterministic PWM waveforms ("programmed switching"), an alternative in the form of randomized modulation using a microprocessor implementation was offered for dc/ac conversion in [48]. The same idea has been pursued in a dc/dc setup in [45], and in numerous references afterwards, for example [11], [2], [20], [49], [47], [21], [19], [12], [3], [44], [37], and [35]. When compared with standard, periodic switching, randomized modulation tends to increase the maximal time excursions of output waveforms that depend on the switching function. These waveforms, however, cease to be periodic and their properties in the time domain are best characterized in a probabilistic framework.

As pointed out in [50], programmed and randomized switching are complementary techniques, and by combining them a designer can achieve improved results. The theoretical setup needed to analyze randomized switching schemes is, however, quite different from the deterministic PWM analysis approach. The natural quantity to study in a randomized switching setup is the **power spectrum** (the Fourier transform of the **autocorrelation** of a signal), and not the harmonic spectrum (i.e., the Fourier transform of the signal itself). Note that the Fourier transform of a random signal is itself a random function, i.e., it is a random variable at each frequency. The power spectrum, on the other hand, has much better properties and can be estimated reliably from the available signal (see, for example, [36]).

The lack of a proper framework for analyzing randomized modulation is, in our opinion, the main reason why most references contain only rudimentary analysis, and rely on plausibility arguments. Judging by a sharp increase in the number of papers describing randomized switching implementations (over a dozen in 1992 alone), there exists a definite need for a unifying analysis framework. This will not only make evaluation and verification of different schemes possible, but will also point out capabilities and limitations of randomized modulation, which are largely not known at present.

Section II of this paper classifies randomized modulation schemes. Section III provides an interpretation of present standards for harmonic distortion that allows them to be applied to the power spectra arising from randomized modulation. Section IV introduces the autocorrelation and power spectrum for the class of signals of interest. In Section V we discuss issues in numerical (Monte Carlo) verification of power spectral formulas. Section VI characterizes the class of stationary randomized modulation schemes, presents a general formula for the power spectra of associated switching functions, and describes specializations to randomized modulation procedures of practical interest in dc/dc converters. The power spectrum of a waveform that is related to the switching function through a linear time-invariant relation is easily derived from the power spectrum of the switching function. However, not all

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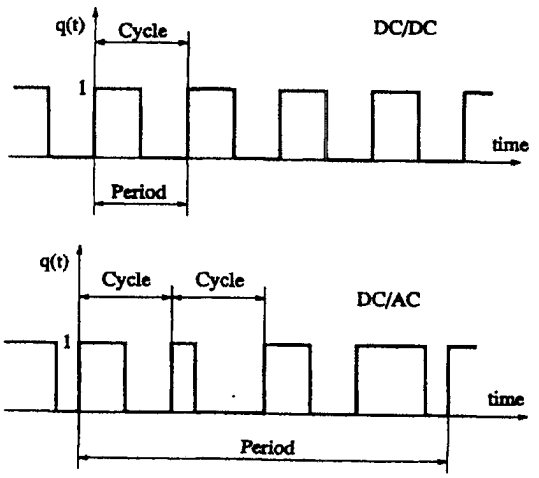

Fig. 1. Nominal switching functions in power converters: (a) dc/dc converters, and (b) dc/ac converters.

waveforms of interest are this simply related to the switching function, and Section VII illustrates how to deal with these cases. Section VIII discusses block-stationary randomized modulation schemes that are suitable for dc/ac converters. In Section IX we discuss synthesis problems in randomized modulation, and present numerical results that suggest that randomized modulation is well suited to meet narrow-band constraints, while it is much less effective in satisfying wide-band constraints.

II. Classification of Randomized Switching Strategies

To find a common ground for comparisons among different randomized modulation methods, we concentrate on the switching function, denoted by $q(t)$, which takes the value 0 when the controllable converter switch is off, and the value 1 when it is on (see Fig. 1). As already mentioned, the power spectra of variables related to $q(t)$ by linear, time–invariant operations can easily be derived from the power spectrum of $q(t)$. Power spectra for waveforms that are not related to $q(t)$ by such operations take more effort to determine (see Section VII).

The main elements characterizing randomized modulation schemes are the underlying (deterministic) nominal switching patterns and the probability laws governing the random dithering of the nominal patterns. We have to check if the nominal patterns, e.g., duty ratios, vary from one cycle to the next, as they do in inverter operation. The other issue is the time variation of the probability densities used to pick the dither at each cycle. If the probabilistic structure is constant from cycle to cycle, we call the switching **stationary**; if it is constant only over a block of cycles (as in inverters), we call it **block-stationary**. More general Markovian schemes, where the probability density used for dither at a cycle depends on past cycles via the state of a Markov chain at the beginning of that cycle are discussed in [39], [41], and [42].

The basic **analysis** problem in randomized modulation is to relate the spectral characteristics of $q(t)$ and other related waveforms in a converter to the probabilistic structure that governs the dithering. The **synthesis** problem in randomized modulation is to design a randomized switching procedure that minimizes given criteria for power spectra. Practically useful synthesis procedures include the minimization of discrete spectral components (which we term narrow–band optimization), and the minimization of signal power in a given frequency segment (which we call wide-band optimization); these are examined in Section IX, see also [39] and [41].

III. Performance Specifications

International standards for power electronic converters [8], [32], [38], [26], [5], [46], [51], [17], [18] that operate off an electric utility or in an FCC regulated environment are aimed at periodically operated converters, and are given in terms of Fourier components of the relevant waveforms. Thus, constraints are on the harmonic spectrum, rather than on the power spectrum, Note, however, that the power density spectrum of a periodic function comprises impulses at the fundamental and its harmonics, with strengths that are the squares of the magnitudes of the corresponding Fourier components. We can therefore map existing standards to the power spectrum domain by simply squaring them. These power spectral constraints can the be carried over to the nonperiodic waveforms obtained by randomized modulation. Thus, we interpret the standards as follows:

- Take the constraints on the power density spectrum to equal the square of the magnitudes of the allowed harmonic spectrum at any given frequency.
- For lower frequencies, where limits on the strength of the 60 Hz (or 50 Hz) fundamental are specified in existing standards, take the corresponding power to be associated with the total signal power in the frequency segment that extends halfway toward the neighboring harmonics.

Present military standards are the only specifications with both narrow-band and wide-band limits: the signal power for waveforms of interest is subject to an integral constraint over a band of frequencies (e.g., of 1 MHz width in the MHz range), in addition to the more common narrow-band constraints that are part of all civilian standards. The latest draft of new military standards [30] replaces the two constraints with a "medium-band" constraint (10 kHz in the MHz range). It is shown in [39] that this revision of standards favors randomized modulation.

IV. Autocorrelation and Power Spectrum

A **random signal** may be thought of as a signal selected from an ensemble (family) of possible signals by a random experiment governed by some specification of probabilities. The ensemble and the specification of probabilities together comprise what is termed the **random process** (or stochastic process) generating the random signal. The signal is termed a realization of the process. We shall not distinguish notationally between the process and a realization of it.

The (time–averaged) **autocorrelation** of a continuous-time random process $x(t)$ is defined as

$$R_x(\tau) = \lim_{W\to\infty} \frac{1}{2W} \int_{-W}^{W} E[x(t)x(\tau + t)]dt \qquad (1)$$

where the expectation operation $E[\cdot]$is taken over the whole ensemble. (The more common definition omits the time-averaging, but the definition in (1) specializes in the desired way to deterministic signals, where the ensemble consists of just a single member.) The **power density spectrum** $S_x(f)$ is defined as the Fourier transform of $R_x(\tau)$:

$$S_x(f) = \int_{-\infty}^{\infty} e^{-j2\pi f\tau} R_x(\tau) d\tau. \tag{2}$$

In cases of practical interest $S_x(f)$ can have both a continuous and an impulsive part [4], [52], [24]. The impulsive part of $S_x(f)$ is referred to as the **discrete** spectrum, and is characterized entirely by the locations $f_1, f_2, \ldots$ of the impulses ("line frequencies", "harmonic frequencies") and by positive numbers $p_1, p_2, \ldots$ representing the strengths of the impulses, which equal the signal power at the harmonic frequencies. When integrated over a frequency range, the continuous part of $S_x(f)$ yields the signal power in that frequency range.

An important result for applications concerns the transformation of the autocorrelation of a process $x(t)$ when it is passed through a stable linear, time-invariant filter. Such a filter is characterized by its impulse response $h(t)$ and corresponding frequency response $H(f)$, which is the Fourier transform of $h(t)$. The output $y(t)$ of the system is given by convolution

$$y(t) = \int_{-\infty}^{\infty} x(t)h(t-u)du. \tag{3}$$

Using this relation, it can be shown [52] that the process $y(t)$ has a well-defined autocorrelation, whenever x does, and that its power spectrum is

$$S_y(f) = \mid H(f) \mid^2 S_x(f). \tag{4}$$

This relation can be used to evaluate the power spectrum of any waveform related to the switching waveform $q(t)$ through a convolution, once the power spectrum of $q(t)$ is known.

A random process $x(t)$ for which

$$E(x(t)) = m_x \tag{5}$$

and

$$E[x(t)x(t+\tau)] = R_x(\tau), \quad \forall t, \tau \tag{6}$$

is termed wide-sense stationary (WSS, weakly stationary). Thus, a WSS random process has a mean and autocorrelation that are independent of the time origin (so that the time averaging in (1) becomes unnecessary). Any stationary randomized modulation generates a switching function that is wide-sense stationary. This can be shown rigorously using the concept of regenerative processes [24]. Special cases of this result can also be found in [9], for example, or in [1] which uses theory of stationary point processes.

Let $X_{2W}(f)$ denote the Fourier transform of the symmetrically **truncated** version of $x(t)$, extending from $-W$ to $+W$. An important result of the Fourier theory [4], [7], [23] due to Einstein, Wiener and Khintchine, shows that if $x(t)$ is a wide-sense stationary process then $S_x(f)$ is related to $X_{2W}(f)$ as follows:

$$S_x(f) = \lim_{W\to\infty} E(\frac{1}{2W} \mid X_{2W}(f) \mid^2). \tag{7}$$

The quantity $\frac{1}{2W} \mid X_{2W}(f) \mid^2$ is called the **periodogram** of $x(t)$. For nonstationary processes that have a well defined autocorrelation via (1), a weaker version of (7) holds, where the equality is in the sense of distributions.

V. Verification Issues

The formulas that will be developed shortly for power spectra of different randomized modulation schemes are rather involved, and a need arises to verify and explore them through simulation. (We also provide experimental verification in some cases.) The power spectrum of a (Monte Carlo) simulation of a randomized switching waveform $q(t)$ is obtained through an estimation procedure. Power spectrum estimation is one of the most important problems in signal processing and has a very rich history [34], [25], [31], [36], [27].

The discussion in this section deals primarily with direct estimation methods that yield estimates of the power spectrum $S_q(f)$ without first estimating the autocorrelation. We concentrate on nonparametric, classical estimation methods, which are well understood and for which software is readily available [36].

Classical direct estimation methods may be thought of as approximate implementations of the operations specified in the Wiener-Khintchine theorem (7). Typically, a single sampled-data realization of the random process of duration $2KW$ is divided into K sections, and the (sampled-data version of the) periodogram is computed for each section. The availability of the Fast Fourier Transform (FFT) to calculate the Fourier transforms involved is a major advantage. The expectation operation in (7) is then approximated by averaging the K individual periodograms. This is referred to as Bartlett's method. Under appropriate conditions (related to ergodicity of the stochastic process, which permits time averages to be substituted for ensemble averages) this computation produces a consistent, asymptotically unbiased estimate of the power spectrum [14], [36], so the estimate converges to the true spectrum as $K \to \infty, W \to \infty$. We shall assume that the switching functions $q(t)$ of interest to us satisfy the conditions required for validity of such an estimation procedure. The close match between our analytical formulas and the Monte Carlo verifications suggest that this is indeed a good assumption.

Although the above estimation procedure is asymptotically unbiased, in practice K and W are finite, so there is inevitable bias. The use of appropriate windows in the time domain contributes to bias reduction. An unpleasant effect of windowing is known as leakage and has its source in the frequency-domain sidelobes of the windows used.

Welch [36] modified Bartlett's method by allowing data segments to overlap, in addition to windowing data in the time domain. This method is widely used and is available in the Matlab [28] software package. A 50% overlap between the data segments produces good results in many applications [36].

A brief discussion of the choice of parameters in implementing Welch's method is presented next; some further discussion may be found in [40]. Let N denote the number of data points in the simulated random signal, let M denote the number of points in a data segment ($N = KM$), and let R denote

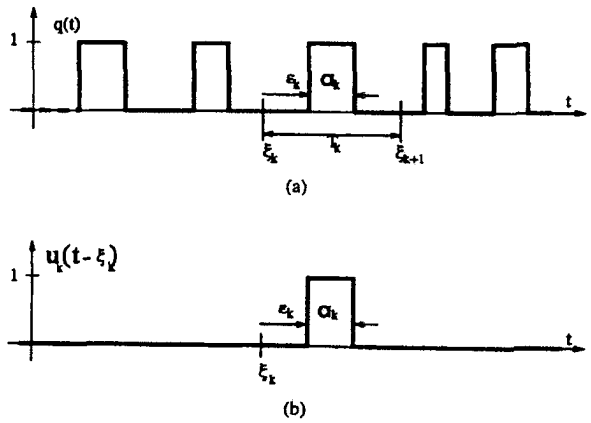

Fig. 2. (a) The switching waveform $q(t)$, and (b) the pulse $u_k(t-\xi_k)$ representing just the k–th cycle of $q(t)$.

the number of points per cycle of the switching function $q(t)$. If R is set to 64, so that the duty ratio resolution is better that 2%, then the spectrum can be estimated up to the 32nd harmonic (which is the Nyquist frequency). The spectral estimate contains $M/2$ points (for positive frequency), and if 32 points per unit frequency are desired, then $M = 2048$. Thus, if $K = 8$, a total of $N = 16,384$ points is needed, which is reasonable within the Matlab package. Given a constraint on N, either M can be increased, thus improving resolution but decreasing K and getting a more "jittery" estimate, or K can be increased, thus reducing the frequency resolution but obtaining smoother estimates. An overlap of $M/2$ between the data segments improves the estimation results, essentially by increasing the effective number of data segments K, while keeping N fixed.

The trade-offs in spectral estimation described in this section apply directly to digital spectral analyzers [13]. Similar trade-offs arise with analog systems for spectral analysis [29], [10] which utilize band-pass filters to isolate a narrow frequency band of interest, followed by squaring devices and low–frequency filters to provide a spectral estimate.

VI. Stationary Randomized Modulation Schemes

Stationary randomized modulation schemes are characterized by invariant deterministic and probabilistic structure, namely:

- The nominal or reference on-off pattern that is being dithered does not change from one switching cycle to the next—there are no variations in the requirements on average quantities such as the duty ratio;
- At each new cycle, the same probabilistic structure is used—the dithering (in time) is based on independent trials.

Stationary switching schemes can be further classified, and the most important classes are randomized pulse position modulation (PPM), randomized pulse width modulation (PWM), and asynchronous schemes [45], [43].

Referring to Fig. 2(a), ξ_k is the time at which the k-th cycle starts, T_k is the duration of the kth cycle, a_k is the duration of the on-state within this cycle, and ε_k is the delay to the turn–on within the cycle. Note that the duty ratio is $d_k = a_k/T_k$. The switching function $q(t)$ that we analyze consists of a concatenation of such switching cycles.

In general, one can dither ε_k, d_k, or T_k, individually or simultaneously. Some combinations used in power electronics are

- randomized pulse position modulation (PPM): ε_k changes; T_k, a_k fixed;
- randomized pulse width modulation (PWM): a_k changes; $\varepsilon_k = 0$; T_k fixed;
- simplified asynchronous modulation [43]: T_k changes; a_k fixed;
- asynchronous modulation [45]: T_k changes; $\varepsilon_k = 0$; d_k fixed.

The tools for analysis of the first three cases have been available from the communication theory literature of the 1960s [29], [22]. This literature seems to have been largely overlooked by the power electronics community. Results for all four categories are presented here.

A. A General Formula for Stationary Randomized Modulation

With $u_k(t-\xi_k)$ denoting the single-pulse waveform defined in Fig. 2(b), we can write the switching function as

$$q(t) = \sum_{k=-\infty}^{\infty} u_k(t-\xi_k). \tag{8}$$

Let $U_k(f)$ denote the Fourier transform of $u_k(t)$. The power spectrum of $q(t)$ can now be computed using the procedure described in detail in [39] and based on [29]. This procedure in effect computes the autocorrelation and takes its Fourier transform, exactly as required by the definition of power spectrum. Alternatively, one could derive the power-spectrum using the Wiener-Khintchine relation (7). The result is

$$S_q(f) = \frac{1}{T}\sum_{k=-\infty}^{\infty} E[U_0(f)U_k^*(f)e^{j2\pi f(\xi_k-\xi_0)}] \tag{9}$$

where T is $E[T_k]$, the expected duration of a cycle.

The result (9), in which $U_k(f)$ is a function of ε_k, a_k, d_k, T_k and possibly other randomization parameters, is very general. The specialization of this formula to various stationary randomized modulation schemes of interest in power electronics is considered in the following subsections. A case of great practical interest is where the randomized modulation in different cycles is based on statistically independent trials and where all cycles are of duration T, but the duration a_k and/or position ε_k of the pulse are randomized. In this case the expectation in formula (9) factors into a product of expectations, and we add and subtract the term $|E[U(f)]|^2/T$ that corresponds to $k = 0$. After invoking the Poisson identity [29]

$$\sum_{k=-\infty}^{\infty} e^{j2\pi kfT} = \frac{1}{T}\sum_{k=-\infty}^{\infty}\delta(f-\frac{k}{T})$$

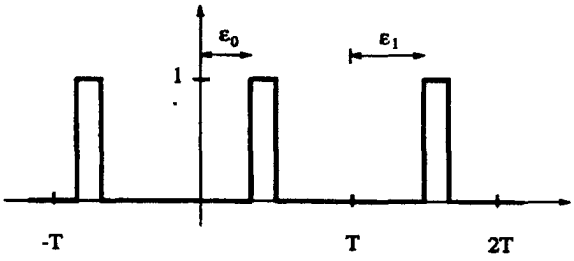

Fig. 3. Randomized pulse position modulation (PPM).

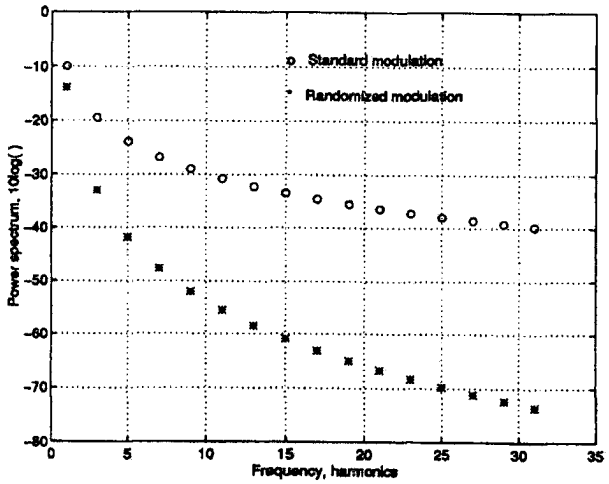

Fig. 4. Discrete spectrum: Comparison of conventional and randomized PPM modulation, period $T = 1$, duty ratio $D = 0.5$.

the power spectrum is shown to equal

$$S_q(f) = \frac{1}{T}\{E[|\,U(f)\,|^2] - |\,E[U(f)]\,|^2 + \frac{1}{T}\,|\,E[U(f)]\,|^2 \sum_{k=-\infty}^{\infty} \delta(f - \frac{k}{T})\} \quad (10)$$

where we have dropped the now unnecessary subscript on $U_k(f)$.

B. Randomized Pulse Position Modulation

In this section the case of randomized pulse position modulation (PPM) is considered, where each cycle has the same length T, and the pulse in each cycle has the same duration a, but now we allow an independent random variation in the position ε_k of the pulse in the k-th cycle, see Fig. 3. Let the probability density function for ε be $p_\varepsilon(t)$ and let the Fourier transform (or characteristic function) of this be denoted by $P_\varepsilon(f)$. We also introduce the notation $\bar{U}(f)$ for the Fourier transform of a rectangular pulse of width a that starts at 0, so that $U(f) = \bar{U}(f)e^{-j2\pi f\varepsilon}$. Then $E[|\,U(f)\,|^2] = |\,\bar{U}(f)\,|^2$ and $E[U(f)] = \bar{U}(f)P_\varepsilon(f)$, so (10) becomes

$$S_q(f) = \frac{|\,U_0(f)\,|^2}{T}\{(1 - |\,P_\varepsilon(f)\,|^2) + \frac{|\,P_\varepsilon(f)\,|^2}{T} \sum_{k=-\infty}^{\infty} \delta(f - \frac{k}{T})\}. \quad (11)$$

This expression is found, for example, in [29].

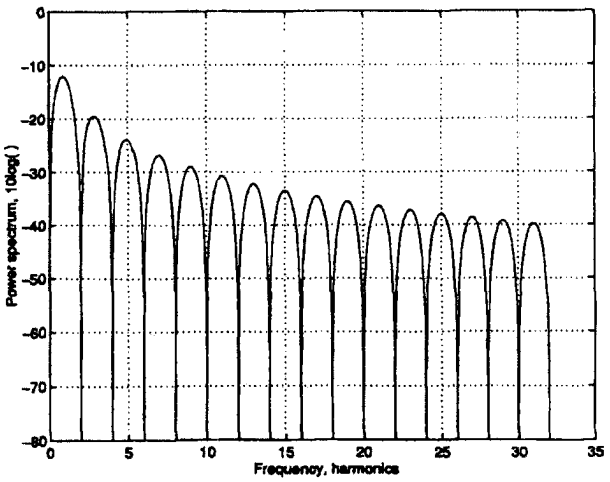

Fig. 5. Continuous spectrum: Randomized PPM, period $T = 1$, duty ratio $D = 0.5$.

As an example, assume $T = 1$. Then for rectangular pulses of width D

$$S_q(f) = (\frac{\sin(\pi f D)}{\pi f})^2 \cdot\{(1 - |\,P_\varepsilon(f)\,|^2) + |\,P_\varepsilon(f)\,|^2 \sum_{k=-\infty}^{\infty} \delta(f - k)\}. \quad (12)$$

The nondithered case is easily recovered. For $\varepsilon_i = 0$, $p_\varepsilon(t) = \delta(t)$, and $P_\varepsilon(f) = 1$, so

$$S_q(f) = (\frac{\sin(\pi f D)}{\pi f})^2 \sum_{k=-\infty}^{\infty} \delta(f - k) \quad (13)$$

as expected for a periodic train of rectangular pulses.

Since $p_\varepsilon(t)$ is a probability density function, it must integrate to 1, so $P_\varepsilon(0) = 1$. Given that $|\,P_\varepsilon(f)\,| \leq 1$ [33], and that from Parseval's equality

$$\int_{-\infty}^{\infty} |\,P_\varepsilon(f)\,|^2 = 1, \quad (14)$$

it follows that $|\,P_\varepsilon(f)\,| < 1$ in some frequency range. The expression (12) shows that in this frequency range the discrete part of the spectrum will be decreased, when compared to the conventional switching strategy. The price paid for this result is the introduction of the continuous part of the spectrum (the "fill-in"), $(\sin(\pi f D)/\pi f)^2(1 - |\,P_\varepsilon(f)\,|^2)$. This might be quite acceptable, given the predominantly narrow-band form of the standards described in Section III, and this is the rationale behind a growing number of applications of randomized modulation.

For illustration, specialize to $D = 0.5$ and ε_i uniformly distributed in the interval $[0, (1 - D)T]$, or $[0, 0.5]$. For these values, the discrete, nondithered spectrum is shown in Fig. 4 together with the discrete spectrum for randomized PPM, and the continuous spectrum is shown in Fig. 5.

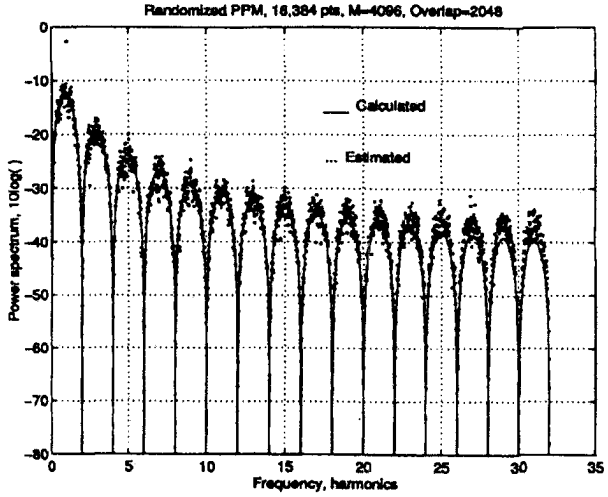

Fig. 6. Randomized PPM: Estimated and calculated spectrum, with $M = 4096$ points.

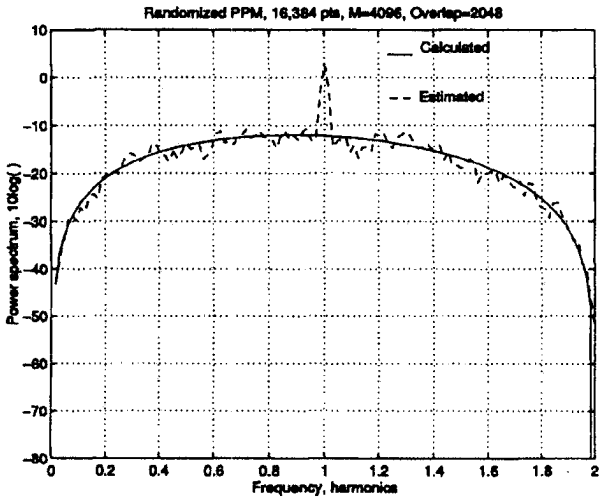

Fig. 7. Randomized PPM: Estimated and calculated spectrum, first two harmonics, corresponding to $M = 4096$ points.

We now describe the application of Welch's method (which is implemented in the signal processing toolbox of the Matlab package) to numerically verify (12) via Monte Carlo simulations, following Section V. The parameter values for the simulation are $D = 0.5$ and $T = 1$, as in the previous example. In each cycle, a random number uniformly distributed between 0 and 0.5 is chosen as the offset for the pulse, and the waveform for that pulse is thereby completely defined. A total of 256 cycles is generated, with 64 samples in each cycle. The total number of points is thus $N = 16,384$ and the width of an individual data segment M can be varied. The approximate frequency resolution of Welch's method, defined as the minimum distance of two distinguishable sinusoids, is approximately $41/M$ in this case [36].

In Figs. 6 and 7 the estimated power spectrum (dotted) is shown together with the calculated continuous spectrum from (12). Welch's procedure generates the estimate of the total power spectrum, i.e., of the sum of continuous and discrete spectra, so the large deviations between the estimated and calculated continuous spectrum near the peaks are due to discrete spectral components. This remark holds for all examples presented in this paper. The general agreement with the calculated continuous spectrum is good.

In Fig. 7 the first two harmonics are magnified. These figures show a "jittery" estimate, as expected for the large $M(= N/4)$ that we have used. To estimate the coefficient associated with the impulse at the unit frequency, we can proceed as follows. From the known width of the frequency segment, $1/64$ for this particular value of M, a value of 0.0296 is obtained for the area of the peak centered at $f = 1$, and 0.0083 and 0.0084 for the neighboring segments (of width $1/64$ each) to the left and right, respectively. The calculated value for the discrete component at $f = 1$ is 0.0411, and the integrals of the calculated continuous spectral component over segments of width $1/64$ to the left and to the right are only 0.0009. The discrepancy in total signal power over all three segments between the estimated and calculated spectra is approximately 5%. The reason for looking at the contributions of three segments rather than one is the spectral "leak" inevitable due to windowing in the time domain [36]. In this particular case the frequency resolution (defined as the minimum frequency difference between the two sinusoids that permits them to be resolved) is approximately 0.01 [36], while the width of a frequency segment is $1/64 = 0.015$. Thus, when estimating coefficients associated with impulses it is necessary to take into account the spectral leak by integrating the signal power over a sufficiently wide frequency segment, and subtracting the contribution of the continuous spectrum.

C. Randomized Pulse Width Modulation

In randomized pulse width modulation (PWM), the on-state duration a_k is varied within a fixed period T. Consider the case where $T = 1$ and a_k lies in the interval $[0, 1]$, with a uniform probability density. With $\alpha = \pi f$, the spectrum is given by

$$S_q(f) = \frac{1}{4\alpha^2}\left[1 - \frac{\sin^2\alpha}{\alpha^2} + \frac{\sin^4\alpha + (\alpha - \sin\alpha\cos\alpha)^2}{\alpha^2} \sum_{k=-\infty}^{\infty} \delta(f-k)\right]. \tag{15}$$

This result is presented in [29] with an unfortunate typographical error (the term α^2 is missing in the last fraction). Conventional switching yields the discrete spectrum given in Fig. 8; the figure also shows the discrete spectrum for randomized PWM. Randomized PWM yields discrete harmonics at even multiples of the switching frequency as well (for $D = 0.5$ conventional modulation has only odd harmonics). In this example, randomized PWM reduces the fundamental more than randomized PPM does (see Fig. 4), but randomized PPM is more efficient at reducing the higher discrete harmonics. The continuous spectrum for randomized PWM is given in Fig. 9, which can be contrasted with the result for randomized PPM in Fig. 5.

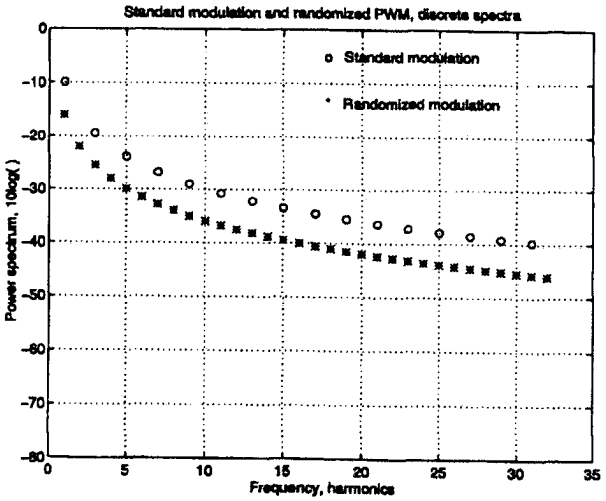

Fig. 8. Discrete spectrum: Comparison of conventional and randomized PWM modulation, period $T = 1$, duty ratio $D = 0.5$, pulse width uniformly distributed in the interval $[0,\ T]$.

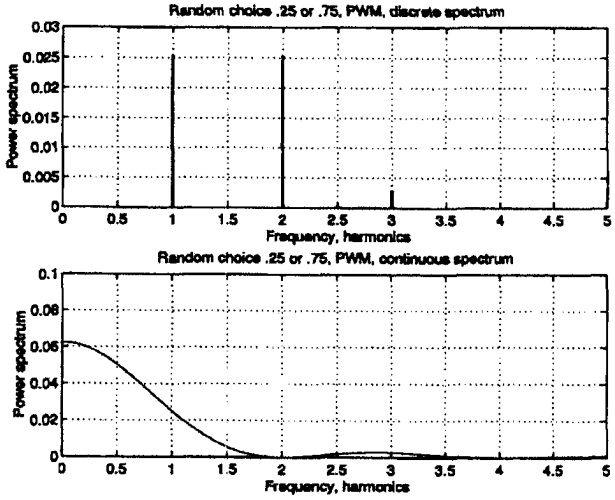

Fig. 10. Randomized PWM: Calculated discrete and continuous spectrum, period $T = 1$, equally probable pulses of duration 0.25 and 0.75.

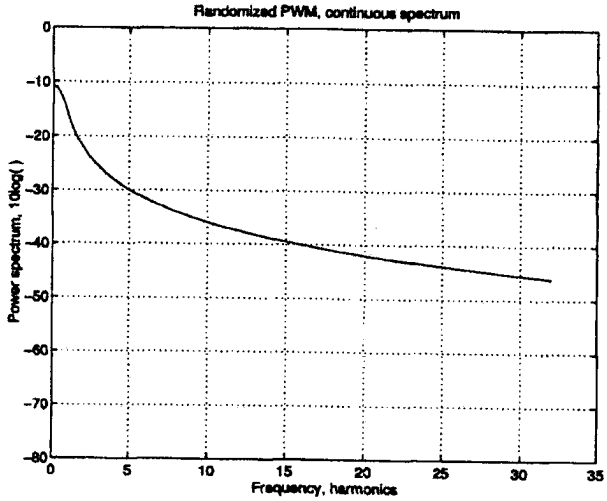

Fig. 9. Continuous spectrum: Randomized PWM, period $T = 1$, duty ratio $D = 0.5$, pulse width uniformly distributed in the interval $[0,\ T]$.

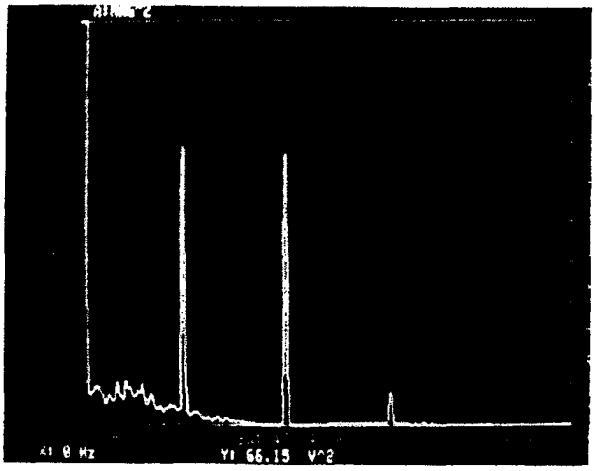

Fig. 11. Randomized PWM: Measured power spectrum, equally probable pulses of durations 0.25 and 0.75.

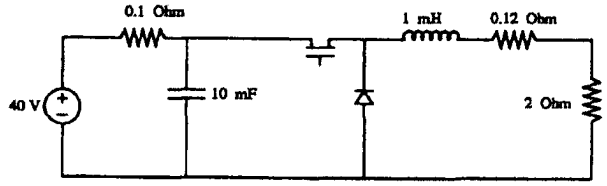

Fig. 12. Buck converter used in verification of power spectral formulas for stationary modulation.

Another case of interest is the example of equally probable pulses of lengths 0.25 and 0.75. In this case application of (10) goes as follows. The Fourier transform of a single unit pulse of duration a_k equals $U(f) = (1 - e^{-j2\pi a_k})/(j2\pi f)$. After taking into account that a_k can take only two values, namely 0.25 and 0.75, we obtain

$$E[|\ U(f)\ |^2] = \frac{1}{(2\pi f)^2}[2 - \cos(\frac{2\pi f}{4}) - \cos(\frac{6\pi f}{4})] \quad (16)$$

and

$$E[U(f)] = \frac{1}{2}[\frac{1 - e^{-j2\pi f 0.25}}{j2\pi f} + \frac{1 - e^{-j2\pi f 0.75}}{j2\pi f}]. \quad (17)$$

Then the formula (10) yields the power spectrum shown in Fig. 10. These theoretical results can be compared with the experimental results for a buck converter shown in Fig. 11. Good agreement can be observed.

We have used the buck converter circuit shown in Fig. 12 to obtain experimental verification of some of our formulas for power spectra under randomized modulation. The fundamental switching frequency in this circuit is 10 kHz. The transistor in our implementation is controlled by a microprocessor, which

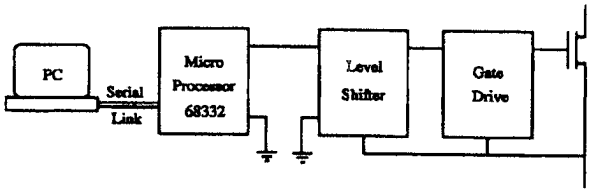

Fig. 13. Block diagram of the experimental setup for verification of power spectral formulas in randomized modulation.

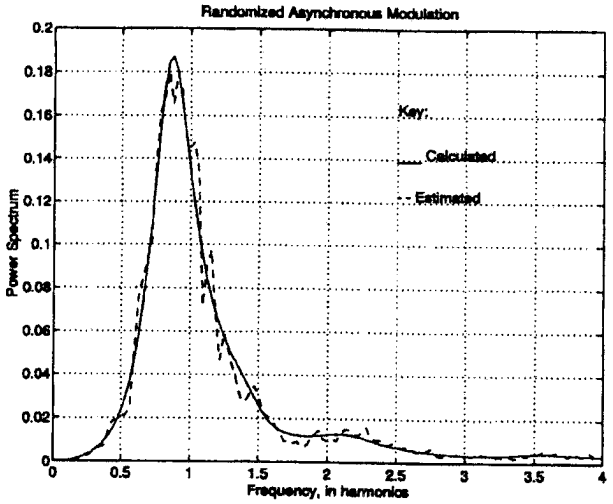

Fig. 14. Calculated and estimated power spectra for $q(t)$ in asynchronous modulation.

is in turn connected to a personal computer. The main role of the personal computer is to facilitate development of the microcode for randomized switching. A block diagram of the experimental system is shown in Fig. 13. Note, however, that practical randomized modulation schemes can be implemented with much simpler hardware, for example with a pseudo-random number generator and auxiliary circuitry.

D. Randomized Aperiodic Modulation

In this section we consider the **asynchronous** dc/dc randomized modulation scheme introduced (but without power spectral formulas) in [45]. In this scheme, the lengths of successive cycles T_k are randomized, while the duty ratio is kept fixed at its nominal value. The scheme is different from the simplified asynchronous version used by the same authors later [43], in which T_k is again random, but the duration of the on-state is constant. This latter simplified scheme has been analyzed in [29] and [22], building on a formula for the power spectrum of a dithered impulse train. The original scheme in [45], where the duty ratio is fixed, is harder to analyze, as two **correlated** dithered impulse trains have to be used; this is the case we treat here.

At this point in our development we can either specialize the formula (9) to the case of aperiodic randomized modulation, or build on the formula presented in [22] for the power spectrum of a dithered impulse train. It has been shown in [39] that both approaches lead to the same results. If we denote by $P_T(f)$

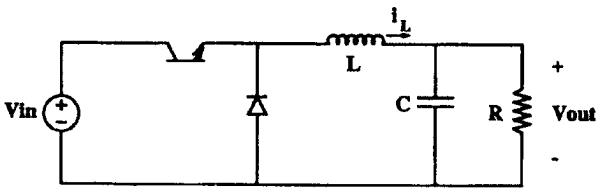

Fig. 15. Standard configuration of a buck dc/dc converter.

the Fourier transform of the probability density function used to determine successive cycle lengths T_k, then our derivation [39] shows that the power spectrum of the asynchronous pulse train is

$$S_q(f) = \frac{2}{(2\pi f)^2}\left[1 + Re\left(\frac{P_T(f)}{1 - P_T(f)}\right) + Re\left(\frac{P_T^2(\frac{f}{2})}{1 - P_T(f)}\right) - 2Re\left(\frac{P_T(\frac{f}{2})}{1 - P_T(f)}\right)\right]. \quad (18)$$

(Note that $P_T(f) \neq 1$ for $f > 0$, unless T_k is governed by a very special "lattice" probability density function; this case is addressed in [39]).

In Fig. 14 we show the calculated spectrum (dotted line) computed using (18), and the estimated spectrum obtained via Monte Carlo simulations and Welch's estimation method, see Section V. The agreement is evidently very good.

VII. Current Spectra

Our results so far allow us to directly determine the power spectra of certain other waveforms in power converters from the spectrum of the switching function $q(t)$. A simple analysis of the standard buck converter [15] shown in Fig. 15 establishes that the inductor current equals the **integral** of

$$\frac{q(t)V_{in} - V_{out}}{L}$$

where V_{in} is the input voltage, V_{out} is the output voltage, and $q(t)$ is the switching function. The average (dc) component of the inductor current is controlled by a separate (outer loop) controller. This allows us to apply (4) to determining the power spectrum of the inductor current at positive frequencies:

$$S_{iL}(f) = \frac{V_{in}}{L}\frac{1}{f^2}S_q(f). \quad (19)$$

For that case calculated and measured spectra are given in Figs. 16 and 17, and good agreement is evident.

Similar relations between the switching function and the inductor current can be observed for other basic dc/dc converters in the continuous conduction mode. In the case of a standard boost converter [15], the inductor current (which happens to be the input current) is the integral of

$$\frac{V_{in} - V_{out} + q(t)V_{out}}{L}$$

In the case of an buck/boost converter, the inductor current is the integral of

$$\frac{q(t)(V_{in} + V_{out}) - V_{out}}{L}.$$

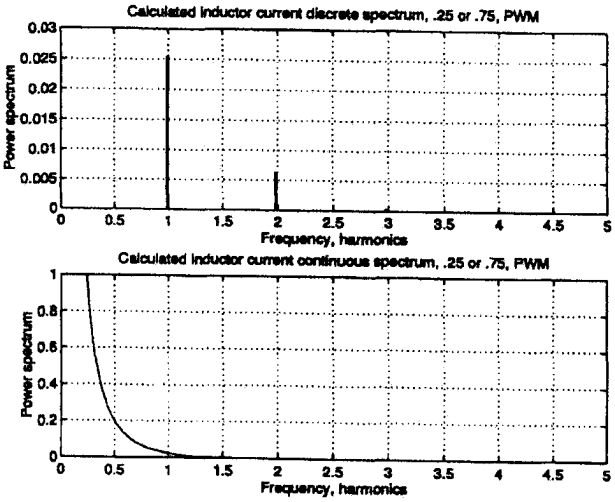

Fig. 16. Calculated spectrum of the inductor current for a buck converter in continuous conduction mode with randomized PWM.

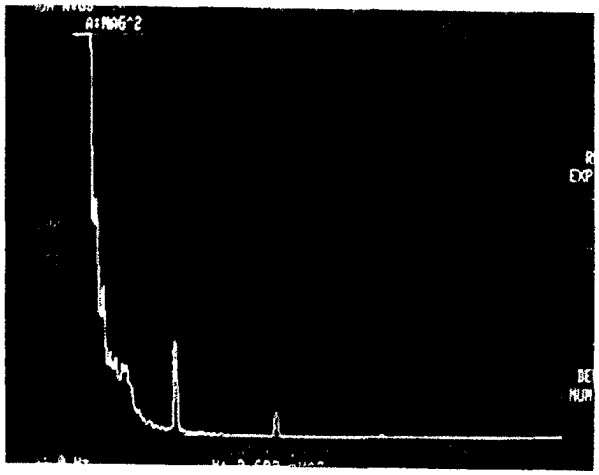

Fig. 17. Measured spectrum of the inductor current for a buck converter in continuous conduction mode with randomized PWM.

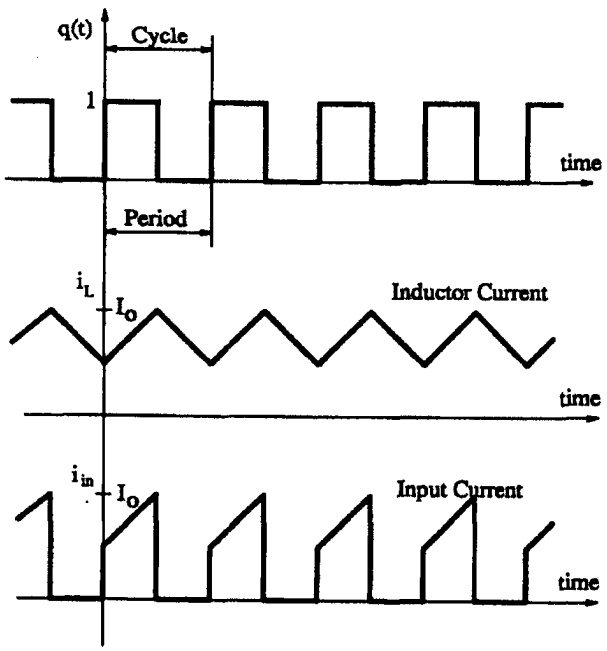

Fig. 18. Nominal switching function, inductor current, and input current for a buck converter in continuous conduction mode.

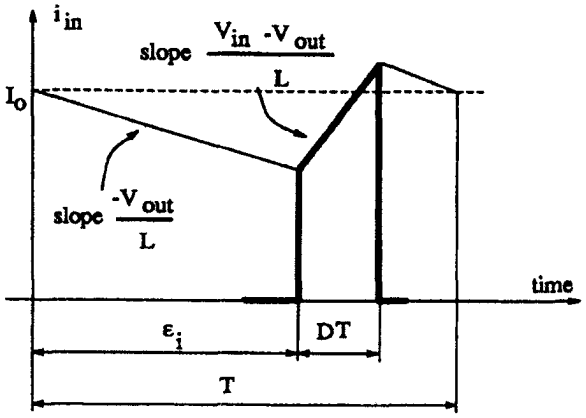

Fig. 19. Input current for a buck converter in continuous conduction mode with randomized PPM.

Analogous relationships could be derived for output voltages V_{out}.

Computation of the power spectrum of the **input** current in buck and buck/boost converters is more intricate. In the remainder of this section, we show how (10) can be used to determine the spectrum of the input current for these converters.

Fig. 18 applies to a buck converter operating in continuous conduction mode, and shows a typical nominal switching function, together with the nominal inductor current and the input current. The input current at the kth cycle under randomized PPM is shown in Fig. 19. Note that the inductor current at the beginning of each dithered cycle is still at its nominal value I_0. The input current at the kth cycle depends only on ε_k, and we can specialize (10) to that case. $U(f)$ is the Fourier transform of the input current waveform, a single cycle of which is shown in Fig. 19. After writing equations for the straight line segments shown in Fig. 19, $U(f)$ turns out to be (for $f > 0$):

$$U(f) = \{(I_0 - \frac{V_{out}\varepsilon}{L})\frac{\sin(\pi f DT)}{\pi f} e^{-j\pi f DT} + \frac{V_{in} - V_{out}}{j2\pi f L} e^{-j\pi f DT}[\frac{\sin(\pi f DT)}{\pi f} - DTe^{-j\pi f DT}]\}e^{-j2\pi f\varepsilon}. \quad (20)$$

Equation (10) can then be evaluated, once probability densities for ε are specified. As an example, we consider the case of randomized pulse position modulation where the delay ε_k is either 0, or $T/2$, each with probability 1/2. For this case calculated and simulated spectra are given in Fig. 20 (there are no discrete spectral components in this example).

It turns out that the power spectrum of the input current in buck and buck/boost converters is harder to calculate for some other randomized modulation schemes, notably for randomized PWM.

VIII. Randomized Modulation for Inverters

In this section, the nominal on–off pattern is assumed to change from one switching cycle to the next, but repeats periodically over a **block** of cycles, as would be required for inverter operation. The randomization then involves dithering this pattern in each cycle using a set of mutually independent trials with a statistical structure that remains constant from block to block, hence the label of block-stationary randomized modulation. Most of the results presented here are either novel, or represent generalizations of previously available results. Their derivation follows the one outlined in Section VI-A, but requires additional algebraic manipulations. We restrict ourselves to single-phase schemes. Power spectra for line-to-line or line-to-neutral variables in a **three-phase** system can be found easily, once the spectrum corresponding to one phase is known.

Two modulation schemes of particular interest in practice are block-stationary PPM and block-stationary aperiodic modulation. In this section we consider block-stationary PPM, and refer the interested reader to [39] for details on block-stationary aperiodic modulation.

Consider the case of N cycles in a block (see Fig. 1 (b)), with possibly different cycle lengths T_k, and possibly different probability densities (with characteristic functions P_k). Let $U_k(f)$ denote the Fourier transform of the pulse $u_k(t)$ in the k-th cycle of the block (defined with respect to a time origin at the start of the corresponding cycle), and let

$$U(f) = \begin{bmatrix} U_1(f) \\ U_2(f)e^{-j2\pi f T_1} \\ \vdots \\ U_N(f)e^{-j2\pi f \sum_{k=1}^{N-1} T_k} \end{bmatrix}$$

and

$$\hat{U}(f) = \begin{bmatrix} U_1(f)P_1(f) \\ U_2(f)P_2(f)e^{-j2\pi f T_1} \\ \vdots \\ U_N(f)P_N(f)e^{-j2\pi f \sum_{k=1}^{N-1} T_k} \end{bmatrix}.$$

Let $\mathbf{1}$ denote an $N \times 1$ vector of ones, and let $\sum_1^N T_i = \bar{T}$. Then the power spectrum of the resulting waveform can be shown to equal

$$S_q(f) = \frac{1}{\bar{T}}(\|U\|^2 - \|\hat{U}\|^2) + \frac{1}{\bar{T}^2}\mathbf{1}^T\hat{U}\hat{U}^H\mathbf{1}\sum_{k=-\infty}^{\infty}\delta(f - \frac{k}{\bar{T}}) \tag{21}$$

where $\|U\|^2$ is the sum of magnitudes squared of the elements of vector U, and U^H is the complex conjugate transpose (Hermitian) of U. Note the similarity to (11). A special case of (21) governs the setup considered in [16].

We now present experimental verification for the previous formula, with an experimental circuit comprising a single phase of a three–phase inverter. The average switching frequency was kept at 250 Hz, as the experiments were aimed at verifying our analytical results. Consider the case $N = 2$, with uniform dither between 0 and $\frac{T}{4} = 0.25$. The basic pulses have $D_1 = 0.25$ and $D_2 = 0.75$. The reference case of deterministic switching with alternate duty ratios D_1 and D_2 is shown in Fig. 21. The calculated spectrum for this randomized PPM is given in Fig. 22. The results shown in Fig. 22 are in close agreement with the experimental results for the same case, which are shown in Fig. 23. In this example the discrepancies between theoretical and experimental results for discrete harmonics are under 5%.

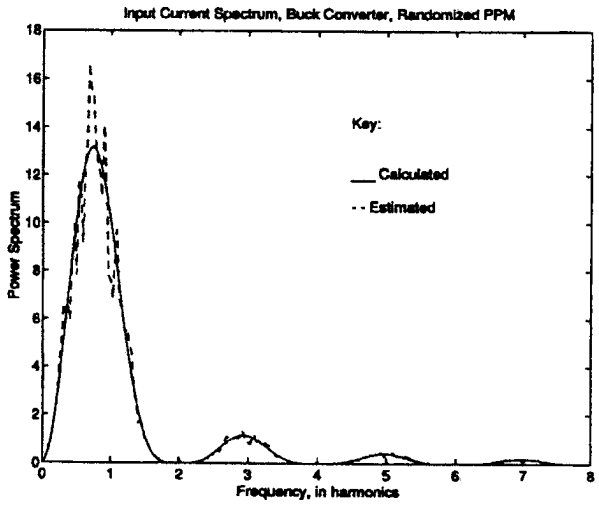

Fig. 20. Calculated and simulated spectrum of the input current for a buck converter in continuous conduction mode with randomized PPM.

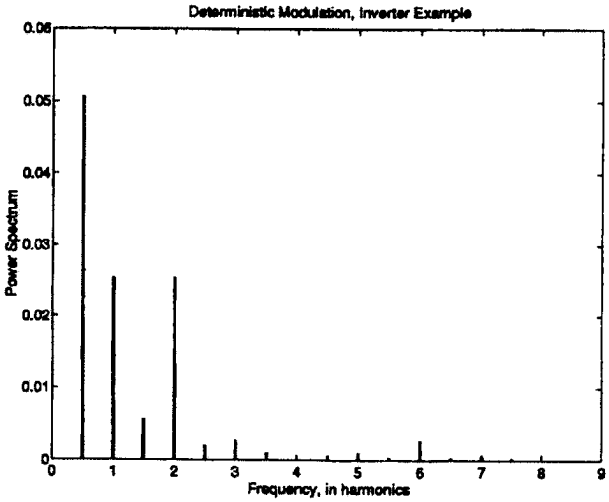

Fig. 21. Calculated power spectrum in deterministic modulation example.

IX. Synthesis Problems

In this section the goal is to explore how effective randomized modulation is in achieving various performance specifications in the frequency domain. Desirable properties of power

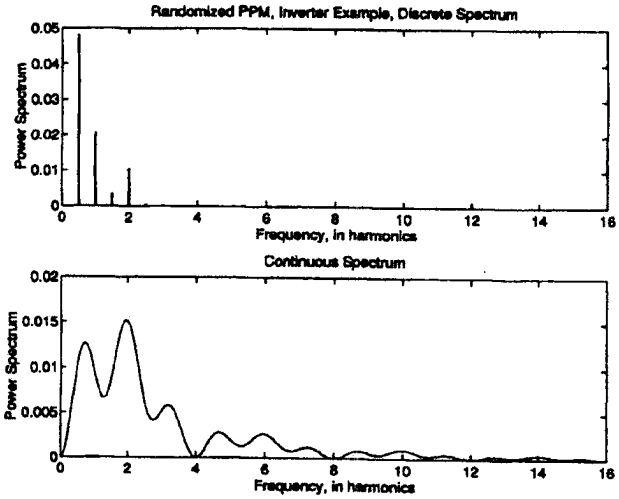

Fig. 22. Calculated spectrum for block-stationary randomized modulation example.

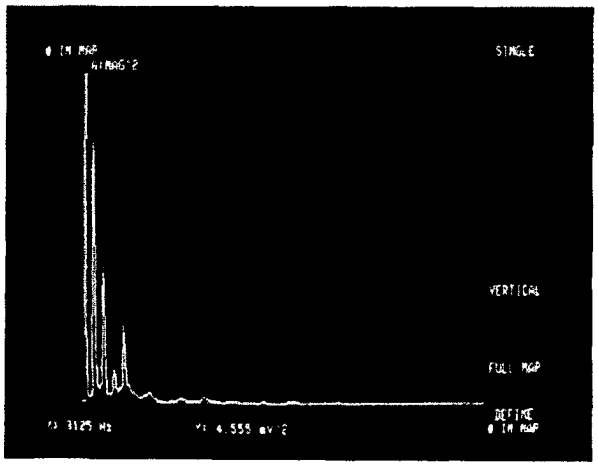

Fig. 23. Measured power spectrum in block-stationary randomized modulation example.

spectra are dependent on the particular application. Requirements of particular interest in practice are the following:

- Minimization of one or multiple, possibly weighted, discrete harmonics. This criterion corresponds to cases where narrow-band characteristics of discrete harmonics are particularly harmful, as for example in acoustic noise, or in narrow-band interference.
- Minimization of signal power (integral of the power spectrum) in a frequency segment that is of the order of an integral multiple of the switching frequency. This criterion corresponds to wide-band constraints in military specifications, and it could be of interest for EMI interference problems.

All the optimization problems in this section are presented for the case of randomized PPM. Formulations for other modulation schemes are analogous, and could be specified using the analytic expressions derived in [39]. To streamline the notation, it is assumed that the period of the reference (deterministic) switching waveform is unity, $T = 1$. In this case the power spectrum for randomized PPM is given by (11):

$$S_q(f) = W(f)\{1 - |P(f)|^2 + |P(f)|^2 \sum_{k=-\infty}^{\infty} \delta(f-k)\} \tag{22}$$

where the non-negative function $W(f)$ represents the square of the Fourier transform of a rectangular pulse of unit height and width D centered at 0. Note that the kth discrete harmonic has intensity $|P(k)|^2$.

A typical narrow-band optimization criterion, which corresponds to the minimization of the sum of discrete harmonics between the l-th and L-th, can now be written as

$$J_{l,L}^{NB} = \sum_{k=l}^{L} W(k)\,|P(k)|^2 \tag{23}$$

where a weighting function could be absorbed in $W(f)$.

The wide-band optimization criterion used for illustration in this section corresponds to the minimization of the signal power for randomized PPM in the frequency segment [0 1.5], where the switching frequency is 1. This criterion can be written as

$$J_1^{WB} = \int_0^{\frac{3}{2}} W(f)(1 - |P(f)|^2)df + W(1)\,|P(1)|^2 . \tag{24}$$

Both the narrow-band criterion J^{NB} and the wide-band criterion J^{WB} are in general nonlinear in $P(f)$; in the PPM case, they are quadratic functions of $P(f)$.

The optimization process, which is performed in the frequency domain, has to generate a *function* that satisfies constraints in the time domain. In the case of stationary modulation schemes, the optimization is performed over the space of candidate probability densities $\mathcal{P}$. In all cases of practical interest these densities have finite support (extent). Not surprisingly, the performance achievable by randomized modulation depends on the extent of the imposed dither (i.e. the width of the support of the dither probability density), which is in turn limited by the duty ratio of the nominal switching waveforms. In the case of PPM, the dither is constrained to lie in the range $[0,\ 1 - D]$, where D is the nominal (undithered) duty ratio.

If global optimality of solutions to optimization problems in randomized modulation is needed, then a complete parametrization of the domain $\mathcal{P}$ *in the frequency domain* is required. None of the results from Fourier theory known to us establishes a complete parametrization of the set of $P(f)$, even in the absence of constraints in the time domain. Thus, for our optimization purposes, we make do with partial parametrizations of the domain $\mathcal{P}$. Several simple parametrizations of $\mathcal{P}$ were used in our numerical procedures, and together they enable optimization over many probability distributions of interest in implementations. The parametrizations used in the optimization problems here are defined in the time domain as

$$p(t) = \sum_{l=1}^{N} \alpha_l p_l(t) \tag{25}$$

TABLE I
NARROW-BAND OPTIMIZATION J_{41}^{NB}: CRIT. ($\times 10^4$)

Modulation	D=0.1	D=0.5	D=0.9
Undithered	450.0	1250.0	450.0
Point Masses	71.8	0.0	197.0
Hanning	3.3	153.0	232.0
Rectangles	3.5	208.0	242.0
Uniform	3.5	417.0	283.0
Uniform Pt. Masses	255.0	211.0	240.0

where the p_l are known probability densities (''basis functions'') with appropriate finite support, and the α_l are coefficients to be determined in the optimization. The coefficients satisfy $\sum_{l=1}^{N} \alpha_l = 1$, and $\alpha_l \geq 0$. It turns out that optimal probability densities obtained with different basis functions are very similar, and that they yield very similar performance in terms of the criterion values. This gives some assurance that the choice of basis functions is not critical for the optimization.

The basis functions used to parametrize the domain of candidate probability densities in this paper are

- rectangles, dividing the available probability density support ($[0, \ 1-D]$ in the PPM case) into N segments of equal width;
- Hanning windows (''raised cosine'' functions), with p_1 and p_N being ''half–windows''.
- discrete probability densities of N point masses summing to 1, at fixed or variable locations;
- β-densities, given (on the segment $[0, \ 1-D]$) by the expression

$$p(t) = \frac{1}{B(a,b)} t^{a-1} \ (1-t)^{b-1}$$

where $B(a,b)$ is the normalizing constant

$$B(a,b) = \int_0^{1-D} t^{a-1}(1-t)^{b-1} dt.$$

A β-density depends on only two parameters, and it can approximate probability densities having a single maximum or minimum.

Other probability densities used for comparison are the uniform density, and a density comprising N equally spaced probability masses with coefficients $\frac{1}{N}$.

Optimization of the narrow-band criterion $J_{1,41}^{NB} = J_{41}^{NB}$ is considered first, with $N = 4$ basis functions in each parametrization. The criterion values at the numerically computed optimum are given in Table I. These optimization results are in agreement with the intuition that in cases when there is a large ''dithering length'' available (i.e., when the nominal duty ratio D is small), then a large reduction in the size of harmonics should be achievable. Though none of our parametrizations for probability densities ends up being superior for all cases, the optimal solutions for different parametrizations are in fact similar. For example, for $D = 0.5$, the optimal rectangle coefficients are $[0.5, \ 0, \ 0, \ 0.5]$, while the optimal peak height ratios for the Hanning basis functions are $[0.5, \ 0, \ 0, \ 0.5]$ in general.

In the case of the duty ratio $D = 0.5$, with equal point masses at 0 and 0.5, the orthogonality of $W(f)$ and $|\ P(f)\ |$ yields 0 as the value of the criterion. This modulation scheme is sometimes referred to as *dual modulation*. Such extreme effectiveness in the reduction of discrete harmonics is not always a characteristic of randomized modulation, but it might account for some dramatic improvements reported in implementations.

The criterion J_1^{WB} is considered next, and results obtained for randomized PPM are given in Table II. The results suggest a limited effectiveness in reducing the total signal power in a wide frequency band (relative peak heights are given in the third column for the Hanning basis). Fig. 24 plots the optimal densities corresponding to the cases in Table II.

These examples suggest that randomized modulation is in general very effective in reducing the size of discrete components, thus providing a quantitative basis for widespread applications of randomized modulation to acoustic noise reduction. As pointed out earlier, the recent draft of new military specifications [30] introduces a single frequency

TABLE II
WIDE-BAND OPTIMIZATION J_1^{WB}, $D = 0.5$: CRIT. ($\times 10^4$)

Modulation	Criterion	Coefficients
Undithered	1013	
Point Masses	965	0.5 at 0.16 and 0.34
Hanning	973	[0.33, 0.17, 0.17, 0.33]
Rectangles	973	[0.35, 0.15, 0.15, 0.35]
β–density	975	$a = b = 0.76$

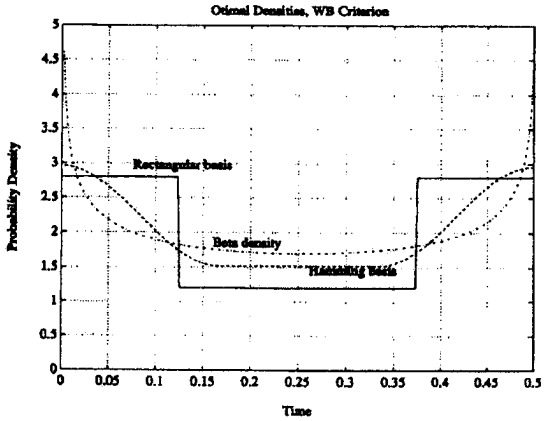

Fig. 24. Optimal probability densities in the wide-band optimization example.

window for all spectral measurements. For example, the width of that window is 10 kHz for measurements in the range 250 kHz–30 MHz, thus favoring randomized modulation for switching frequencies 10^5–10^6 Hz.

On the other hand, randomized modulation is much less effective in addressing wide-band spectral requirements. Spectral changes introduced by randomized modulation are mostly localized in frequency.

X. Conclusions

The main motivation for the use of randomized modulation so far has been the possibility of acoustic noise reduction in inverter-based motor drives. It is argued in this paper that randomized modulation could be beneficial for operation of any power converter. The main benefit from randomized switching strategies in this context is better utilization of the allowable harmonic content of waveforms at the equipment/utility interface. Randomized modulation is not merely a way to take advantage of present regulations, which have been written for a deterministic switching discipline, but also a flexible approach to solving problems caused by electromagnetic or acoustic noise. To that end, the analytical results presented here might serve as an aid to assessment of the potential benefits of randomized modulation, and as a basis for design.

We have presented results for the power spectra of the switching functions for various stationary randomized modulation schemes, and have analyzed input currents as examples of waveforms that are not related to the switching function through a linear relationship. Synthesis problems in randomized modulation were considered in the last section of the paper, where both optimization criteria and numerical results are described. It is shown that randomized modulation can be very efficient in reducing the size of discrete harmonics and in satisfying narrow-band constraints, but is much less effective in dealing with wide–band requirements.

Results on stationary modulation can be generalized additional cases, described in detail in [39]. If one randomized modulation scheme, say randomized PPM, is applied to an already aperiodically modulated pulse train, the procedure is denoted as *cascaded* randomized modulation. In *alternate* modulation two different randomized modulation schemes are applied in alternation. In *random choice* of randomized modulation, at each cycle a random choice between two modulation schemes is made, and independent random experiments are performed afterwards to get values for the associated random parameters. These results are described in [39].

Switching based on a Markov chain possesses additional generality when compared to the randomized switching strategies described in this paper. The switching pattern in each cycle is made dependent on the state of the underlying Markov chain, thus providing an additional degree of flexibility. State transition probabilities can be chosen so that large local deviations from desired average steady-state behavior are discouraged or prevented altogether. This permits simultaneous control of spectral characteristics and time-domain ripple, for instance. Results on randomized modulation governed by Markov chains are presented in [39] and [42].

Modern motor drive systems require tailored PWM schemes. Deterministic PWM optimization, often labeled "programmed switching," is very successful in meeting the wide-band spectral requirements, while it has deficiencies in dealing with narrow-band spectral constraints. This paper shows that randomized modulation could play a complementary role.

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David J. Perreault (S'91), for a photograph and biography, see p. 262 of the May 1995 issue of this TRANSACTIONS.

EXHIBIT 23
(Random Pulse Modulation With Applications to Power Electronic Converters)

RANDOM PULSE MODULATION WITH APPLICATIONS TO POWER ELECTRONIC CONVERTERS

by

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Submitted to the Department of Electrical Engineering and Computer Science
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Doctor of Philosophy in Electrical Engineering

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RANDOM PULSE MODULATION WITH APPLICATIONS TO POWER ELECTRONIC CONVERTERS

by

Aleksandar Mihajla Stanković

Submitted to the Department of Electrical Engineering and Computer Science on January, 1993, in partial fulfillment of the requirements for the degree of Doctor of Philosophy in Electrical Engineering

Abstract

The research presented in this thesis addresses random pulse modulation and its applications to power electronic converters. The thesis describes relevant power electronics implementations, international standards for harmonic distortion, and a unifying theoretical setup. The basic randomized switching strategies are classified, and verification issues for power spectrum formulas are given. The main elements characterizing a random modulation scheme are the nominal switching pattern and the probability laws governing deviations from the nominal. If both elements are constant from cycle to cycle, as would be the case for DC/DC converters, the corresponding modulation is denoted as stationary. The stationary random modulation schemes analyzed in the thesis include random pulse position modulation, random pulse width modulation, and aperiodic modulation. In block–stationary random modulation, the nominal pattern varies from cycle to cycle, but is repeated periodically over a block of cycles, as needed for inverter (DC/AC) operation. Novel formulas for power spectra of stationary and block–stationary random modulation are presented. Modulation schemes specified by Markov chains are suggested as a way to explicitly constrain time–domain deviations from a deterministic switching pattern. A new power spectral formula for periodic asynchronous Markov chains is derived. Approaches to synthesizing random modulation strategies with prescribed spectral properties are presented, and corresponding optimization problems are discussed. Monte–Carlo simulations and experimental results presented for stationary and block–stationary random modulation, as well as for random modulation based on Markov chains demonstrate the validity and usefulness of the analytical results developed in the thesis.

Thesis Supervisor: George C. Verghese
Title: Professor of Electrical Engineering

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The light shines in the darkness,

and the darkness has never put it out.

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Chapter 1

Introduction and Outline

Switching power converters are the most widespread systems in the area of power conditioning. The reasons for their popularity are numerous, the most outstanding being their ability to achieve a very high efficiency of operation, the capability to operate at different voltage and current levels, and the relative abundance of circuit topologies that can be matched to various requirements. The control of switching converters is an area of intensive growth [63],[106],[87],[11]. There exists an array of interesting control problems, motivated primarily by the wide range of operating conditions characterizing a power converter and the very constrained nature of control actions: one can only choose the instants at which power switches are closed or opened, to select one of a fairly small total number of circuit configurations. Many questions in power converter control are still not answered in sufficient detail (e.g. geometrical control [112], digital implementations [36]), while a host of new questions arise naturally when the robustness of operation is considered [25].

Switching Functions

The switching function for a given power switch, denoted by $q(t)$, is a time waveform taking the value 1 when the switch is on, and the value 0 when the switch is off. In the case of DC/DC converters, the nominal switching function is typically periodic, with a period equaling the duration of a single on–off cycle, as shown in the upper trace in Fig 1.1. In the case of DC/AC converters, the nominal switching function is often periodic, with a period that comprises several on–off cycles, as indicated by the

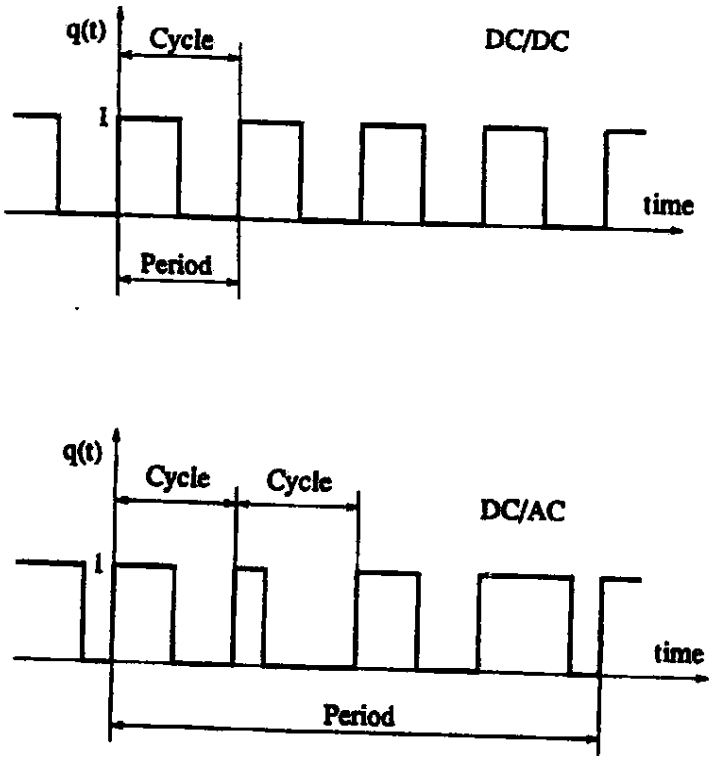


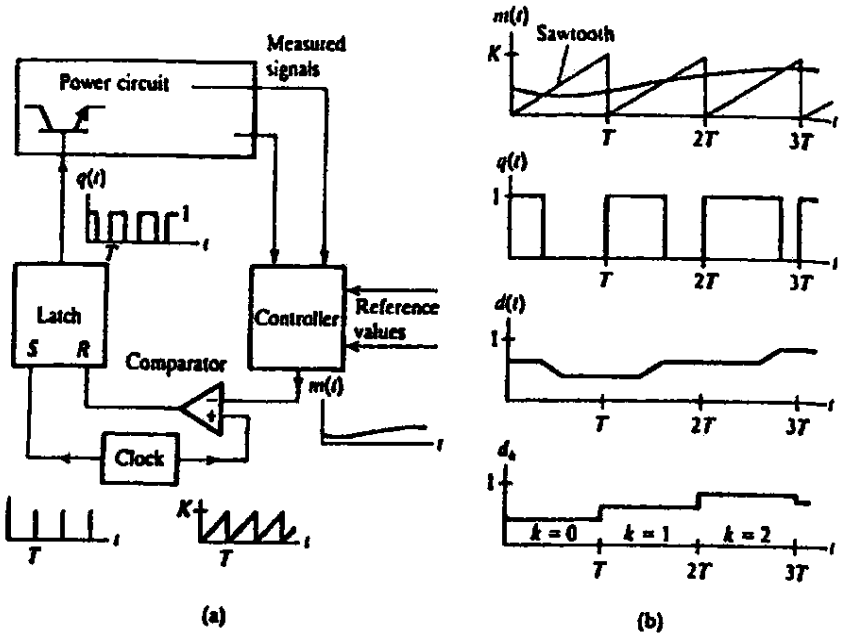
Figure 1.1: Basic Classes of Switching Functions: (a) Nominal Switching Function for DC/DC Converters; (b) Nominal Switching Function for DC/AC Converters;

lower trace in Fig. 1.1.

The conventional switching scheme for a power converter involves generating the switching function $q(t)$ by the controller and clock/comparator configuration shown in Figure 1.2 [63]. In this scheme, the reference values fed to the controller reflect the desired steady-state quantities (e.g. voltages and currents). Any necessary feedback control signals are combined with these reference values to specify the modulating signal $m(t)$, which in turn determines $q(t)$. Since power converters generally operate in a periodic steady state, converter waveforms of interest are typically periodic functions of time.

Spectral Characteristics of Switching Functions

The harmonic content of some of these waveforms is often constrained — an example is the current in the interface to the electric utility. In this case, stringent filtering requirements may be imposed on the power converter operation. Since the filter size is in general related to these requirements, a significant part of a power



(a) Generating a switching function $q(t)$, with duty ratio determined by a modulating function $m(t)$. (b) Relationships among $m(t)$, $q(t)$, d_k, and $d(t)$.

Figure 1.2: Switching Function Generation

converter's volume and weight can be due to an input or output filter. This conflicts with requirements to miniaturize power supply components, which have been the driving force behind much of modern power electronics. As pointed out in [126], work on control of harmonic content has paralleled power electronics development from its inception [122], and has since received much attention [96], [97], [30], [127].

Random Modulation

The motivations for this thesis stem from a new randomized switching discipline in power converters, which has received considerable attention lately, as described in Section 2.1. In these random modulation schemes, a signal with appropriately chosen statistical properties is added to the reference values and/or clock/comparator blocks in Figure 1.2. This has the effect of randomly 'dithering' $q(t)$ from its nominal form. The randomization can alter the harmonic content of waveforms of interest without excessively affecting the proper operation of the converter. In terms of Fig. 1.1, randomization occurs in each cycle of the reference waveform. Such schemes have been successfully applied in practice [120], [116], [121], [74], [48]. The main tasks at

which this thesis aims are:

- To provide a unified spectral analysis of switching patterns that have a random component introduced in a variety of ways relevant to power electronics. Specifically, the thesis seeks to describe the power spectra of switching functions $q(t)$ obtained by randomly dithering nominally periodic switching functions.
- To address the synthesis problem, namely the choice of switching statistics needed to shape the power spectrum of the switching waveform as desired.

The research in this thesis lies in the intersection of the theory of applied stochastic processes (as developed in statistical communication theory primarily) with power electronics. Results from Fourier theory and Markov chain analysis have been used extensively. Numerous random modulation schemes of interest in power electronics have been analyzed during the course of research documented here, most for the first time. New randomized switching schemes for power electronics, notably modulation based on Markov chains, have been suggested and verified.

The engineering relevance of the research described in this thesis is presently in the areas of power electronics and electric machine drives. The theoretical significance is in a fairly detailed and complete analysis of random pulse trains. Several new results have been obtained.

1.1 Scope of the Thesis

The major problems addressed in the thesis are specified in this section. Quantities of interest in a switching cycle are:

- total cycle duration,
- duration of the on–portion of the cycle,
- position of the on–portion within the cycle.

The ratio of the duration of the on–portion to the total cycle length is called the *duty ratio.*

Each of these quantities (or their ratios) could be randomized. If the randomization is based on identical and statistically independent trials in each cycle, i.e. if the statistics used for randomization are the same in each cycle and they do not depend on the outcomes of previous trials, then we shall term the modulation *stationary*. Switching waveforms of this kind are used for DC/DC power electronic converters. If the reference switching waveforms are periodic functions, with a period being comprising several 'on–off' cycles, then the randomization based on statistically identical and independent random modulation in each period yields *block–stationary* waveforms. Such waveforms are used in inverter (DC/AC) operation of power converters.

If the randomization applied in any period depends on the outcomes of a finite number of previous periods, then the random modulation can be modeled as evolving on a Markov chain. When the chain leaves a state, an on–off cycle associated with that state is generated; the overall switching waveform is a concatenation of such cycles.

The basic *analysis* problem in random modulation is to relate the spectral characteristics of $q(t)$ and other related waveforms in a converter to the probabilistic structure that governs the dithering. The design problem in random modulation is to synthesize a random switching procedure that minimizes given criteria for power spectra. Practically useful optimization procedures include the minimization of discrete spectral components (denoted as narrow–band optimization in this thesis), and the minimization of signal energy in a given frequency segment (denoted as wide–band optimization).

The specific classes of problems addressed in this thesis are:

Problem 1 *Given the probability density functions used for stationary or block–stationary dithering of nominal or reference switching signals, determine the power spectrum (both continuous and discrete) of the resulting* $0-1$ *pulse train, and of related waveforms.*

Problem 2 *Given a finite Markov chain, with known transition probabilities between the states, and given switching cycles corresponding to each state, determine the power spectrum of the resulting pulse train.*

Problem 3 *Given a (narrow-band or wide-band) criteria in the frequency domain and given a stationary or block-stationary random modulation scheme, determine what choice of associated probability densities minimizes the criterion. In the case of modulation based on a Markov chain, given the optimization criterion, determine the state transition matrix and waveforms associated with each state, that minimize the criterion.*

Problem 1 can be generalized, so that a modulation process consisting of alternate application of different random modulation schemes is considered, or so that a random choice of random modulation scheme is performed in each cycle. One special case of Problem 3 that is considered in the thesis is a form of queue modulation, in which random modulation is performed whenever there are customers at the server, and a deterministic waveform is generated otherwise.

Problem 1 and its generalizations are solved for stationary schemes in Chapter 4 and in Appendices A–C, and for block-stationary schemes in Chapter 5. Problem 2 and its generalizations are solved in Chapter 6. Problem 3 is addressed in Chapter 7.

1.2 Main Contributions

The main contributions of this thesis are:

- Development of a unifying theoretical setup that makes connections with results from statistical communication theory and enables a comparative study of different random modulation schemes in power electronics. These results are presented in Chapter 3.

- Analysis of stationary schemes, with new results for aperiodic random modulation, alternate modulation, and random choice of random modulation. This material is presented in Chapter 4, with additional details in Appendices B and C.

- Analysis of block-stationary schemes, which are applicable to inverter operation in power converters. In Chapter 5 a generalized expression for pulse position

modulation is derived and verified, together with a new result for aperiodic block–stationary modulation.

- Introduction of modulation based on Markov chains is proposed in Chapter 6 as a means to explicitly impose time–domain constraints on the switching waveform, while shaping the spectrum. A new formula for the power spectrum of signals defined on cyclic (periodic) Markov chains with asynchronous transitions (which implies different lengths of switching cycles) is developed and verified.

- Synthesis results for different random modulation schemes are presented in Chapter 7. New optimization problems are formulated and solved in that chapter, quantifying for the first time the capabilities of random modulation in spectral shaping. The results in Chapter 7 provide the first systematic evidence for observations made in numerous implementations, namely that random modulation is very efficient in handling the narrow–band spectral constraints, while it is not particularly well suited for the wide–band spectral requirements.

1.3 Contents

In Chapter 2, the necessary background on power electronic implementations of random modulation is provided, together with a characterization of the set of operating constraints. In Chapter 3, random switching strategies are classified, and a basic theoretical framework is outlined. Issues that arise in verifying the power spectral formulas described in this thesis by Monte–Carlo simulation, followed by a spectral estimation procedure, are also described in this chapter.

Power spectra of basic stationary random modulation schemes are analyzed in Chapter 4 and in Appendices A–C. The spectral shaping at frequencies which are one to three orders of magnitude higher than the basic switching frequency is described in Appendix E. Results for block-stationary random modulation, which is utilized in power converters in the inverter operation mode, are given in Chapter 5. Power spectra of signals specified by Markov chains are analyzed in Chapter 6.

Appendix D contains a description of an experimental setup used to verify spectral formulas for random modulation which were developed in this thesis. Results in random modulation synthesis are presented in Chapter 7. A summary of the thesis and suggestions for future research are given in Chapter 8. Issues in dynamical operation of power converters employing random modulation are addressed in Appendix F. The concept of piecewise deterministic processes is outlined in Appendix G. It is a promising theoretical framework for analysis of random modulation schemes.

Readers with interest in theoretical aspects of random pulse modulation could skip Chapter 2, skim over Chapter 3, and then read Chapters 4–7 and Appendix F. A suggestion for readers with primary interest in practical aspects of random modulation in power electronics is to read Chapters 2 and 3. Results applicable to DC/DC converters are then given in Chapters 4, 6, 7 and in the Appendices, while the material of interest for inverters (DC/AC converters) is in Chapter 5, in Sections 6.3 and 7.2, and in Appendix D.

Chapter 2

Background

2.1 Literature Survey

This section contains descriptions of implementations of randomized switching strategies reported in the literature. Over the last three decades, power converter designers have resorted to random switching for different reasons. During the early development, switching speed of semiconductor devices was a limiting factor, and acoustic noise was present in DC/DC converters [19]. Random modulation was originally suggested as a way to reduce the acoustic noise. The development of fast switching devices, especially with the MOSFET technology, alleviated that problem.

As pulse width modulation (PWM) technology matured in the seventies and in the early eighties, a need was felt to address previously neglected effects. These efforts have included the acoustic noise in inverter (DC/AC) applications, and the use of modulation to reduce problems related to Electromagnetic Interference (EMI). The advent of capable and affordable microprocessors has enabled a more systematic approach to PWM improvement, mainly in terms of optimization of deterministic PWM waveforms.

At the same time, the use of random switching has been suggested for both DC/AC applications [120], and for DC/DC converters [116]. As pointed out in [126], approaches based on optimization of deterministic and random switching to PWM improvement are complementary. This thesis shows that the complementarity is es-

pecially valid if a broad-band spectral shaping is needed.

An increasing number of articles on random modulation has been published recently in the power electronics literature (over a dozen in 1992 alone), and most of them are reviewed in this section. Before pointing out some of their salient features, their common properties are noted:

- They all claim significant reduction in unwanted (higher) harmonic content in waveforms of interest;
- The theoretical analysis in the papers is quite limited.

There is one difficulty in interpreting results presented in some of the references in this area. A randomly modulated pulse train is a stochastic process (wide-sense stationary in all present implementations), and its Fourier transform (i.e. its harmonic spectrum) is a random variable at each frequency. One therefore has to settle for stochastic descriptions, for instance using averaged quantities (which is the way results in [48] and [74] are interpreted). A certain amount of time averaging, which is always present in measurements of signal harmonic spectra, makes the Fourier transforms of signals of interest useful in developing an intuition about the particular randomized switching strategy. It is very hard, however, to make precise theoretical predictions about harmonic spectra beyond the DC component.

It turns out, however, that the power density spectrum (i.e., the Fourier transform of the *autocorrelation*) of a random waveform has much better limiting properties, and can be estimated reasonably well from waveforms of finite duration. One remaining problem is the fact that the international standards in power electronics are given in terms of Fourier components of a waveform, not in terms of its power spectrum. This drawback can be somewhat alleviated if the assumption is made that the regulations are meant for a *periodic* operation, in which case the power density spectrum at each frequency is the square of the magnitude of the corresponding Fourier component. In that case the standards can be simply mapped to the power spectrum domain, and effects of random modulation can be properly evaluated.

The lack of analytic tools has been a serious impediment for wider application of

randomized switching strategies. In some implementations, apparently any reasonable random modulation procedure yields substantial benefits. The heuristic approach does not, however, determine whether additional spectral requirements could be satisfied, and what are the limits of achievable performance with random modulation. It turns out that some analytic tools have been provided by information and communication theory since the early sixties, while some other tools had have to be developed during the course of research documented in this thesis.

Randomized switching shares one property with other engineering concepts which have spread from one application area to another: it is very hard to establish a historical precedent. This section is not an attempt to write a definitive historical account; instead, the references are grouped along themes and described briefly.

Apparently, the first paper on random modulation in the power electronics context was written by Clarke in 1970 [19]. The paper discusses a DC/DC converter which employs self–commutating thyristor circuitry. Due to a low switching frequency used at the time, the acoustic noise had been a major problem even for DC/DC converters. A random dithering signal is injected directly in the comparator (see Fig 1.2), and the implementation is entirely analog. No analysis is presented, but the experimental results in acoustic noise reduction are impressive (assuming that Figs. 6 and 7 in the paper have been swapped). It is also claimed in the paper that shielding is easier when random switching is employed. From today's perspective, it seems that improvements in switching devices, in terms of frequencies of operation, have provided a more direct answer to the acoustic noise problem. Thus, the random switching idea had been set aside, only to resurface almost two decades later.

An inherent randomness in switching times which characterizes current–hysteretic converters is mentioned in [84]. An approach to analysis of complicated deterministic switching patterns based on probabilistic arguments has been advocated by [84], [54]. That approach is a part of a much wider methodology which addresses the behavior of complex (disordered, chaotic) systems using a probabilistic framework [73].

The first application of random switching in a modern power electronics setup, including a microprocessor implementation, appears to be the paper by Trzynadlowski,

Legowski and Kirlin [120]. The paper considers the case of voltage–controlled three phase bridge inverters. The random switching is based on a uniform probability density function. The authors consider power spectra in the analytical section of the paper. and present a qualitative argument. The experimental results are obtained with a large inverter (8.7 kVA, 240 V). The switching frequency is up to 240 kHz. which is high for this power range. The paper presents measured Fourier transforms (harmonic spectra) of line–to–line and line–to–neutral voltages. without providing details about the measurement procedure.

Another paper by the same group of authors is [75]. It describes a "hypersonic" power inverter (with 250 kHz switching frequency), which uses randomized PWM. A uniform probability density function is again used to provide the deviations from the deterministic switching pattern.

Most of the material from [120] has appeared as a journal article [121]. The implementation results are very encouraging while the analysis part is limited. In the experimental setup an 8–bit pseudo–random number generator is used, and the generator consists of 8 independent digital subsystems operating at a frequency of 480 kHz.

The same authors apply a random PWM to delta inverters, suitable for automotive applications. in [119]. A uniform probability density is used to generate dither in the switching signal.

It is common in the power electronics literature to define the ripple of a variable as the excursion of the variable around its mean value. From the switching generation mechanism it is immediate that a simple dithering scheme, which perturbes *individual* on–off cycles. inevitably leads to an increased ripple, when compared to the deterministic case. Thus, if the ripple is to be of a comparable size. random modulation requires a higher switching frequency. There exists. however. a clever scheme [74] which "preprocesses" a switching waveform in order to detect "back–to–back" ON patterns. reducing the average switching frequency in inverter operation mode.

The paper [119] contains measurements of acoustic spectra taken in an anechoic chamber. The existing guidelines suggest that individual harmonics corresponding

to pure sinusoids in 1–5 kHz are the most annoying. Random PWM is often very effective in reducing the acoustic noise in that frequency range.

The reference [76] deals with details of the hardware implementation in a setup similar to the papers just described. It is shown by experiments that "blurred" harmonic spectra of output voltages and currents are obtained. The authors present improved shapes of both acoustic and harmonic spectra of the output voltage at different loading conditions. A novel aspect of randomized switching strategies is explored when effects on torsional vibrations in motor drives are studied. It is shown that the stability of operation is improved at frequencies close to natural mechanical frequencies of the load.

The paper [74] proposes "gray–noise" PWM, which combines the features of a standard space–vector (deterministic) PWM with random switching for inverter control. In each on–off cycle of length T, the switch is either kept off first for $(1-D)T$, and then turned on for DT, or vice versa (D being the duty ratio). The uniform probability density function used in earlier publications by the same authors is thus replaced with an atomic probability density (or probability mass) function. In this particular case, the delay is either 0 or $(1-D)T$, each with probability 0.5, and all other delays have zero probability. One advantage of this policy is that two consecutive "on" states (or two consecutive "off" states) can be detected very easily in a digital implementation, and the switch could be kept "on" (respectively, "off") for the duration of both states. The average switching frequency is reduced up to 25%, as will be shown in Chapter 5. In communication theory terms this is a special case of randomized pulse position modulation (PPM) [86], and is studied in detail later. Inverter operation, however, presents some additional difficulties, which are considered in Chapter 5.

The most recent paper by the same group of authors is [64]. In this paper power spectra of signals are considered, and a result from communication theory is invoked in the analysis part of the article. After a sequence of involved algebraic manipulations, an expression is obtained for the power spectrum of the output voltage. This thesis considers the same type of modulation. In Chapter 5 a general result is presented,

which agrees with the one presented in [64] when applied to the same numerical example. Calculations in [64] are compared to experiments and the agreement is excellent.

Paper [116] is chronologically the first paper in the sequence of references written by Tanaka, Harada and Ninomiya. Although it mostly emphasizes the high frequency phenomena related to semiconductor imperfections, it also describes in detail two randomized switching strategies. One of them is a standard random pulse width modulation (PWM) from communication theory [86], while the other one is more complicated. The paper concentrates on a down (buck) DC-DC converter, mainly because of its simplicity. The analysis part of the paper contains plausibility arguments only, but the authors rightly point out the need to consider power spectra of randomly modulated signals, instead of their Fourier transforms. The randomized switching strategies described are:

- "Control Circuit I", which is a simplified version of the randomized PWM scheme [86]. In terms of Fig. 1.2, $m(t)$ is constant for a down converter in steady state. To randomize this, one of two possible values is chosen and added to m at each clock period T, resulting in a random choice between the two corresponding duty ratios $d(t)$.

- "Control Circuit II", in which the sawtooth signal fed from the clock to the comparator in Fig. 1.2 is modulated, so that the period length T is varied by adding a random variable to it. Thus, the same duty ratio is maintained at all times, but $q(t)$ ceases to be periodic. In experiments described in [116], this strategy appears to be superior to the first scheme. This scheme is denoted as aperiodic modulation and it is analyzed later in Chapter 4 of this thesis, using two different methods.

The reference [114] is a more recent paper by the same group of authors. The authors consider the power spectrum of a randomly modulated impulse train, but seem not to be aware of earlier results on the problem ([77], [86]). A modern survey of these results is given in [6]. The derivation produces a correct formula for

the power spectrum of an independent–increment impulse train, but unfortunately contains some inconsistencies (e.g. in the treatment of products of δ–functions or the lack of positivity constraint for time increments). The main result (formula (11)) is given as equation (71) in [77]. The normal density function used in [114] in the example is not entirely realistic (since it allows, with finite probability, both for arbitrarily long switching cycles and for cycles with negative length). The waveform used for the experimental confirmation consists of the convolution of an impulse train with a rectangular pulse. Although the actual probability density function used in the implementation is not described analytically, the results for a normal probability density function seem to approximate experimental observations well. The analytical expression for the same case is given in Problem 4.16 in [86]. In Section 4.4 of this thesis, some additional comments regarding the analysis of the "Control Circuit II" and the treatment in [114] are made.

The most recent paper by the same authors is [115]. It considers the same basic setup as [114], and the authors view random switching as a way to improve the reliability of electronic subsystems in a power converter. The effects on the power spectrum of variations in standard deviation of the probability density function used for modulation are studied. This is a rudimentary formulation of the power spectrum synthesis problem, which is considered in detail later in this thesis. The authors show that an approximate formula for bounds on the power spectrum holds for normal and uniform probability densities, but the estimate is not tight. The experimental confirmation uses a "hill–shaped" probability density function with finite support, and the results are close to theoretical predictions. In this paper, the authors concentrate on frequencies that are integer multiples of the switching frequency of 100 kHz.

Another important and widely referenced paper in the area of random modulation applied to inverters is [48], first published as a research report in March of 1989. It considers acoustic noise reduction in sinusoidal PWM drives. The basic setup involves a three phase induction machine supplied by a power converter. In addition, it is assumed that the random modulation is band–limited. The analytical argument in the paper is unfortunately quite difficult to read , due mainly to several

critical typographical errors. The implementation results, however, are impressive, and demonstrate a potential for significant noise reduction. An approximate analysis of this random modulation scheme is given in Chapter 5.

The reference [15] describes the origin and reduction of acoustic noise in an increasingly widespread class of motors, namely doubly–salient variable–reluctance motors. The results contained in the paper are part of the first author's M.S. thesis, published in 1990. The authors show that the dominant source of acoustic noise is the ovalizing deformation of the stator. Random dithering is used to shape currents, while producing the required torque. It is concluded that current shaping is an important means of acoustic noise control. In the experiment, turn–on and turn–off angles are randomly perturbed by just 1 mechanical degree, yet a 12 dB acoustic noise reduction is observed. During the course of experiments, no disadvantages have been identified related to random switching.

In [54] a three–phase inverter system in the megawatt range, suitable for electric traction applications, is considered. The PWM scheme used is deterministic, but very complicated (nonperiodic, or even chaotic, if Fig. 7 in the paper is representative). An interpretation based on probabilistic models appears to be the most economical in that case. The author does not pursue analysis of the problem, but presents very good experimental results. Acoustic noise reduction is again very pronounced.

A more recent review paper by the same author [53] studies mechanisms that generate acoustic noise in electric machines. The distribution of the signal energy over a larger frequency range is considered to be advantageous, except in the lowest frequency band ("subharmonics"). A probabilistic interpretation, without analytical derivations, is used again to characterize complicated deterministic switching patterns.

Another interesting body of work is presented in [49] and [14]. Random switching is applied to choppers (DC/DC converters) supplying a DC motor in [49]. It is the first paper to outline possible problems regarding the choice of probability density functions for the random PWM dither, since natural frequencies unaffected by conventional switching could get excited. The authors point out analytical difficulties in

solving that problem, which is consider in detail later in this thesis, and implement uniform and "square-law" dither densities.

The paper [14] is the most recent paper by the same authors, and is again very readable and contains numerous examples. The authors briefly discuss issues in psychoacoustics, describing ways to evaluate the annoyance created by acoustic noise of different power spectra. The need to tailor dither probability densities is argued for, highlighting a desirable adjustability of the switching discipline in various installations. A deterministic solution to this problem has been developed and is manufactured by Hitachi [109]. In that case, a PWM carrier switching frequency can be selected by a user (from a menu of 19 choices), to allow for adaptation. The authors of [14] argue that if no prior information is available, then a uniform probability density function is a reasonable choice for the dither. Their reasoning is that with uniform dither a uniform spreading of the signal is the most likely. Although this holds on an intuitive and qualitative level, it will be demonstrated later that a more detailed study of the modulation technique often leads to significantly better solutions.

Two very recent papers on random switching in inverter systems are considered next. The first of them [104] describes an application-specific integrated circuit (ASIC) designed specifically for random PWM control. It is shown that hardware requirements are very modest for modern semiconductor technology. The paper claims originality of the proposed PWM scheme, which is hard to justify. An evaluation of actual performance is not straightforward, since only time domain waveforms are presented. The other paper is [98], concerned with acoustic noise reduction as well. The authors point out that noise could be reduced by either hardware means (by increasing the switching frequency, or by adding filters), or by software means (deterministic optimal PWM, random PWM). The implementation results, presented in terms of harmonic spectra, are very encouraging.

The paper [126] reviews both deterministic and random techniques in PWM. The authors describe a combined scheme in which programmed PWM waveforms are additionally dithered in a random manner. An application to a DC/DC converter yielded very good results in terms of spectral shaping.

The paper [127] considers an elaborate deterministic PWM scheme. The authors formulate and solve the associated optimization problem for harmonic minimization, using a min–max algorithm. In a deterministic setup. it is appropriate to consider the Fourier components of the waveforms involved. so that the interpretation of relevant standards is straightforward. The implementation results are very good and the authors observe that a combination of programmed PWM and some form of random modulation could offer a solution to numerous modulation problems. This opinion is substantiated by research described in this thesis, and deterministic and random modulation are viewed as complementary methods needed to generate switching waveforms in power converters.

This overview of references is concluded by considering a review paper [85], which discusses trends in power electronics in the 1990's. The author points out that acoustic noise continues to be a serious problem in power converters. At the same time, advanced development is often governed by applications where performance or size reduction has a greater significance relative to the cost. Randomized switching strategies may be in that group of applications at present, but continuing improvements in microprocessors might contribute to a major change, spreading the area of applicability of random modulation, possibly as a part of wider class of variable frequency control [105]. According to [85], the probabilistic setup is likely to be used for analysis of complex deterministic behavior of modulation circuits. The use of a probabilistic framework for analysis of randomized switching schemes is very natural, and is discussed in detail in Section 3.2.

2.2 Standards for Harmonic Distortion

The main motivation for use of random modulation so far has been the possibility of acoustic noise reduction in inverter–based motor drives. Reference [15] presents detailed experimental evidence that a reduction of peaks of harmonics, with associated "filling–in" between the harmonics, causes a reduction in acoustic noise. The main reason is that less energy is available to produce resonance inside the mechanical

structure of a motor, assuming that mechanical resonances act as narrow band–pass filters.

It is argued in this thesis that random modulation could be beneficial for operation of any power converter, and not just for inverters. This section describes relevant international and U.S. standards governing the harmonic spectrum of power converters. The aim is to show how random switching should be tailored to meet specifications, while reducing filtering requirements. The main benefit from randomized switching strategies in this context is better utilization of the allowable harmonic content of waveforms at the equipment/utility interface. Random modulation is not merely a way to take advantage of present regulations, which have been written for a deterministic switching discipline, but also a flexible approach to solving problems caused by electromagnetic or acoustic noise. To that end, the description of standards given here notes some of the technical motivations, as an aid to assessment of the potential benefits of random modulation.

Power converters often contain numerous subsystems other than the power processing module, e.g. for control and for protection purposes. Input and output filters themselves usually contain multiple energy storage elements (capacitors and inductors). Random modulation could reduce functional problems, by decreasing unwanted interactions among the energy storage components. Auxiliary subsystems in a converter could prove susceptible to signal energy in certain frequency bands, and a smearing of signal power, which is characteristic for random modulation, is likely to improve the converter operation. Although these phenomena are electrical in nature, they have similarities with acoustic noise problems of the sort mentioned earlier, since they are characterized by narrow–band effects. The problems of electromagnetic compatibility influence power electronic systems in the following ways:

- Input filters take valuable space in power electronic converters,
- Waveforms have to be "clean" to prevent interactions with auxiliary equipment,
- Layout and packaging are affected by EMI.

Random modulation reduces the noise signal energy in some frequency bands, and

may avoid the need for redesigning the system, if a fixed set of constraints is to be satisfied at certain points. The conventional approach is to modify transfer functions from the noise source to points of interest, but this often requires expensive and bulky filters. Size and cost reduction of input filters is thus a promising application for random modulation. Random switching is not the only way to reduce input filtering requirements in terms of price and volume. Active filters are another possibility [32]. The two approaches are complementary, since they require modifications in different parts of the converter.

The potential of random modulation to shape broad-band frequency characteristics is harder to evaluate. In Chapter 7 this problem is quantified, and it is shown that the potential benefits in adapting to broad-band constraints are much smaller than in the case of narrow-band effects.

A possible drawback of random switching is that signal energy might be introduced in a frequency slot where no appreciable energy exists in conventional switching, and that the system might be very sensitive to this particular frequency band. Even in this case random modulation should not be immediately abandoned, since with a proper choice of modulation statistics the signal spectrum can be significantly altered. Related issues in random modulation synthesis are discussed in Chapter 7.

In this section the goal is to quantify the input filtering requirements that power electronic converters must comply with. This information is not readily available, since a number of international and federal organizations (both civilian and military) have introduced separate regulations imposing constraints on equipment operation.

In a random modulation setup, the natural quantity to study is the power density spectrum and not the harmonic spectrum (i.e., not the Fourier transform of the signal), due to the limiting properties of stochastic signals. All existing specifications on harmonic distortion are given in terms of the harmonic spectrum, and in this thesis their interpretation is as follows:

- Take the allowed power density spectrum to equal the square of the magnitude of the allowed harmonic spectrum at any given frequency.

- For lower frequencies, where the size of a multiple of the 60 Hz (or 50 Hz) fundamental is specified in standards, take the corresponding power to be associated with the sum of powers of the discrete and the continuous spectrum in the frequency interval halfway towards the neighboring harmonics of this 60 Hz fundamental.

2.2.1 Harmonic Distortion Standards at Low Frequencies

Standards covering the lower part of the spectrum, namely multiples of the standard 60 Hz supply frequency, are considered first. This is mainly of interest for AC-DC and DC-AC converters, since the switching frequency of DC-DC converters is usually of the order of 10^5 Hz. The main international body setting guidelines for national standards is the International Electrotechnical Commission (IEC). Member countries, which include all industrial nations, are expected to adopt IEC regulations as national standards within reasonable periods. Documents of interest in this area have been put forth by IEC Subcommittee 77A-555-2; IEEE; ANSI; and by U.S. military services (DoD Document 1399, Sec.300; U.S. Naval Code and MIL-STD-461) [18],[66], [128].

Consider first the international IEC-555-2 standard, which is quite comprehensive. An illustrative portion of IEC-555-2 specification is shown in Table 2.1. The standard divides all electronic equipment into four classes:

- Class A - balanced three–phase loads and loads not belonging to other classes;
- Class B - portable tools;
- Class C - lighting equipment;
- Class D - equipment with an input current of the special "inverted T" shape. Switching power supplies are in this group, unless corrective measures are taken.

This standard makes the case for power factor correction, enabling equipment that would otherwise belong to class D to qualify as class A, with substantially relaxed harmonic requirements. Note that for class A equipment, the maximal permissible harmonic current is not given in relative units, which allows small loads to draw

Table 2.1: IEC-555 Harmonic Current Limits.

Harmonic order	Class	Absolute limit (A)	Relative limit (mA/W)
2	A	1.08	
2	D	0.30	1.0
3	A	2.30	
3	D	1.08	3.6
4	A	0.43	
4	D	0.15	0.5
5	A	1.14	
5	D	0.60	2.0

significant harmonic current. This inconsistency is alleviated by the requirement that class A equipment load has to be phase balanced, thus somewhat constraining the higher harmonics.

U.S. military standards are somewhat more stringent. They allow total harmonic distortion of 5% with each individual harmonic below 3%.

2.2.2 Harmonic Distortion Standards at High Frequencies

Harmonic content limitations in the 10 kHz — 10 GHz range are considered next. EMI can be divided into two parts:

- Noise being *conducted* to the mains (10 kHz - 30 MHz).
- Interference *radiated* from a power electronic converter (30MHz - 10 GHz).

The two parts are closely related. as conducted noise may lead to unwanted radiation from power lines. At higher frequencies power electronic devices themselves can act as radio frequency transmitters.

The standards specify limits on the EMI measured between each phase and a neutral. It is often advantageous to decompose the EMI into two components. namely the differential mode and the common mode. The differential mode current flows through one conductor (say phase) and returns through the other (neutral). The common mode current flows through both conductors and then through the ground conductor. The differential mode currents are generally a direct result of switching,

while the common mode currents result mostly from stray capacitances to ground. Typical EMI problem areas for power supplies for each mode are described in detail in [35].

The coordination among national regulatory bodies is achieved through the International Electrotechnical Commission (IEC). It sponsors CISPR ("Comité International Special des Perturbations Radioelectriques"), which makes regulations for the radio frequency range. This part of the frequency domain is regulated in the U.S. by the FCC (Federal Communications Commission). The equivalent body is VCCI in Japan and FTZ/VDE in Germany (FTZ is a part of the postal service and VDE is an industry organization). The corresponding military standard is MIL-STD-461 with parts A/B/C [108], MIL-STD-462 which gives the testing procedures, and MIL-STD-463 which provides the definitions. MIL-STD-461 contains both narrow-band and broad-band (1 MHz) regulations. Military standards also contain extensive equipment susceptibility requirements, which are absent from other standards, although a need for such regulation is expressed often [35], [92].

The FCC regulation distinguishes between two classes of equipment, A being industrial and B consumer products. Docket 20718, Part 18 covers devices that use radio-frequency energy directly, i.e., industrial, scientific and medical equipment used for non-communication purposes. Docket 20780 Part 15, Subpart J covers units (both industrial and consumer) where radio-frequency energy is not used directly (e.g. computers. electronic games connected to TV receivers). Part 68 covers equipment connected to the telephone network. This distinction is not always easy to apply. For example, power electronic supplies are classified as radio-frequency devices with respect to Part 18 and have to meet stringent EMI limits. Some classes of equipment are temporarily exempted from meeting the standards. for instance transportation vehicle electronics and microprocessor controlled appliances. but this situation may change in the near future.

Modern power converters operate in switching frequency ranges of a few hundred kHz up to several MHz, thus overlapping with AM radio. Higher harmonics of the switching frequency ("switch transition rings") are not far away from the FM radio

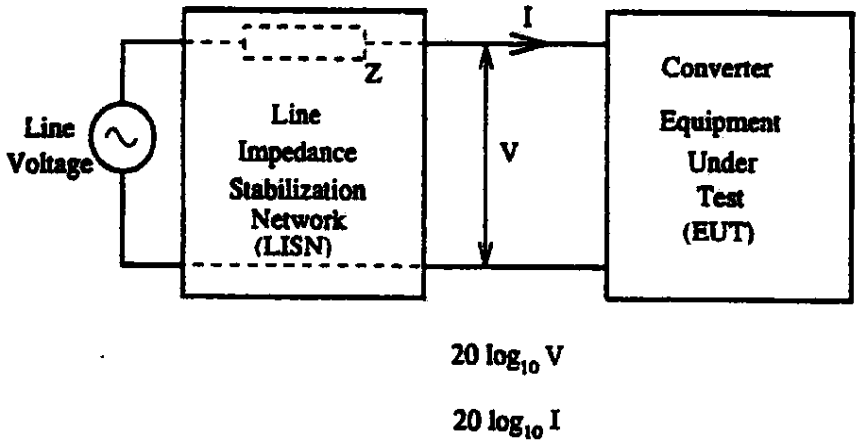


Figure 2.1: A Schematic Illustrating Conducted Noise Measurement.

range (90–110 MHz), or the TV range (60–80 MHz). Effects of random modulation at these frequencies are analyzed in Appendix E.

Recorded levels of conducted noise in power lines in urban office buildings are only 15–35 dB below the levels of these communication signals [110]. Taken together, these effects are likely to lead towards an increasing importance of EMI specifications.

Constraints on radiated emissions are in general hard to study analytically, since they depend very much on construction details, e.g. shielding and grounding. A detailed description of hardware used in measurements of radiated emissions is given in [80].

A circuit schematic for conducted emission measurement is illustrated in Fig. 2.1, and a more detailed setup (from [92]) is given in Fig. 2.2. The corresponding specifications are given in Fig. 2.3.

A radiated emission measurement is illustrated in Fig. 2.4. and the FCC setup (from [92]) is given in Fig. 2.5. The corresponding harmonic constraints are given in Fig. 2.6.

The emission limits are expressed either in decibels above one microvolt ($dB\mu V$) or in decibels above one microampere ($dB\mu A$). Since the "line impedance stabilization network" (LISN) impedance used in all non-military measurements is dependent on frequency, conversion between $dB\mu V$ and $dB\mu A$ is generally difficult. It can be seen

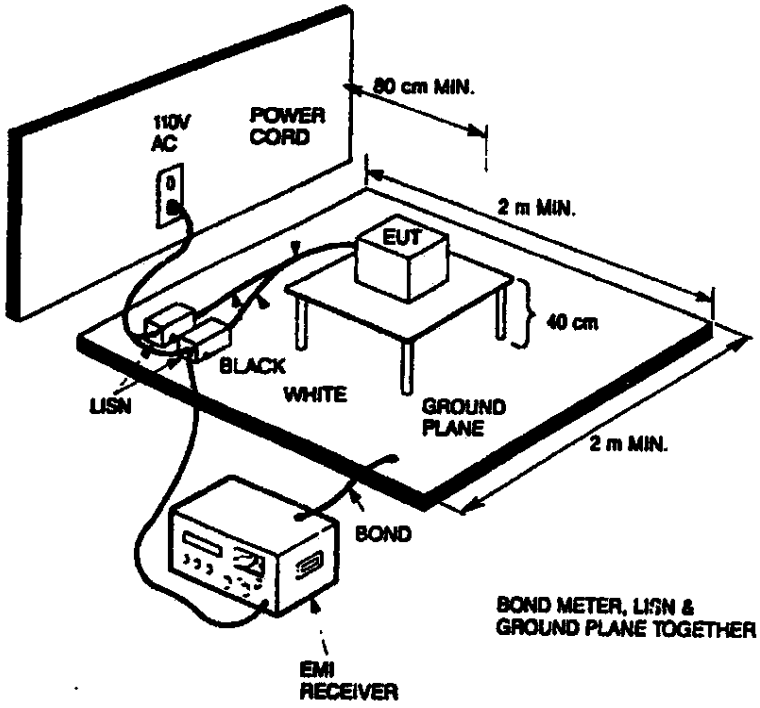


Figure 2.2: Conducted Noise Measurement - Testing Site.

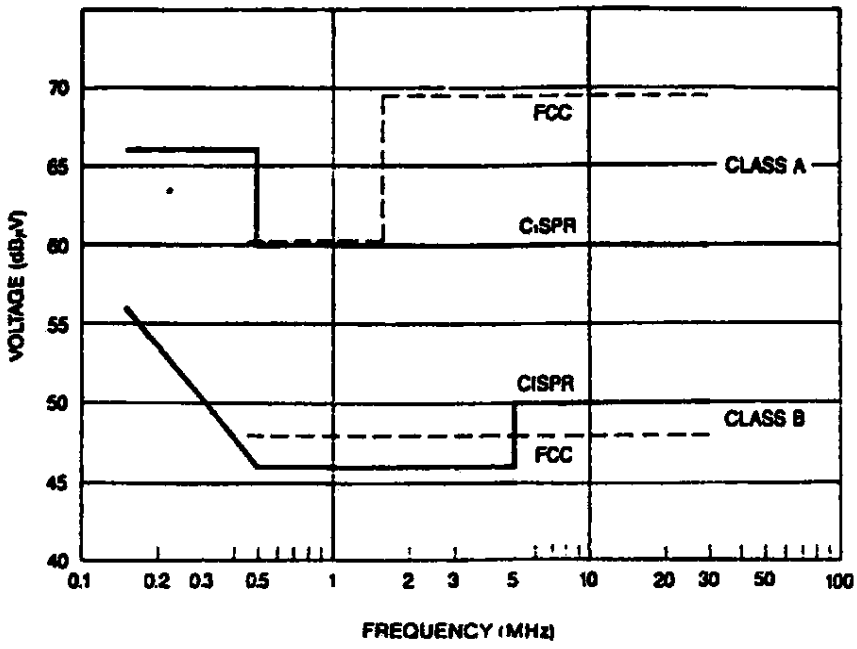


Figure 2.3: Different Standards for Conducted Emission Limits.

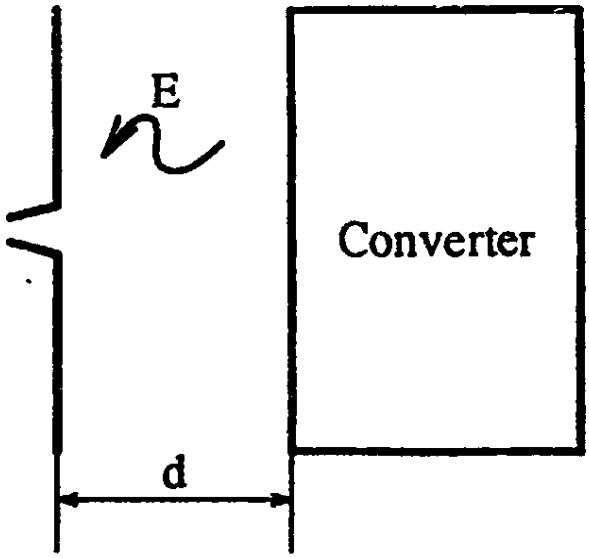


Figure 2.4: A Schematic Illustrating Radiated Noise Measurement.

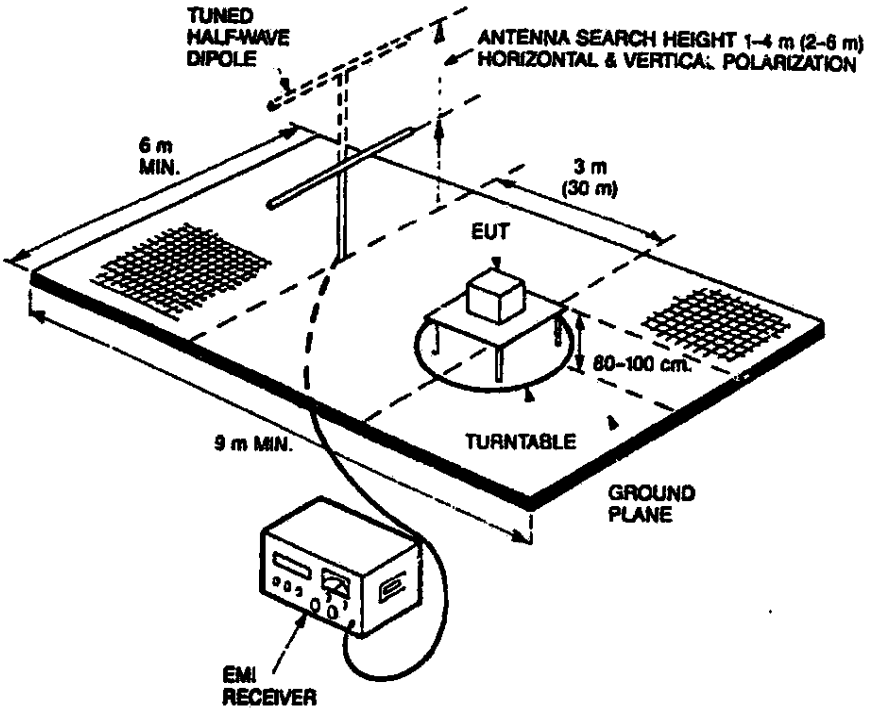


Figure 2.5: Radiated Noise Measurement - FCC Testing Site.

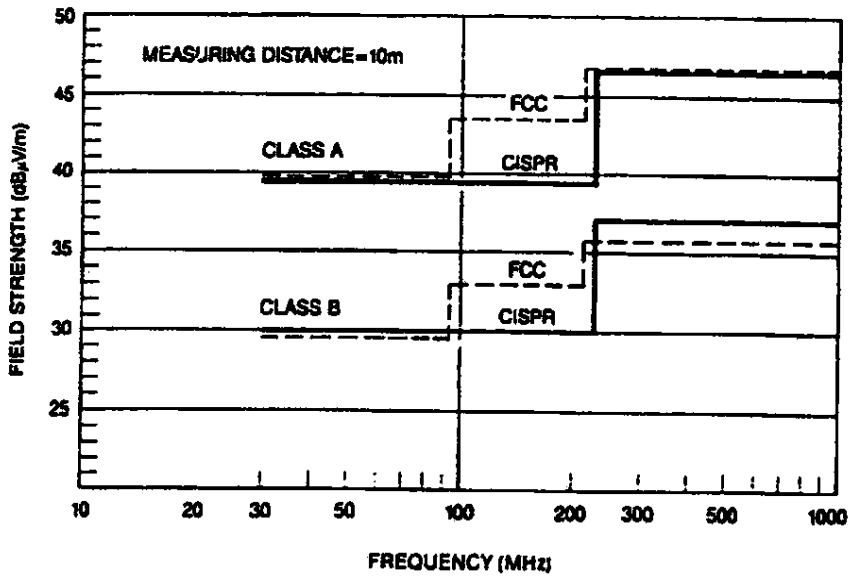


Figure 2.6: Different Standards for Radiated Emission Limits. Extrapolated for Measurements at a 10 m Distance.

from Fig. 2.6 that the class B requirements, where most power electronics supplies belong, are harder to satisfy.

Military standards [117],[108] are the only specifications with both narrow- and wide-band requirements. A detailed knowledge of measurement procedures is needed for a numerical comparison. All military measurements are obtained with current probes, and a comparison with FCC LISN networks is not straightforward. In a brief calculation which follows. a standard impedance value of 50 Ω has been used [117]. This value is not critical for a relative comparison of narrow-band (NB) and wide-band (WB) constraints.

The frequency range 1–2 MHz (of width 1 MHz) is considered, for which the wide-band constraint *per* MHz is 62.5 $dB\mu A$ at 1 MHz and 50.0 $dB\mu A$ at 2 MHz. When averaged to 56.3 $dB\mu A$, the allowed signal power in the 1–2 MHz range is 20.8 μW (assuming the 50 Ω impedance). The narrow-band constraints in the same range vary between 29.3 $dB\mu A$ at 1 MHz and 20 $dB\mu A$ at 2 MHz. The constraints are given for a sinusoidal signal, and to evaluate the total power of NB constraints in the 1–2 MHz band, the bandwidth of each harmonic measurement is assumed to be 1000 Hz. The total power of NB constraints in the 1–2 MHz band is thus approximately 12.6 μW, i.e., approximately 2 times less than for WB constraints. This calculation

Table 2.2: Receiver Performance Degradation due to NB and WB Interference

Signal S Modulation Type	Interference I Type	$\frac{S}{I}, dB$
AM (voice)	NB (AM)	6
·	NB (FM)	18
·	WB (Pulse–radar)	-18
FM (voice)	NB (AM)	8
·	NB (FM)	0
·	WB (Pulse–radar)	-20
AM (TV)	NB (AM)	18
·	WB (Pulse–radar)	0

implies that NB rather than WB specifications constrain the total signal energy in a 1 MHz band. The assumption made in the preceding calculations that all 1000 Hz wide channels in a 1 MHz band could be fully utilized is not realistic, and it is meant to provide an upper limit only.

It is shown in Chapter 7 that random modulation holds great promise in meeting NB constraints. On the other hand, it has to be combined with other methods, e.g. deterministic PWM optimization, to meet the WB constraints.

Narrow–band interference is a very serious problem in communications [68], [52]. In studies of receiver degradation, usual measures of performance are bit error probabilities for digital systems, and articulation index and articulation score for analog systems [68]. The measures are studied as functions of the signal–to–interference ratio, parameterized by different signal–to–noise (white noise) ratios. Cases of interest include interference from the same channel as the signal (cochannel interference, with the same or nearby frequency), and interference from an adjacent channel. A very detailed study of receiver performance degradation is given in [68]. Signal–to–interference ratios yielding lowest acceptable performance, for a high signal–to–noise ratio, are given in Table 2.2.

The Table 2.2 shows that NB interference is more detrimental than a WB interference, justifying the approach taken in all civilian specifications, which are written for NB signals only. The interference issue is, however, very complicated, and detailed studies are often needed [68]. Narrow–band effects on auxiliary circuitry, e.g. on phase–locked loops used in FM systems, are often very serious [52].

Impulsive noise in the time–domain, which is very wide in the frequency domain, is often a limiting factor in communication systems. Its effects on systems with little redundancy (e.g. some data networks) are very harmful [125]. An analog solution based on smearing–desmearing (SD) filtering has been proposed in [125]. This idea is in a sense dual to random modulation, since the roles of time and frequency domain quantities are reversed. The goal of SD filtering is to reduce effects of channel noise that contains impulses in the time domain. The signal is purposely smeared (filtered in the frequency domain) before entering the channel and desmeared at the receiver end, while the impulsive channel noise is passed through the desmear filter only. The desmear filter is designed to minimize the transfer function between the noise and a frequency band containing the signal.

2.3 Summary

Literature on power converters utilizing random modulation has been described in this chapter. Applications of random modulation have been largely influenced by developments of semiconductor power devices and microprocessors. As applications of random modulation are becoming more diverse, there is a growing need to address analysis and design issues quantitatively. The choice of probability density used for random switching is one such example.

Most implementations of random modulation in power converters have concentrated on acoustic noise reduction. While this remains a very important area of application, it has been argued in this chapter that randomized switching strategies also hold promise in reducing filtering requirements. To that end, they are not just a way to take advantage of contemporary regulations, which have been devised for a deterministic switching strategy. The narrow–band interference due to switching is often the most serious problem in communication systems. Random modulation can be helpful by broadening and leveling the power spectrum of the switching signal, and reducing the signal energy in frequency bands where deterministic switching would cause objectionable interference.

Capabilities of random modulation in the shaping of power spectra are addressed in more detail in Chapter 7. Before that issue can be studied, a unified analysis framework for random modulation has to be developed. First steps in that direction include a classification of random switching strategies, a description of the basic theoretical setup, and a discussion of the main issues in the verification of analytical formulas for random modulation. These topics are considered in the next chapter.

Chapter 3

Preliminaries

3.1 Classification of Randomized Switching Strategies

As a common ground for comparisons among different random modulation methods is needed, it is useful to concentrate on the switching function, denoted by $q(t)$, which can take only 0–1 values. Many waveforms of interest in implementations are related to such a pulse train via linear transformations (e.g. a simple integral in the case of the input current of a boost converter). The power spectrum of variables related to $q(t)$ by linear, time–invariant (LTI) operations can easily be derived from the power spectrum of $q(t)$. The power spectrum of many other waveforms of interest can be derived by methods similar to those used for $q(t)$, as illustrated in the following chapter.

The main elements characterizing a random modulation scheme are the time variation of the nominal (non–randomized) switching pattern and the time variation of the probability laws that govern the randomization. First, it is necessary to check if the nominal patterns, e.g. duty ratios, vary from one cycle to the next, as they do in inverter operation. This property defines the deterministic structure of the modulation. The other issue is the time variation of the probability densities used to determine the "dither" at each cycle. This component is thought of as the probabilistic structure of

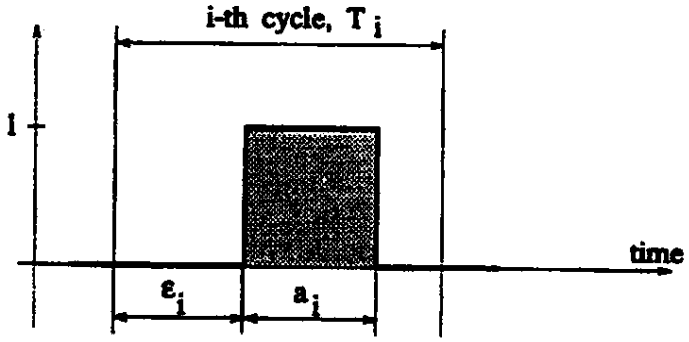


Figure 3.1: Classification of Basic Stationary Random Switching Strategies.

the modulation.

If both the deterministic and probabilistic structures are constant in time (implying DC/DC operation), the switching will be called *stationary*. In *block–stationary* random modulation, the nominal pattern varies from cycle to cycle, but is repeated periodically over a block of cycles, as needed for inverter (DC/AC) operation. This thesis also considers a third type of structure, where the probability density used for dither in each cycle depends on the state of a Markov chain at the beginning of that cycle. It will be argued later that switching based on a Markov chain enables explicit control of the ripple, while maintaining analytical tractability.

Stationary switching schemes can be further classified, and the most important classes are randomized pulse position modulation (PPM), randomized pulse width modulation (PWM), and asynchronous schemes [116], [114]. To describe these, we first introduce some notation. Figure 3.1 shows one cycle of the switching waveform; T_i is the duration of the i-th cycle, a_i is the on-time within a basic switching cycle, and ε_i is the position of the turn–on within the cycle. The duty ratio is $d_i = a_i/T_i$. All switching functions $q(t)$ that are analyzed in this thesis consist of concatenations

of such switching cycles. In general, ε_i, d_i or T_i, can be dithered, individually or simultaneously. Some combinations used in power electronics are:

- Random PPM: ε_i changes; T_i, a_i fixed. The scheme in reference [74] is a special case, where ε_i can take only two values.
- Random PWM: a_i changes; $\varepsilon_i = 0$; T_i fixed. Within random PWM, d_i can be varied either continuously, or it can take finitely many distinct values, as in [116],[121].
- Asynchronous modulation [116]: T_i changes; $\varepsilon_i = 0$; d_i fixed.
- Simplified asynchronous modulation: T_i is varied. a_i is fixed. $\varepsilon_i = 0$, as in [114].

Some other possibilities involve varying more than one variable simultaneously, or dithering their sums, differences and the like:

- Vary T_i and d_i simultaneously, $\varepsilon_i = 0$, with prespecified time averages,
- Vary independently the "on" and "off" times [86], with prespecified averages. An example of this kind is the random telegraph wave with different transition rates from 0 to 1 and from 1 to 0.

Stationary switching schemes are analyzed in Chapter 4, while block–stationary switching schemes are considered in Chapter 5. Switching schemes having variable probabilistic structure, with both fixed and variable deterministic structure, are analyzed in Chapter 6.

3.2 Autocorrelation and Power Spectrum

The basic objects of study in this thesis, namely the autocorrelation and its Fourier transform, the power spectrum, are defined in this section. The definitions are given for both deterministic and stochastic signals. The random signals of primary interest in random modulation are wide–sense stationary signals, and they are discussed in this section. It will turn out that although not all signals of interest are wide–sense

stationary. they can be 'stationarized' for the purposes of power spectral analysis. The stationarization procedure could be motivated on physical grounds as well, given that the power spectrum should be measurable in physical experiments. and that it should not depend on the choice of the time origin. Ergodicity is a property of a stochastic signal that requires all sample (temporal) averages to equal ensemble (statistical) averages. It will turn out that this property too has to be postulated for signals analyzed in this thesis.

As mentioned earlier, power spectral formulas for the 0–1 switching function corresponding to different modulation schemes will be derived in the following chapters. The transformation of power spectrum under linear filtering is also discussed in this section.

The power spectral formulas developed in the following chapters are sometimes rather intricate, and a need arises to verify them. The numerical experiments used to validate analytical results in this thesis consist of Monte–Carlo simulations followed by spectral estimation procedures. Estimation of the power spectrum is a long–standing problem in signal processing, and methods of interest for this thesis are considered towards the end of this section.

3.2.1 Deterministic Signals

A study of randomized switching strategies necessitates a common framework for deterministic and stochastic (random) signals. Random signals are visualized as ensembles (families) of deterministic signals. The class of deterministic signals u considered in this thesis are those that have a well–defined *autocorrelation* for all τ:

$$R_u(\tau) := \lim_{T\to\infty} \frac{1}{2T} \int_{-T}^{T} u(\sigma)u(\tau+\sigma)d\sigma \tag{3.1}$$

This class of deterministic time signals is denoted by $\mathcal{W}$, and it is shown later that it contains all signals of interest in random modulation. The Fourier transform of $R_u(\tau)$ is called the *power density spectrum* (or spectral density) $S_u(f)$. The reason for the name will become clearer shortly.

Let $U_{2\hat{T}}$ denote the Fourier transform of the symmetrically *truncated* version of $u(\cdot)$ of length $2\hat{T}$. The existence of this transform can be guaranteed by requiring $u(\cdot)$ to be locally L^2 (square integrable). An important result of the Fourier theory [16], [28], due to Wiener and Khintchine, shows that S_u is related to $U_{2\hat{T}}$ as follows:

$$S_u(f) = \lim_{\hat{T}\to\infty} \frac{1}{2\hat{T}} \mid U_{2\hat{T}}(f) \mid^2 \tag{3.2}$$

In some references (3.2) is used to *define* $S_u(f)$ and then R_u and S_u are shown to be a Fourier pair, a result that is referred to as the Wiener-Khintchine theorem. The quantity $\frac{1}{2\hat{T}} \mid U_{2\hat{T}}(f) \mid^2$ is called the *periodogram* of $u(\cdot)$, and plays a prominent role in the analysis of random modulation.

The plausibility of (3.2), and the origin of the name "power spectrum" for the Fourier transform of the autocorrelation, are suggested by the following considerations (for a more thorough review, see for example [100]). Assume that a deterministic signal $x(\cdot)$ is a voltage on a 1 Ω resistor. Then

$$R_x(0) = \lim_{\hat{T}\to\infty} \frac{1}{2\hat{T}} \int_{-\hat{T}}^{\hat{T}} x^2(\sigma)d\sigma \tag{3.3}$$

or, from the Parseval-Plancherel equality, with $X_{2\hat{T}}$ being the Fourier transform of $x(t)$ truncated to an interval of length $2\hat{T}$.

$$R_x(0) = \lim_{\hat{T}\to\infty} \frac{1}{2\hat{T}} \int_{-\infty}^{\infty} \mid X_{2\hat{T}}(f) \mid^2 df \tag{3.4}$$

The integral (3.3) is the average power dissipated by the resistor, so the quantity $\frac{|X_{2\hat{T}}(f)|^2}{2\hat{T}}df$ describes the power in the frequency range f to $f + df$.

The class W of signals includes "power signals" [25] (by setting $\tau = 0$), which in turn contains all globally L^2 (or bounded power) signals. In addition, from the Schwartz inequality,

$$\mid R_u(\tau) \mid \leq R_u(0), \quad \forall \tau \tag{3.5}$$

For periodic signals $u(\cdot)$, with period T. the following can be established:

$$u(t) = \sum_{n \in Z} c_n e^{in2\pi t/T}, \tag{3.6}$$

$$R_u(\tau) = \sum_{n \in Z} | c_n |^2 e^{in2\pi\tau/T}, \tag{3.7}$$

$$R_u(0) = \sum_{n \in Z} | c_n |^2 \tag{3.8}$$

and

$$S_u(f) = \sum_{n \in Z} | c_n |^2 \delta(f - \frac{n}{T}) \tag{3.9}$$

The spectrum in this case is referred as *discrete.*

The above results can be generalized to cover the class of *almost periodic functions*, which are defined as follows. Suppose that $f(\cdot)$ is continuous on R, real or complex valued. Let $\varepsilon > 0$ and τ_ε be such that

$$| f(t + \tau_\varepsilon) - f(t) | \leq \varepsilon \tag{3.10}$$

Then τ_ε is a *translation number* of ε. If, $\forall \varepsilon > 0, \exists F_\varepsilon \in$ R such that every $(a, a + F_\varepsilon)$ contains translation numbers belonging to ε, then $f(\cdot)$ is said to be *almost periodic.* Periodic functions are a special case, where $T, 2T, 3T \ldots$ are translation numbers $\forall \varepsilon$. It can be noted that for $u(\cdot)$ almost periodic, R_u is also almost periodic. S_u is discrete and many relations analogous to the case of periodic functions can be established.

3.2.2 Stochastic Signals

The stochastic equivalent of the autocorrelation defined in (3.1) is considered next. Let $(\Omega, \mathcal{A}, P)$ denote the usual probability space [27], Ω being a set (sample space, or the set of elementary outcomes or trials), $\mathcal{A}$ a σ-algebra in Ω (event space, i.e., a collection of subsets of Ω), and P a measure on $\mathcal{A}$ with $P(\Omega) = 1$. Let $I \subset$ R be the indexing set for the time variable. A real stochastic signal is a mapping ξ that, for every trial $\omega \in \Omega$, produces the corresponding point (function) in R^I, denoted by

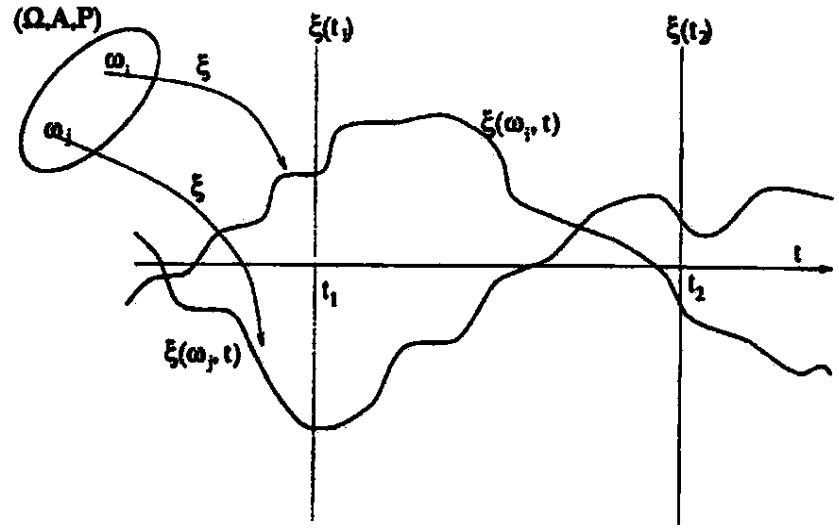


Figure 3.2: Basic Notation for a Stochastic Process.

$\xi(\omega, t)$, or simply by $\xi(t)$. This is the *realization* of the random signal ξ corresponding to the trial $\omega \in \Omega$. In the words of [44], a stochastic process is a family of random variables indexed by I.

The autocorrelation of a random process $u(\cdot)$ is defined as

$$R_u(\tau) := \lim_{T \to \infty} \frac{1}{2T} \int_{-T}^{T} E(u(\sigma)u(\tau + \sigma))d\sigma, \tag{3.11}$$

where the expectation E is taken over the whole ensemble. This definition is consistent with (3.1), since for deterministic signals the ensemble consists of a single realization. The power (density) spectrum S_u is again defined as the Fourier transform of R_u.

The impulsive part of S_u is again referred to as the *discrete* spectrum, and it is characterized entirely by the locations $f_1, f_2, \ldots$ of the impulses ("line frequencies", "harmonic frequencies") and by positive numbers $k_1, k_2, \ldots$ representing the strengths of the impulses ("line intensities" in optics).

3.2.3 Wide–Sense Stationary (WSS) Signals

The class of signals for which (3.11) holds without time–averaging is the class of wide-sense stationary (WSS, weakly stationary) random signals. WSS signals satisfy:

$$E(x(t)) = m_x \in \mathsf{R}, \quad \forall t \in I, \tag{3.12}$$

and

$$E[x(t)x(t+\tau)] = \hat{R}_x(\tau), \quad \forall t, \tau \in I \tag{3.13}$$

Important properties of $R_u(\tau)$ for WSS signals with finite mean power (i.e. globally L^2 on I) are enumerated next:

1. $R_u(\tau) = R_u(-\tau), \forall \tau$.
2. $\mid R_u(\tau) \mid \leq R_u(0)$.
3. A random signal $u(\cdot)$ is continuous in the mean square if and only if $R_u(\tau)$ is continuous at the origin, which in turn implies continuity everywhere. In the general case, $R_u(\tau)$ differs from a continuous function on at most a null set.
4. $R_u(\tau)$ is non–negative definite [16]. This implies that its Fourier transform is integrable and non–negative.
5. In general, $R_{x+y} \neq R_x + R_y$ and $x \neq y \not\Rightarrow R_x \neq R_y$

The stochastic version of the Wiener–Khintchine theorem (3.2) states that

$$\lim_{T \to \infty} E(\frac{1}{2T} \mid U_{2T}(f) \mid^2) = S_u(f) \tag{3.14}$$

The strong (pointwise) convergence does not hold for non–stationary signals. The convergence in (3.14) for non–stationary signals fails to be pointwise even if $S_u(f) \in C^\infty$. For details on weak convergence the reader is referred to [21]. Precise convergence statements for non–stationary random processes can be found, for instance, in [16].

3.2.4 Stationarizable Signals

The main benefit of wide–sense stationarity in random modulation is the pointwise convergence result in (3.14). It turns out that some signals of interest in random modulation are not WSS. For example, a deterministic, periodic function $x(t)$ with a period $\bar{T}$ is not WSS, since its autocorrelation calculated from (3.13) depends on t. However, it is wide–sense *cyclostationary* (or periodically stationary, [95]), in that $R_x(t+\tau+m\bar{T}, t+m\bar{T}) = R_x(t+\tau, t)$. The class of random processes for which

$$E[x(t+\bar{T})] = E[x(t)] \tag{3.15}$$

and

$$\bar{R}_x(t+\tau+m\bar{T}, t+m\bar{T}) = \bar{R}_x(t+\tau, t) \;\; \forall m \in \mathbf{N} \tag{3.16}$$

where $\bar{R}_x(t1, t2) = E[x(t_1)\; x(t_2)]$. References on cyclostationarity are numerous [43],[38],[39],[40], [42],[57],[88], but definitions vary. Wide–sense cyclostationary processes are covered by the definition (3.11). It is easy to see that

$$R_x(\tau) = \frac{1}{\bar{T}} \int_0^{\bar{T}} \bar{R}_x(\sigma+\tau, \sigma) d\sigma \tag{3.17}$$

Alternatively, analysis in this case can be based on the shifted process

$$\hat{x}(t) = x(t-\theta) \tag{3.18}$$

where θ is a random shift of the time origin, i.e., a random variable with a uniform density in $[0, \bar{T}]$. The shifted process is WSS and $\bar{R}_{\hat{x}} = R_x$. In some references a periodic random signal $x(t)$ is *defined* as an ensemble of realizations $\hat{x}(t)$, in which case the wide–sense stationarity follows immediately [28]. Some authors [7] have the postulate that a power spectrum has to be independent of time shifts in the waveform, and the random shift is a simple way to build the property into the definition of power spectra.

Cycle lengths in random modulation are not necessarily equal (e.g., in aperiodic

modulation). In that case, it turns out to be natural to consider the class of processes that are *almost stationary* in the wide sense, as defined by Gardner [38]. The autocorrelation function of such processes is almost periodic, in the sense of (3.10). It turns out that such almost stationary processes can be stationarized by a random shift of the origin [38], [39].

3.2.5 Stationarization of Signals Defined on Markov Chains

Of special concern in the context of the novel random modulation schemes for power electronics proposed here are signals defined by Markov chains, where each transition of the underlying Markov chain generates a cycle of the switching waveform. The waveform $q(t)$ is a concatenation of such cycles. In this case the autocorrelation $R_x(t+\tau,t)$ depends on the state of the underlying Markov chain. The power spectrum for this class of signals can be defined either formally, via the weak convergence of the periodogram (due to non–stationarity) [37], or via a suitable conditioning. The second approach is adopted in this thesis, and is described in more detail in Chapter 6. Conditional correlations for Markov chains in FM modulation are considered in [94].

The conditioning procedure is based on a random incidence assumption, in addition to taking the expectation in the autocorrelation calculation. Random incidence is based on a random choice of time after which the observation of the stochastic process begins. Random incidence is also assumed to occur long after the Markov chain has been initialized, and it is done in a manner that is independent from the actual history of the process [26]. The random incidence assumption plays the role of the random time shift θ in (3.18) in stationarizing the underlying process.

3.2.6 Power Spectra and Linear Systems

An important result for applications is the transformation of the autocorrelation when a signal $x(\cdot)$ is passed through a linear time invariant filter, characterized by its impulse response $h(\cdot)$. For the purpose of analysis of random modulation, $x(\cdot)$ can be assumed to be a stationary (or stationarized) signal. The expression (3.20) below

could be generalized to linear time varying filters, and formula (3.22) given below holds for more general signals $x(\cdot)$ [16].

For each realization of the random process $x(\omega, t)$, the output $y(\omega, t)$ of the system is given by convolution:

$$y(\omega, t) = x(\omega, t) * h(t), \quad \forall \omega \in \Omega \tag{3.19}$$

or, after suppressing the ω notation,

$$y(t) = \int_{-\infty}^{\infty} x(t)h(t-u)du \tag{3.20}$$

Simple calculations then show that the expected value of y is

$$E(y) = H(0) \cdot E(x) \tag{3.21}$$

and the power spectrum of y is given by

$$S_y(f) = \mid H(f) \mid^2 S_x(f), \tag{3.22}$$

assuming $H(f)$ stable. This mapping of power spectra through linear systems serves as further justification for the use of the term *power spectrum* for the Fourier transform of the autocorrelation. The power of the signal is localized on the frequency axis in a sense that if a signal is the input to a narrow-band system (i.e., narrow band-pass filter), then the power of the output is proportional to the power spectrum of the input.

3.3 Monte–Carlo Verification of the Power Spectral Formulas

The formulas for power spectra of different random modulation schemes developed in Chapters 4–6 are rather involved, and a need arises to verify and explore them

through simulation. The power spectrum of a simulated switching waveform is obtained through an estimation procedure. Power spectrum estimation is one of the most important problems in signal processing and has a very rich history [95], [78], [90]- [82].

In this thesis power spectral formulas for random modulation are verified by applying power spectrum estimation methods to Monte–Carlo realizations of the switching function $q(t)$. The discussion in this section deals primarily with direct estimation methods that yield the power spectrum $S_q(f)$. Indirect procedures that estimate *both* the autocorrelation and the power spectrum [91] are briefly noted. We concentrate on non-parametric, classical estimation methods, which are well understood and for which software is readily available [101].

Classical direct estimation methods may be thought of as approximate implementations of the operations specified in the Wiener-Khintchine theorem (3.14). Typically, a single realization of the process of length $2KT$ is divided into K sections, and the periodogram is computed for each of these. The availability of the Fast Fourier Transform (FFT) to calculate the Fourier transforms involved is a major advantage. The expectation operation in (3.14) is then approximated by averaging the K individual periodograms. This is referred to as Bartlett's method. Under appropriate conditions (related to ergodicity) on the stochastic process, this computation produces a consistent, asymptotically unbiased ($K \to \infty, T \to \infty$) estimate of the power spectrum [60], [101]. We shall assume that the switching functions $q(t)$ of interest to us satisfy the conditions required for validity of such an estimation procedure. The close match between our analytical formulas and the Monte–Carlo verification suggest that this is indeed a good assumption.

Although the above procedure is asymptotically unbiased, in practice K and T are finite, so there is inevitable bias. The use of appropriate windows in the time domain contributes to bias reduction. An unpleasant effect of windowing is known as leakage and has its source in the side–lobes (in the frequency domain) of the windows used.

Welch (1967) modified Bartlett's method by allowing data segments to overlap

in addition to windowing data in the time domain. This method is widely used and is available in the Matlab software package. Use of different windows enables, for instance, increased frequency resolution. A heuristic suggested in [101] is that a 50% overlap between the data segments improves results in many applications.

The Blackman–Tukey method is an indirect procedure with performance characteristics comparable to Welch's method [101]. Although Welch's method requires a little more computational effort than Bartlett or Blackman–Tukey, this is not a major factor in the verification process, due to its off-line nature.

A brief heuristic argument about the choice of parameters in Welch's method is presented next. Let N denote the number of points in the simulated record, M denote the number of points in a data segment ($M = KN$), and let R denote the number of points per cycle of the switching function $q(t)$. If R is set to 64, so that the duty ratio resolution is better that 2 %, then the spectrum can be estimated up to the 32–nd harmonic (Nyquist frequency). The spectral estimate contains $\frac{M}{2}$ points (for positive frequency), and if 32 points per unit frequency are required, then $M = 2048$. Thus, if $K = 8$, a total of N=16384 points is needed, which is reasonable within the Matlab package. Given a constraint on N, either M can be increased, thus improving resolution, but decreasing K and getting a more "jittery" estimate, or K can be increased, thus reducing the frequency resolution, but obtaining smoother estimates. An overlap of $\frac{M}{2}$ between the data segments improves the estimation results, essentially by increasing the number of data segments K, while keeping N fixed.

Another practical issue is the estimation of impulse coefficients in a discrete spectrum. The use of windowing in Welch's method introduces side lobes, and a part of the signal power gets "smeared" into the nearby frequencies. The signal power in a particular frequency segment is approximated by multiplying the estimated value of the power spectrum by the width of the frequency segment. If the product of the continuous part of the spectrum with the segment width is appreciable, then it can be subtracted from the total signal power in the segment, thus yielding a better estimate of the impulse strengths.

Problems in spectral estimation described in this section apply fully to digital spectral analyzers [50]. Analog systems for spectral analysis [86], [41] utilize narrow band-pass filters to isolate a narrow frequency band of interest, followed by squaring devices and low–frequency filters to provide a spectral estimate. The design of analog narrow band–pass filters that operate accurately over different frequency ranges is a difficult technical problem. The principle of heterodyning, similar to AM radio, is typically used in analog spectral analyzers to avoid that problem [50].

3.4 Summary

A classification of random modulation schemes that are applicable to power converters is given in this chapter. The proposed categorization distinguishes between the deterministic and stochastic structure of random modulation and enables a systematic classification. It includes not only all random modulation schemes reported in the power electronics literature, but also classifies a variety of random modulation procedures that are likely to be advantageous in the future.

A unified treatment of deterministic and stochastic signals is given in this chapter. The concept of power spectrum as the Fourier transform of a suitably defined autocorrelation is introduced. The class of wide–sense stationary signals is described in more detail, and the Wiener–Khintchine theorem is noted. It is shown that certain non–stationary signals of interest, namely cyclostationary signals and signals specified by Markov chains, can be brought into a correspondence with WSS signals. The main instruments in the derivation of this equivalence are a random shift of the time origin and the random incidence assumption for Markov chains.

The power spectral formulas developed in the following chapters are somewhat delicate, and a need arises to verify them through simulations. The approach adopted in this thesis consists of Monte–Carlo simulations of randomized switching waveforms, followed by spectral estimation procedures. Methods described in this chapter are suited for a digital measurement and estimation setup. Welch's estimation procedure is outlined in more detail, together with important practical considerations regarding

the choice of parameters in Monte–Carlo simulation and estimation.

The three most important classes of random modulation, namely stationary modulation. block–stationary random modulation (intended for inverter operation), and random modulation based on Markov chains. are analyzed in the next three chapters.

Chapter 4

Stationary Random Modulation Schemes

Stationary random modulation schemes are considered in this chapter. They are characterized by invariant deterministic and stochastic structure, namely

- The nominal or reference on-off pattern being dithered does not change from cycle to cycle (no variations in the requirements on average quantities, e.g., in duty ratio).
- At each new cycle, the same statistical structure is used — the dithering (in time) is based on independent trials.

Results on random modulation obtained in [86] are reviewed first. It turns out that many basic stationary randomized switching strategies can be analyzed within this framework, and that the practical DC/DC implementations described in Chapter 2 can be assessed using these results.

4.1 Random Pulse Amplitude Modulation

To outline the salient features of the method, pulse trains with *periodic* position (i.e., no dithering in time), but random amplitude are considered first. Although our real interest is in the switching function $q(t)$, which can take only binary values, the

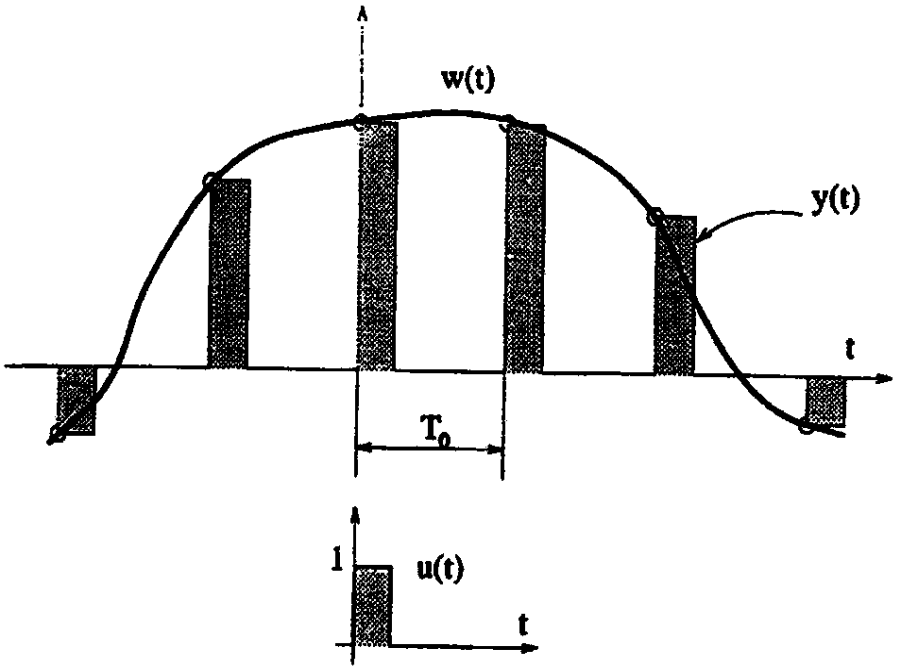


Figure 4.1: Sampling of the Random Process $w(t)$ with a Rectangular Pulse $u(t)$ with a Constant Width and Height Proportional to w.

analysis of random pulse amplitude modulation (PAM) will allow appreciation of the basic approach to analysis.

Assume that $w(t)$ is a wide-sense stationary (WSS) process which is being sampled by a series of periodic pulses $u(t - nT_0)$. resulting in a waveform with pulse whose shape and position are fixed, but whose amplitude from pulse to pulse is determined by the magnitude of $w(t)$ at the various sampling times. This setup is illustrated in Fig. 4.1. where $u(t)$ is a single rectangular pulse of unit height and constant width, $w(t)$ is a WSS random process (the bold line in the figure), and the resulting pulse train is denoted by $y(t)$. Thus,

$$y(t) = \sum_{-\infty}^{\infty} w(nT_0)\, u(t - nT_0) \tag{4.1}$$

The procedure to calculate the power spectrum of the signal $y(t)$ consists of the following steps [86]:

- Consider a truncated realization $y_N(t)$ of the signal $y(t)$ consisting of $2N+1$ pulses, and study its autocorrelation. Let the period be denoted by T_0, and let $y_n = w_n\, u(t - nT_0)$. Then

$$y_N(t) = \sum_{n=-N}^{N} y_n \tag{4.2}$$

$$\tilde{R}_{yN}(\tau) = \frac{1}{(2N+1)T_0} \int_{-NT_0}^{NT_0} y_N(\sigma) y_N(\sigma - \tau) d\sigma \tag{4.3}$$

where the autocorrelation of the sampled process y_N can be evaluated as $R_{yN}(\tau) = E[\tilde{R}_{yN}]$, and the fact that R_{yN} is an even function has been used. Substituting (4.1) we get

$$\tilde{R}_{yN}(\tau) = \sum_{m=-N}^{N} \sum_{n=-N}^{N} w_m w_n \int_{-NT_0}^{NT_0} u(\sigma - mT_0) u(\sigma - \tau - nT_0) d\sigma] \tag{4.4}$$

Observe that $u(t)$ is bounded in time, so that the integral over σ can be extended to $(-\infty, \infty)$ without changing its value.

- On the second step, the inverse Fourier transform of $u(t)$ is used:

$$\begin{aligned} \tilde{R}_{yN}(\tau) \;=\; & \int_{-\infty}^{\infty} \sum_{m=-N}^{N} \sum_{n=-N}^{N} w_m w_n \int_{-\infty}^{\infty} U(f_1) e^{i2\pi f_1 \sigma} \\ & e^{-i2\pi f_1 m T_0} df_1 \int_{-\infty}^{\infty} U(f_2) e^{i2\pi f_2 \sigma} e^{-i2\pi f_2 \tau} e^{-i2\pi f_2 n T_0} df_2 d\sigma \end{aligned} \tag{4.5}$$

which together with the Poisson identity [86]

$$\int_{-\infty}^{\infty} e^{i2\pi(f_1+f_2)\sigma} d\sigma = \delta(f_1 + f_2) \tag{4.6}$$

and the fact that the signal u is real (so $U(-f_1) = U^*(f_1)$) yields the expression containing a single integral over frequency:

$$\tilde{R}_y(\tau) = \int_{-\infty}^{\infty} \sum_{m=-N}^{N} \sum_{n=-N}^{N} w_m w_n e^{i2\pi f(n-m)T_0} \mid U(f) \mid^2 e^{i2\pi f \tau} df \tag{4.7}$$

where $U(f)$ is the Fourier transform of $u(t)$. Next, letting $l = n - m$, and recalling that y_N vanishes outside the window of length $(2N+1)T_0$ so that the

sums can be rewritten in terms of l and n, we get

$$\tilde{R}_{yN}(\tau) = \int_{-\infty}^{\infty} \mid U(f) \mid^2 \sum_{l=-N}^{N} e^{i2\pi flT_0} \sum_{n=-N}^{N} w_m w_{m+l} e^{i2\pi f\tau} df \qquad (4.8)$$

- On the third step we take the ensemble average, followed by the limiting operation in time to get

$$R_y(\tau) = \lim_{N\to\infty} [\frac{1}{(2N+1)T_0} \int_{-\infty}^{\infty} \mid U(f) \mid^2 E[\sum_{l=-N}^{N} e^{i2\pi flT_0} \sum_{n=-N}^{N} w_m w_{m+l}] e^{i2\pi f\tau} df] \qquad (4.9)$$

The wide–sense stationarity of $w(\cdot)$ guarantees

$$E[\sum_{l=-N}^{N} w_m w_{m+l}] = (2N+1)E[w_0 w_l] \qquad (4.10)$$

where w_0 and w_l are samples of $w(\cdot)$ that are lT_0 apart. Then the power spectrum can be recognized on the right–hand side of equation (4.9) as the quantity that is being inverse–transformed to obtain R_y:

$$S_y(f) = \frac{\mid U(f) \mid^2}{T_0} \sum_{l=-\infty}^{\infty} E[w_0 w_l] e^{i2\pi flT_0} \qquad (4.11)$$

This is a key equation, and will be used as a starting point in derivations of the power spectra of different stationary random modulation methods. The only modification will be that instead of w, some related waveforms are used in the expectation operator E in (4.11).

4.2 Random Pulse Position Modulation

In this section the case of random pulse position modulation (PPM) is considered, where a WSS process $w(\cdot)$ is sampled with $u(\cdot)$, but now we allow for a variation in the (time) position of each pulse, i.e we consider $u(t - nT_0 - \varepsilon_n)$. The dither ε_n has to be bounded, so that overlap between adjacent intervals is prevented. In this case a (fictitious) complex time series $w_n e^{-i2\pi f\varepsilon_n}$ is considered, and the same procedure as

before yields:

$$S_y(f) = \frac{|\,U(f)\,|^2}{T_0} \sum_{l=-\infty}^{\infty} E[w_0 w_l e^{i2\pi f(\varepsilon_l - \varepsilon_0)}] e^{i2\pi f l T_0} \qquad (4.12)$$

For the switching function q. $w(t) = 1$, implying $R_w(0) = m_w^2 = 1$. Note that constraints on ε are needed to make the overall random process WSS. The autocorrelation of y equals the inverse Fourier transform of S_y in (4.12), and the wide–sense stationarity condition (3.13) requires that the autocorrelation $\hat{R}_y$ does not depend on the time origin for y. A sufficient condition, which is the most important in practice, is that $w(\cdot)$ and $\varepsilon(\cdot)$ are statistically independent of each other (so that the expectation in (4.12) factors to a product), and that ε's are mutually independent. In that case the expectation in equation (4.12) factors to a product of expectations for $w_0 w_l$ and $e^{i2\pi f(\varepsilon_l - \varepsilon_0)}$. Next, we use the facts that w is a WSS process. and that the expectation of $e^{i2\pi f(\varepsilon_l - \varepsilon_0)}$ depends only on l, given that ε's are mutually independent, and establish the wide–sense stationarity of the process y.

Let the probability density function for ε be $p_\varepsilon(\cdot)$ and let its Fourier transform be denoted by $P_\varepsilon(f)$. For $l = 0$ the term under the summation in equation (4.12) equals 1, and otherwise it equals $|\,P_\varepsilon(f)\,|^2$. Thus, by adding and subtracting $|\,P_\varepsilon(f)\,|^2$, and after invoking the Poisson identity,

$$S_y(f) = S_u(f)[(1 - |\,P_\varepsilon(f)\,|^2) + \frac{|\,P_\varepsilon(f)\,|^2}{T_0} \sum_{k=-\infty}^{\infty} \delta(f - \frac{k}{T_0})] \qquad (4.13)$$

where $S_u(f) = \frac{|U(f)|^2}{T_0}$. This expression is found, for example, in [86]

As an example, assume $T_0 = 1$. Then for rectangular pulses of width D

$$S_y(f) = (\frac{sin(\pi f D)}{\pi f})^2[(1 - |\,P_\varepsilon(f)\,|^2) + |\,P_\varepsilon(f)\,|^2 \sum_{k=-\infty}^{\infty} \delta(f - k)] \qquad (4.14)$$

The non-dithered case is easily recovered. For $\varepsilon_i = 0$. $p_\varepsilon(t) = \delta(t)$, and $P_\varepsilon(f) = 1$, so

$$S_y(f) = (\frac{sin(\pi f D)}{\pi f})^2 \sum_{k=0}^{\infty} \delta(f - k) \qquad (4.15)$$

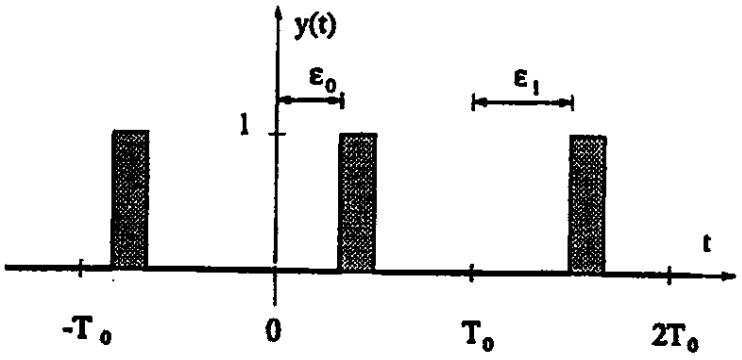


Figure 4.2: Pulse Position Modulation.

as expected for a periodic train of rectangular pulses.

Since $p_\varepsilon(\cdot)$ is a probability density function, it must integrate to 1, thus $P_\varepsilon(0) = 1$. Given that $| P_\varepsilon(f) | \leq 1$ [93], and that from Parseval's equality

$$\int_{\mathbb{R}} | P_\varepsilon(f) |^2 = 1, \tag{4.16}$$

then $| P_\varepsilon(f) | < 1$ in some frequency range. The expression (4.14) shows that in this frequency range the discrete part of the spectrum will be decreased, when compared to the conventional switching strategy. The price paid for this result is the introduction of the continuous part of the spectrum (the "fill-in") $1 - | P_\varepsilon(f) |^2$. This might be quite acceptable, given the standards described earlier. and this is the rationale behind a growing number of applications.

For illustration, specialize to $D = 0.5$ and ε_i uniformly distributed in $[0, 0.5]$. For these values, the discrete, nondithered spectrum is shown in Fig. 4.3 together with the discrete spectrum for random PPM, and the continuous spectrum is shown in Fig. 4.4.

An application of Welch's method (which is implemented in the signal processing toolbox of the Matlab package) to numerically verify (4.14) via Monte–Carlo simulation is described next. Numerical values are $D = 0.5$, $T_0 = 1$, as in the previous example. A total of 128 periods is analyzed, with 64 samples in each, thus enabling a

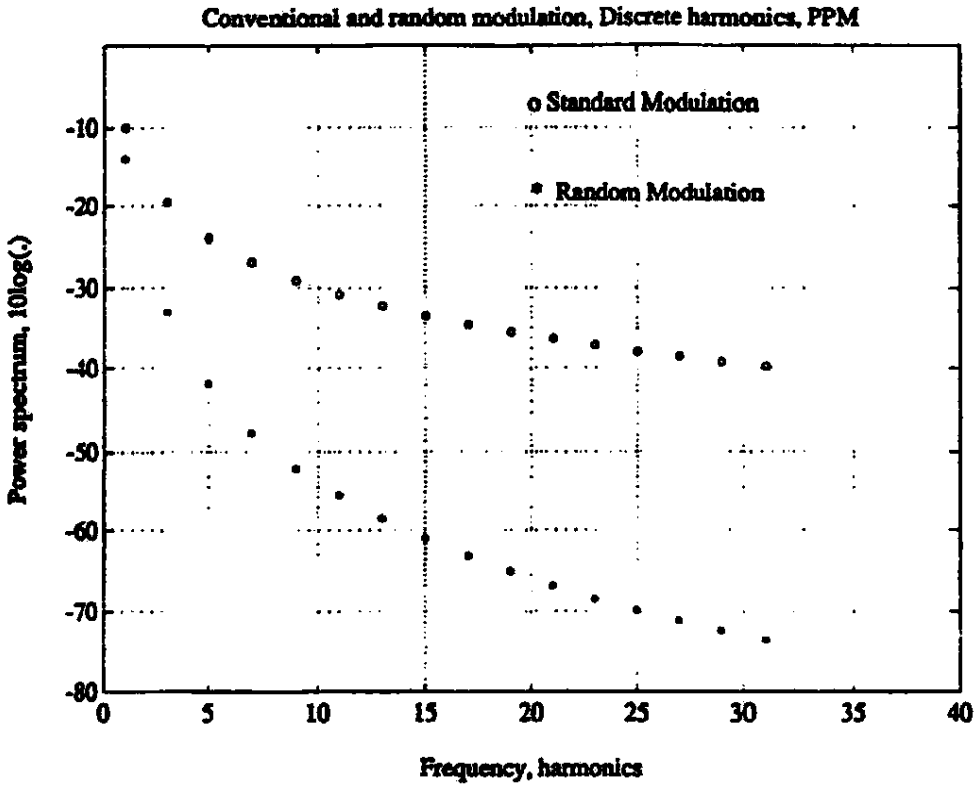


Figure 4.3: Discrete Spectrum - Comparison of Conventional and Random PPM Modulation, Period $T_0 = 1$, Duty Ratio $D = 0.5$.

resolution below 2% in the pulse position and with the Nyquist frequency of 32. The total number of points is thus $N = 8192$ and the width of an individual data segment M is varied. The approximate frequency resolution of Welch's method, defined as the minimum distance of two distinguishable sinusoids, is $\frac{40.96}{M}$ in this case [101].

In Figs. 4.5 and 4.6 the estimated power spectrum (dotted) is shown together with the calculated continuous spectrum. Welch's procedure generates the estimate of the total power spectrum, i.e., of the sum of continuous and discrete spectra, so the large deviations between the estimated and calculated continuous spectrum near the peaks are due to discrete spectral components. Welch's procedure generates the estimate of the total power spectrum, i.e., of the sum of continuous and discrete spectra. This remark holds for all examples presented in this thesis. The general agreement is good. In Fig. 4.6 the first two harmonics are magnified. These figures show a "jittery" estimate, as expected for a large $M = \frac{N}{2}$. Overlapping the frequency windows by a half width, as suggested in the literature [101],[90], does not improve the

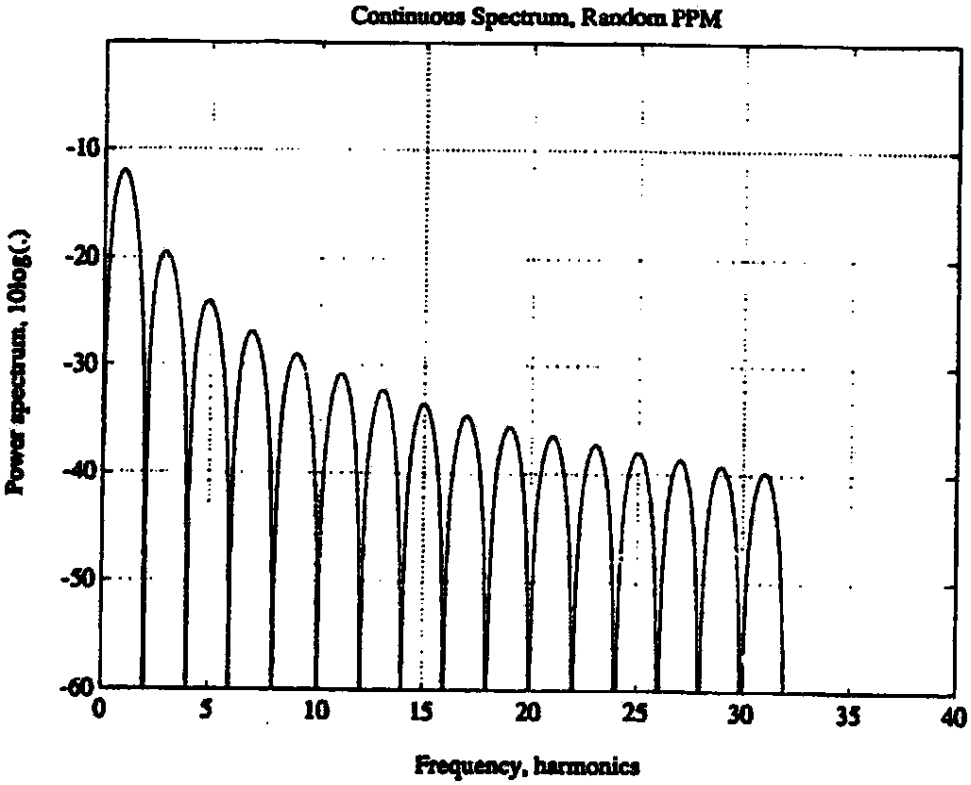


Figure 4.4: Continuous Spectrum - Random PPM, Period $T_0 = 1$, Duty Ratio $D = 0.5$.

situation significantly. It is also important to estimate the coefficient associated with the impulse at the unit frequency. From the known width of the frequency segment, $\frac{1}{64}$ for the particular value of M, the value of 0.0296 is obtained for the area of the peak centered at $f = 1$, and 0.0083 and 0.0084 in the neighboring segments to the left and right, respectively. Calculated values for the discrete component at $f = 1$ are 0.0411, and 0.0009 for the integrals of the continuous components to the left and to the right. The discrepancy in total signal power over all three segments is approximately 5%, and the error in the estimate of the impulse strength (0.0296 instead of 0.0420) is due to the spectral "leak" inevitable due to windowing in the time domain [101]. In this particular case the frequency resolution (defined as the ability to distinguish between the two sinusoids at nearby frequencies) is approximately 0.01, while the width of a frequency segment is $1/64 = 0.015$

The same quantities are shown in Figs. 4.7–4.8, for a reduced value of $M = 1024$. In this case the spectrum estimate is smoother, as expected, and spectral leakage of

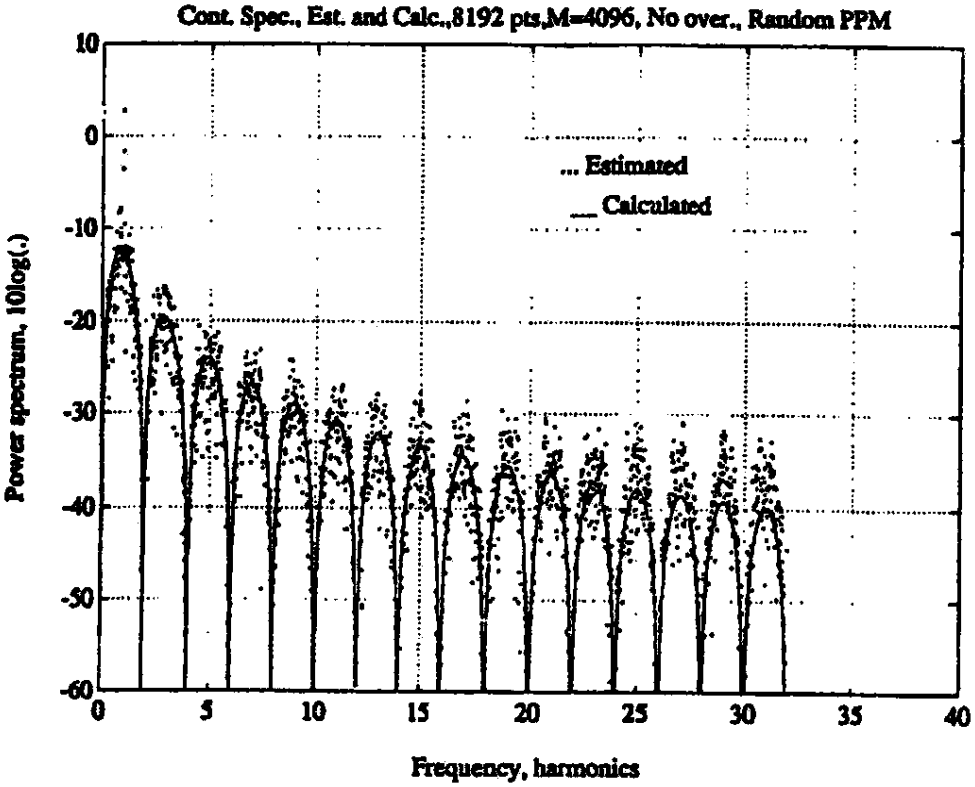


Figure 4.5: Random PPM - Estimated and Calculated Spectrum, Calculated in M=4096 Points.

the impulse due to windowing is again observed. The frequency resolution is reduced, which in this particular case is not a major concern, due to the wide separation of impulses in the spectrum.

As another example, consider a very special case of PPM in which ε can take only two extreme values, namely 0 and $(1-D)T = D'T$. This is a DC/DC version of the block-stationary (inverter) modulation scheme described in [74]. In this case

$$S_v(f) = \left(\frac{sin(\pi f D)}{\pi f}\right)^2 [sin^2(\pi f D') + cos^2(\pi f D') \sum_{k=-\infty}^{\infty} \delta(f-k)] \qquad (4.17)$$

For $D = D' = 0.5$, the discrete part of the spectrum vanishes altogether, except for a "dc" part at $f = 0$. A plot of the expression in (4.17) is shown in Fig. 4.9.

Our results so far allow us to directly determine the power spectra of certain other waveforms in power converters from the spectrum of the switching function $q(t)$. A simple analysis of the standard down converter [63] shown in Fig. 4.10 establishes

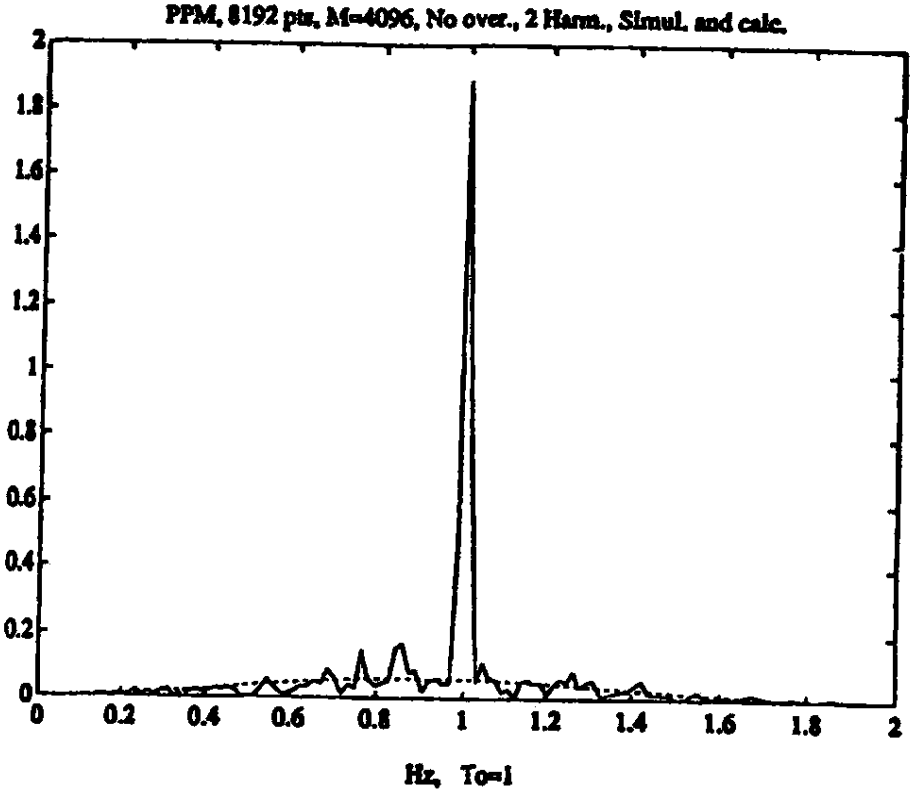


Figure 4.6: PPM - Estimated and Calculated Spectrum, First Two Harmonics, Corresponding to M=4096 Points.

that the inductor current equals the *integral* of

$$\frac{q(t)V_{in} - V_{out}}{L}$$

where V_{in} is the input voltage, V_{out} is the output voltage, and $q(t)$ is the switching function. Thus, from (3.22) the power spectrum of the inductor current at positive frequencies equals

$$S_{iL} = \frac{V_{in}}{L}\frac{1}{f^2}S_q(f) \tag{4.18}$$

Similar relations between the switching function and the *inductor* current can be observed for other basic DC/DC converters in the continuous conduction mode. In the case of a standard up (boost) converter [63], the inductor current (which happens

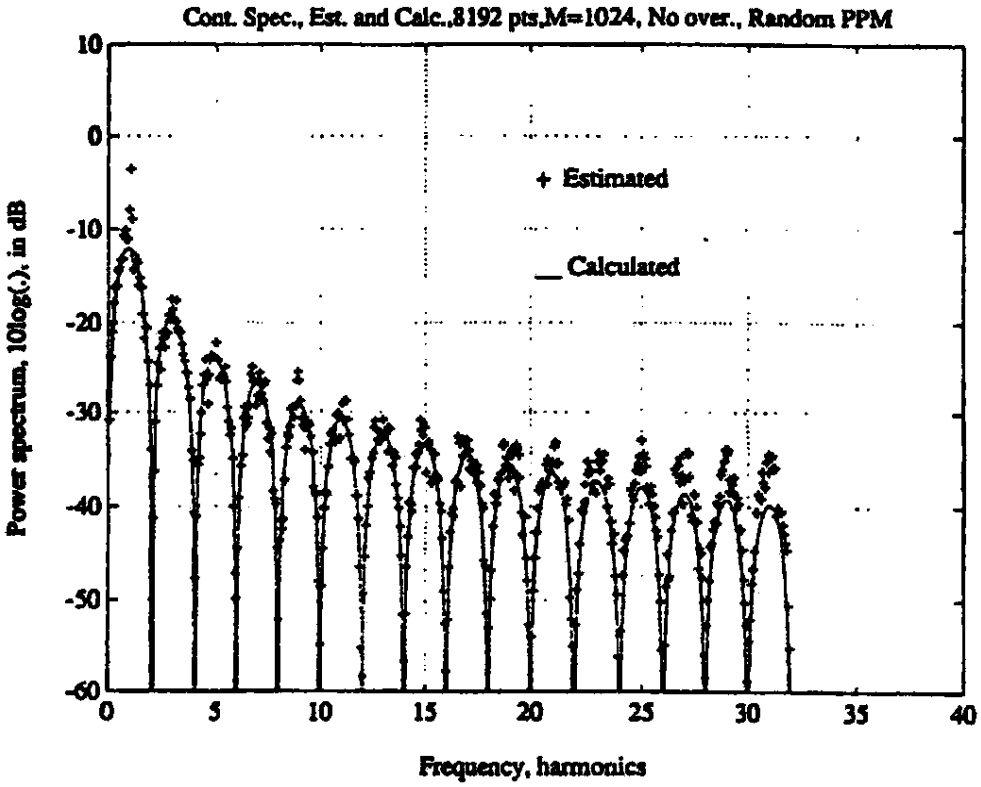


Figure 4.7: Random PPM - Estimated and Calculated Spectrum, Calculated in M=1024 Points.

to be the input current) is the integral of

$$\frac{V_{in} - V_{out} + q(t)V_{out}}{L}$$

In the case of an up-down (buck-boost) converter, the inductor current is the integral of

$$\frac{q(t)(V_{in} + V_{out}) - V_{out}}{L}$$

Analogous relationships could be derived for output voltages V_{out}.

Computation of the power spectrum of the *input* current in down and up/down converters is more intricate. We shall turn to this in the next section, after introducing a significant generalization of (4.13).

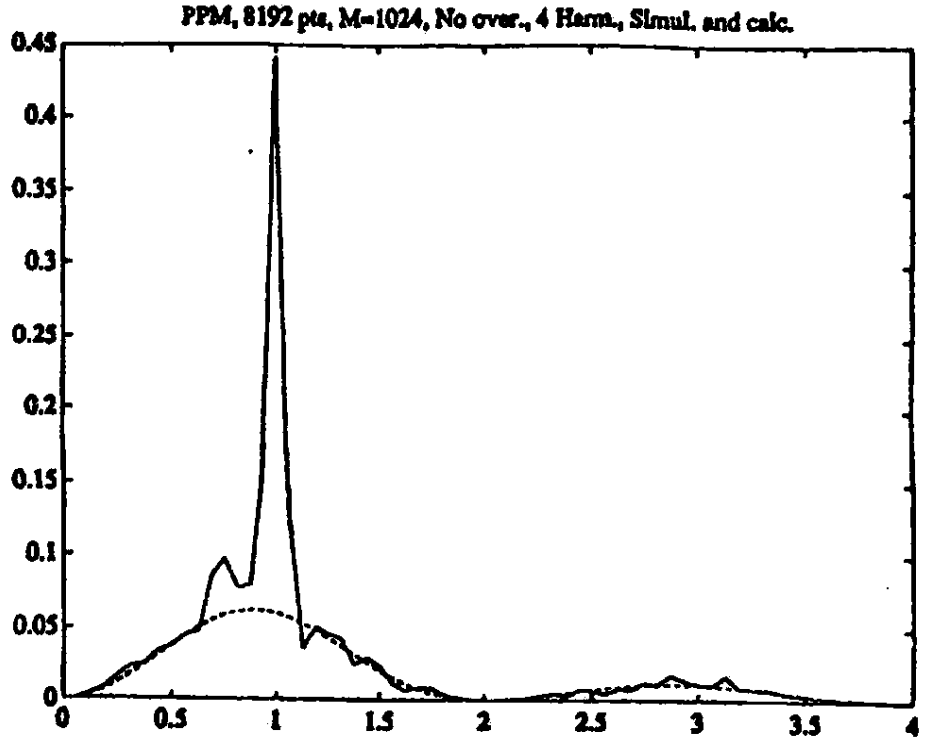


Figure 4.8: Random PPM - Estimated Total Spectrum (solid line) and Calculated Continuous Spectrum, First Four Harmonics, Corresponding to M=1024 Points.

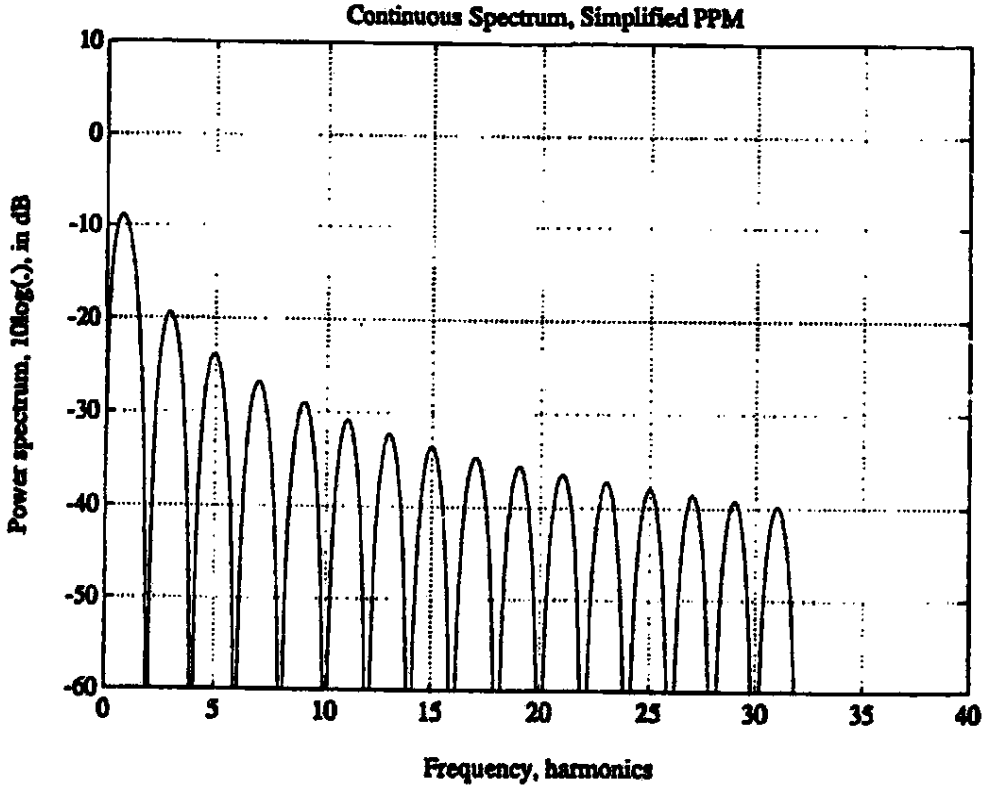


Figure 4.9: Calculated Continuous Spectrum for Simplified PPM.

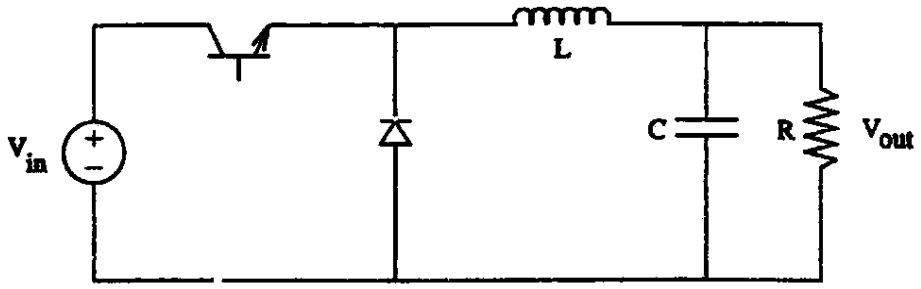


Figure 4.10: Standard Configuration of a Down (Buck) DC/DC Converter

4.3 A General Formula for Stationary Random Modulation

In the most general case of stationary random pulse modulation, the i–th cycle is parametrized by the following quantities:

1. Cycle length, T_i;
2. Duration of the "on" state. a_i;
3. Position of the "on" state with respect to the beginning of the cycle, ε_i;
4. Position of the beginning of the i–th cycle with respect to the absolute time origin ξ_i.

Let T denote the expected value of the cycle length T_i. Then the same procedure that has been applied to the case of random pulse amplitude modulation (4.4)–(4.11), with obvious changes in the parametrization of the pulse shapes $u(\cdot)$, yields the following generalization of equation (4.11):

$$S_y(f) = \frac{1}{T} \sum_{l=-\infty}^{\infty} E[w_0 w_l U_0(f, T_0, \varepsilon_0, a_0) U_l(f, T_l, \varepsilon_l, a_l) e^{i2\pi f(\xi_l - \xi_0)}] \qquad (4.19)$$

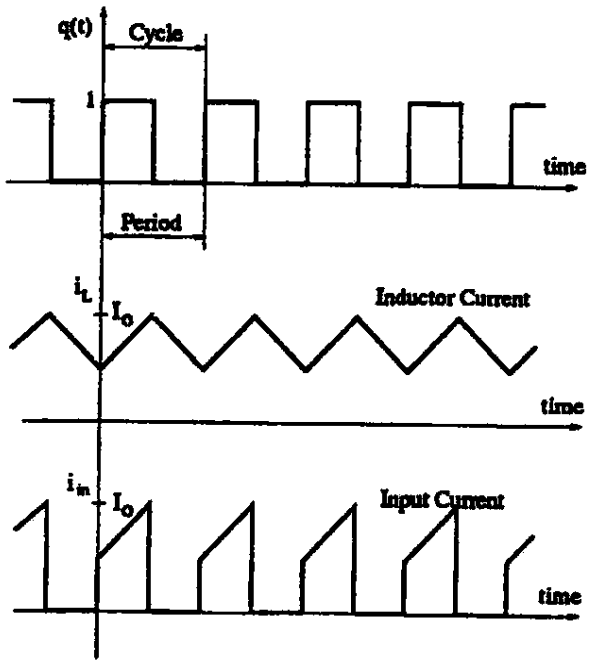


Figure 4.11: Nominal Switching Function, Inductor Current and Input Current for a Down Converter in a Continuous Conduction Mode

The specialization of this formula to various stationary random modulation schemes of interest in power electronics is considered in Section 4.4. In the remainder of this section. we show how (4.19) can be used to determine the spectrum of the input current for down and up/down converters.

In Fig. 4.11 a typical nominal switching function is given, together with the nominal inductor current and the input current, for a down converter operating in continuous conduction mode. The input current at the i–th cycle under random PPM is shown in Fig. 4.12. Note that the inductor current at the beginning of each dithered cycle is still at its nominal value I_0. The input current at the i–th cycle depends only on ε_i, and we can specialize (4.19) to that case: $(U_l(f, T_l, \varepsilon_l, a_l) = U_l(f, \varepsilon_l))$. In random pulse position modulation the lengths T_i of all cycles equal T_0, and the lengths of the "on" states a_i are equal to DT_0 for all cycles. The resulting formula

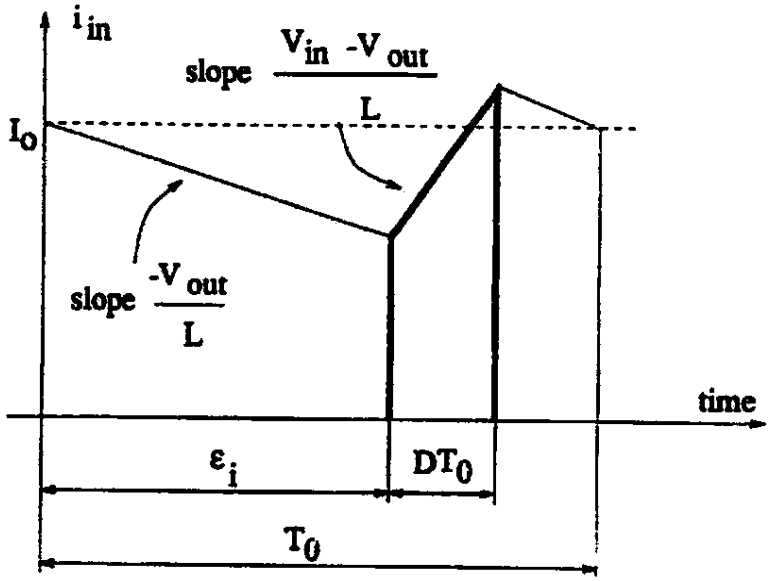


Figure 4.12: Input Current for a Down Converter in a Continuous Conduction Mode with Random Pulse Position Modulation

for the power spectrum is

$$S_y(f) = \frac{1}{T_0}[E[|U(f,\varepsilon)|^2] - |E[U(f,\varepsilon)]|^2 + \frac{1}{T_0}|E[U(f,\varepsilon)]|^2 \sum_{k=-\infty}^{\infty} \delta(f - \frac{k}{T_0})] \quad (4.20)$$

$U(f,\varepsilon)$ is the Fourier transform of the input current waveform. a single cycle of which is shown in Fig. 4.12. After writing equations for the straight line segments shown in Fig. 4.12, $U(f,\varepsilon)$ turns out to be (for $f > 0$):

$$U(f,\varepsilon) = [(I_0 - \frac{V_{in}\varepsilon}{L})\frac{\sin(\pi f DT_0)}{\pi f}e^{-i\pi f DT_0} + \frac{V_{in} - V_{out}}{L}\frac{\sin(\pi f DT_0)}{\pi f}e^{-i\pi f DT_0}\frac{1}{(i2\pi f)}]e^{-i2\pi f\varepsilon} \quad (4.21)$$

Equation (4.20) can then be evaluated, once probability densities for ε are specified.

It will turn out that the power spectrum of the input current of a down (and up/down) converter is harder to calculate for some other random modulation schemes, notably for random pulse width modulation.

4.4 Other Stationary Random Modulation Schemes

In this section results for some other stationary random modulation schemes are listed. More detailed descriptions, derivations, and simulations used for their verification are given in Appendices A–C.

4.4.1 Random Pulse Width Modulation

In random pulse width modulation (PWM), the ON state length a is varied within a fixed period T_0. Consider the case where $T_0 = 1$ and $a \in (0,1)$, with a uniform probability density. With $\alpha = \pi f$, the spectrum is given by (see equation (A.3) in Appendix A):

$$S_y(f) = \frac{1}{4\alpha^2}[1 - \frac{sin^2(\alpha)}{\alpha^2} + \frac{sin^4(\alpha) + (\alpha - sin(\alpha)cos(\alpha))^2}{\alpha^2} \sum_{k=-\infty}^{\infty} \delta(f-k)] \quad (4.22)$$

This result is presented in [86] with an unfortunate typographical error (the term α^2 is missing in the first fraction). Conventional switching yields the discrete spectrum given in Fig. 4.13 which also shows the discrete spectrum for the random PWM. Random PWM yields discrete harmonics at even multiples of the switching frequency as well (for $D = 0.5$ conventional modulation has only odd harmonics). In this example, random PWM reduces the first harmonic more than random PPM, but at higher frequencies random PPM is more efficient in reducing the discrete harmonics. The continuous spectrum for random PWM is given in Fig. 4.14.

Another case of interest, which will be contrasted later with the example of modulation based on a Markov chain, is the example of equally probable pulses of lengths $\frac{1}{4}$ and $\frac{3}{4}$. In this case

$$E[|\ U(f,a)\ |^2] = \frac{1}{(2\pi f)^2}[2 - cos(\frac{2\pi f}{4}) - cos(\frac{6\pi f}{4})] \quad (4.23)$$

and

$$E[U(f,a)] = \frac{1}{2}[\frac{1 - e^{-i2\pi\frac{f}{4}}}{i2pif} + \frac{1 - e^{-i2\pi\frac{3f}{4}}}{i2pif}] \quad (4.24)$$

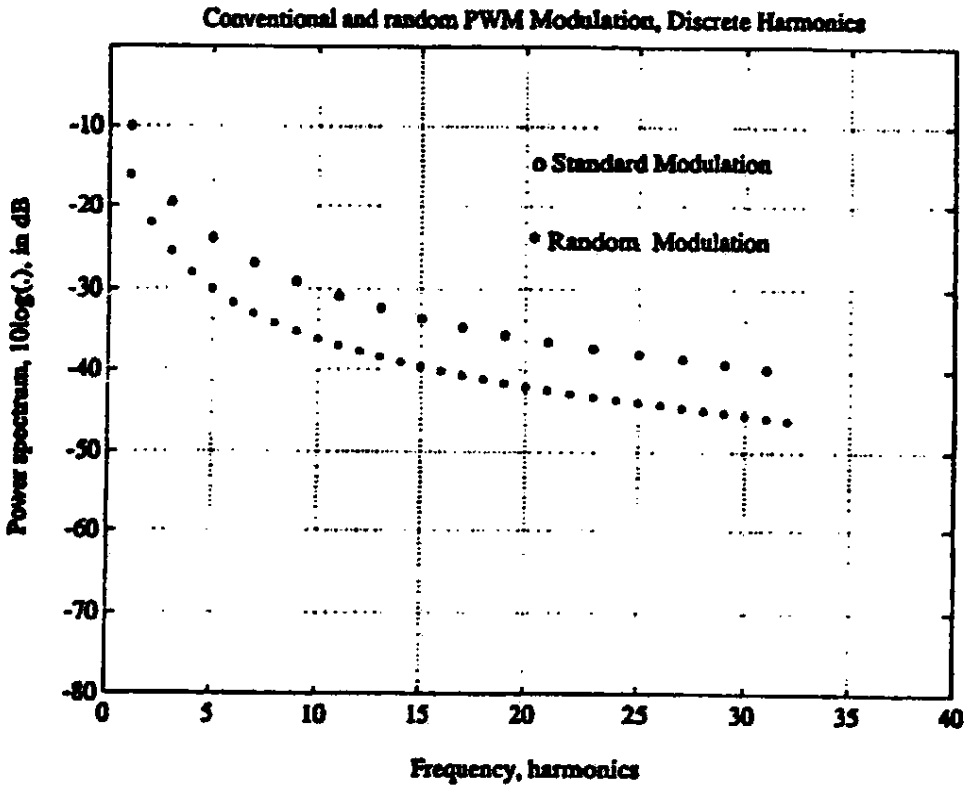


Figure 4.13: Discrete Spectrum - Comparison of Conventional and Random PWM Modulation, Period $T_0 = 1$, Duty Ratio $D = 0.5$, Pulse Width Uniformly $\in [0, T_0]$.

Then the formula A.1 yields the power spectrum shown in Fig. 4.15

These theoretical results can be compared with the experimental results for a down (buck) converter shown in Fig. 4.16. Good agreement can be observed. Experimental results presented in this thesis have been obtained by D.J. Perreault at MIT's Laboratory for Electromagnetic and Electronic Systems. A description of the experimental setup is presented in Appendix D, together with additional results. The switching frequency in this case is 10 kHz.

Next, we present experimental results for the inductor current of this down converter when the same random pulse width modulation with two possible pulse widths is employed. The standard configuration shown in Fig. 4.10 is different from the one used in the experiments, which is shown in Fig. 4.17. The main difference is the absence of the capacitor across load resistor in Fig. 4.17. Given the large size of the input capacitor in the experiment, the circuit in Fig. 4.17 can be approximated by a voltage source to the left of the switch. The first-order RL circuit to the right of the

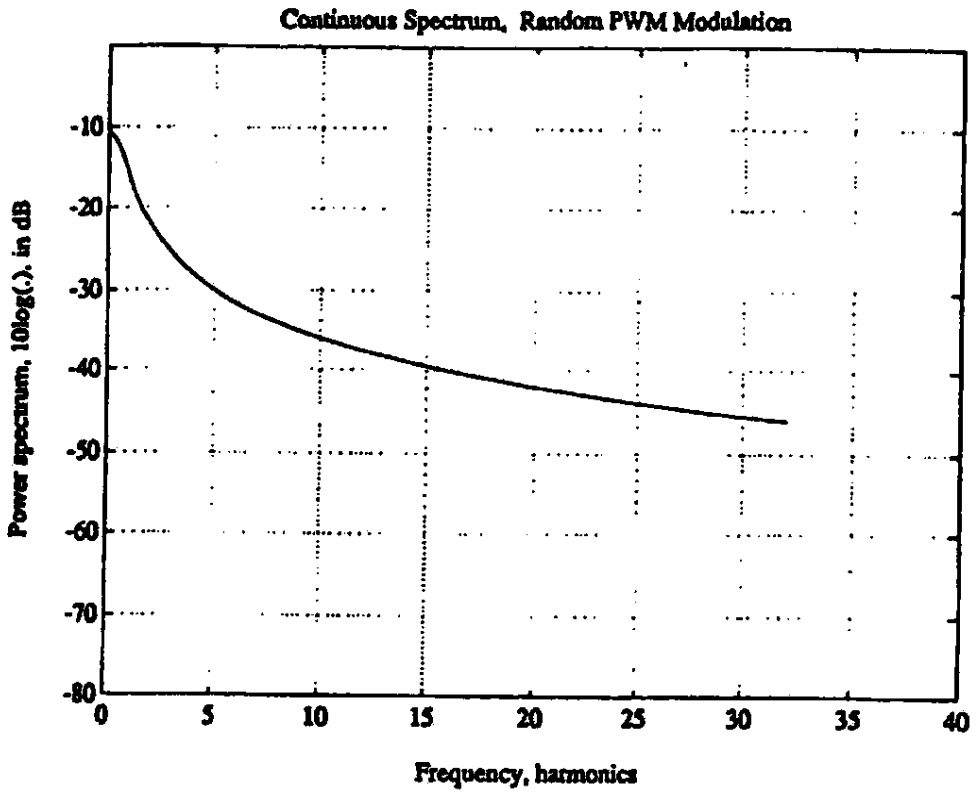


Figure 4.14: Continuous Spectrum - Random PWM, Period $T_0 = 1$, Duty Ratio $D = 0.5$, Pulse Width Uniformly $\in [0, T_0]$.

switch has time constant $L/R = 472\mu s$, and the nominal switching period is $100\mu s$ (given the nominal switching frequency of 10 kHz). Thus, the inductor current in the circuit in Fig. 4.17 can be approximated by straight line segments, in which case it is a scaled integral of the switching function $q(t)$, as in the case of a standard down converter.

The calculated continuous and discrete spectrum for the inductor current are shown in Fig. 4.18, and the experimentally observed spectrum is shown in Fig 4.19. The good agreement seen here between the theoretical predictions for power spectra of inductor currents and measured spectra is characteristic for other modulation schemes as well (e.g. for random modulation generated by a Markov chain). Calculation of the power spectrum of the *input* current of a down converter with random pulse width modulation is an interesting topic for further research, and preliminary results in that direction are outlined in Chapter 8.

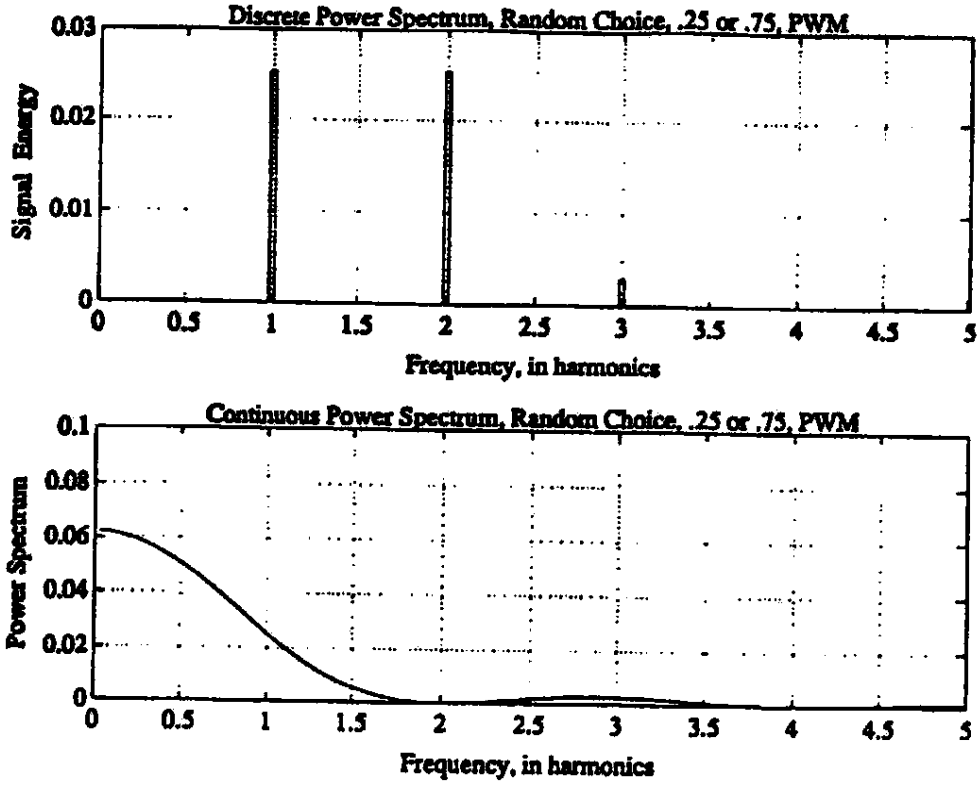


Figure 4.15: Random PWM – Calculated Discrete and Continuous Spectrum, Period $T_0 = 1$, Equally Probable Pulses of $\frac{1}{4}$ and $\frac{3}{4}$.

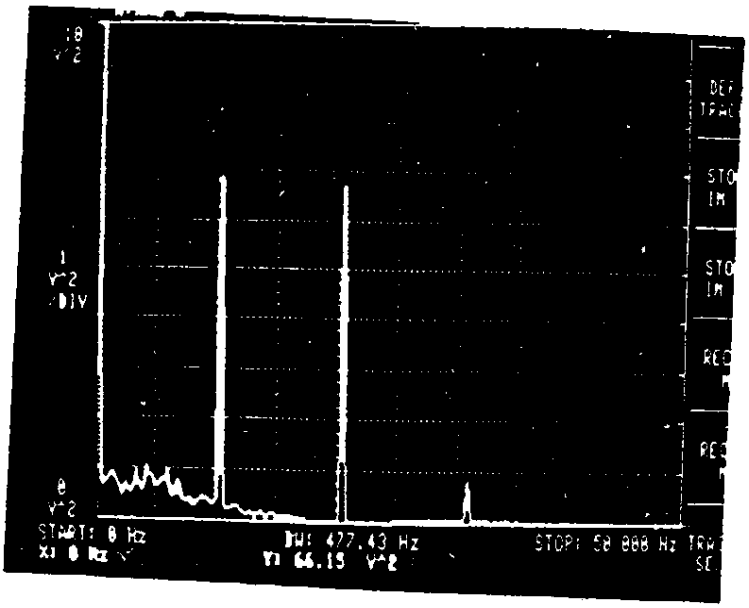


Figure 4.16: Random PWM - Measured Power Spectrum, Equally Probable Pulses of $\frac{1}{4}$ and $\frac{3}{4}$.

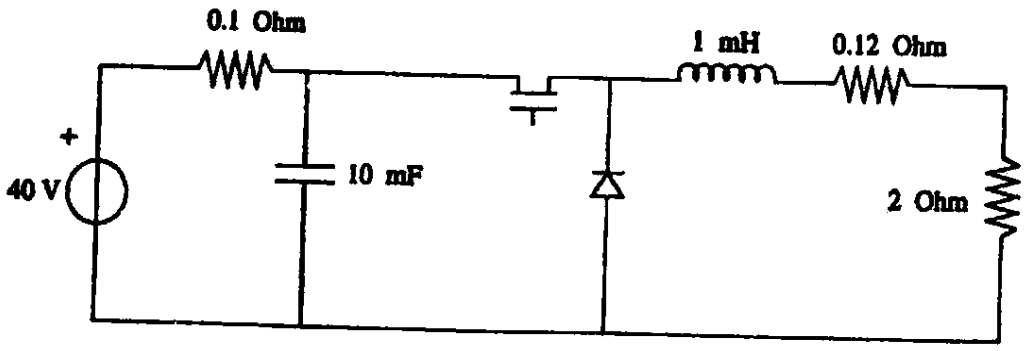


Figure 4.17: Down Converter Used in Verification of Power Spectral Formulas Stationary and Markov Chain Based Modulation.

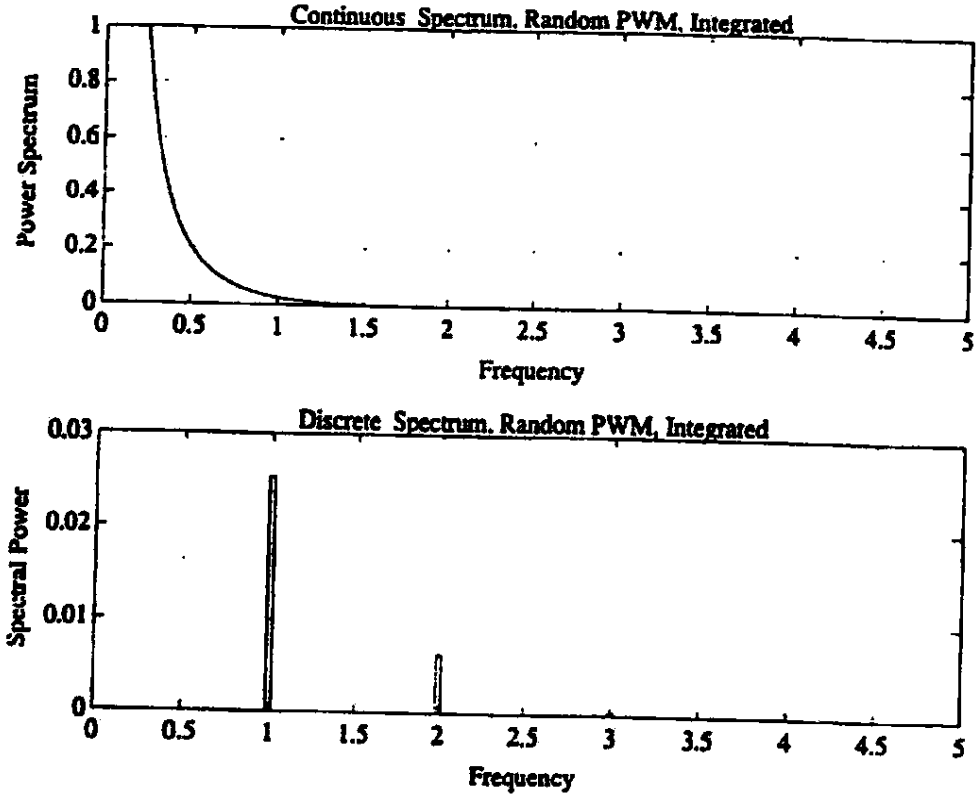


Figure 4.18: Calculated Inductor Current Spectrum, Independent Random Pulse Width Modulation

4.4.2 Random Aperiodic Modulation

In the case of random aperiodic modulation [116], the cycle length T_i is varied, while the duty ratio is fixed. Let $P(f)$ denote the Fourier transform of the probability density for T_i; then the power spectrum of the pulse train is purely continuous (see Appendix B, equation (B.13)):

$$S_v(f) = \frac{1}{(2\pi f)^2}[1 + 2Re(\frac{P(f)}{1-P(f)}) + 1 + 2Re(\frac{P^2(\frac{f}{2})}{1-P(f)}) - 2(2Re(\frac{P(\frac{f}{2})}{1-P(f)}))] \quad (4.25)$$

This result is believed to be novel. The calculated spectrum for $T_i \in [0.5\ 1.5]$, with a uniform probability density, and with $D = .5$, is shown in Fig. 4.20.

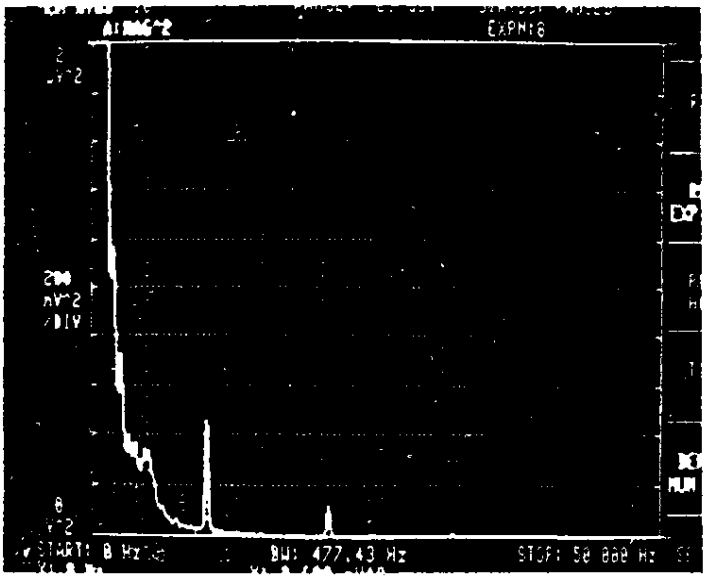


Figure 4.19: Measured Inductor Current Spectrum, Independent Random Pulse Width Modulation

4.4.3 Cascaded Random Modulation

Random PPM can be applied to an already aperiodically modulated pulse train. Assuming the PPM to be independent of the modulation of the period, with the PPM probability density having Fourier transform $P_c(f)$, the power spectrum is given by (see Appendix B, equation (B.20))

$$S_y(f) = |\frac{P_c(f)}{2\pi f}|^2 [2Re(\frac{P(f)}{1-P(f)}) + 2Re(\frac{P^2(\frac{f}{2})}{1-P(f)}) - 2Re(\frac{P(\frac{f}{2})}{1-P(f)}) - Re(\frac{P(f)P(\frac{f}{2})}{1-P(f)})] + (\frac{1}{2\pi f})^2[2 - 2Re(P(\frac{f}{2}))] \quad (4.26)$$

This random modulation idea and the result for the power spectrum are new. For the case of random PPM with uniform probability density added to the aperiodic modulation from the previous example. the difference between spectra is small, as discussed in Appendix B.

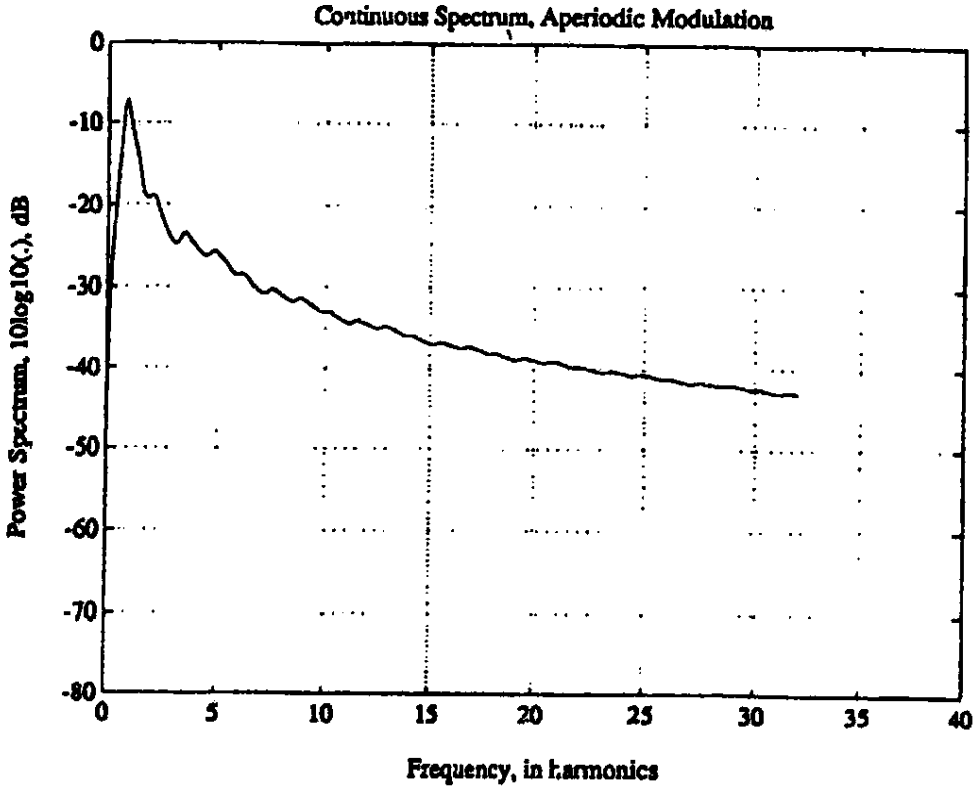


Figure 4.20: Continuous Spectrum - Aperiodic Modulation $T_i \in [0.5\ 1.5]$, Uniform, $D = .5$

4.4.4 Alternate Random Modulation

In one example of *alternate* random modulation, the pulse train consists of pairs of pulses, with a a PPM pulse in a cycle of length T_0 and pulse delay ε, is followed by an aperiodically modulated pulse of duration τ. Let U_1 and U_2 denote the Fourier transforms of the pulses in the first and the second cycle, respectively (defined with the time origin being the beginning of the pulse in each case.). Let P_σ denote the Fourier transform of the probability density function for $\sigma = T_0 + \tau$. Then the power spectrum of the pulse train equals (see Appendix C):

$$S_y(f) = 2Re\left(\frac{E[U_1 e^{-i2\pi f\varepsilon}]^* E[U_2 e^{i2\pi f\tau}]}{1 - P_\sigma}\right) + 2Re\left(\frac{E[U_1 e^{-i2\pi f\varepsilon}] E[U_2 e^{i2\pi f\tau}]^*}{1 - P_\sigma^*}\right) \quad (4.27)$$

This result is believed to be new.

Verification results for the formula (4.27) are given in Fig. 4.21, for the stan-

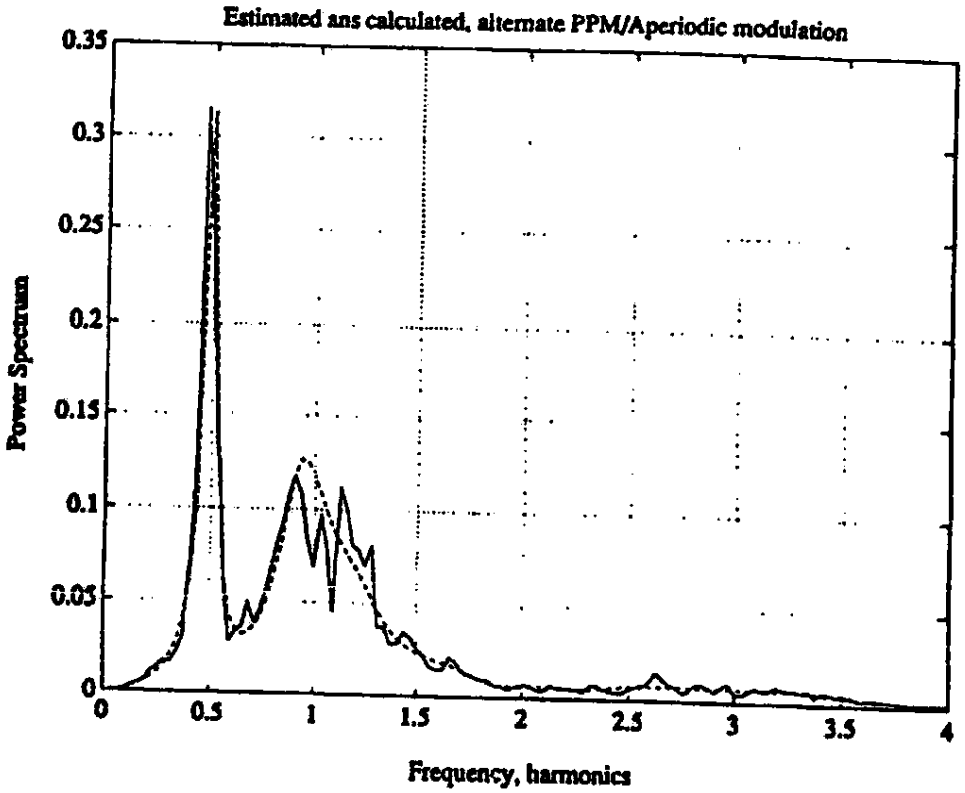


Figure 4.21: Simulated and Calculated Spectrum, Alternate Modulation, Random PPM and Aperiodic Modulation; PPM Uniform $\varepsilon \in [0,\ 0.5]$, Duty Ratio $D = 0.5$; Aperiodic Modulation $\tau \in [0.5\ 1.5]$, Duty Ratio $D = 0.5$.

dard example (PPM dither $\in [0 \quad .5T_0]$, aperiodic modulation with pulse lengths $\in [.5T_0, \quad 1.5T_0]$, duty ratio .5). The resulting power spectrum is continuous, and it has significant power at half the switching frequency, which approximately corresponds to cycles of length two (i.e., one PPM cycle of unit length, and one aperiodic cycle with average length one).

4.4.5 Random Choice of Random Modulation

An example of a random choice of random modulation is considered next. At each cycle, a random choice between random PPM and aperiodic modulation is made. with probabilities p and $q = 1 - p$, respectively. After a choice of modulation is made, another independent experiment is performed to get a value for the associated random parameter (pulse position, or cycle length). Other random modulation schemes can be combined using the same approach. The resulting formula for the power spectrum

in the random PPM — random aperiodic modulation case is (C.3) in Appendix C:

$$S_y(f) = E[|\, U(f,\tau,\varepsilon)e^{i2\pi f(\tau-\epsilon)}\,|^2] + 2Re\left(\frac{E[U(f,\tau,\varepsilon)e^{i2\pi f(\tau-\epsilon)}]E[U(f,\tau,\varepsilon)e^{i2\pi f\epsilon}]^*}{1-P_\tau^*}\right) \tag{4.28}$$

where

$$U_1 = \frac{1-e^{-i2\pi f\frac{T_0}{2}}}{2\pi f} \tag{4.29}$$

$$U_2 = \frac{1-e^{-i2\pi f\frac{\tau}{2}}}{2\pi f} \tag{4.30}$$

$$E[|\, U(f,\tau,\varepsilon)e^{i2\pi f(\tau-\epsilon)}\,|^2] = pE_\varepsilon[|\, U_1\,|^2] + qE_\tau[|\, U_2\,|^2] \tag{4.31}$$

This result is believed to be new. Let

$$P_\tau = E[e^{-i2\pi f\tau}] \tag{4.32}$$

$$P_\epsilon = E[e^{-i2\pi f\epsilon}] \tag{4.33}$$

then

$$E[U(f,\tau,\varepsilon)e^{i2\pi f(\tau-\epsilon)}] = pU_1e^{i2\pi fT_0}P_\epsilon(f) + q\frac{P_\tau^*(f)-P_\tau^*(\frac{f}{2})}{2i\pi f} \tag{4.34}$$

$$E[U(f,\tau,\varepsilon)e^{i2\pi f\epsilon}] = pU_1^*P_\epsilon^*(f) + qE[U_2] \tag{4.35}$$

Verification results for this random choice of random modulation are given in Fig. 4.22, for the standard example of random PPM and random aperiodic modulation, and with $p = q = 0.5$.

4.5 Summary

Power spectra of basic stationary random modulation schemes are described in this chapter. The main assumptions are that the reference deterministic pattern does not change from one cycle to the next and that the dithering is based on independent trials.

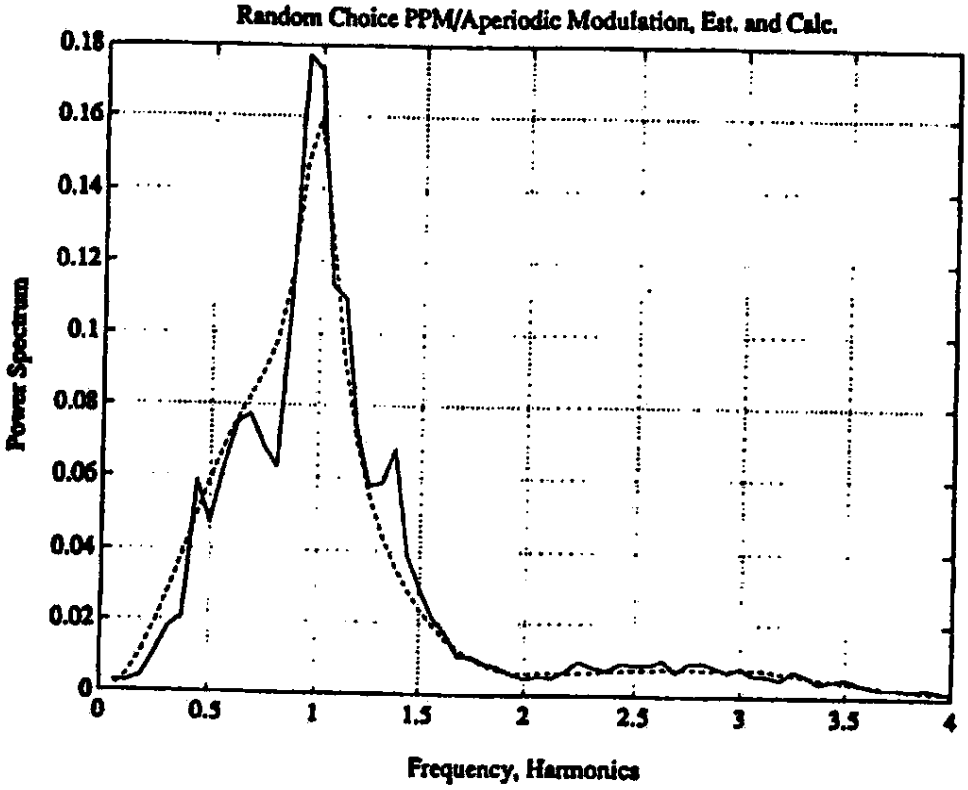


Figure 4.22: Simulated and Calculated Spectrum, Random Choice of Random Modulation, Equally Probable Choice Between PPM and Aperiodic Modulation; PPM Uniform $\varepsilon \in [0,\ 0.5]$, Duty Ratio $D = 0.5$; Aperiodic Modulation $\tau \in [0.5\ 1.5]$, Duty Ratio $D = 0.5$.

Random pulse position modulation is considered in detail and a verification procedure based on Monte–Carlo simulations is presented. Results are given for random pulse width modulation, which is analyzed in more detail in Appendix A. The spectral formula for aperiodic modulation, which has been practically implemented [116], is believed to be novel. It is derived in Appendix B, using two different analysis methods. The effects of adding an additional random PPM modulation are studied in the same appendix.

Two new stationary random modulation frameworks analyzed in Appendix C are alternate modulation and random choice of random modulation. In alternate modulation, two different modulation schemes are applied in succession, for example PPM and aperiodic modulation. In the random choice modulation, for each cycle a random decision is made as to which scheme to apply in the current cycle. A second stochastic experiment is then performed to obtain the appropriate random parameter for the chosen modulation scheme.

In the next chapter, the assumption of invariant deterministic structure of the modulation is removed. In block-stationary (inverter) modulation, the reference pulse train changes in a deterministic fashion. This class of modulation schemes, used in numerous implementations for acoustic noise reduction, is the subject of Chapter 5.

Chapter 5

Block–Stationary Random Modulation

A generalization of the class of stationary random modulation schemes is considered in this chapter. The nominal (reference) on–off pattern is assumed to change from one cycle to the next in a deterministic fashion, but the pattern repeats periodically over a *block* of cycles. This pattern is then dithered in each cycle using a set of mutually independent trials with constant statistical structure. Most of the results presented here are either novel, or represent generalizations of previously available results. Their derivation follows the one presented in the previous chapter, but requires additional algebraic manipulations.

Deterministic optimization of the harmonic content in DC/AC conversion is a significant task in power electronics. Its importance has been recognized very early [122], and it has since received much attention [96], [97], [30]. More recent developments related to "space–vector" modulation are described in [123], [13], [55].

Random modulation is a complementary method for spectral shaping. It is very efficient in reducing discrete (or narrow–band) spectral components, as shown in Chapter 4. On the other hand, signal power minimization over wide bands, e.g. over frequency segments that are multiples of the switching frequency, is not easily achievable by random modulation, as shown in Chapter 7. Deterministic modulation methods typically generate periodic switching functions, thus yielding well de-

fined harmonic spectra. Deterministic harmonic reduction can be effective over wide bands, but often leads to demanding optimization problems, [96], [97], [12], [4]. In applications that require extensive spectral shaping, it may be advantageous to combine both methods. An implementation that combines optimized deterministic and random modulation, with very encouraging results, is described in [126].

Power spectra for line–to–line and line–to–neutral variables in a three phase system can be found easily, once the spectrum $S_y(f)$ corresponding to one phase is known. Waveforms in the second and third phase are assumed to be time–delayed copies of the waveforms in the first phase. The delay is $\frac{T_s}{3}$ per phase, where T_s is the period of the AC waveform. Thus, the line–to–line spectrum in a Y connected system is the spectrum of the waveform $y_{ll}(t) = y(t) - y(t - \frac{T_s}{3})$. The line–to–line power spectrum can be calculated from the definition of the autocorrelation $R_{ll}(\tau) = E[y_{ll}(t)\ y_{ll}(t + \tau)]$, using wide–sense stationarity of y. The result is given by

$$S_{ll}(f) = 2[1 - cos(\frac{2\pi f T_s}{3})]S_y(f) \tag{5.1}$$

Similarly, the line–to–neutral spectrum in a Δ connected system corresponds to the waveform $y_{ln}(t) = \frac{2}{3}(2y(t) - y(t + \frac{T_s}{3}))$, and equals

$$S_{ln}(f) = \frac{4}{81}[6 - 4cos(\frac{2\pi f T_s}{3})]S_y(f) \tag{5.2}$$

5.1 Block–Stationary Random PPM

As a motivational example, consider a PPM train consisting of alternating cycles with pulses of widths D_1T_0 and D_2T_0. This is illustrated in Fig. 5.1. Let $U_i(f)$ denote the Fourier transform of $u_i(t)$, where each u_i is defined with respect to a time origin that coincides with the beginning of the corresponding cycle. Then the same derivation (for random PPM) as in the previous chapter is applicable. The only difference is that four terms $U_i U_j^*$ are encountered instead of the single term $|U|^2$, as in (4.12). After some straightforward algebra, the following formula is obtained:

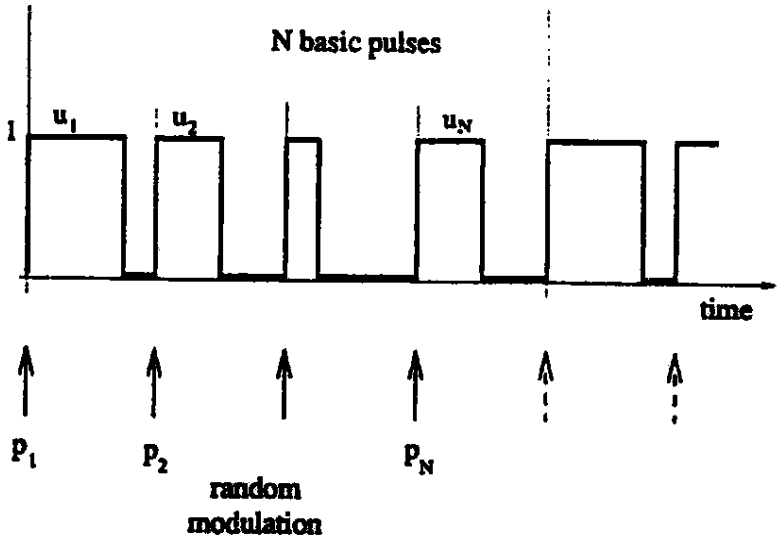


Figure 5.1: Block-Stationary Random Modulation.

$$
\begin{aligned}
S_y(f) \;=\; & \frac{|\,U_1(f)\,|^2 + |\,U_2(f)\,|^2}{2T_0}[1 - |\,P_e(f)\,|^2 + \\
& + \frac{|\,P_e(f)\,|^2}{2T_0} \sum_{k=-\infty}^{\infty} \delta(f - \frac{k}{2T_0})] \\
& + \frac{U_1(f)U_2^*(f) + U_1^*(f)U_2(f)}{2T_0} \\
& [|\,P_e(f)\,|^2\, e^{i2\pi f T_0} \frac{1}{2T_0} \sum_{k=-\infty}^{\infty} \delta(f - \frac{k}{2T_0})]
\end{aligned}
\tag{5.3}
$$

For $u_1(\cdot) = u_2(\cdot)$, this formula reduces to the PPM case presented before. Observe that in the second impulse train the term $e^{i2\pi f T_0}$ for $f = \frac{k}{2T_0}$ becomes $e^{i\pi k} = (-1)^k$. The coefficient multiplying the second term equals $Re(U_1 U_2^*)$.

The equation (5.3) is now verified, before presenting its generalization. Consider the case of PPM, with uniform dither between 0 and $\frac{T_0}{4} = \frac{1}{4}$. The basic pulses have $D_1 = \frac{1}{4}$ and $D_2 = \frac{3}{4}$ and the calculated spectrum is given in Fig. 5.2, using (5.3).

The spectrum is estimated using a waveform of 128 pulses with 64 points each. The estimated spectrum, together with the calculated continuous component of the spectrum (i.e., the top figure of Fig. 5.2), are shown in Fig. 5.3. The large deviations between the estimated and calculated continuous spectrum at frequencies that are

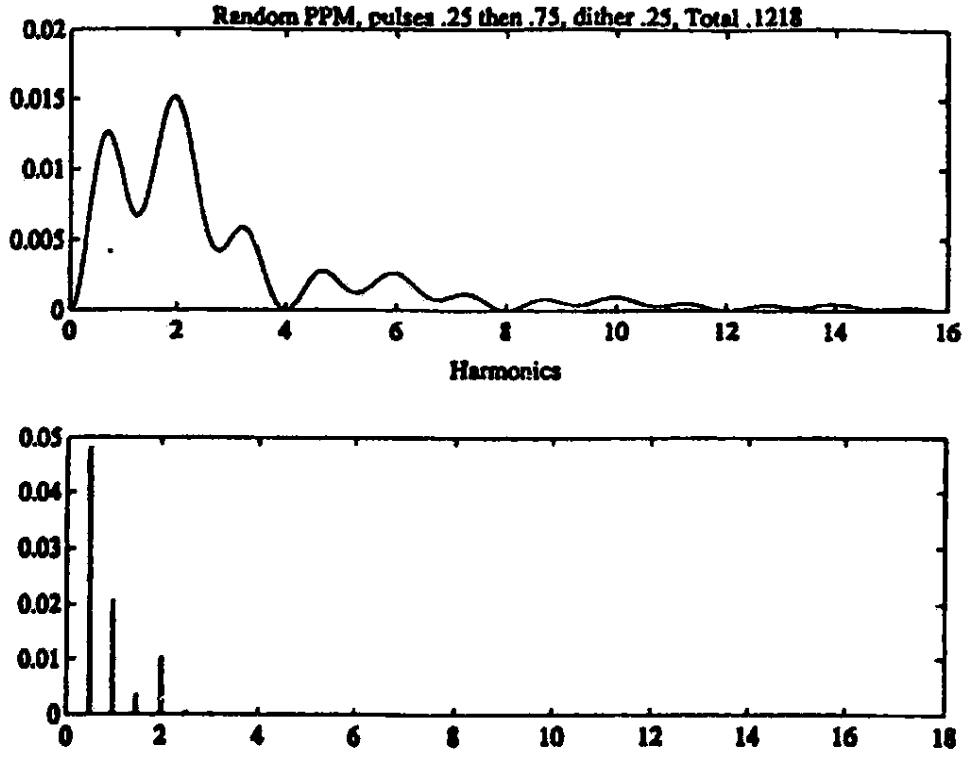


Figure 5.2: Calculated Spectrum for Block-Stationary Random Modulation Example.

multiples of 1/2 are due to discrete spectral components, because Welch's procedure generates the estimate of the total power spectrum, i.e., of the sum of continuous and discrete spectra. In Fig. 5.4 part of the estimate is presented, showing the first twenty harmonics of the estimate, and verifying the discrete spectrum shown in the lower part of Fig 5.2.

The results shown in Fig. 5.4 are in close agreement with the experimental results for the same case, which are shown in Fig 5.5. As noted in Chapter 4, experimental results presented in this thesis have been obtained by D.J. Perreault at MIT's Laboratory for Electromagnetic and Electronic Systems. A description of the experimental setup is presented in Appendix D, together with additional results. The switching frequency in this example is 250 Hz, and the discrepancies between theoretical and experimental results for discrete harmonics are under 5%. The reference case of deterministic switching with alternate duty ratios $\frac{1}{4}$ and $\frac{3}{4}$ is shown in Figs. 5.6 and 5.7. The vertical scale in the measurements depends on details of the experimental setup, so the *relative* heights of components are what should be compared. This ex-

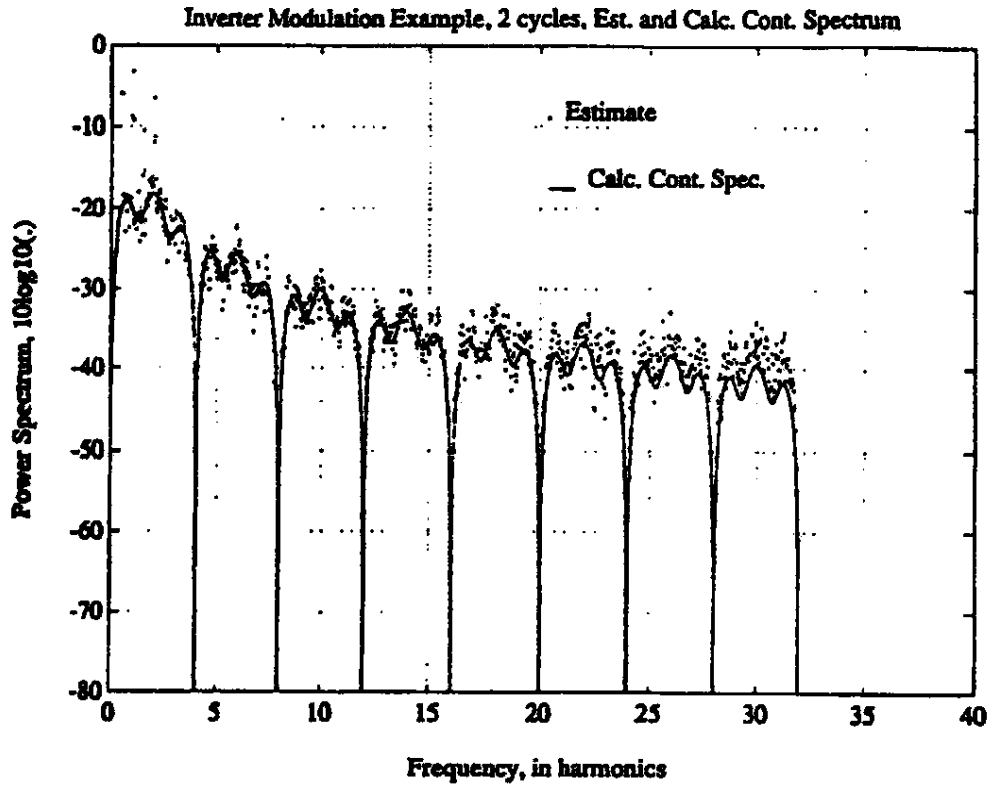


Figure 5.3: Estimated and Calculated Continuous Spectrum for Block-Stationary Random Modulation Example, Total Number of Points M=2048, Overlap M/2.

ample is constructed for the purpose of validation of theoretical results, and it does not illustrate the ultimate capabilities of random modulation in discrete harmonic reduction.

The formula (5.3) can be generalized to the case of N basic duty ratios in a block of states, with possibly different cycle lengths T_i, and possibly different probability densities (with characteristic functions P_i). Let $U_i(f)$ again denote the Fourier transform of the pulse $u_i(t)$ in the i–th cycle of the block (defined with respect to a time origin at the start of the corresponding cycle), and let

$$U(f) = \begin{bmatrix} U_1(f) \\ U_2(f)e^{-i2\pi f T_1} \\ \vdots \\ U_N(f)e^{-i2\pi f \sum_{l=1}^{N-1} T_l} \end{bmatrix}$$

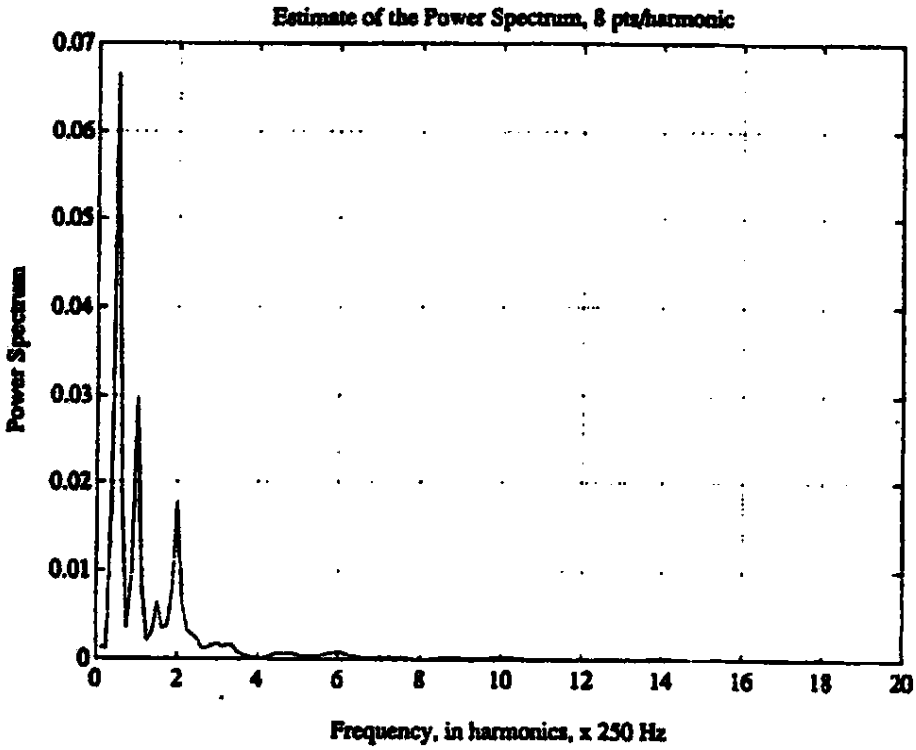


Figure 5.4: Estimated Spectrum for Block-Stationary Random Modulation Example, First 20 Harmonics.

and

$$\hat{U}(f) = \begin{bmatrix} U_1(f)P_1(f) \\ U_2(f)P_2(f)e^{-i2\pi f T_1} \\ \vdots \\ U_N(f)P_N(f)e^{-i2\pi f \sum_{l=1}^{N-1} T_l} \end{bmatrix}$$

Let $\mathbf{1}$ denote an $N \times 1$ vector of ones, and let $\sum_1^N T_i = \bar{T}$. The formula (5.3) can be generalized to N pulses by induction, and the resulting expression can be written with the previously introduced notation:

$$\begin{aligned} S(f) &= \frac{1}{\bar{T}}(\|U\|^2 - \|\hat{U}\|^2) + \\ &\quad \frac{1}{\bar{T}^2}\mathbf{1}^T\hat{U}\hat{U}^H\mathbf{1}\sum_{k=-\infty}^{\infty}\delta(f - \frac{k}{\bar{T}}) \end{aligned} \qquad (5.4)$$

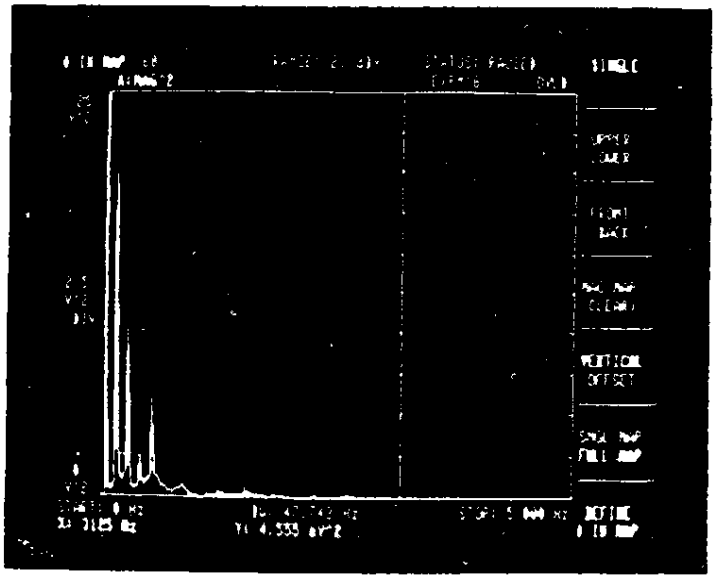


Figure 5.5: Measured Power Spectrum in Block-Stationary Random Modulation Example.

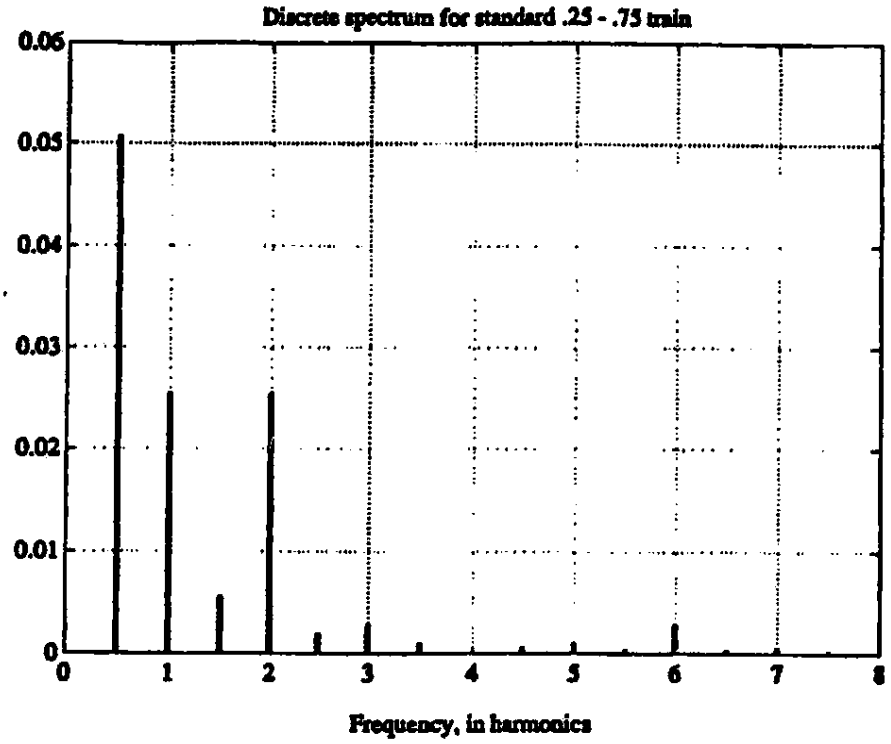


Figure 5.6: Calculated Power Spectrum in Deterministic Modulation Example.

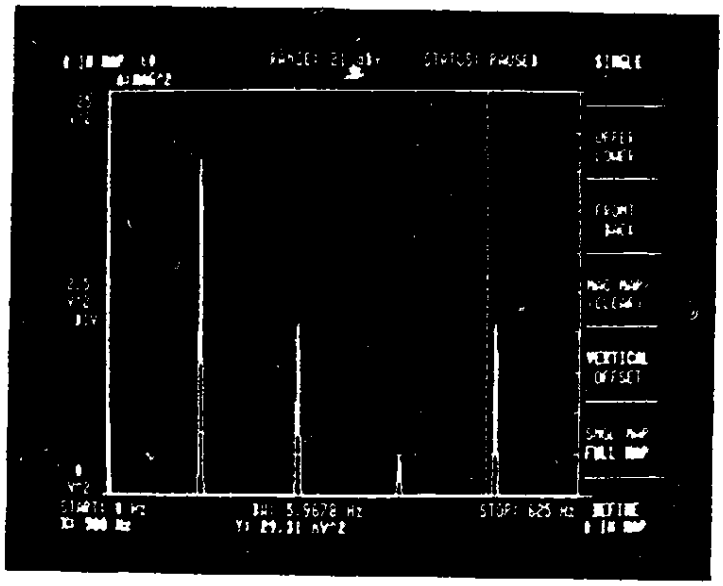


Figure 5.7: Measured Power Spectrum in Deterministic Modulation Example.

where $\|U\|^2$ is the sum of magnitudes squared of the elements of vector U (i.e., the standard 2-norm), and U^H is the complex conjugate transpose (Hermitian) of U.

A special case of (5.4) is the setup considered in [64] and [65], in which $N = 120$, $T_i = T$. D_i follows a trapezoidal shape between .25 and .75, as shown in Fig. 5.8. Given a pulse length D_i at cycle i, the following dual-position probability density function is used:

$$p_i(t) = \frac{1}{2}(\delta(0) + \delta(t - (1 - D_i)T)) \tag{5.5}$$

It implies that the "on" part of a cycle either begins the period T, or ends it. In other words, each cycle has a single "on" and a single "off" part, and they are equally likely to be generated in either order.

Numerical results obtained by applying the formula (5.4)to this case are shown in Figs. 5.9 and 5.10, and exactly match the results in [65]. The formulas in [64] and [65] were obtained by starting from a result on PPM from communication theory [111], and performing a sequence of algebraic manipulations. Formulas (13) and (14)

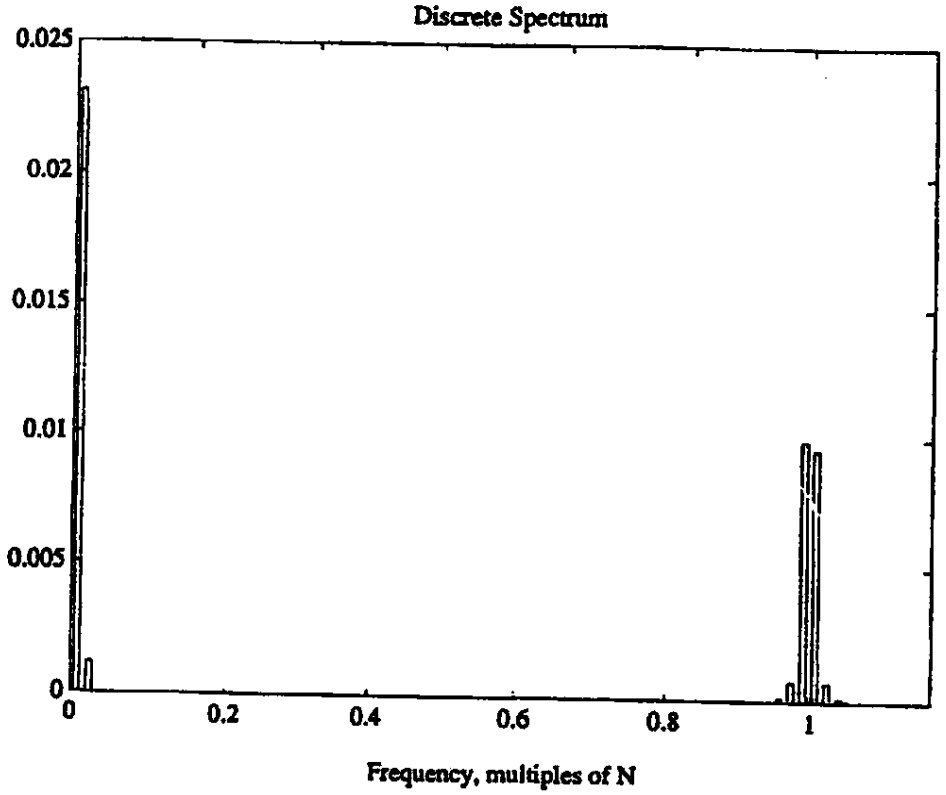


Figure 5.9: Discrete Spectrum for the Block–Stationary Random Modulation Example.

5.2 Block–Stationary Random Aperiodic Modulation

An aperiodic random modulation scheme for the block–stationary case is presented in this section. It is motivated by the implementation described in [48].

Consider a pulse train that is obtained by convolving the *impulse* train shown in Fig. 5.12 with a step function. During each cycle of the pulse train, two random experiments are performed, and two pulse durations T_i', T_i'' are obtained. The switch is kept off for $(1 - D_i)\ T_i'$, then on for $D_i(T_i' + T_i'')$, and then again off for $(1 - D_i)\ T_i''$. This scheme approximates the case of sinusoidal PWM with a triangle carrier whose slopes are randomly modulated [48]. It is an approximation, since the duty ratio in sinusoidal PWM changes between the first and second segment of a cycle, but the change is small if the total number of cycles N within the output (AC) period is large.

Let the Fourier transform of the probability density function for T_i be denoted

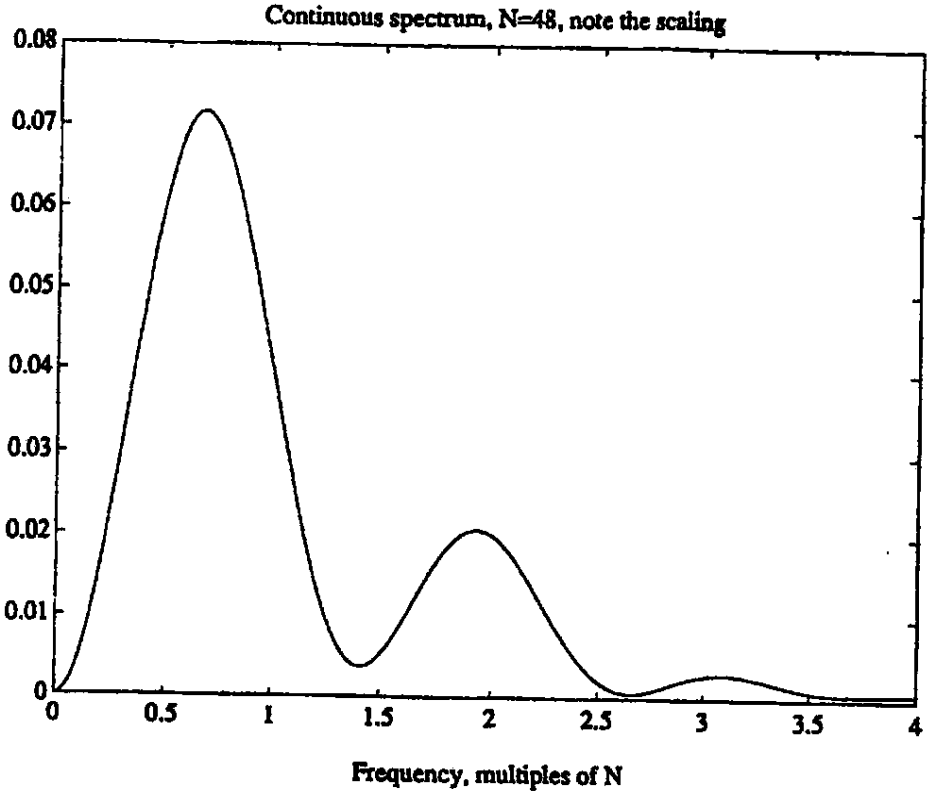


Figure 5.10: Continuous Spectrum for the Block-Stationary Random Modulation Example.

by $P(f)$. The resulting switching waveform $q(t)$ will be obtained as an integral of the sum of $2N$ impulse trains. The standard approach from Chapter 4 is used again, but now there are $2N$ impulse trains to be considered. The autocorrelation of $q(t)$ will thus be a sum of $(2N)^2$ terms, each representing a crosscorrelation between two impulse trains.

Let $\tilde{S}$ be a matrix of spectral components, constructed as follows. The (k,l)–th entry of $\tilde{S}$ is the Fourier transform of the crosscorrelation between the k–th and l–th impulse train. In this calculation [77], it is convenient to pick an impulse in the k–th impulse train, and to consider the elapsed time to all impulses in the l-th impulse train. In matrix $\tilde{S}$, the first row (and column) correspond to contributions to the autocorrelation due to the + impulse train of the first cycle, second row (and column) to the – impulse train of the first cycle and so on. In the calculation that follows, it is important to notice which time segments are statistically independent, since the characteristic function (i.e., the Fourier transform of the probability density)

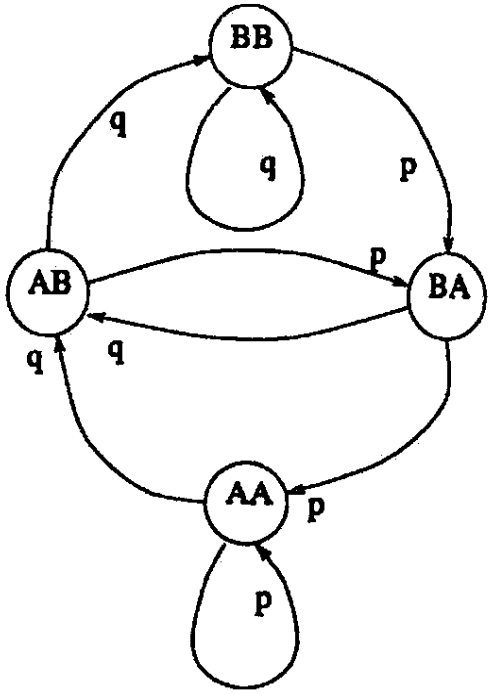


Figure 5.11: Markov Chain Model for the Switching Frequency Reduction in Dual Position Modulation for Block-Stationary Random Modulation.

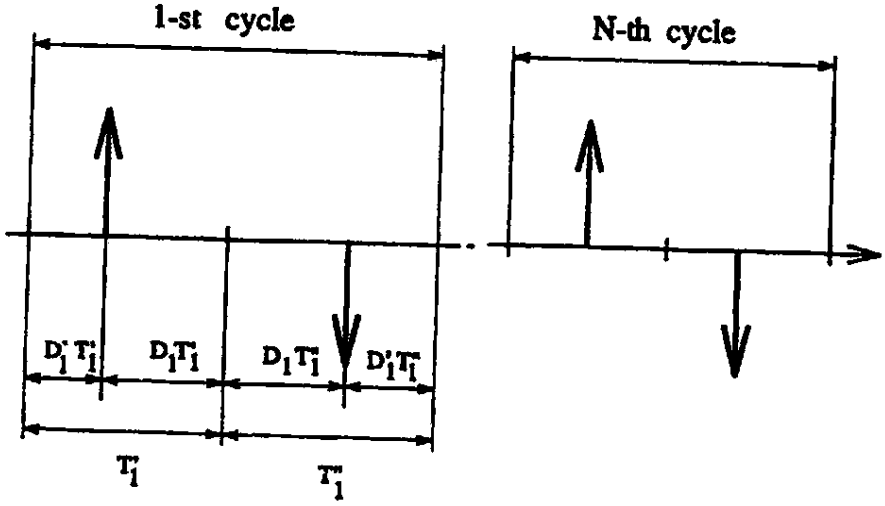


Figure 5.12: Impulse Train Used in Aperiodic Modulation for Block-Stationary Random Modulation.

for their sum will be the product of the characteristic functions of the individual components. Using the basic result of [77] on the power spectrum of an impulse train with independent increments, and the derivation shown in more detail in Appendix B, we get

$$\tilde{S}_{11} = 1 + 2Re(\frac{P(D_1 f)P^3(f)P((1-D_1)f)}{1-P^4(f)})$$

In this expression, $P(D_1 f)$ is the characteristic function for a segment to the right of a + impulse in the first cycle, while $P^3(f)$ is the characteristic function for three independent segments of length T_i (one in the first and two in the second cycle). Similarly, $P((1-D_1)f)$ is the characteristic function for a segment to the left of a + impulse in the first cycle in the next group of N pulses. In the denominator, the term $1-P^4(f)$ is a consequence of the summation of a geometric series, with $P^4(f)$ being the characteristic function of a sum of $2N = 4$ independent segments of length T_i each. To get $\tilde{S}_{1,2}$, we consider the crosscorrelation corresponding to the impulse trains that include the positive and the negative impulse in the first cycle. By an analogous argument, the result is

$$\tilde{S}_{12} = -2Re(\frac{P(D_1 f)P((1-D_1)f)}{1-P^4(f)})$$

To explain this result, let us pick a fixed group of N cycles. The coefficient 2 arises from the equality of contributions to the crosscorrelation of all negative impulses to the right of the positive impulse in the first cycle of the chosen group, and of all positive impulses to the left of the negative impulse in the first cycle of the chosen group. The same reasoning yields

$$\tilde{S}_{21} = -2Re(\frac{P((1-D_1)f)P^2(f)P(D_1 f)}{1-P^4(f)})$$

The remaining entries of the matrix $\tilde{S}$ can be calculated in the same manner, and the resulting spectrum is

$$S_y(f) = \frac{1}{2(2\pi f)^2}\sum_{k=1}^{4}\sum_{l=1}^{4}\tilde{S}_{k,l}$$

The same result can be extended to the case of N pulses. and the result is:

$$S_y(f) = \frac{1}{N}\frac{1}{(2\pi f)^2}\mathbf{1}_{2N}^T \tilde{S} \mathbf{1}_{2N} \tag{5.6}$$

where $\mathbf{1}_{2N}$ is a $2N$ vector of ones. $\tilde{S}$ is a $2N \times 2N$ matrix whose entry in the k-th row and k-th column, denoted by $\tilde{S}_{kk}$ equals:

$$\tilde{S}_{kk}(f) = 1 + 2Re\{\frac{P(D_k f)P((1-D_k)f)P^{2N-1}(f)}{1-P^{2N}(f)}\} \tag{5.7}$$

while the entry in the k-th row and l-th column is:

$$\tilde{S}_{kl}(f) = (-1)^{k-l}2Re\{\frac{P(D_{ak}f)P(D_{bl}f)P^{a}(f)}{1-P^{2N}(f)}\} \tag{5.8}$$

where

$$D_{ak} = \begin{cases} D_k & k \text{ odd} \\ 1-D_k & k \text{ even} \end{cases} \tag{5.9}$$

and

$$D_{bl} = \begin{cases} 1-D_l & l \text{ odd} \\ D_l & l \text{ even} \end{cases} \tag{5.10}$$

and

$$a = \begin{cases} l-k-1 & k < l \\ 2N-1-(k-l) & k > l \end{cases} \tag{5.11}$$

We can observe that entries on the same subdiagonal have numerators involving the same powers of $P(f)$, so the matrix $\tilde{S}$ has a Toeplitz structure.

It is assumed that $P(f) \neq 1$ for $f > 0$, which is true for all probability densities of practical interest, as discussed in Appendix B. The case when $P(f) = 1$ can be treated as a special case of results presented in the following chapter.

If $P(f)$ is the characteristic function of a dual-position probability density, with $T_i \in [0.75, 1.25]$, then the three-phase line-to-line spectrum (assuming the Y connection) shown in Fig. 5.13 is obtained. This can be compared with Fig. 9 in [48], and qualitative similarities can be observed. The unit frequency in Fig. 5.13 corresponds

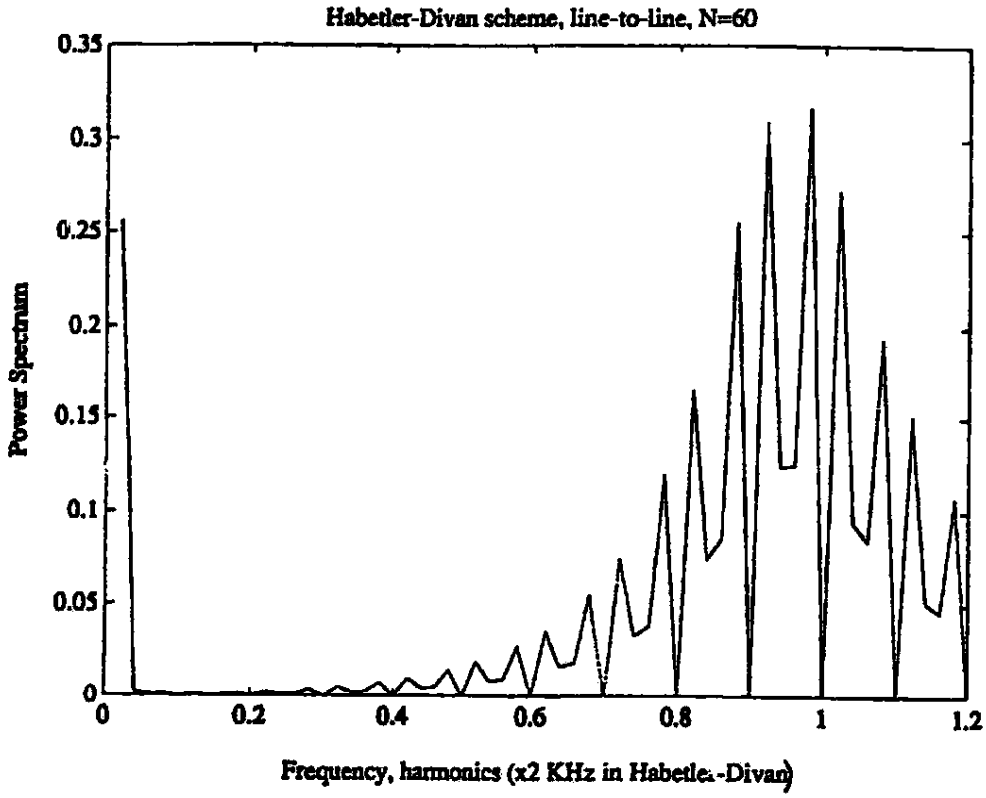


Figure 5.13: Line–to–line Spectrum. Aperiodic Block–Stationary Random Modulation, $T_i \in [0.75, 1.25]$, Dual Position Probability Density Function.

to the $2kHz$ point in [48].

In the case of a uniform probability density, the spectrum shown in Fig. 5.14 is obtained. The unit frequency in Fig. 5.14 corresponds to the $2kHz$ point in [48].

5.3 Summary

Random modulation for block–stationary (inverter, DC/AC) operation is described in this chapter. Novel formulas for both periodic (PPM) and aperiodic modulation have been derived, and verified on examples.

The general formula (5.4) for PPM modulation specializes correctly to results reported in [64]. The expression for the spectrum in aperiodic modulation (5.6) provides a new analytical way to explain results reported in [48].

The approach described in this chapter could perhaps be used for analysis of deterministic modulation schemes that are characterized by complicated behavior,

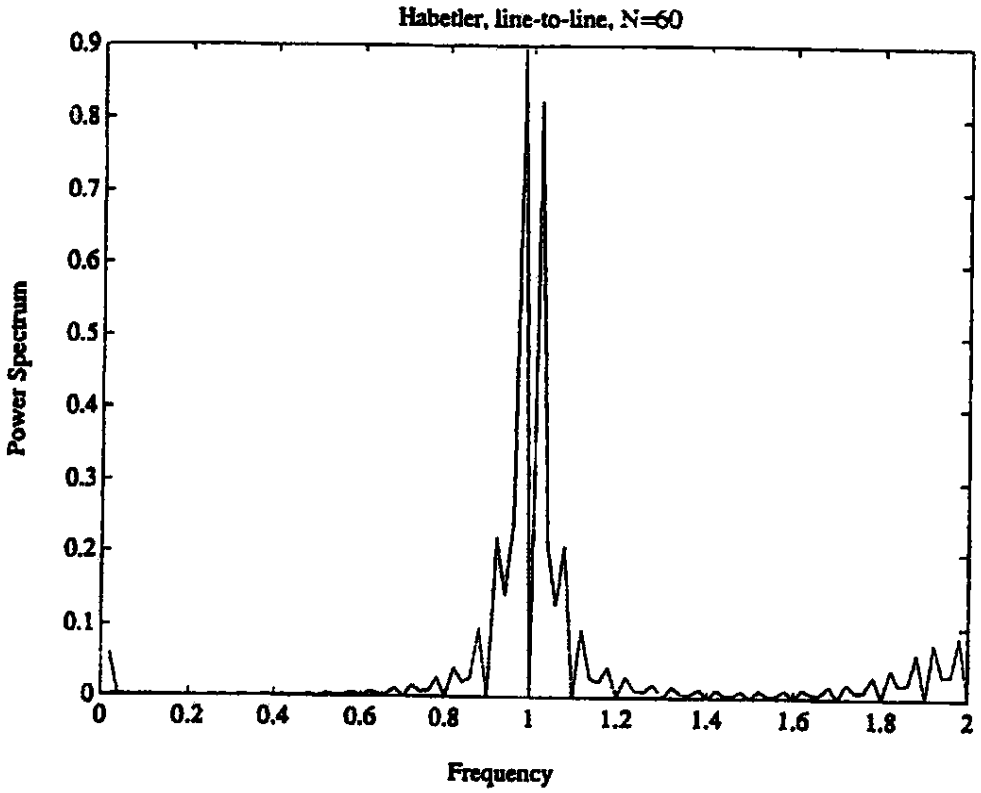


Figure 5.14: Line–to–line Spectrum, Aperiodic Block–Stationary Random Modulation, $T_i \in [0.75, 1.25]$, Uniform Probability Density Function.

e.g. in $\Sigma - \Delta$ modulation [45]. This direction is a promising course for future research.

Chapter 6

Switching Governed by Markov Chains

In this chapter another generalization of the class of stationary random modulation schemes is considered, in which the switching signal $q(t)$ comprises a sequence of waveform segments, each of length T_i, governed by Markovian probabilistic laws.

Switching based on a Markov chain possesses additional generality when compared to the randomized switching strategies described earlier. A waveform segment of length T_i is associated with the Markov chain being in the i-th state. Since a switching pattern in one cycle can be made dependent on the state of the underlying Markov chain, an additional degree of flexibility is available. State transition probabilities can be chosen so that large deviations from desired average steady-state behavior are discouraged or prevented altogether. For instance, a short duty ratio can be made very likely after a long one in randomized PWM. Similarly, in PPM, a short delay ϵ_i can be discouraged after a long ϵ_{i-1}, to prevent a large "local" on-time and thereby reduce the current ripple. Electronic circuits that implement switching based on a Markov chain are not necessarily more complicated than circuits employed in stationary modulation, as demonstrated by the realizations described in this chapter and in Appendix D.

The Markov chains analyzed in this thesis are discrete–time chains with finitely many states (say n), and a continuous–time 0–1 waveform is associated with the

evolution of the chain. Let $\Pi(k)$ be $1 \times n$ row vector whose i-th entry $\Pi_i(k)$ is the probability that at the k-th stage the system is in state i. Then the evolution of Π is governed by the equation [67]

$$\Pi(k+1) = \Pi(k)\bar{P} \tag{6.1}$$

$\bar{P}$ is the $n \times n$ state-transition matrix, and its (i,j)-th element is the probability that at the next transition the chain goes to state j, given that it is currently in state i. Although $\bar{P}$ can also depend on k, we shall only consider the case of time-invariant (or homogeneous) chains, where $\bar{P}$ is constant. In each state of the chain, a cycle of the switching waveform is generated. The lengths of the cycles can be equal for all states, in which case the chain is called *synchronous* (i.e., T_i equal for all i). Otherwise, the Markov chain is denoted as *asynchronous*.

The field of Markov chain analysis uses a specialized terminology, and a brief list of important results is given next. For a complete review, see for example [67], [58], [26]. A Markov chain is *irreducible* if every state can be reached from every other state. The state i is *recurrent* (or essential) if the chain can eventually return to i from every state that may be reached from i; every state in an irreducible chain is therefore recurrent. A recurrent state to which the chain can return only after an integer multiple of d transitions ($d \geq 2$) is called a periodic state, with period d. The property of irreducibility, which is assumed in this thesis, implies that, if any state is periodic, then the periods of all states are the same.

A Markov chain with finitely many states is classified as *ergodic* if it is irreducible and aperiodic (i.e. has no periodic states) [67]. The limiting state probability Π_i of the state i is the probability that the chain is in state i after a great many state transitions. This quantity is independent of the initial state under ergodicity assumptions. In homogeneous Markov chains the probability distribution for the time spent in each state (holding time) is a geometric random variable [67].

The concept of signals generated by Markov chains has been introduced by Huggins [56], and later refined in [3]. The case of synchronous Markov chains ($T_i = T$)

with a periodic structure is discussed in [37], and applied to continuous–time frequency shift keyed modulation. General capabilities of Markov chains for spectral shaping in digital communications are outlined in [72]. Discrete spectra of codes specified by Markov chains are studied in [62], and power spectra of binary sequences generated by finite state machines are analyzed in [59]. The design of Markov sources with dc–free power spectra is discussed in [61]. The application of Markov chains to power electronics as proposed here appears to be entirely novel.

The next task is to establish relations linking the discrete–time Markov chain that governs the generation of the switching function with the continuous–time switching function $q(\cdot)$. This connection is complicated by the fact that switching cycles corresponding to individual states of the chain could have different durations T_i (in the case of asynchronous chains). It turns out that a convenient way to achieve that goal is the mechanism of *recursive* Markov chains. They are described in more detail in the Section 6.2.

Another development presented in this chapter is the study of periodic (but possibly asynchronous) Markov chains. The n states are divided into N classes, and state transitions of the underlying discrete–time Markov chain are constrained to occur between one class and the next ($i \longrightarrow i+1$, $1 \leq i < N$, and from N-th class to the first). In that case liniting state probabilities as defined earlier do not exist (they do exist, however, conditioned on the knowledge of the class in which the chain is). This setup represents a generalization of the block–stationary random modulation analyzed in Chapter 5, and is analyzed in Section 6.3

6.1 Stationarization of Signals Governed by Markov Chains

The stationarization procedure for Markov chains, which has been mentioned in Chapter 3 will be explained next. First, consider the case of an ergodic (i.e. aperiodic and irreducible) Markov chain with finitely many states, i.e., the case when limiting or steady–state probabilities exist. Let $x(\cdot)$ be the waveform obtained by a concatenation

of the cycles associated with the states that the chain visits in a particular realization of the random process. The product $x(t+\tau)x(t)$ depends on both t and τ, in general. Let $s(t)$ denote the state of the chain at time t and let $\bar{T}$ denote the expected duration of a cycle in the steady state. The probability $Pr[s(t-\tau)=j, s(t)=i]$ is needed to evaluate the autocorrelation. The number m of state transitions between t and $t+\tau$ is a member of a set of mutually exclusive and collectively exhaustive events. Let the maximal number of state transitions in the interval $2\hat{T}$ under consideration be M; note that $M\bar{T}/2\hat{T} - 1$ [130]. Then,

$$Pr[s(t+\tau)=j, s(t)=i] = \sum_{m=1}^{M} Pr[s(t+\tau)=j, s(t)=i, m=m] \qquad (6.2)$$

The right hand side of this equation can be evaluated using a derivation described later in this chapter. The procedure is based on a random incidence assumption, in addition to taking the expectation in the autocorrelation calculation, as pointed out in Chapter 3. It is assumed that the $Pr[s(t)=i]$ equals Π_i, where Π_i is the steady-state probability of the state i. In that case the right hand side of (6.2) can be evaluated, using an m-fold convolution of the state transition matrix. An autocorrelation calculated in this way is time-averaged (via the steady-state probabilities), and depends on τ only. The corresponding power spectrum is labelled as the mean or time-average power spectrum.

In the special case of synchronous transitions with a cycle duration T, the calculations are simplified. For a given $\tau > 0$, the number of transitions m equals either the integer part of $\frac{\tau}{T}$, or exceeds this by 1.

In the case of periodic Markov chains, the state goes through $N-1$ other classes before returning to the starting class C_i, as discussed in Section 6.3. A conditioning is added in the calculation of the autocorrelation, where $Pr[s(t+\tau)=j, s(t)=i \mid s(t) \in C_i]$ is used instead of $Pr[s(t+\tau)=j, s(t)=i]$. The random incidence assumption yields the probability of the event $s(t) \in C_i$ which equals $T_i / \sum_{j=1}^{N} T_j$, where T_j is the expected length of a waveform segment generated in the class C_j in the steady state. The other steps in the calculation of the power spectrum are the same as in

the aperiodic case. with the same simplifications if a synchronous Markov chain is considered.

6.2 Ergodic Markov Chains

Ergodic Markov chains (i.e irreducible and aperiodic chains) are considered in this section. Our goal is to analyze the continuous–time switching waveforms associated with an n–state discrete–time Markov chain. The chain is characterized by the $n \times n$ state transition matrix $\bar{P} = [\bar{P}_{k,l}]$. This matrix is a stochastic matrix, i.e. its rows sum to 1.

At a state transition from state k, a switching cycle of length T_k is generated, and the switching function $q(t)$ is a concatenation of such cycles. The main source of analytical difficulties is the fact that cycle durations could be different for different states, so care needs to be exercised when the continuous–time switching waveform is related to the discrete–time Markov chain used for random modulation.

We assume throughout that the Markov chain is in steady state. The steady state probabilities of the chain can be found from [67]:

$$\Pi \bar{P} = \Pi \tag{6.3}$$

$$\sum_{i=1}^{n} \Pi_i = 1 \tag{6.4}$$

The vector Π is thus the normalized left eigenvector of the matrix $\bar{P}$ corresponding to the eigenvalue 1, and its existence follows from the assumed ergodicity properties of the underlying Markov chain. Estimates of times needed for a given Markov chain to essentially reach stationarity are discussed in [34].

Let $\bar{T}$ be the average transition time:

$$\bar{T} = \sum_{k=1}^{n} \Pi_k T_k \tag{6.5}$$

The next task is to find the autocorrelation of the continuous–time waveform

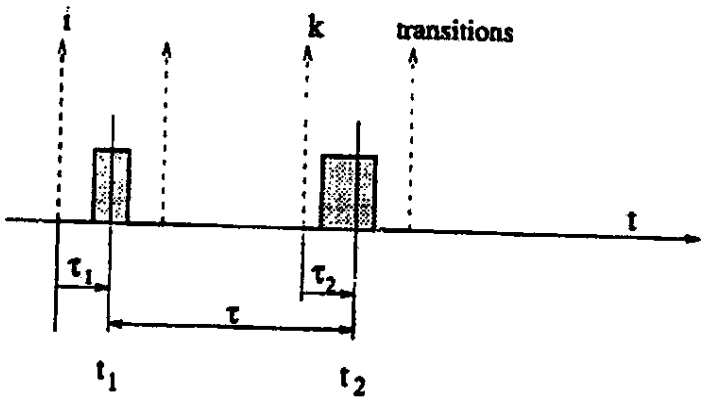


Figure 6.1: Notation for a Waveform Generated by a Markov Chain.

generated by a Markov chain, assuming a random incidence. A typical waveform is shown in Fig. 6.1. Let the waveform in the switching cycle of duration T_k associated with the state k be u_k, and let u be an n-vector with entries u_k. The number $\hat{m}$ of state transitions between t and $t+\tau$ is a member of a set of mutually exclusive and collectively exhaustive events. If $\tau > 0$ and $\hat{m} \geq 1$,

$$R_y(\tau) = \sum_{m=1}^{M} R_y(\tau \mid \hat{m} = m) \tag{6.6}$$

where $R_y(\tau \mid \hat{m} = m)$ denotes $E[y(t)y(t+\tau) \mid \hat{m} = m]$.

Referring to Fig. 6.1, we can identify the components that go into computing this conditional autocorrelation. We assume random incidence at time t_1. The probability of being in state i at t_1 is Π_i. We denote the time of incidence relative to the start of the switching cycle in this incident cycle by τ_1. At time $t_2 = t_1 + \tau$, we are in state k, m transitions later. We denote this time, relative to the start of the associated switching cycle, by τ_2. The probability of being in state k after m transitions is given by the (i,k)–th entry of $\tilde{P}^m$. Weighting the product $u_i(\tau_1)u_k(\tau_2)$ by the appropriate probabilities and averaging in time yields the desired result. In general, for $\hat{m} = m$, the autocorrelation is obtained from

$$R_y(\tau \mid \hat{m} = m) = \int_0^{T_M} \int_0^{T_M} \frac{\mathbf{u}^T(\tau_1)}{\tilde{T}} \Theta Q^{\mathrm{m}}(\tau + \tau_1 - \tau_2)\mathbf{u}(\tau_2) d\tau_1 \, d\tau_2 \tag{6.7}$$

In this expression $\Theta = diag(\Pi_i)$, T_M denotes $\max_k T_k$, $Q(\sigma)$ is the $n \times n$ matrix whose (k,l)-th entry is

$$Q_{k,l} = \bar{P}_{k,l}\delta(\sigma - T_k)$$

and $Q^{\mathrm{m}}(\cdot)$ denotes the m–fold convolution of $Q(\cdot)$ with itself, with $Q^0 = I$. The m–fold convolution of the δ–functions in the definition of Q serves to keep track of all the possible combinations of m cycle lengths between t_1 and t_2. Because of the steady state assumption, the time average can be computed via integrals over length just T_M, scaled by the factor $\bar{T}$ that appears in (6.7).

Let M denote the maximal number of state transitions in a truncated realization of length $2\hat{T}$ (cf. Section 3.2). Note that $\frac{M\bar{T}}{2\hat{T}} \longrightarrow 1$, as $\hat{T} \to \infty$. Let $S_y^+(f)$ be the Fourier transform of $R_y(\tau \mid \hat{m} \geq 0)$ for $\tau > 0$, and $S_y^-(f)$ be the Fourier transform of the same autocorrelation for $\tau < 0$. Then, after the symmetrical truncated realization of the signal y of duration $M\bar{T}$ is introduced [130], [28],

$$S_y^+(f) = \lim_{M\to\infty} \sum_{\hat{m}=0}^{M} R_y(\tau \mid \hat{m}) e^{-i2\pi f\tau} d\tau \tag{6.8}$$

yielding (after neglecting certain terms that vanish as $M \to \infty$)

$$\begin{aligned} S_y^+(f) \;=\; & \lim_{M\to\infty} \int_0^{M\bar{T}} \sum_{\hat{m}=0}^{M} \int_0^{T_M} \int_0^{T_M} \frac{\mathrm{u}^T(\tau_1)}{\bar{T}} \Theta \\ & Q^{\mathrm{m}}(\tau + \tau_1 - \tau_2)\mathrm{u}(\tau_2) d\tau_1 \, d\tau_2 e^{-i2\pi f\tau} d\tau \end{aligned} \tag{6.9}$$

By defining $\sigma = \tau + \tau_1 - \tau_2$ and recognizing appropriate terms, we get

$$S_y^+(f) = \frac{1}{\bar{T}} U^T(-f)\Theta F(f) U(f) \tag{6.10}$$

where $U(f)$ is the Fourier transform of the vector $u(t)$ and

$$F(f) = \sum_{m=0}^{\infty} (\hat{Q}(f))^m \tag{6.11}$$

and $\hat{Q}(f)$ is the Fourier transform of the matrix $Q(\sigma)$. From the construction,

$\hat{Q}_{k,l}(f) = [\bar{P}_{k,l}e^{-i2\pi T_k f}]$. Assuming that the eigenvalues of $\hat{Q}(f)$ have moduli less than 1, the geometric series involving $\hat{Q}^m(f)$ converges yielding

$$F(f) = (I - Q(f))^{-1} \tag{6.12}$$

Using the fact that $S_y^-(f) = S_y^+(-f)$, we arrive at the spectral formula:

$$S_{cy}(f) = U(f)^H[\Theta F(f) + (\Theta F(f))^H - \Theta]U(f) \tag{6.13}$$

The subscript c is used to emphasize that this is a continuous spectrum.

If $Q(f)$ has eigenvalues of modulus 1, the spectrum will have discrete components located at k/T, where k is any positive integer and T is the greatest common denominator of the T_k's. Asymptotic properties of $Q(f = k/T)$ [130] establish that at $f = k/T$

$$\lim_{M\to\infty} \frac{1}{M} \sum_{m=1}^{M} Q(f)^m = \mathbf{1_n}\Pi^T \tag{6.14}$$

where $\mathbf{1_n}$ is an n–vector of ones. The final result for the intensities of the lines in the discrete spectrum is

$$S_{dy}(\frac{k}{T}) = \frac{1}{T^2} \mid \Pi^T U(\frac{k}{T}) \mid^2 \tag{6.15}$$

6.2.1 Synchronous Transitions

In the case of Markov chains with synchronous transitions, with the time between transitions T, $Q(f) = \bar{P}e^{-i2\pi fT}$, and its eigenvalues have moduli < 1, for $f \neq \frac{k}{T}$, $k \in Z$. The same problem has been addressed in [37], [5]. The reference [37] considers synchronous Markov chains that are allowed to be periodic, and corrects a minor error in an earlier derivation [118].

The result in [37] is that if $p_{uv}(l)$ denotes the probability of getting from the state u to the state v in *exactly* l steps, then the spectrum of the pulse train is:

$$S_y(f) = \frac{1}{T}\{\sum_{k=1}^{n} \Pi_k \mid U_k(f) \mid^2 + 2Re \sum_{l=1}^{\infty} \sum_{u=1}^{n} \sum_{v=1}^{n} \Pi_u p_{uv}(l) U_u'(f) U_v'(f) e^{i2\pi flT}$$

$$+\frac{1}{T}\mid\sum_{k=1}^{n}\Pi_k U_k(f)\mid^2\sum_{l=0}^{\infty}\delta(f-\frac{l}{T})\} \tag{6.16}$$

where

$$U'_u(f)=U_u(f)-\sum_{k=1}^{n}\Pi_k U_k(f) \tag{6.17}$$

The equation (6.16) corrects a minor typographical error in [37] in scaling of the discrete spectral component.

A similar setup is discussed in [5], where a binary (vector valued) process is considered, with intended application in digital communications, specifically for analysis of a finite–state sequential machine driven by a stationary Markov chain. The paper [5] is characterized by a very readable matrix notation, but it does not cite the earlier reference [37].

6.2.2 An Example of Switching Governed by a Markov Chain

An example with a 4–state Markov chain is considered next. This chain corresponds to the following switching policy:

- Either long (L, $D=0.75$) or short (S, $D=0.25$) pulses can be fired.
- The controller observes the last two pulses and if they are SL or LS, then either L or S is fired with probability 0.5.
- If the pair observed is LL, then an S pulse is applied with probability 0.75 (and an L pulse with probability 0.25).
- If the pair observed is SS, then an L pulse is applied with probability 0.75 (and an S pulse with probability 0.25).

The corresponding Markov chain is illustrated in Fig. 6.2, and the associated state transition matrix is:

$$\bar{P}=\begin{bmatrix}0.25 & 0.75 & 0 & 0\\ 0 & 0 & 0.5 & 0.5\\ 0.5 & 0.5 & 0 & 0\\ 0 & 0 & 0.75 & 0.25\end{bmatrix} \tag{6.18}$$

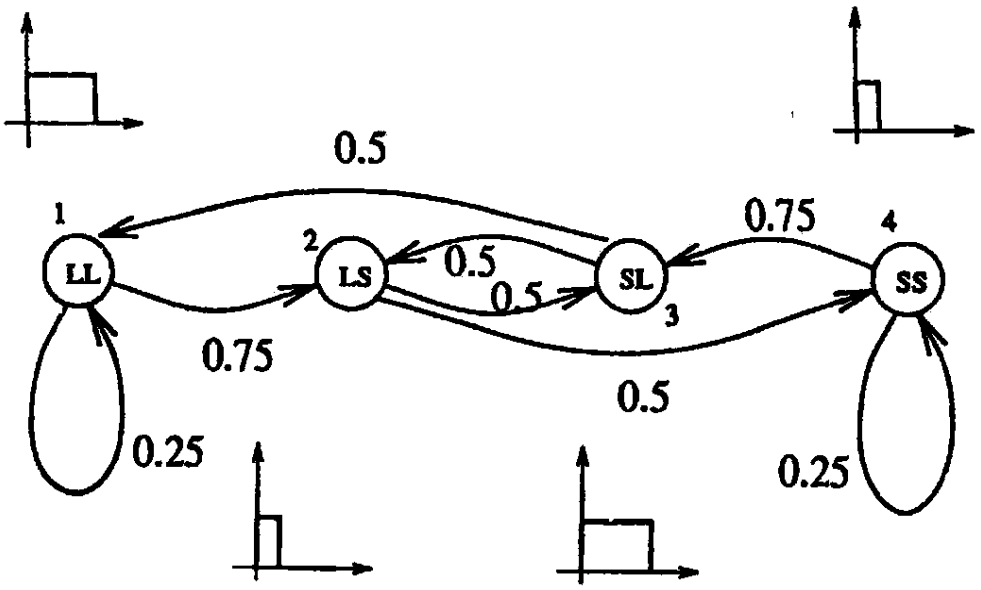


Figure 6.2: An Example of the Markov Chain Based Random Switching.

This Markov chain is ergodic so the limiting probabilities exist, satisfying

$$\Pi \bar{P} = \Pi \tag{6.19}$$

In our example

$$\Pi = [0.2 \;\; 0.3 \;\; 0.3 \;\; 0.2] \tag{6.20}$$

The matrix $\bar{P}$ belongs to the class of irreducible stochastic matrices. for which all eigenvalues have modulus less than or equal to 1, $\lambda = 1$ is a simple eigenvalue and other eigenvalues of modulus 1 (if they exist) are simple and correspond to a complex root of 1 of appropriate order. Π is a left eigenvector corresponding to $\lambda = 1$ and the corresponding right eigenvector is $[1\ 1\ 1\ 1]^T$.

The discrete and continuous spectrum corresponding to the example are shown in Fig. 6.3. The example can be analyzed using either (6.13) or (6.16). The differences between the results obtained from (6.13) and (6.16) are small, and they can be attributed to numerical sources.

Simulation results for the same example are given in Figure 6.4. Estimates of the power corresponding to the first two harmonics could be obtained using the same pro-

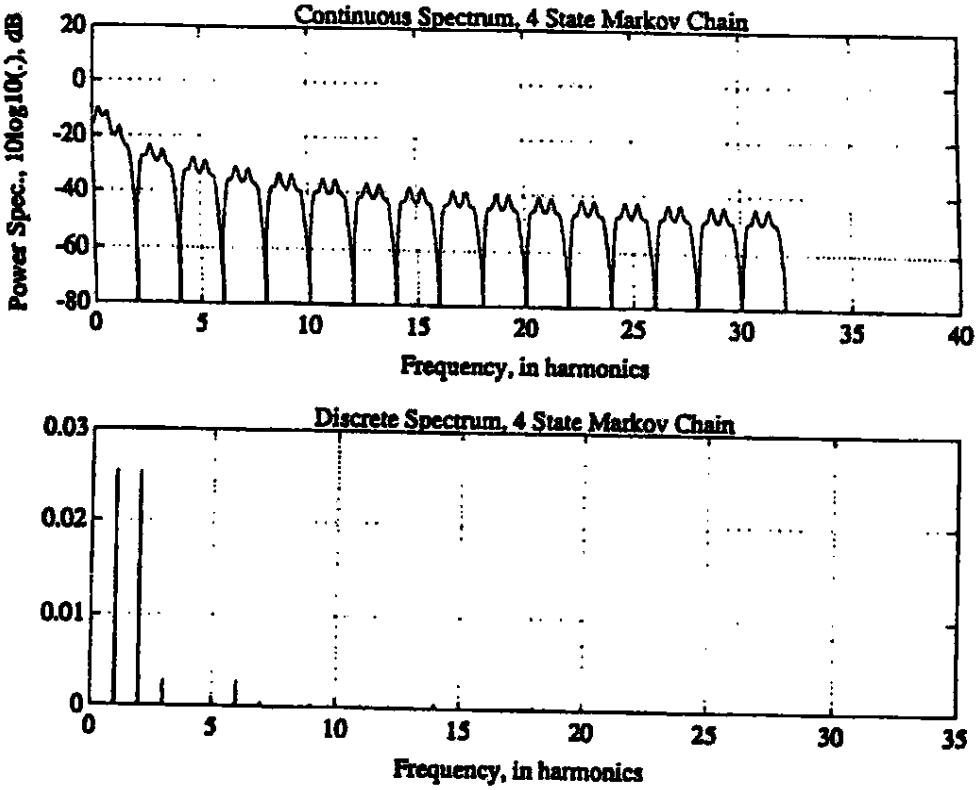


Figure 6.3: Calculated Spectrum for the Markov Chain Example.

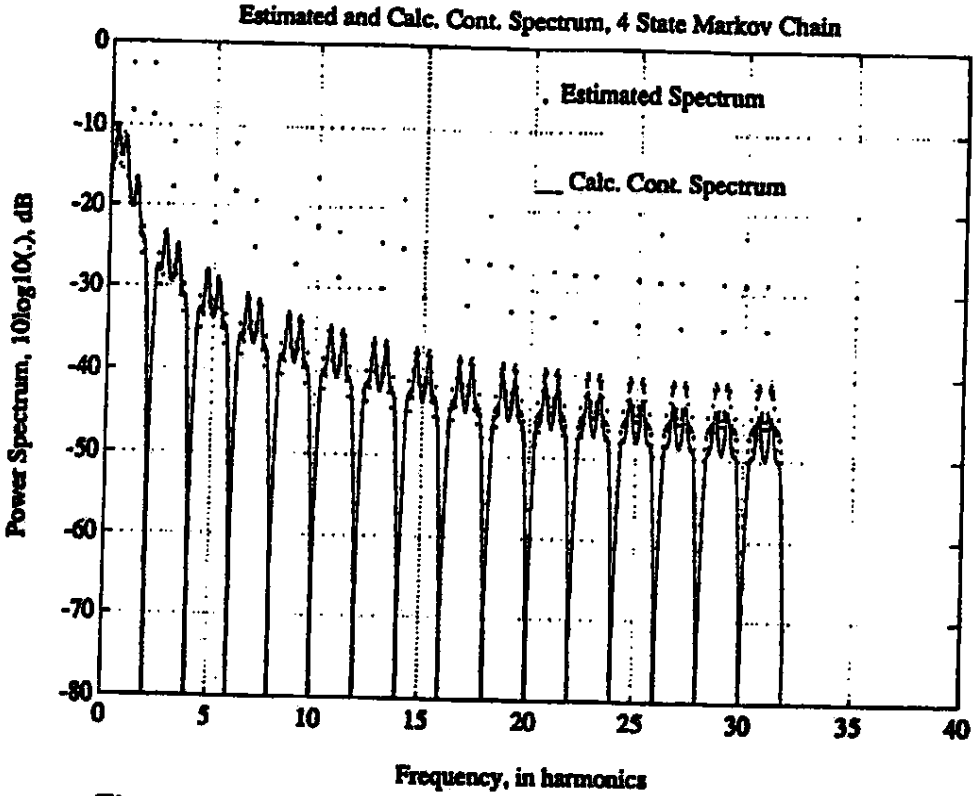


Figure 6.4: Simulated Spectrum for the Markov Chain Example.

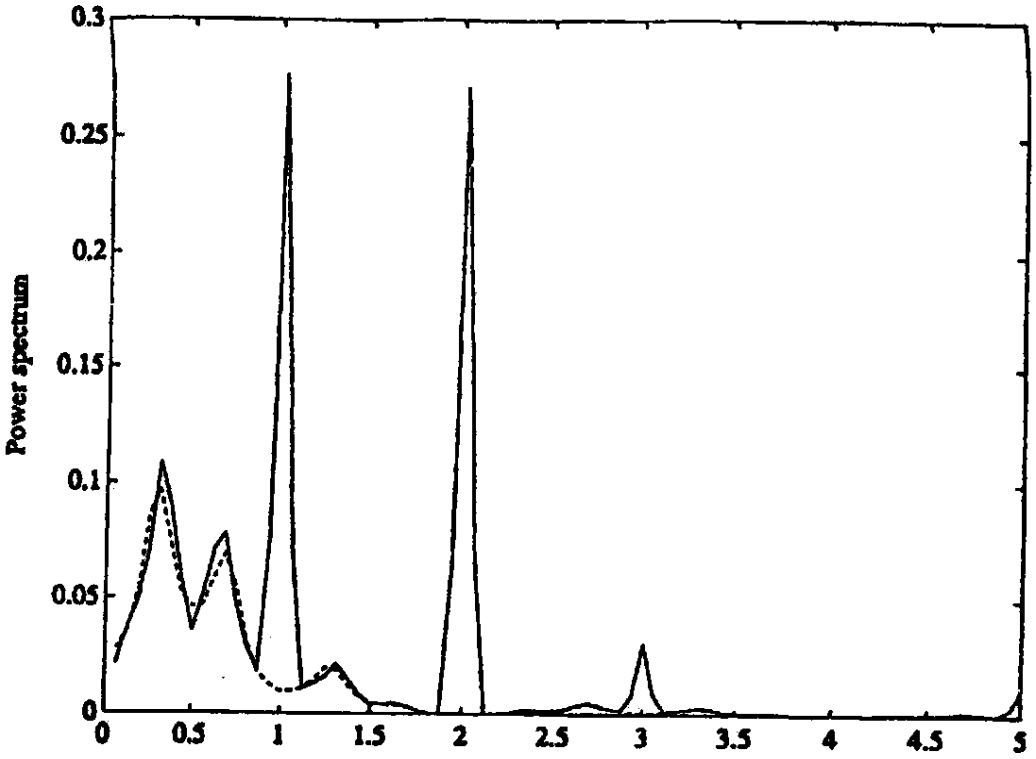


Figure 6.5: Comparison of the Estimated Total Spectrum (solid line) with the Calculated Continuous Spectrum (dotted line) for the Markov Chain Example.

cedure as in the previous chapters. The numerical values for the first two harmonics are 0.0268 and 0.0254, respectively, which are close to the calculated values shown in Fig. 6.3. The continuous part of the spectrum is compared with the estimate for the complete spectrum in Figure 6.5 and very good agreement is observed. The localized large deviations between the estimated and calculated continuous spectrum are due to the discrete spectral components. (Recall that Welch's procedure generates the estimate of the total power spectrum, i.e., of the sum of continuous and discrete spectra.)

The effects of Markov random modulation on the ripple reduction in this example can be compared with the random PWM example in Chapter 4, in which a random choice between duty ratios $\frac{1}{4}$ and $\frac{3}{4}$ is made. This discussion can be analogously modified to other cases of interest. In the case of independent choice between S pulses (with probability p) and L pulses (with probability q), as in Chapter 4, the event "five successive long pulses" can be modeled with the Markov chain shown in

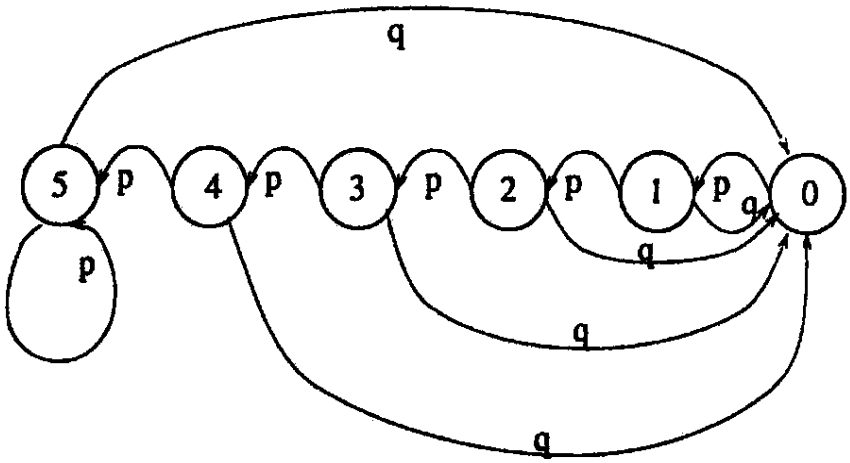


Figure 6.6: A Markov Chain Corresponding to 5 Successive L Pulses.

Fig. 6.6, where state numbers denote the number of long pulses observed in a row. This chain is ergodic, and the limiting state probability of the state 5 is $\Pi_5 = p^5$. Limiting state probabilities could be interpreted [69] as the average proportion of time which the chain spends in each state. A sequence of 1000 simulations has been performed to validate the model shown in Fig. 6.6. Each simulation consists of 256 independent trials with $p = \frac{1}{2}$. The value obtained for $\Pi_5 = p^5$ was 0.03117, which is within 0.3% of the calculated value 0.03125.

In the Markov random switching example shown in Fig. 6.2. the probability of observing 5 long pulses in a row after a random incidence is 3125×10^{-6}. which is the product of $\Pi_1 = 0.2$ and the probability of having three more long pulses. which equals $(\frac{1}{4})^3$. The value obtained from a sequence of 1000 simulations with 256 transitions is 3111×10^{-6}, which is within 0.4% of the calculated value. Thus, the application of a simple Markov chain reduces the probability of large deviations (from the expected value of the duty ratio) by an order of magnitude. Markov chain switching can reduce these deviations even further, for example by setting the transition probabilities to $q_{12} = 1$, $q_{43} = 1$ (and $q_{11} = 0$, $q_{44} = 0$), as shown in the Appendix D. A portion of the calculated power spectrum for the standard example from Fig. 6.2 is shown in Fig. 6.7 on a linear scale. The experimental verification is shown in Fig. 6.8, and a very

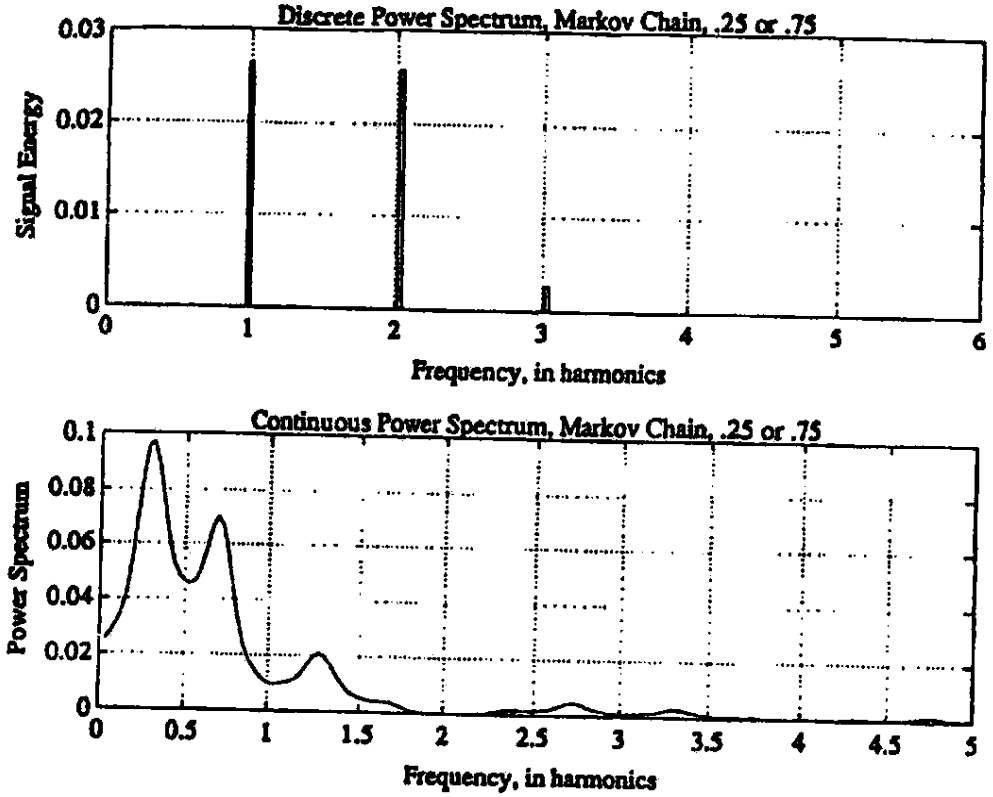


Figure 6.7: A Part of the Calculated Spectrum in the Markov Chain Based Random Modulation Example.

good agreement should be noted (switching frequency is 10 kHz). A more detailed description of the experimental setup, together with illustrations of the time-domain performance, are shown in Appendix D.

Variations in duty ratios in the example (while the average $D = 0.5$ is kept fixed) do have a large impact on the spectrum. Compare the results in Figure 6.9, where $D_1 = 0.95, D_2 = 0.05$, with Fig. 6.3. The effects of changes in the matrix $\bar{P}$ are much less pronounced. In Figure 6.10, the probability of an L pulse after LL is 0.05 instead of 0.25 and symmetrically for an S pulse. but the results are not much different from those in Fig. 6.3.

6.2.3 Asynchronous Transitions

As an example of an aperiodic Markov chain with asynchronous transitions, consider the chain shown in Fig. 6.11, with waveform durations $T_1 = 3$, $T_2 = 0.5$, duty ratio $D = 0.5$. In this case

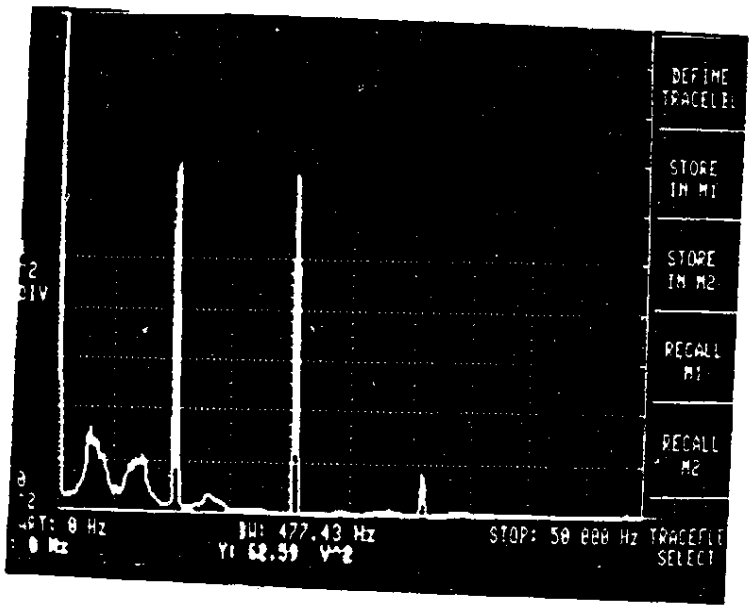


Figure 6.8: Measured Power Spectrum in the Markov Chain Based Random Modulation Example.

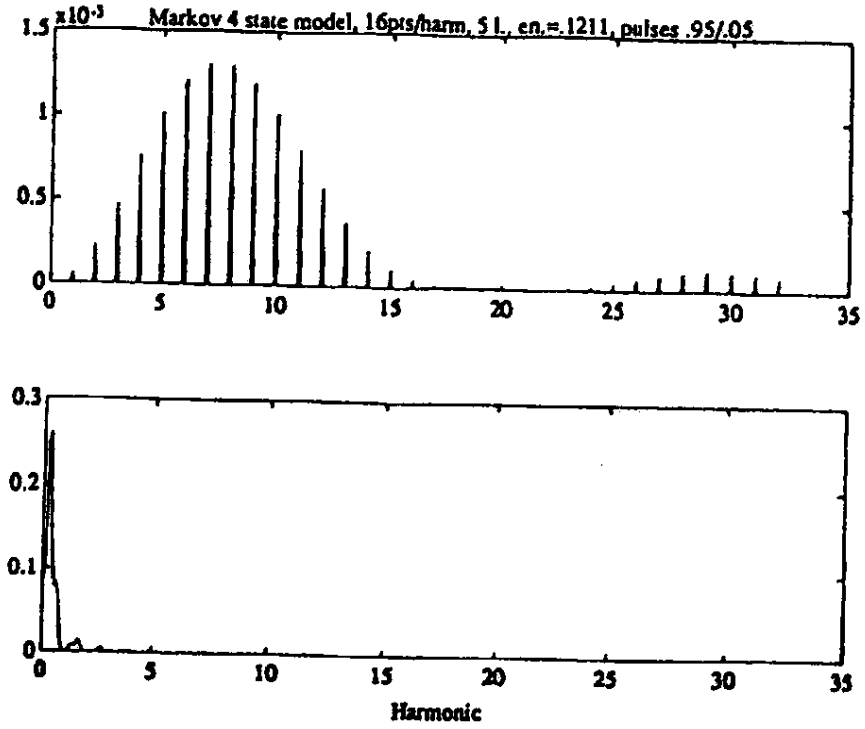


Figure 6.9: Duty Ratio Variation in the Markov Chain Example.

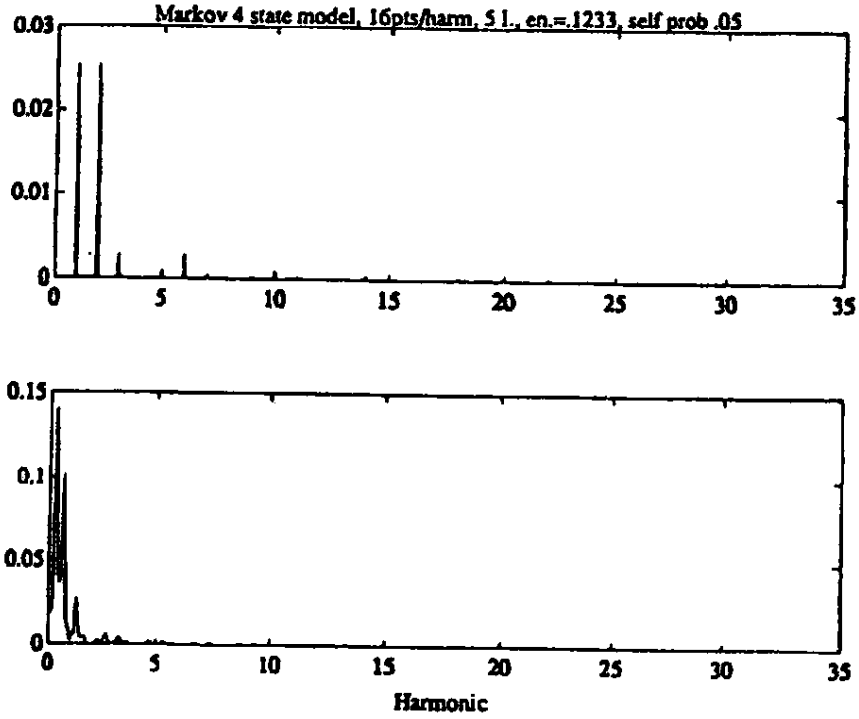


Figure 6.10: Transition Matrix Variation for the Markov Chain Example.

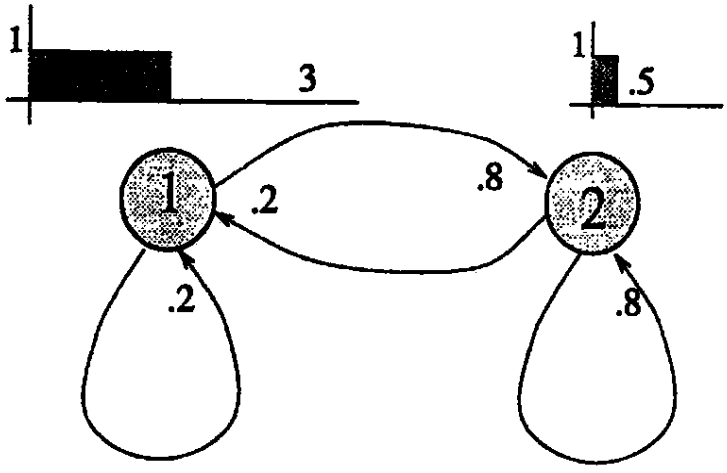


Figure 6.11: Example of an Aperiodic Markov Chain with Asynchronous Transitions.

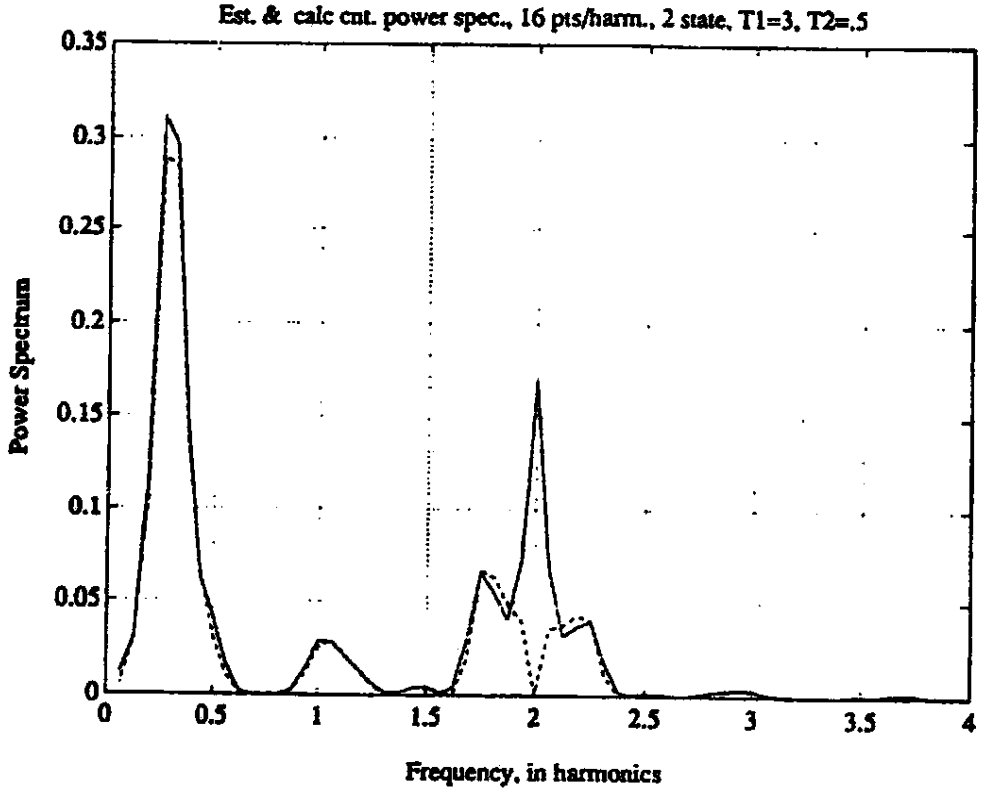


Figure 6.12: Estimated and Calculated Continuous Spectrum for the Aperiodic Asynchronous Markov Chain Example.

$$\hat{Q}(f) = \begin{bmatrix} 0.2e^{i2\pi f3} & 0.8e^{i2\pi f3} \\ 0.2e^{i2\pi f0.5} & 0.8e^{i2\pi f0.5} \end{bmatrix} \tag{6.21}$$

$$U(f) = \begin{bmatrix} e^{i2\pi f0.750}\frac{\sin(\pi f1.50)}{\pi f} \\ e^{i2\pi f0.125}\frac{\sin(\pi f0.25)}{\pi f} \end{bmatrix} \tag{6.22}$$

and the greatest common denominator of the two waveform durations is $T = 0.5$ The steady state probabilities are $\Pi_1 = 0.2$, $\Pi_2 = 0.8$. The calculated continuous spectral component (using (6.13)) and the full estimated spectrum are shown in Fig. 6.12. The discrete harmonic at $f = 2$ is evident in the estimate, and is accurately predicted by (6.15).

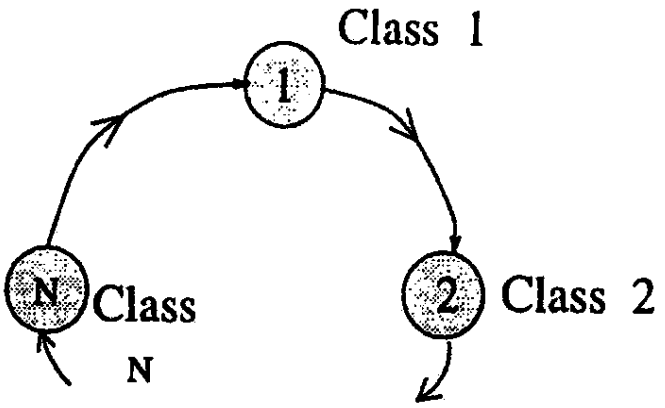


Figure 6.13: Schematic Representing State Trajectory Through Classes of States of a Periodic Markov Chain.

6.3 Periodic Markov Chains

The case of pulse trains specified by periodic Markov chains is considered in this section. A related result for the special case of synchronous Markov chains is given in [37]. The class of recursive Markov chains is analyzed, and it is assumed that the state of the chain goes through a sequence of N classes of states C_i, occupying a state in each class for the average time T_i, $i = 1, \cdots, N$, where the T_i are allowed to be different. This framework is illustrated in Fig. 6.13. In the power electronic setup, periodic Markov chains are of interest in random modulation for DC/AC applications, where the basic (reference) on–off pattern changes from one cycle to the next in a deterministic fashion. This pattern is in turn dithered in each cycle using a set of dependent (Markovian) trials in order to satisfy time–domain constraints (for example to control ripple of waveforms of interest).

The conditioning used in the derivation of the power spectrum formula in Section 6.2 has to be adjusted in the following way. The probability that the state of the Markov chain belongs to the class C_i, after a random incidence, equals $T_i / \sum_{j=1}^{N} T_j$, where T_j is the expected time spent in the class C_j, before a transition into the class C_{j+1}. It can be shown (e.g. in [5]) that after a possible renumbering of the states,

the matrix Q for a periodic Markov chain can be written in a block form

$$Q = \begin{bmatrix} 0 & Q_{12} & 0 & \cdot & 0 \\ 0 & 0 & Q_{23} & \cdot & 0 \\ \cdot & \cdot & \cdot & \cdot & \cdot \\ 0 & 0 & 0 & \cdot & Q_{N-1,N} \\ Q_{N,1} & 0 & 0 & \cdot & 0 \end{bmatrix}$$

Let $\hat{T} = \sum_{j=1}^{N} T_j$, let Π^i denote the steady-state probabilities, conditional on the system being in class C_i, and let $\Theta_i = diag(\Pi^i)$. Then the same procedure as was used in Section 5.2 yields the power spectrum:

$$\begin{aligned} S_y(f) &= \sum_{i=1}^{N} \frac{T_i}{\hat{T}} U_i^H(f)\Theta_i U_i(f) + 2Re(1_N^T S_c 1_N) \\ &\quad + \frac{1}{\hat{T}^2} Re(1_N^T S_d 1_N) \sum_{n=-\infty}^{\infty} \delta(f - \frac{m}{\hat{T}}) \end{aligned} \tag{6.23}$$

where $\hat{T}$ is the greatest common denominator of all waveform durations, 1_N is an $N \times 1$ vector of ones and U_i is the vector of Fourier transforms of waveforms assigned to states in class C_i. A circular indexing scheme (i.e. modulo N) is used in this section.

The matrix S_c has a Toeplitz structure, with (k,l)-th entry

$$S_{c\,k,l} = \frac{1}{\hat{T}} \frac{T_k}{T_{k-1}} U_k^H (I - \Lambda_k)\Lambda_{k,l} U_l \tag{6.24}$$

where Λ_k is a product of N matrices

$$\Lambda_k = Q_{k-1,k} \cdots Q_{k,k+1} \tag{6.25}$$

and

$$\Lambda_{k,l} = Q_{l-1,l} \cdots Q_{k,k+1} \tag{6.26}$$

with no repetitions allowed in $\Lambda_{k,l}$, so that the number of matrices forming $\Lambda_{k,l}$ is

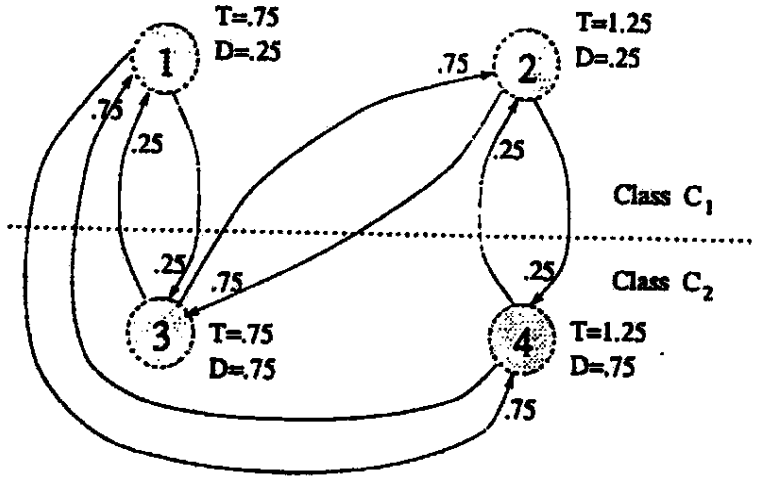


Figure 6.14: Example of a Periodic Four State Markov Chain with Two Classes and Different Cycle Lengths.

$N-|k-l|$. Also

$$S_{d\,k,l} = \frac{T_k}{T_{k-1}} U_k^H \Pi^k (\Pi^l)^T U_l \tag{6.27}$$

The result (6.23) appears to be novel. The formula (6.23) is verified using the example shown in Fig. 6.14. The part of the calculated spectrum in the example where most of the spectral power is located is shown in Fig. 6.15, and the estimated and calculated continuous spectrum are shown in Fig. 6.16.

6.4 Queue Modulation

The scheme for random modulation described in this section can be reduced to one governed by a Markov chain, but may nevertheless be of independent interest. Assume that a discrete–time system generates Bernoulli arrivals with rate λ, and that each new arrival ('customer', in queuing theory terminology) requests that the next μ pulses should be randomly modulated, where μ has a geometric probability mass function. An example of this sort would be a pulse position modulation, which is randomized whenever there are customers being served. This setup, illustrated in Fig. 6.17, corresponds to a discrete–time M/M/1 queue [67]. More elaborate schemes

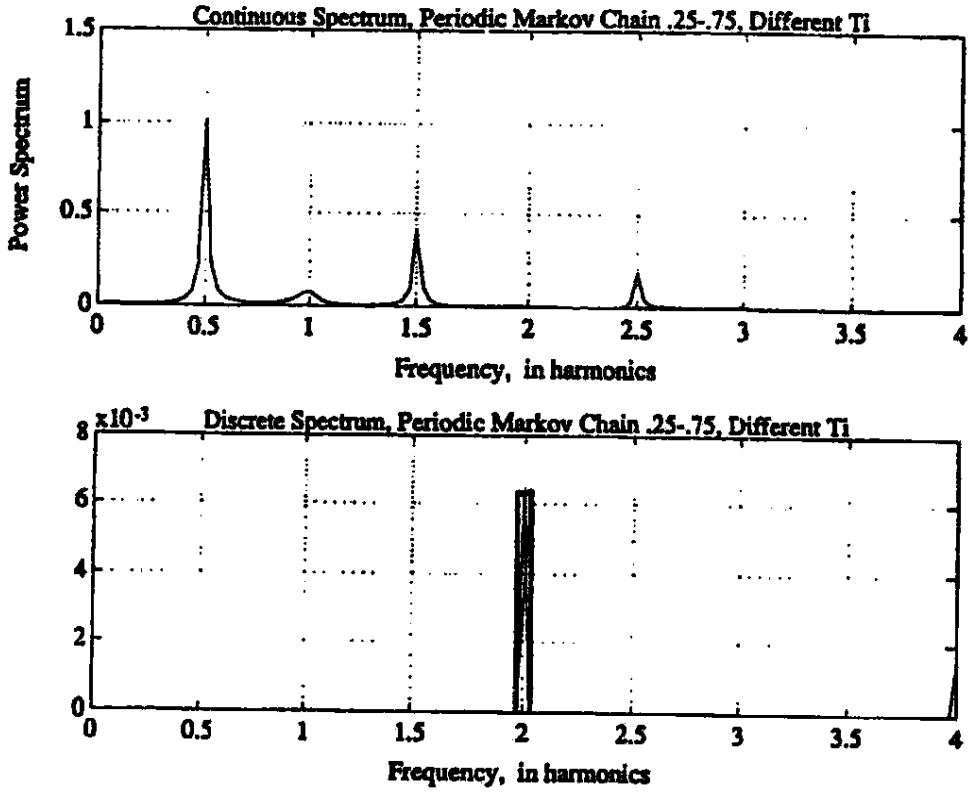


Figure 6.15: Calculated Continuous and Discrete Spectrum in a Periodic Chain with Two Classes and Cycles of Different Length.

can be devised similarly.

It can be shown [67] that the probability that the server is idle is $1 - \frac{\lambda}{\mu}$ ($\lambda < \mu$ is the stability condition for an M/M/1 queue). Any arrival terminates the idle state. These two facts yield the transition probability $\lambda - \mu$ from the busy to the idle state. The corresponding Markov chain is shown in Fig. 6.18.

The calculated spectrum in the example is shown in Fig. 6.19, while the estimated total spectrum and calculated continuous spectrum are shown in Fig. 6.20. A time history of the unfinished work of the server in one simulation is shown in Fig 6.21.

The queue modulation setup can be further refined, for example by adjusting the modulation depending on the number of customers in the queue, leading to Markov chains with more states. Time dependent performance measures for the M/M/1 queue have been studied in [1], [113]. In power electronics applications the queue modulation could be of interest when a request for operation employing random modulation comes as an exogeneous input that includes a random component.

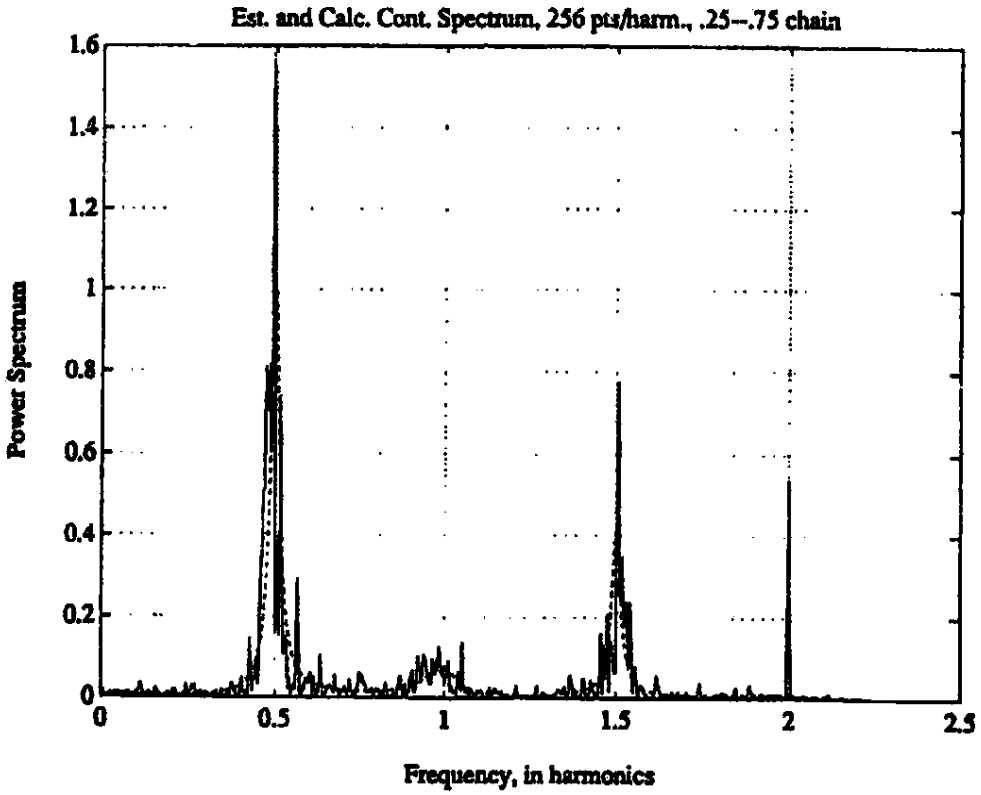


Figure 6.16: Estimated and Calculated Continuous Spectrum in a Periodic Chain with Two Classes and Cycles of Different Length.

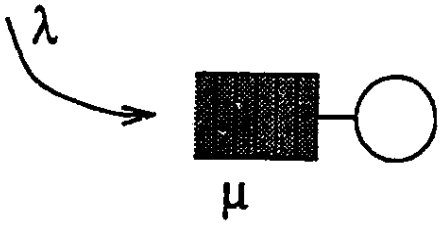


Figure 6.17: Queue Modulation Setup.

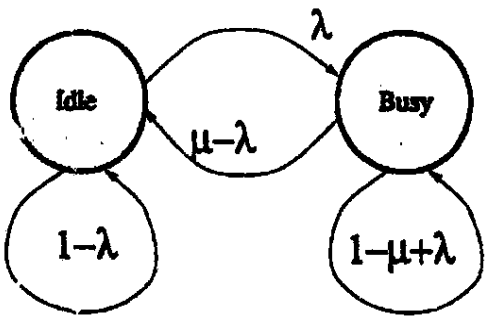


Figure 6.18: Markov Chain Corresponding to a M/M/1 Queue Modulation.

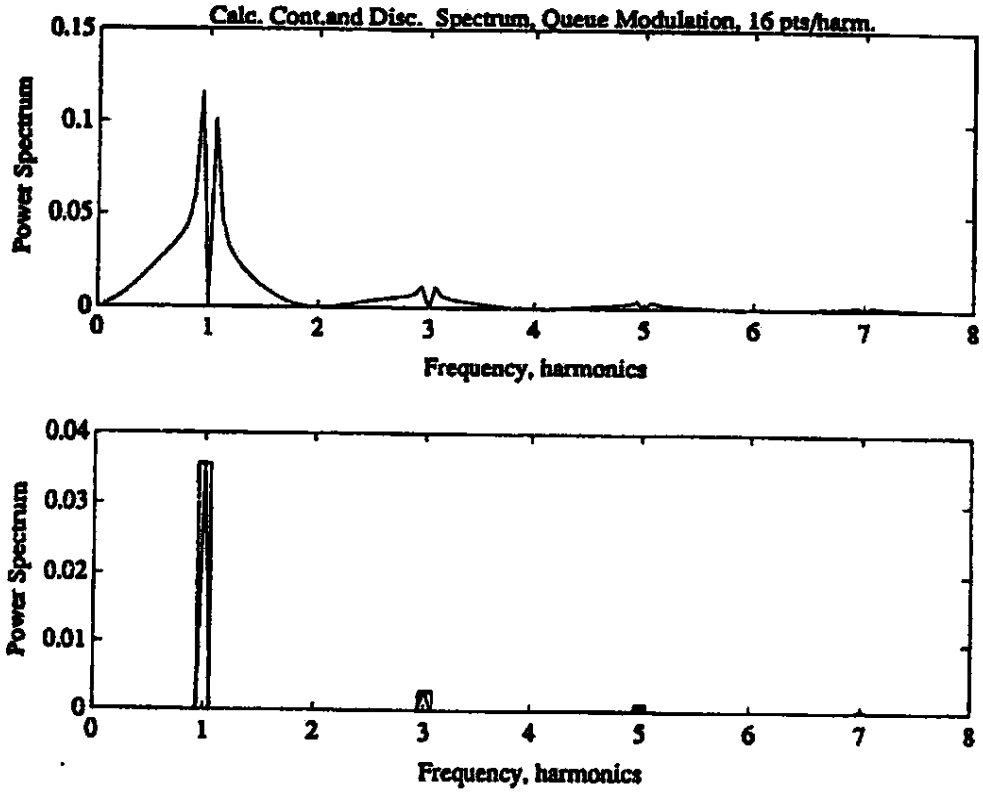


Figure 6.19: Calculated Continuous and Discrete Spectrum in a Queue Modulation Example, Duty Ratio 0.5, Random PPM, Uniform $\in [0,\ 0.5]$.

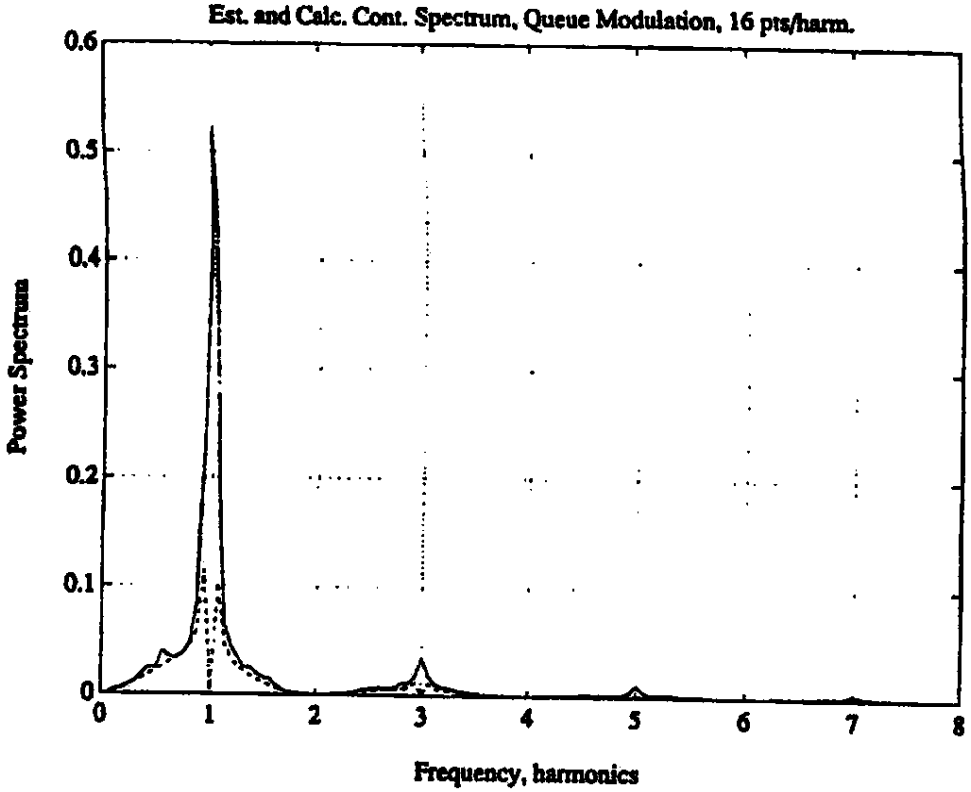


Figure 6.20: Estimated Total Spectrum and Calculated Continuous Spectrum in a Queue Modulation Example, Duty Ratio 0.5, Random PPM, Uniform $\in [0,\ 0.5]$.

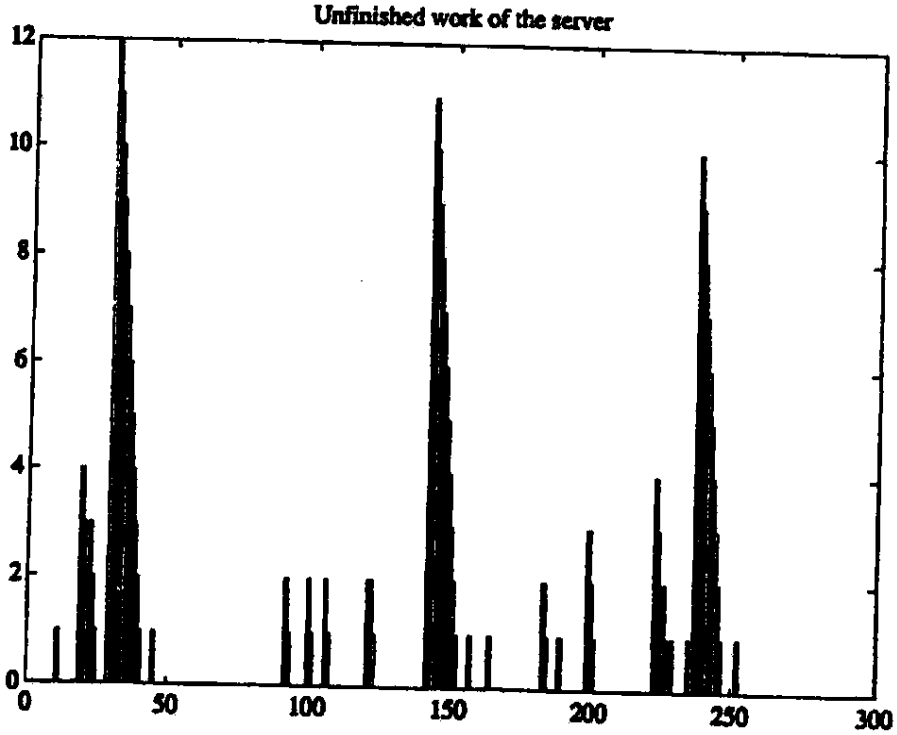


Figure 6.21: Unfinished work of the Server in an M/M/1 Queue Modulation Example.

6.5 Summary

Random modulation based on Markov chains is described in this chapter. It belongs to the class of random modulations with variable stochastic structure; if periodic Markov chains are used, the deterministic structure changes as well. Such random modulation offers additional generality over schemes described in previous chapters. In addition to the spectral shaping, which is a frequency domain requirement, time domain constraints (for example ripple control) can be *explicitly* included into the switching strategy. These possibilities have not been addressed in this manner in power electronics, prior to this thesis.

Waveforms generated by Markov chains are characterized by synchronicity (i.e. whether waveforms associated with the different states are of the same length), and by the periodicity of the chain. Analytical results presented in this chapter enable analysis of all possible cases. The case of periodic asynchronous chains is the most general, and the results presented in this thesis appear to be novel.

Modulation based on a queue framework is described in Section 6.4. This is a new random modulation scheme, and its analysis is based on the theory of signals generated by Markov chains.

This chapter concludes the part of the thesis concerned with the analysis of random modulation schemes. The next chapter addresses the converse problem, namely the synthesis issues in random modulation.

Chapter 7

Synthesis Problems in Random Modulation

In this chapter the goal is to explore how effective random modulation is in achieving various performance specifications in the frequency domain. Desirable properties of power spectra are dependent on the particular application. Requirements of particular interest in practice are the following:

- Minimization of one or multiple, possibly weighted, discrete harmonics. This criterion corresponds to cases where narrow-band characteristics of discrete harmonics are particularly harmful, as for example in acoustic noise, or in narrow-band interference, described in Section 2.2.

- Minimization of signal power (integral of the power spectrum) in a frequency segment that is of the order of an integral multiple of the switching frequency. This criterion corresponds to wide-band constraints in military specifications, and it could be of interest for EMI interference problems.

Further experimental work in random modulation is needed, however, before more precise criteria can be established.

Synthesis problems in random modulation have not been addressed in the available literature to any significant extent, mostly due to the scarcity of analytical formulas for power spectra of random modulation schemes. The need for a systematic approach

to the choice of probability densities in random modulation has been pointed out in [14]. Optimization problems involving *linear* functionals of probability density functions have been considered in [22]. In an estimation setup, bounds for the total spectral energy in a frequency interval have been derived in [83]. That bounding technique has been later generalized to linear functionals of estimated signals in [71]. In a communication theory setup, the problem of specifying Markov chains with spectra that have no DC component is addressed in [61].

In the case of stationary or block-stationary random modulation schemes, the domain of optimization $\mathcal{P}$ comprises of all characteristic functions (Fourier transforms of probability distributions) that have appropriately bounded support in the time domain. In the case of signals dithered by Markov chains, the synthesis procedure has to yield a state transition matrix $\bar{P}$, as well as waveforms associated with each state. It will be shown later that it is hard to completely characterize the optimization domain $\mathcal{P}$, and that partial parametrizations have to be used instead.

Analytical expressions presented in this thesis enable the study of numerous random modulation schemes. In this chapter random PPM and simplified random aperiodic modulation are treated in detail, but the other modulation procedures could be analyzed in an analogous manner. Synthesis problems for signals defined on Markov chains are illustrated on the example used in Section 6.2.1.

The performance achievable by random modulation depends on the width of the support of the dither probability density, which is in turn dictated by the duty ratio of the nominal switching waveforms. The duty ratios considered in the numerical examples in this chapter are 0.1, 0.5 and 0.9. With the duty ratio 0.1 the switching function can be dithered in a wide range under PPM, while the value 0.5 corresponds to "average" operating conditions, and the duty ratio 0.9 allows very little PPM dithering. Additional constraints could exist in implementations, for example minimal on-state, or minimal off-state durations.

7.1 Optimization Problems in Synthesis of Random Modulation

All optimization problems in this section are presented for the case of random PPM. Formulations for other modulation schemes are analogous, and could be specified using the analytic expressions derived in previous chapters and in the appendices.

To streamline the notation, it is assumed that the period of the reference (deterministic) switching waveform is unity, $T_0 = 1$. In that case the power spectrum for random PPM is given by

$$S_v(f) = W(f)[1 - |P(f)|^2 + |P(f)|^2 \sum_{k=-\infty}^{\infty} \delta(f-k)] \tag{7.1}$$

where the non-negative function $W(f)$ represents the square of the Fourier transform of a rectangular pulse of unit height and width D centered at 0. Note that the k-th discrete harmonic has intensity $|P(k)|^2$. Then a typical narrow-band optimization criterion, which corresponds to the minimization of the sum of discrete harmonics between the l-th and L-th, can be written as

$$J_{l,L}^{NB} = \sum_{k=l}^{L} W(k) |P(k)|^2 \tag{7.2}$$

where a weighting function could be absorbed in $W(f)$.

A wide-band optimization criterion used for illustration in this section corresponds to the minimization of the signal energy for random PPM in the frequency segment [0 1.5], where the switching frequency is 1. This criterion can be written as

$$J_1^{WB} = \int_0^{\frac{1}{2}} W(f)(1 - |P(f)|^2) df + W(1) |P(1)|^2 \tag{7.3}$$

Its minimization is equivalent to the maximization of the criterion

$$\bar{J}_1^{WB} = \int_0^{\frac{1}{2}} W(f) |P(f)|^2 \, df - W(1) |P(1)|^2 \tag{7.4}$$

Both the narrow-band criterion J^{NB} and the wide-band criterion J^{WB} are in general nonlinear in $P(f)$: in the PPM case, they are quadratic.

7.1.1 Parametrizing the Domain of Optimization

In some optimization problems it is possible to obtain useful bounds on criterion values from basic properties of $P(f)$, and from the Parseval-Plancherel equality. For example, in random PPM with a duty ratio $D = 0.5$, the total signal power is 0.5, and the DC component of the power spectrum is $(0.5)^2 = 0.25$, so the signal power for $f > 0$ is $\frac{0.5-(0.5)^2}{2} = 0.1250$. If the J_1^{WB} is used as the criterion, then from the properties of $W(f)$ and $P(f)$ it follows that the optimal criterion value satisfies $(J_1^{WB})^* \geq 0.0770$. This bound is not achievable, since the bounding procedure assumes $P(f) = 0$ between the switching harmonics, and $P(f) = 1$ at the second and higher harmonics, which is not possible for a time function of bounded support [29]. Nevertheless, the bound is not too far away from the achievable performance in PPM, which our numerical results suggest is around 0.0965, as will be seen shortly. The simplicity of such bounding schemes makes them suitable for quantitative assessments. The tightness of bounds based on the Parseval-Plancherel equality depends on the speed of decrease of $W(f)$, so they improve as the duty ratio increases. An intuitive explanation is that in such cases the support of the dithering probability distribution is decreased. Thus, the performance is expected to get closer to deterministic switching, which for $D = 0.5$ yields $J_1^{WB} = \frac{1}{\pi^2} = 0.1013$.

The optimization process, which is performed in the frequency domain, has to generate a *function* that satisfies constraints in the time domain. In the case of stationary modulation schemes, the optimization is performed over the space of candidate probability distributions $\mathcal{P}$. In all cases of practical interest these distributions have finite support, which in the example of PPM is constrained to be at most $[0,\ 1-D]$, where D is the nominal (undithered) duty ratio. Probability distributions having point masses (or atomic measures) are also in the set $\mathcal{P}$. They are of practical interest due to the simplicity of their implementation with microprocessor hardware.

If global optimality of solutions to optimization problems in random modulation

is needed, then a complete parametrization of the domain $\mathcal{P}$ *in the frequency domain* is required. Properties of characteristic functions are described in detail in [33], [79]. In this thesis probability densities with absolutely continuous and with discrete parts are considered (leaving out singular densities, which are of theoretical interest). Properties of characteristic functions that are useful in addressing optimization problems in random modulation are [33]:

- $P(f)$ is continuous;
- $P(0) = 1$, $P(f) \leq 1$, $\forall f$;
- if a random variable T with probability density p has characteristic function $P(f)$, then the characteristic function for $aT + b$ is $e^{i2\pi fb}P(af)$.
- $Re(P(f))$ is an even function, and $Im(P(f))$ is an odd function.

Cases where $P(f) = 1$ for some $f \neq 0$ are of special interest, for example in aperiodic random modulation. After discarding the trivial case of a single point mass, the following statements turn out to be equivalent for $\lambda \neq 0$ [79]:

1. $P(\lambda) = 1$,
2. P has period λ, i.e. $P(f + n\lambda) = P(f)$ $\forall n \in \mathbf{N}$,
3. All points of increase of the cumulative distribution (i.e., all locations of point masses in the probability density) are among $\frac{k}{\lambda}$, $k \in \mathbf{Z}$. Such distributions are referred to as lattice distributions.

The following results on asymptotic properties of $P(f)$ are needed for later reference: For a purely discrete probability distribution,

$$\limsup_{f \to \infty} | P(f) | = 1, \tag{7.5}$$

and for an absolutely continuous distribution

$$\lim_{f \to \infty} P(f) = 0 \tag{7.6}$$

Necessary and sufficient conditions on a function for it to be a characteristic function are given by Bochner's theorem [79], [33]. Such a function has to be non-negative definite, in addition to satisfying the normalization condition $P(0) = 1$. A complex valued function G of a real argument is said to be non-negative definite for $-\infty < f < \infty$ if both of the following conditions hold

1. $G(f)$ is continuous, bounded, and $G^*(-f) = G(f)$,
2. For $\forall n \in \mathsf{N}$, $f_1, \ldots, f_n \in \mathsf{R}$, and $\xi_1, \ldots, \xi_n \in \mathsf{C}$:
   $\sum_{j=1}^{n} \sum_{k=1}^{n} G(f_j - f_k)\xi_j \xi_k^*$ is real and non-negative.

The conditions from Bochner's theorem are unfortunately very difficult to check and use in practice. Partial results exist in the form of sufficient conditions for absolutely continuous distributions (due to Polya), and for lattice distributions [79]. In the case of absolutely continuous distributions, sufficient conditions for a real-valued $P(f)$ to be a characteristic function are:

1. $P(0) = 1$,
2. $P(f) = P(-f)$,
3. $P(f)$ is convex,
4. $\lim_{f \to -\infty} P(f) = 0$.

None of these results establishes a complete parametrization of the set of characteristic functions, even in the absence of constraints in time domain. Thus, for our optimization purposes, it is necessary to construct partial parametrizations of the domain $\mathcal{P}$. These parametrizations have to enable efficient search over the domain, so it is desirable that they depend on only a small number of parameters. The other, conflicting requirement is to include all distributions of practical interest in $\mathcal{P}$. Several simple parametrizations of $\mathcal{P}$ are proposed in this thesis, and together they enable optimization over many probability distributions of interest in implementations.

Probability distributions of interest in random modulation synthesis can have both continuous and discrete parts, so the corresponding probability densities are

allowed to have impulsive components. The parametrizations used in the optimization problems here are defined in the time domain as

$$p(t) = \sum_{l=1}^{N} \alpha_l p_l(t) \tag{7.7}$$

where the p_l are known probability densities with appropriate finite support, and the α_l are coefficients to be determined in the optimization. The coefficients satisfy $\sum_{l=1}^{N} \alpha_l = 1$, and $\alpha_l \geq 0$.

With this parametrization, the wide–band criterion in random PPM modulation J_1^{WB} can be brought to a quadratic programming form. Let

$$\alpha = \begin{bmatrix} \alpha_1 \\ \alpha_2 \\ \vdots \\ \alpha_N \end{bmatrix}$$

$$P(f) = \begin{bmatrix} P_1(f) \\ P_2(f) \\ \vdots \\ P_N(f) \end{bmatrix}$$

and

$$\hat{H}(f) = P(f)\, P^H(f) \tag{7.8}$$

Also, let

$$H = \int_0^{\frac{1}{2}} \hat{H}(f) W(f) df - W(1)\hat{H}(1) \tag{7.9}$$

where

$$W(f) = \left(\frac{\sin(\pi f D)}{\pi f}\right)^2 \tag{7.10}$$

If required, a weighting function could be absorbed in $W(f)$. Then

$$\min_{\alpha} J_1^{WB} = \min_{\alpha} \alpha^T H \alpha \tag{7.11}$$

with the standard constraints $\sum_{l=1}^{N} \alpha_l = 1$, and $\alpha_l \geq 0$. The problem (7.11) is *not* necessarily a standard quadratic programming problem, however, since H is not necessarily a positive definite matrix, as evident from (7.9). Thus, with the proposed simple parametrization of $\mathcal{P}$, general nonlinear optimization methods have to be used.

In the PPM example, the support of probability densities used for dither is constrained to $[0, \ 1 - D]$, where D is the duty ratio. It seems desirable for numerical reasons to make the different p_l as independent as possible. This task is made harder by the requirements that $p_l \geq 0$ (as probability densities), and by the fact that the frequency domain optimization is performed over a finite segment for wide–band criteria, and over a sequence of equidistant points for narrow–band criteria.

The different sets of "basis functions" $p_l(t)$ utilized in the optimization procedure described in the next section were chosen for their simplicity and engineering relevance, and not for their numerical performance. It turns out that optimal probability densities obtained with different basis functions are very similar (if measured for example in the $\mathcal{L}^\infty$ norm), and that they yield a very similar performance in terms of the criterion values. This gives some assurance that the choice of basis functions is not critical for the optimization. If the number of basis functions N is significantly increased from values used in this thesis, then the issue of the choice of basis functions will have to be addressed again.

The basis function used to parametrize the domain of candidate probability densities in this chapter are:

- Rectangles, dividing the available probability density support ($[0, \ 1 - D]$ in the PPM case) into N segments of equal width;
- Hanning windows ("raised cosine" functions), with p_1 and p_N being "half–windows", as shown in Fig. 7.1;

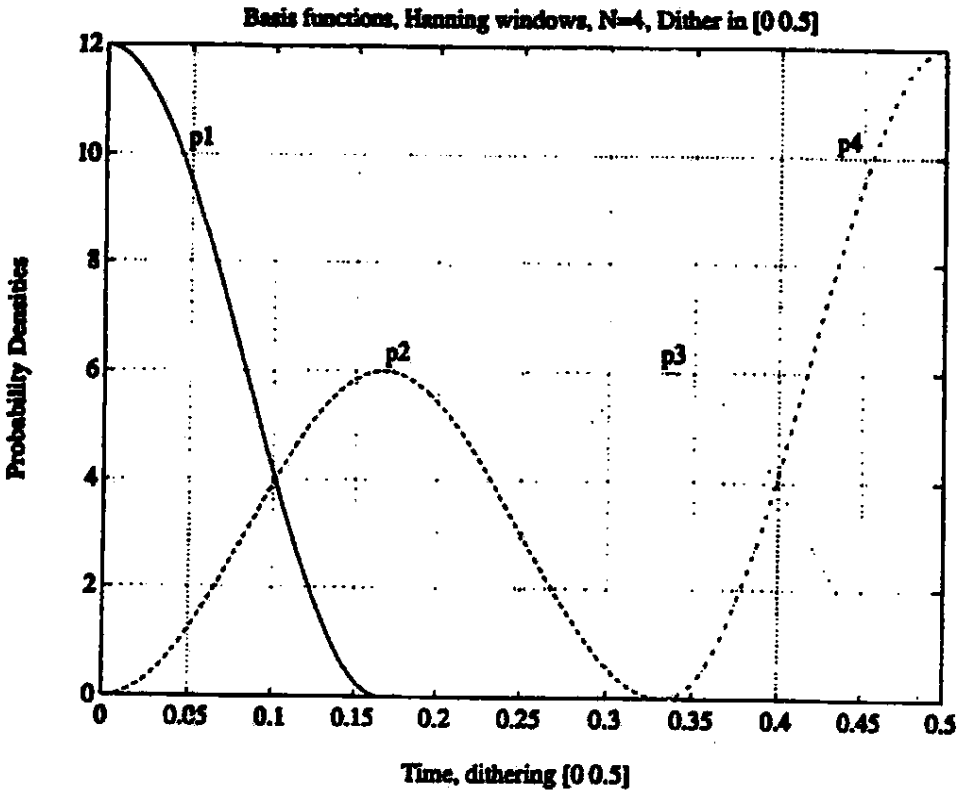


Figure 7.1: Hanning Windows as Basis Functions, N=4, Dither in [0 0.5].

- Atomic measures of N point masses summing to 1, at fixed or variable locations;
- β–densities, given (on the segment $[0,\ 1-D]$) by the expression

$$p(t) = \frac{1}{B(a,b)} t^{a-1}\ (1-t)^{b-1} \tag{7.12}$$

where $B(a,b)$ is the normalizing constant

$$B(a,b) = \int_0^{1-D} \sigma^{a-1}(1-\sigma)^{b-1} d\sigma \tag{7.13}$$

A β–density depends on only two parameters, and it can approximate probability densities having a single maximum or minimum.

Other probability densities used for comparison are the uniform density, and a density comprising N equally spaced probability masses with coefficients $\frac{1}{N}$.

Table 7.1: Narrow-Band Optimization J_{41}^{NB}: Criterion Values ($\times 10^4$).

Modulation	D=0.1	D=0.5	D=0.9
Undithered	450.0	1250.0	450.0
Point Masses	71.8	0.0	197.0
Hanning	3.3	153.0	232.0
Rectangles	3.5	208.0	242.0
Uniform	3.5	417.0	283.0
Uniform Pt. masses	255.0	211.0	240.0

7.2 Numerical Results

7.2.1 Narrow–Band Optimization for Random PPM

Optimization of the narrow-band criterion $J_{1,41}^{NB} = J_{41}^{NB}$ is considered first, with $N = 4$ basis functions in each parametrization. The criterion values at the numerically computed optimum (multiplied by 10^4) are given in Table 7.1 These optimization results are in agreement with the intuition that in cases when there is a large "dithering length" available (i.e., when the duty ratio D is small), then a large reduction of the size of harmonics should be achievable. Though none of our parametrizations for probability densities ends up being superior for all cases, the optimal solutions for different parametrizations are in fact similar. For example, for $D = 0.5$, the optimal rectangle coefficients are [0.5 0 0 0.5], while the optimal peak height ratios for the Hanning basis functions are [0.5 0 0 0.5]. Because of the widths of Hanning basis functions differ from those of the other parametrizations, direct comparison of optimal coefficients α_i^* with other parametrizations is less informative, in general.

In the case of the duty ratio $D = 0.5$, with equal point masses at 0 and 0.5, the orthogonality of $W(f)$ and $|P(f)|$ yields 0 as the value of the criterion. This modulation scheme is sometimes referred to as dual modulation. Such extreme effectiveness in the reduction of discrete harmonics is not always a characteristic of random modulation, but it might account for some dramatic improvements reported in implementations.

The case of a narrow–band minimization of just the first harmonic ($J_{1,1}^{NB} = J_1^{NB}$) is considered next. For duty ratios $D = 0.1$ and $D = 0.5$, this optimization problem

Table 7.2: Narrow-Band Optimization J_1^{NB}: Criterion Values ($\times 10^4$).

Modulation	D=0.9
Undithered	97.0
Point Masses	87.5
Hanning	92.2
Rectangles	91.0
Uniform	94.0
Uniform Pt. masses	92.0

Table 7.3: Wide-Band Optimization J_1^{WB}: Criterion Values ($\times 10^4$).

Modulation	D=0.1	D=0.9
Undithered	96.8	96.8
Point Masses	87.7	96.8
Rectangles	97.3	102.2

is relatively straightforward, and the parametrization with point masses can achieve a criterion value of 0. Just two equal point masses suffice for these cases, one at zero and the other at $\tau = 0.5$, since the resulting characteristic function $P(f) = \frac{1}{2}(1 + e^{-i2\pi\tau})$ satisfies $\mid P(1) \mid = 0$. Thus, the interesting case is $D = .9$, for which the results shown in Table 7.2 are obtained. Thus, with little dithering space available, improvements of the order of 10% are achievable.

7.2.2 Wide–Band Optimization for Random PPM and Simplified Aperiodic Modulation

The criterion J_1^{WB} is considered in this section, and results obtained for random PPM are given in Tables 7.3 and 7.4. Note in Table 7.3 that when the probability density is constrained to rectangular basis functions, the achievable performance is worse than in the undithered case. The results also suggest a limited effectiveness in reducing the total signal energy in a wide frequency band. and this is further illustrated with the $D = 0.5$ case in Table 7.4 (relative peak heights are given in the third column for the Hanning basis). The optimal probability densities for the last three rows in Table 7.4 are illustrated in Fig. 7.2.

Table 7.4: Wide-Band Optimization J_1^{WB}, $D = 0.5$: Criterion Values ($\times 10^4$).

Modulation	Criterion	Coefficients
Undithered	1013	
Point Masses	965	0.5 at 0.16 and 0.34
Hanning	973	[0.33 0.17 0.17 0.33]
Rectangles	973	[0.35 0.15 0.15 0.35]
β–density	975	$a = b = 0.76$

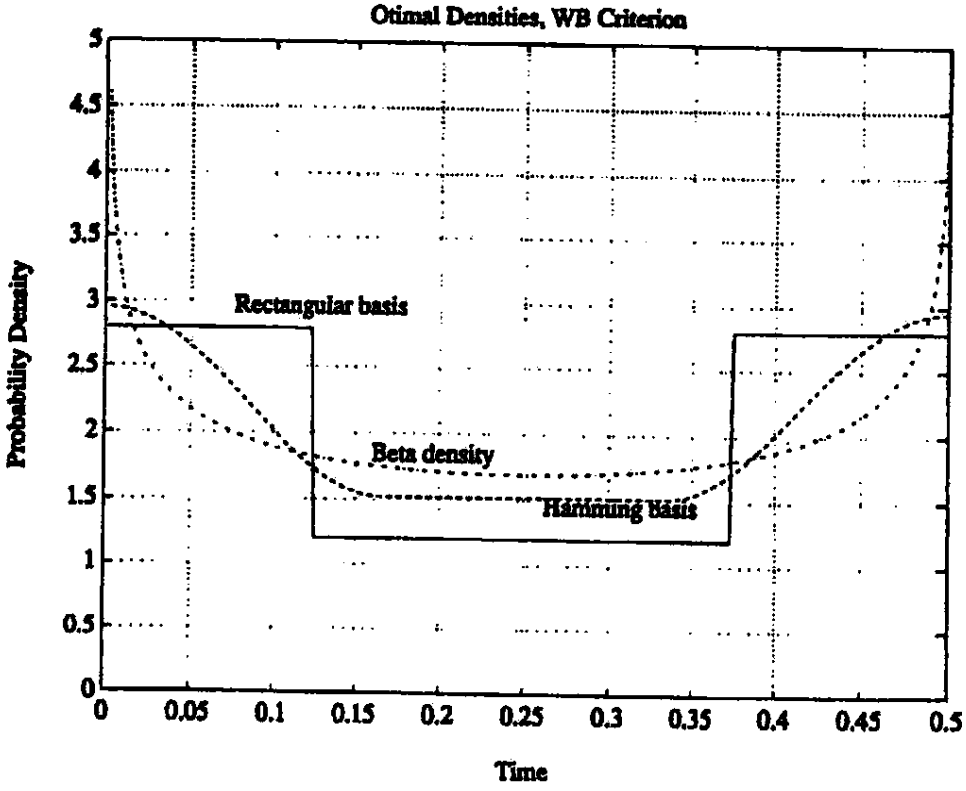


Figure 7.2: Optimal Probability Densities for the Wide-Band Criterion J_1^{WB} for Three Parametrizations.

The performance of random PPM is now compared with simplified aperiodic modulation, which is described in detail in Appendix B. In this aperiodic modulation scheme the "on" part of each cycle is of a fixed length, and it is positioned at the beginning of the cycle, while the length of each cycle is a random variable. The power spectrum has a continuous component, which is given by the expression

$$S_y(f) = W(f)\,(1 + 2Re(\frac{P(f)}{1 - P(f)})) \tag{7.14}$$

where

$$W(f) = (\frac{\sin(\pi f D)}{\pi f}) \tag{7.15}$$

As observed earlier in this chapter, $P(f)$ can equal 1 only if $p(t)$ belongs to the class of lattice distributions. In that case there is a discrete component of the spectrum at frequencies where $P(f) = 1$. The general result derived for Markov chains (6.15) is applicable, and in the above case the discrete harmonics equal

$$S_{dy}(f_d) = W(f_d) \tag{7.16}$$

where f_d is a multiple of the basic frequency of λ, defined in the previous section.

To make synthesis for random aperiodic modulation comparable with results on random PPM, it is necessary to constrain the probability density $p(t)$, so that the expected value of the cycle length equals 1, which is the average switching period. The cycle length T_i is assumed to be $T_i \in [D,\ \ 2 - D]$, yielding the same maximal and minimal "on" and "off" states as the random PPM. The results of optimization for random aperiodic modulation are shown in Table 7.5 The results presented in Table 7.5 are comparable to those obtained with random PPM, and suggest that both methods have limited capabilities in reducing the wide–band signal energy.

The preceding results corroborate observations in [126] that it is easier to satisfy wide–band constraints using optimized deterministic switching ("programmed switching"), while the random modulation is more suitable for narrow–band constraints. This complementarity of the two approaches suggests a sequential procedure

Table 7.5: Wide-Band Optimization J_1^{WB}, Aperiodic Modulation, Criterion Values ($\times 10^4$).

Modulation	$D = .1$	$D = 0.5$	$D = 0.9$
Undithered	96.8	1013	96.8
Point Masses	112.0	971	110.0
Hanning	91.4	951	96.1
Rectangles	97.1	929	109.0
β–density	96.1	964	96.6

in spectral shaping: at the first step, a wide–band optimization is performed using a deterministic methodology, and at the second step, optimization of the random modulation is performed to satisfy narrow–band requirements. A conclusion from the numerical experiments described in this section is that random modulation does not influence the wide–band performance significantly, thus suggesting that the wide–band spectral energy distribution optimized at the first step will not be excessively degraded in the second step.

The difference in wide–band performance for different stationary modulation schemes is not very significant. An advantage of aperiodic modulation is the absence of the discrete spectrum for all non–lattice probability distributions. This property is offset by the fact that significant signal energy could be concentrated in very narrow frequency segments. as shown in examples in Appendix B.

7.2.3 Optimization of Signals Specified by Markov Chains

Synthesis problems for random modulation governed by Markov chains will be illustrated on the example from Section 6.2.1. The transition probabilities $p_{1,2}$ from state 1 to state 2, and $p_{2,3}$ from state 2 to state 3 are optimized. while the symmetry of the chain is preserved. Thus the transition matrix is

$$\bar{P} = \begin{bmatrix} p_{1,2} & 1-p_{1,2} & 0 & 0 \\ 0 & 0 & p_{2,3} & 1-p_{2,3} \\ 1-p_{2,3} & p_{2,3} & 0 & 0 \\ 0 & 0 & 1-p_{1,2} & p_{1,2} \end{bmatrix} \tag{7.17}$$

Table 7.6: Narrow-Band Optimization, Markov Chain Example, Criterion Values ($\times 10^4$).

Modulation	Probabilities	J_1^{NB}	J_{41}^{NB}
PWM	Independent, $D_1 = 0.25$, $D_2 = 0.75$	253	613
Standard Markov Chain	$p_{1,2} = .75, p_{2,3} = .5, D_1 = 0.25$, $D_2 = 0.75$	253	613
Optimal Markov Chain	$p_{1,2} = .75, p_{2,3} = .5, D_1 = 0.05$, $D_2 = 0.95$	0	11.5

Table 7.7: Wide-Band Optimization, Markov Chain Example. Criterion Values ($\times 10^4$).

Modulation	Probabilities	J_1^{WB}
PWM	Independent, $D_1 = 0.25$, $D_2 = 0.75$	800
Standard Markov Chain	$p_{1,2} = .75, p_{2,3} = .50, D_1 = 0.25$, $D_2 = 0.75$	806
Optimal Markov Chain	$p_{1,2} = .05, p_{2,3} = .95, D_1 = 0.22$, $D_2 = 0.77$	786

The duty ratios of the short and long pulses are also made variable, with the same average value $D = 0.5$ as in Section 6.2.1. For $D = 0.5$, the optimized narrow-band criteria are shown in Table 7.6. As in the case of independent random modulation, a considerable improvement in criterion value is attained as a consequence of optimization.

On the other hand, switching based on a Markov chain is not particularly effective in reducing wide-band signal energy, as illustrated with the $D = 0.5$ case in Table 7.7. In numerical experiments reported here, as well as in examples with different average duty ratios, the duty ratio variations seem to be most effective in dealing with narrow-band constraints. This fact is expected from the performance analysis of stationary schemes. Also, transition matrix variations have effects mostly on wide-band criteria, but their overall effectiveness is limited. The true importance of the transition matrix optimization is in the time domain, where it influences the ripple.

These results suggest a decomposition of the Markov chain optimization problem into two subproblems. The first subproblem is the transition matrix optimization, and it is concerned mostly with time domain requirements (ripple control), and to a certain extent with the wide-band constraints in the frequency domain. The second subproblem is the optimization of the waveforms at each state, and its primary effects are in satisfying the narrow-band requirements. The proposed decomposition could

significantly improve the tractability of the optimization of Markov chains with many states.

7.3 Summary

The spectral shaping capabilities of random PPM, simplified aperiodic modulation, and modulation based on a Markov chain are explored via examples in this chapter. Two optimization criteria have been formulated, one corresponding to narrow-band spectral requirements, and the other corresponding to wide-band spectral optimization. The domain of optimization $\mathcal{P}$ for stationary modulation schemes comprises probability distributions (both absolutely continuous and discrete) that have finite support in the time domain. A complete parametrization of the set $\mathcal{P}$ in the frequency domain is not available. Partial parametrizations are utilized instead to describe the domain $\mathcal{P}$, and several examples of parametrizations of practical importance are discussed. For modulation based on Markov chains, both a state transition matrix $\bar{P}$ and waveforms associated with each state have to be specified.

The performance of random modulation schemes is illustrated for three different undithered duty ratios, and it is shown that in general a reduction of the support of the probability density used for dithering degrades the attainable performance. A simple bounding procedure based on Parseval's equality is applied to a random PPM example.

It is shown that random modulation is in general very effective in reducing the size of discrete components, thus providing a quantitative basis for widespread applications of random modulation to acoustic noise reduction. Effects at high frequencies are also of interest, since random modulation could offer a simple tool for spectral shaping at frequencies where filtering becomes difficult. On the other hand, random modulation is much less effective in addressing wide-band spectral requirements. Results presented in this chapter provide numerical evidence for suggestions made in the literature [126] that deterministic and random modulation are of complementary nature. A decomposition based on the same principle is proposed for the optimization

of random modulation based on Markov chains, and it should help make the overall synthesis problem more tractable in implementations. Results of this chapter are in an agreement with the choice of switching function as the basic object of study in this thesis. Spectral changes introduced by random modulation are mostly localized in frequency. Thus, if the transfer function to the part of circuit under study is known in the frequency band of interest, then an adequate assessment of effects of random modulation is possible.

Chapter 8

Conclusions and Further Research

8.1 Summary

This thesis addresses spectral properties of randomly modulated pulse trains. Cases of particular interest are related to the operation of power electronic converters. Results on both analysis and synthesis of random pulse trains are presented. Random modulation procedures based on independent and dependent (Markovian) stochastic experiments are studied.

A detailed description of power electronic implementations of random modulation is given in Chapter 2. The number and diversity of such implementations are growing rapidly, with over a dozen reported in 1992 alone. An overview of standards for harmonic distortion is given in Section 2.2. Fourier transforms of switching waveforms are not a proper object to study in a random modulation setup, due to their erratic behavior. Power spectra, defined as the Fourier transforms of the autocorrelation functions of random switching waveforms, have much better limiting properties. In addition, well developed methods are available for estimation of power spectra from switching waveforms of finite duration. Specifications for power converters are designed for a deterministic switching discipline. and a simple way to map these standards to the power spectral domain is suggested in Chapter 2.

The classification of random pulse modulation, given in Chapter 3, provides a systematic arrangement of different schemes proposed in practice, and at the same time

establishes connections with results from statistical communication theory. In Section 3.2, which sets up the basic theoretical framework, the autocorrelation function of a waveform is defined. A stationarization procedure that establishes a correspondence between random switching waveforms and wide-sense stationary signals is also described in Section 3.2. The analytical derivation of power spectral formulas turns out to be somewhat intricate. Monte-Carlo simulation of random switching waveforms, together with spectrum estimation methods, is a way to validate the theoretically derived formulas, and is described in Section 3.3. The role of the Wiener-Khintchine theorem in the verification of analytical formulas is pointed out.

Power spectra of various stationary random modulation schemes are presented in Chapter 4. Results for random pulse width modulation, and for aperiodic, cascaded and alternate modulation, as well as results for random choice of random modulation are described in detail in Appendices A-C. Block-stationary random modulation is analyzed in Chapter 5. An experimental setup used for the verification of analytical expressions for power spectra is described in Appendix D. High frequency switching phenomena are described in Appendix E. The issues arising in a closed-loop spectral control are addressed in Appendix F. Piecewise deterministic processes described in Appendix G are a comprehensive theoretical framework for study of random pulse modulation.

The case where random experiments based on Markov chains are used for modulation is addressed in Chapter 6. A Markov chain scheme applicable to DC/DC converters is described and analyzed in Section 6.2, and an extended scheme for inverters is treated in Section 6.3.

Synthesis problems in random modulation are the topic of Chapter 7, where both optimization criteria and numerical results are described. It is shown that random pulse modulation can be very efficient in reducing the size of discrete harmonics and in satisfying narrow-band constraints, but is much less effective in dealing with wide-band requirements. Some issues arising in dynamical operation of a controller for a power converter employing random modulation are discussed in Appendix F. The class of piecewise deterministic processes includes all random pulse modulation

schemes, and its main features are outlined in Appendix G.

8.2 Suggestions for Future Research

It is hoped that the research documented in this thesis will contribute towards a better understanding of the capabilities of random modulation in power conversion. On the theoretical side, it has supplemented earlier results on random pulse modulation. At the same time, this thesis opens several directions for future research:

- A practical study in a power conversion setup of effects of random modulation on electromagnetic interference is needed, before specific conclusions regarding random modulation effects on input and output filtering can be drawn. The high–frequency effects of switching nonidealities should be quantified carefully, using analytical results presented in this thesis. Some initial results in this direction are presented in Appendix E. Another problem of practical interest in inverter applications is the evaluation of effects of different random modulation schemes on acoustic noise.

- The analysis of deterministic switching schemes that include hysteretic and other nonlinear elements is quite complicated, and numerous approximations have been derived, in both the communication and power electronics literature. The probabilistic descriptions reported in this thesis may offer additional insight, while retaining numerical tractability.

- It will be of interest to explore connections with recent work on randomized signal processing [6].

- The analysis of spectral properties of waveforms that are not related to the switching function through linear transformations requires further attention. Consider, for example, a down converter and random PWM modulation with two duty ratios. In that case the input current in each cycle depends on the inductor current at the end of the preceding pulse and on the choice of duty ratio in the present pulse. This situation can be modeled as a Markov chain that has finitely many states, if additional constraints (e.g on extremal values of the inductor current) are added. Then the results derived for signals generated

by Markov chains are applicable. It is of interest, however, to consider more general examples.

- A new theoretical direction would be the generalization of results for Markov chains to the broader class of semi-Markov chains. In Markov chains, the holding time in each state has an exponential probability density, while in semi-Markov chains holding times are allowed to have more general distributions. The modeling capabilities of semi-Markov chains are closely related to those of Petri nets, which represent another case of theoretical interest [46], [47].

- Synthesis results from Chapter 7 could be extended to the case of richer parametrizations. Computational requirements could quickly become prohibitive, especially in the case of optimization on Markov chains. The nonlinearity of the associated optimization problems leads to a host of interesting numerical questions.

- Results presented in this thesis suggest that random modulation should be combined with deterministic optimization, within a unified design methodology. This would open a large set of new theoretical and empirical questions. Fortunately, the size of the challenge seem to be proportional to benefits that are likely to be achieved in implementations.

- The thesis has focused on the steady-state behavior of power converters. An important issue for future work is whether and how to dynamically regulate the spectral properties of waveforms of interest. The dithering described here has been conceived of as open-loop dithering, but there may well be situations in which dynamic, closed-loop spectral regulation is of interest. Some preliminary ideas on this are outlined in Appendix F.

- The area of piecewise deterministic processes is a theoretical framework that includes random pulse modulation as a special case. Its main properties are outlined in Appendix G, and it may prove useful in future explorations of random pulse modulation in power electronic converters.

Appendix A

Random Pulse Width Modulation

In the case of random pulse width modulation (PWM), the pulse shape $u(\cdot)$ is parametrized by the random variable a_k, which is independent of the WSS process, $w(\cdot)$, being sampled. For random PWM, $\varepsilon_l = 0$, $T_l = T = T_0$, $\xi_l - \xi_0 = lT_0$; see Fig. A.1. After introducing the notation $u(\cdot, a)$ for pulse shape, the same procedure as in the PPM case is followed. The expectation is taken over a as well as over w. Recalling that w and a are independent, the following spectral formula is obtained from the equation (4.19), using the geometric series summation formula and the Poisson identity (as in deriving equation (4.19)) in Section 4.3):

$$\begin{aligned} S_y(f) &= \frac{1}{T_0}[E[|\,U(f,a)\,|^2] - |\,E[U(f,a)]\,|^2 \\ &\quad + \frac{1}{T_0}\,|\,E[U(f,a)]\,|^2 \sum_{k=-\infty}^{\infty} \delta(f - \frac{k}{T_0})]. \end{aligned} \tag{A.1}$$

This formula can be evaluated for cases of interest. For example, assume $a \in (0, \frac{T_0}{2})$, uniform, and that rectangular unit pulses are used. This is used as an example in [86], but the suggested solution contains an unfortunate typographical error. The corrected solution is, with $\beta := \frac{\pi f T_0}{2}$,

$$S_y(f) = \frac{T_0^2}{8\beta^2}[1 - \frac{sin^2(\beta)}{\beta^2} + \frac{sin^4(\beta) + (\beta - sin(\beta)cos(\beta))^2}{\beta^2 T_0} \sum_{k=-\infty}^{\infty} \delta(f - \frac{k}{T_0})] \tag{A.2}$$

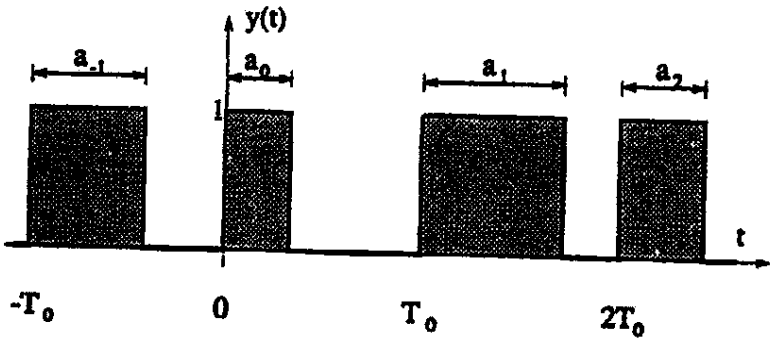


Figure A.1: An Illustration of the Pulse Width Modulation.

The spectrum contains both a continuous and a discrete part, as in the case of random PPM.

Another analytically tractable case, which is used for a comparison with random PPM is $a \in (0, T_0)$, uniform, $T_0 = 1$ and $\alpha = \pi f$:

$$S_y(f) = \frac{1}{4\alpha^2}[1 - \frac{sin^2(\alpha)}{\alpha^2} + \frac{sin^4(\alpha) + (\alpha - sin(\alpha)cos(\alpha))^2}{\alpha^2} \sum_{k=-\infty}^{\infty} \delta(f-k)] \quad (A.3)$$

This example is an illustration only, and in actual operation the pulse width is likely to be more constrained. Conventional switching yields the discrete spectrum given in Fig. A.2. Also shown in in this figure is the discrete spectrum for random PWM. The continuous spectrum for random PWM is given in Fig. A.3.

In Fig. A.4 the shape of the estimated total power spectrum is shown, using 8192 data points (128 cycles, 64 points each). The localized large deviations between the estimated and calculated continuous spectrum are due to the discrete spectral components, since Welch's procedure generates an estimate of the total power spectrum, i.e., of the sum of continuous and discrete spectra. In Fig. A.5 the estimate of the first two harmonics is magnified. From the known width of the frequency segment, $\frac{1}{64}$ for the particular value of M, the value of 0.017 is obtained for the area of the

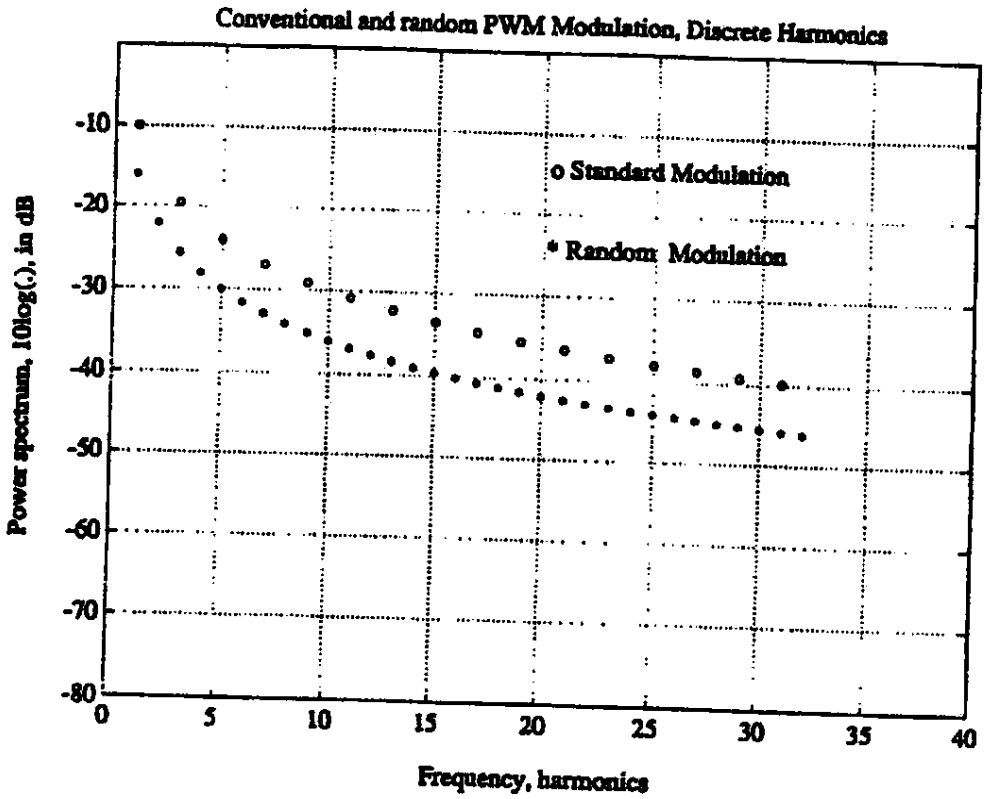


Figure A.2: Discrete Spectrum - Comparison of Conventional and PWM Modulation, Period $T_0 = 1$, Duty Ratio $D = 0.5$, Pulse Width Uniformly $\in [0, T_0]$.

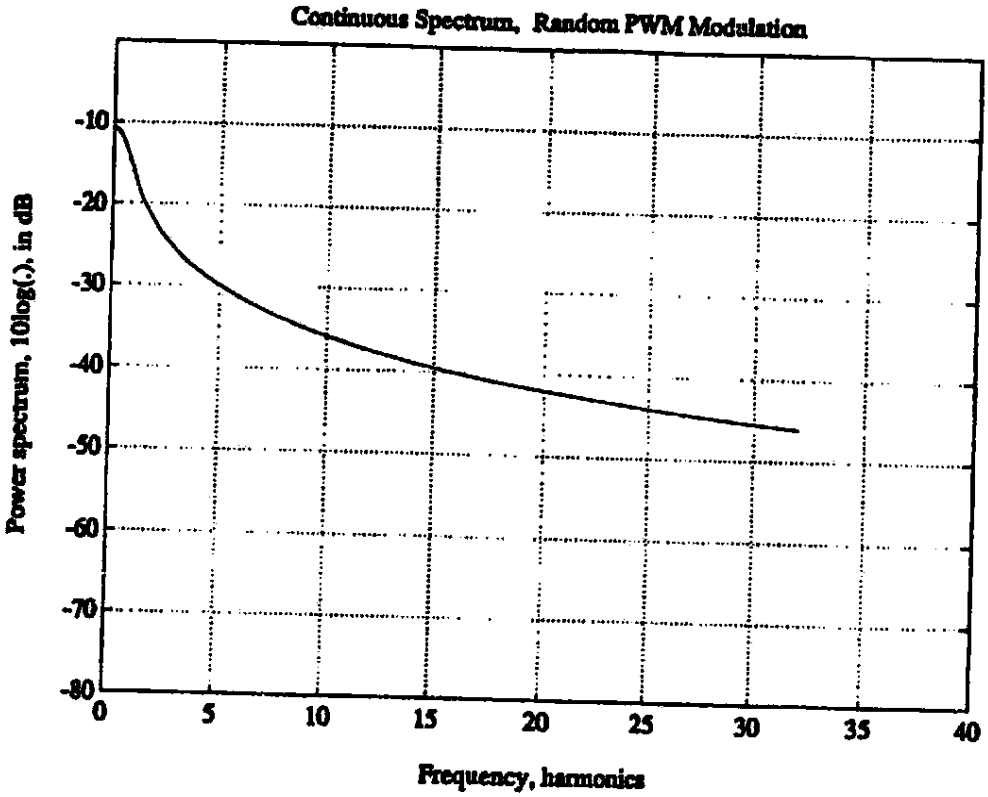


Figure A.3: Continuous Spectrum - Random PWM, Period $T_0 = 1$, Duty Ratio $D = 0.5$, Pulse Width Uniformly $\in [0, T_0]$.

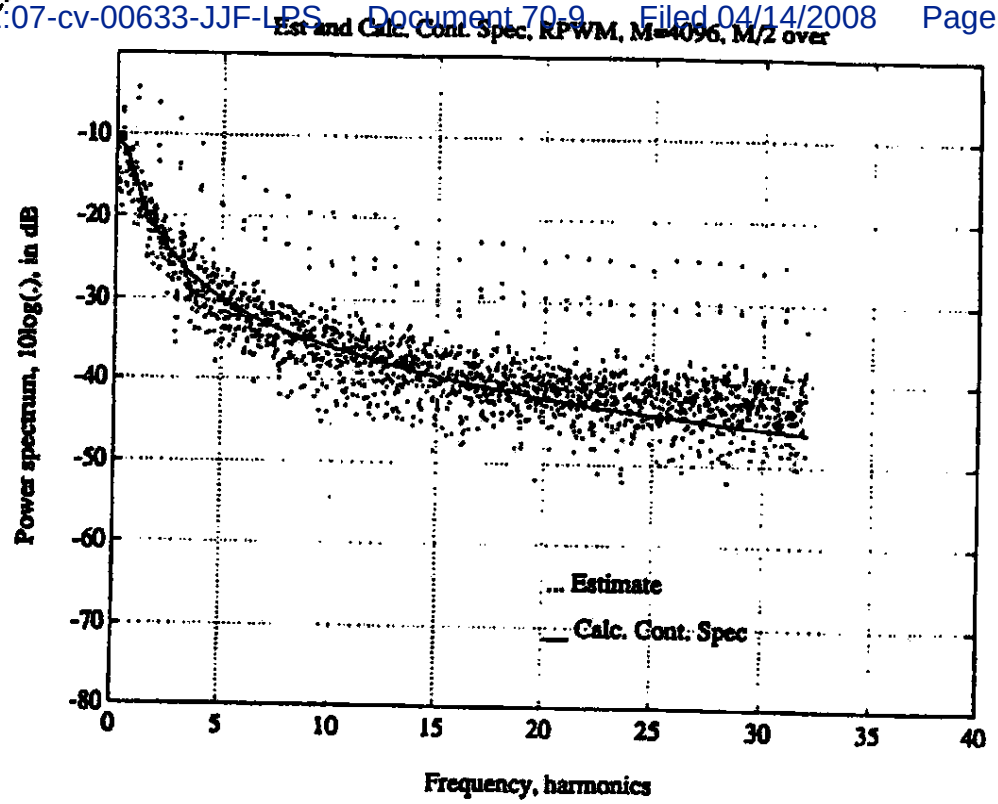


Figure A.4: PWM – Estimated and Calculated Spectrum, Calculated in M=4096 Points, Period $T_0 = 1$, Duty Ratio $D = 0.5$, Pulse Width Uniformly $\in [0, T_0]$.

peak centered at $f = 1$, and 0.005 and 0.005 in both neighboring segments to the left and right. Calculated values for the discrete component at $f = 1$ are 0.0253, and very small for the integrals of the continuous components to the left and to the right. The agreement between calculated and estimated values is acceptable, given the properties of the spectral estimation procedure described in Sectionřefsec:ppm. Figs. A.4–A.5 are obtained by averaging periodograms of only two windowed data segments, 4096 points each. Thus, they are characterized by a high frequency resolution, but the estimates tend to be jittery. In Figs. A.6–A.7 the same quantities are plotted, while averaging 8 data segments, 1024 points each. As expected, the estimates are smoother and follow the theoretical predictions better. The value of 0.018 is obtained for the area of the peak centered at $f = 1$, and 0.006 and 0.006 in both neighboring segments to the left and right. As before, the calculated value for the discrete component at $f = 1$ is 0.0253.

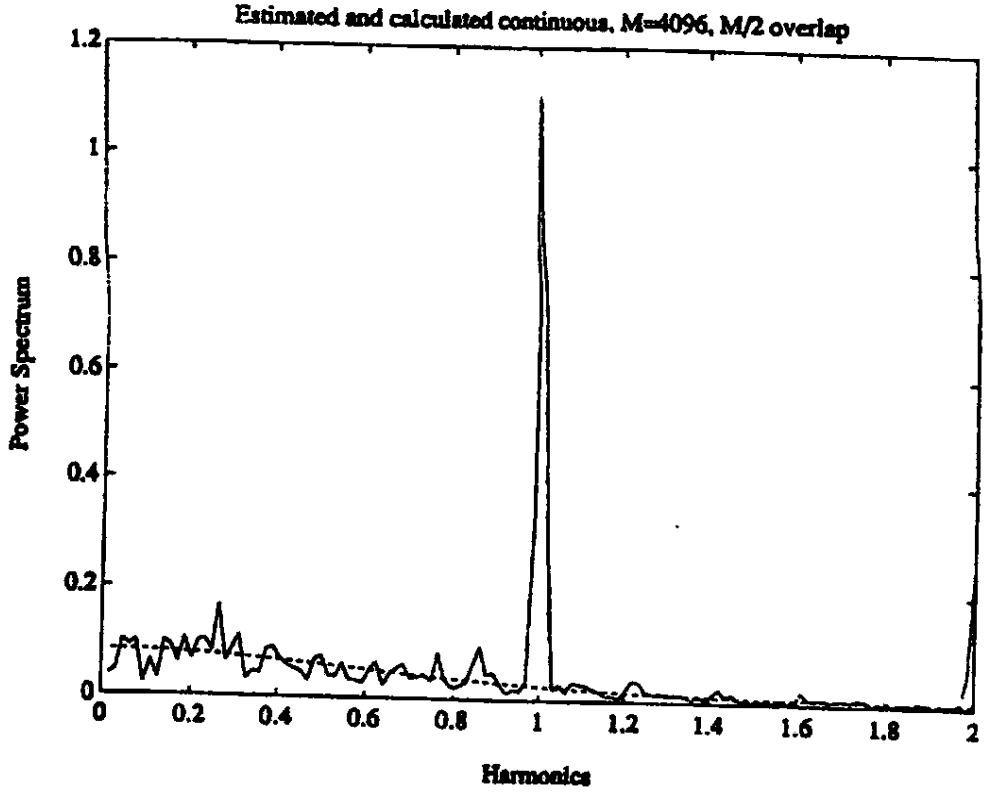


Figure A.5: PWM – Estimated and Calculated Spectrum, First Two Harmonics, Calculated in M=4096 Points, Period $T_0 = 1$, Duty Ratio $D = 0.5$, Pulse Width Uniformly $\in [0, T_0]$.

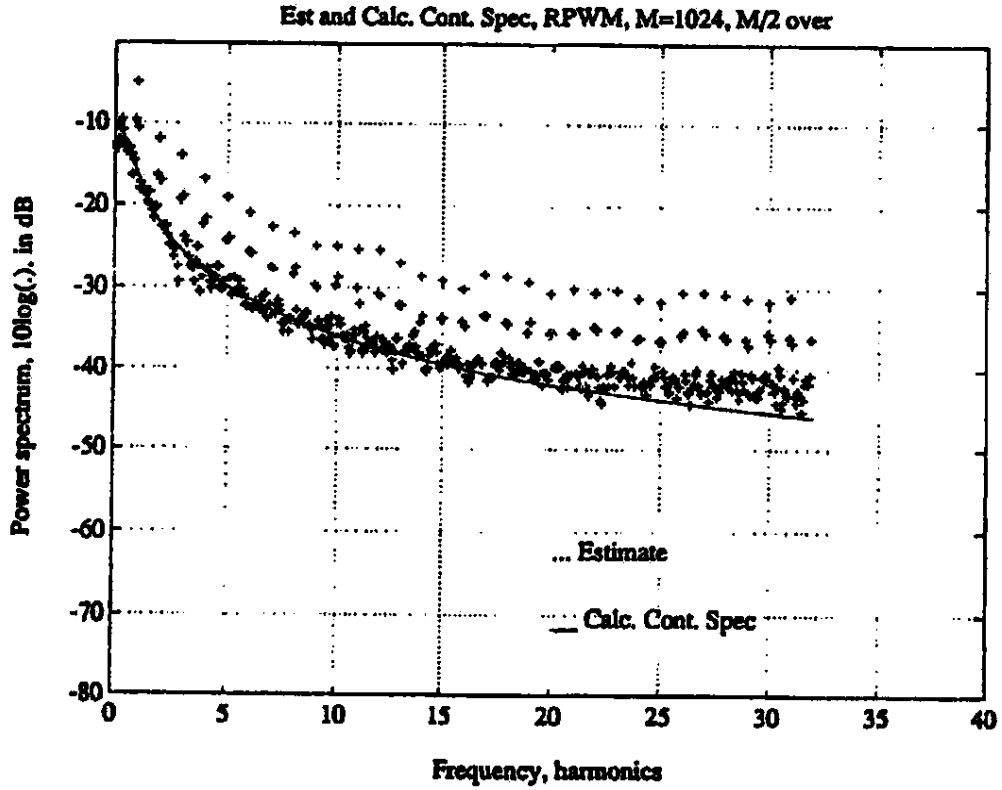


Figure A.6: PWM – Estimated and Calculated Spectrum, Calculated in M=1024 Points, Period $T_0 = 1$, Duty Ratio $D = 0.5$, Pulse Width Uniformly $\in [0, T_0]$.

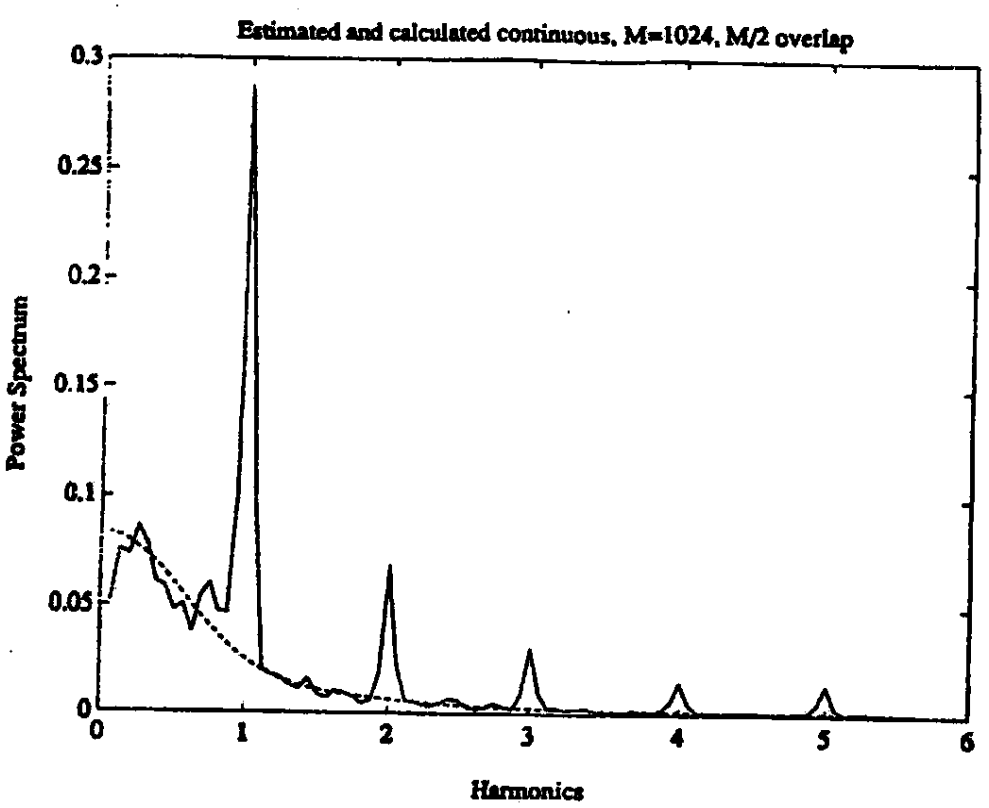


Figure A.7: PWM – Estimated and Calculated Spectrum, First Five Harmonics, Calculated in M=1024 Points, Period $T_0 = 1$, Duty Ratio $D = 0.5$, Pulse Width Uniformly $\in [0, T_0]$.

Appendix B

Aperiodic Modulation Schemes

The goal in this appendix is to study aperiodic non-overlapping random pulse trains, using the result given in Section 4.3, equation (4.19)). The sampling pulse shape u depends now on *two* random variables:

$$u(t, T_n) = u(t - \xi_n, T_n), for\ \xi_n < t < \xi_{n+1} \qquad \text{(B.1)}$$

and zero elsewhere. Thus, ξ_n denotes now the epoch (calculated from the absolute time origin) and T_n parametrizes the pulse shape (it is the cycle duration in cases we consider). For aperiodic random modulation, $\varepsilon_n = 0$. In the case of the aperiodic modulation that is considered in [116], the on–state width is proportional to the cycle length ($a_n = DT_n$, D is the duty ratio). In the case of simplified aperiodic modulation [114], the on–state width a_n is constant.

Denote the mean cycle duration by T, and the Fourier transform of the pulse shape $u(\cdot, \cdot)$ by $U(f, T_i)$. Using the same steps as in previous derivations, it turns out that the expression corresponding to equation (4.19)

$$S_y(f) = \frac{1}{T} \sum_{k=-\infty}^{\infty} E\{w_0 y_k U(f, T_0) U(f, T_k)^* e^{i2\pi f(\xi_2 - \xi_1)}\}_k \qquad \text{(B.2)}$$

where the subscript k denotes separation by k successive cycle lengths.

Assume that w, ξ and T_k are statistically independent from cycle to cycle. This

implies that distinct cycles are statistically independent, which is the most important case in practice. We now make the definitions

$$\alpha(f) = y_m U(f, T_m) e^{i2\pi f T_m}, \tag{B.3}$$

$$\beta(f) = y_{m+k} U(f, T_{m+k}), \tag{B.4}$$

$$\gamma(f) = e^{i2\pi f \tau}, \tag{B.5}$$

in order to factor equation (B.2). In this case (B.2) splits into three parts, two of which are one-sided summations involving conjugates of each other that can be combined to yield the last term in the equation below:

$$S_y(f) = \frac{1}{\bar{a}}\{E(\alpha\beta^*\gamma^*) + 2Re\frac{E(\alpha)E(\beta^*)}{1 - E(\gamma)}\} \tag{B.6}$$

The previous expression can be simplified for cases of interest. This method is applicable to "control circuit II" from [116], in which case $w = 1$, but the sampling is performed with rectangular pulses of width DT, where D is the duty ratio. As an example, consider cycles of length T_i, $D = 0.5$, and T_i is a uniform random variable between 0.5 and 1.5 time units. The length of an on-state within a cycle of length T_i is DT_i. The expected value of $\gamma(f)$ for uniform τ is

$$E[\gamma(f)] = \hat{g}(f) = e^{i2\pi f} sinc(\pi f) \tag{B.7}$$

Also $E[T_i] = 1$, and the spectrum equals

$$S_y(f) = E(\alpha\beta^*\gamma^*) + 2Re\frac{E(\alpha)E(\beta^*)}{1 - E(\gamma)} \tag{B.8}$$

which becomes

$$S_y(f) = \frac{2 - \hat{g}(\frac{f}{2}) - \hat{g}^*(\frac{f}{2})}{(2\pi f)^2} + \frac{2}{(2\pi f)^2} Re\frac{[\hat{g}(f) - \hat{g}(\frac{f}{2})][1 - \hat{g}(\frac{f}{2})]}{1 - \hat{g}(f)} \tag{B.9}$$

This result is believed to be novel.

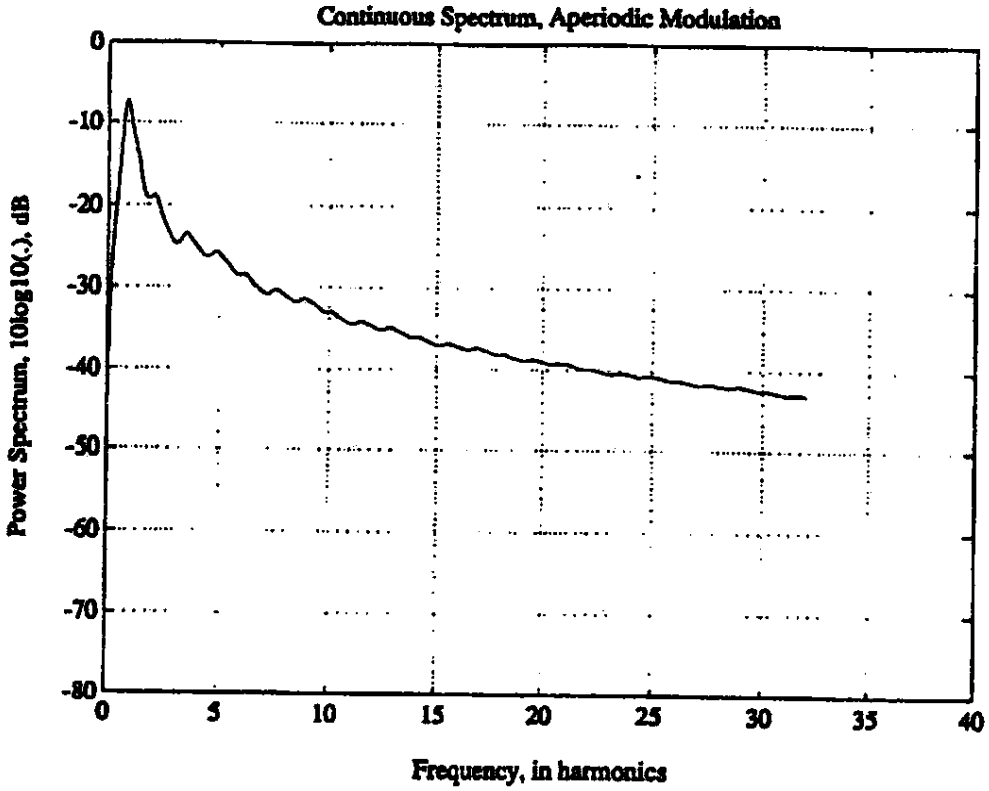


Figure B.1: Continuous Spectrum - Aperiodic Modulation $\tau \in [0.5\ 1.5]$, Uniform, $D = .5$

Observe the "frequency folding", in the sense that $S_v(f)$ depends on $\hat{g}(\cdot)$ at different frequencies. Fig. B.1 shows the corresponding power spectrum . The absence of the discrete part and the fairly complicated shape between the first and fifth harmonic are apparent. It is assumed that $|\hat{g}(f)| < 1$. which is guaranteed, except in cases when $\hat{g}$ is a Fourier transform of a lattice distribution [33]. A lattice probability density function consists of point masses at $0, h, -h, 2h, -2h \cdots$. The case of lattice distributions can be treated using the apparatus from Section 6.2.3, based on [130], as shown in Chapter 7.

This example is difficult to analyze by other methods, due to the absence of a periodic structure, and the fact that the modulating waveform does *not* represent the response of a linear system to a train of independently dithered impulses. In Fig. B.2 overall shapes of the estimated and calculated spectrum are compared, and in Fig. B.3 the first 4 harmonics are shown. The estimates are jittery, as expected after dividing the data set into only two segments of 4096 points each, but follow the theoretical

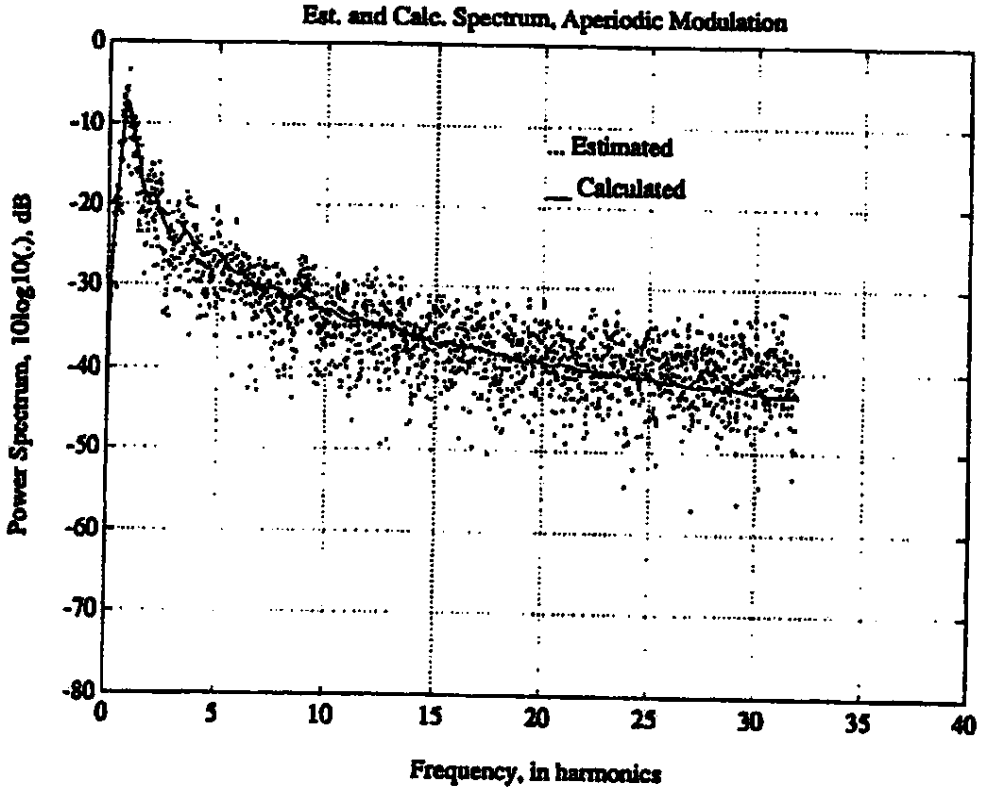


Figure B.2: Spectral Estimate for Aperiodic Modulation, Calculated in M=4096 Points, $\tau \in [0.5\ 1.5]$, Uniform, $D = .5$.

prediction. The agreement is even better if the available data set is divided into eight segments, whose periodograms are averaged, as shown in Fig. B.4.

The preceding spectral formula will now be derived using a different route. The main tool is a result of [77], describing the power spectrum of a randomly dithered impulse train. An easy corollary of this derivation is the power spectral formula for the case described in [114], where an impulse train with statistically independent time increments is *convolved* with a rectangular pulse. Assume that the intervals between impulses T_i are generated by a sequence of independent trials, using a probability density function $p(\cdot)$, whose Fourier transform is denoted with $P(f)$, and that the pulse width is a known constant a. This is the case we have labeled as simplified aperiodic modulation. Then, the power spectrum of the pulse train is given by

$$S_v(f) = \left(\frac{sin(\pi f a)}{\pi f}\right)^2 \left[1 + 2Re\left(\frac{P(f)}{1 - P(f)}\right)\right] \qquad \text{(B.10)}$$

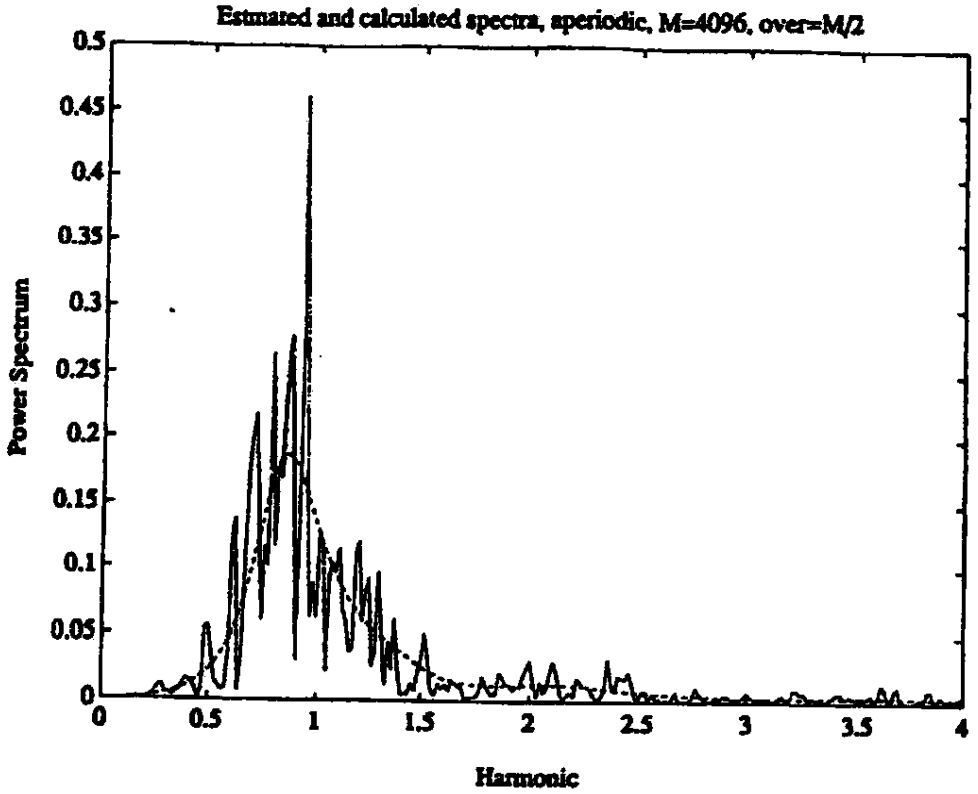


Figure B.3: Spectral Estimate for Aperiodic Modulation, First 4 Harmonics, Calculated in M=4096 Points, $\tau \in [0.5\ 1.5]$, Uniform, $D = .5$.

The case of T_i being uniform between [1, 1.5], and the pulse width being 0.5 is illustrated in Fig. B.5. The formula (B.10) is verified using the Welch's estimation procedure described before, and the spectra are compared in Fig. B.6.

The "Control Circuit II" from [116] is different from the previous scheme, since the switching waveform of interest cannot be generated by a convolution of an independent increment impulse train with a linear time–invariant filter impulse response. For a complete analysis, two *correlated* impulse trains (turn–on and turn–off instants) have to be considered, as shown in the sequel.

The switching function corresponding to the "Control Circuit II" [116] can be generated by convolving the impulse train shown in Fig. B.7 with a step function. Assume again that intervals T_i are generated by a sequence of independent trials using a probability density function whose Fourier transform is denoted by $P(f)$. The Fourier transform of the random variable DT_i (D being a known constant) is found to be $P(Df)$.

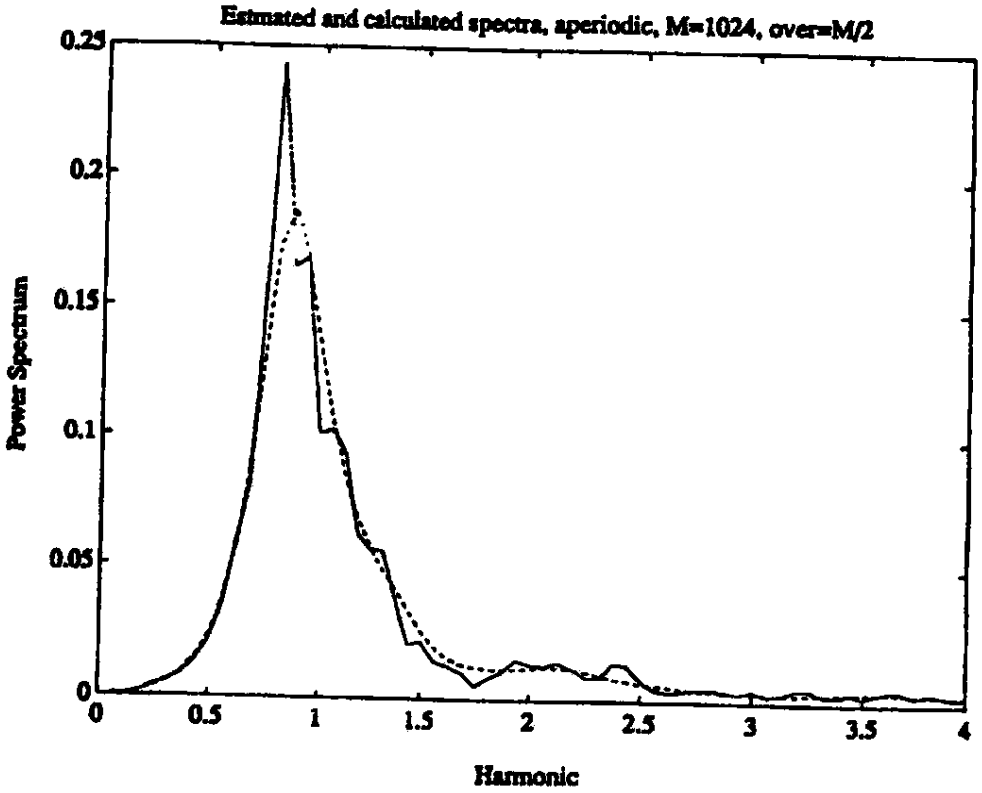


Figure B.4: Spectral Estimate for Aperiodic Modulation, First 4 Harmonics, Calculated in M=1024 Points, $\tau \in [0.5\ 1.5]$, Uniform, $D = .5$.

In calculating the crosscorrelations and the autocorrelation of the negative pulse train care should be exercised to consider sums of *independent* random variables should be considered. The formula for the spectrum of a positive impulse train, which is an independent–increment process. is given in [77]:

$$S_{y++}(f) = 1 + 2Re(\frac{P(f)}{1 - P(f)}) \tag{B.11}$$

In the standard example T_i is uniform between 0.5 and 1.5, so in terms of the old notation,

$$P(f) = e^{-i2\pi f} sinc(\pi f) = \hat{g}(f)^* \tag{B.12}$$

The final result for the pulse train in the example is

$$S_y(f) = S_{y++} + S_{y--} - S_{y+-} - S_{y-+} = \frac{1}{(2\pi f)^2}[1 + 2Re(\frac{P(f)}{1 - P(f)})$$

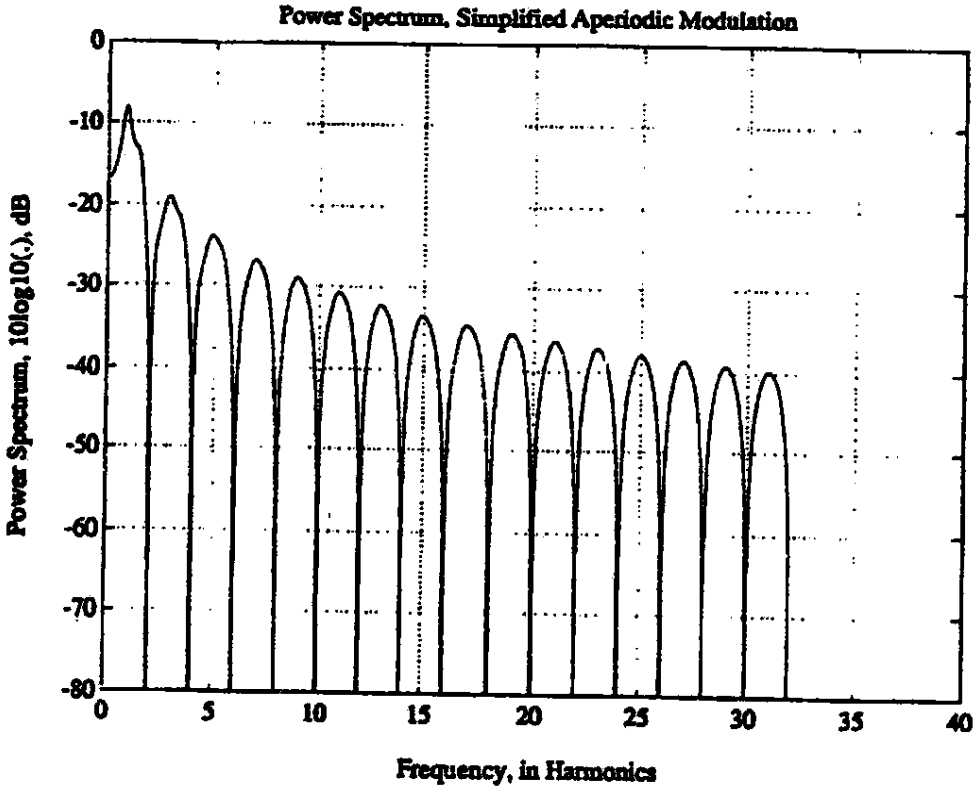


Figure B.5: Continuous Spectrum for the Simplified Aperiodic Modulation $T_i \in [0.5\ 1.5]$, Uniform, On–pulse 0.5.

$$+1 + 2Re(\frac{P^2(\frac{f}{2})}{1-P(f)}) - 2(2Re(\frac{P(\frac{f}{2})}{1-P(f)}))| \qquad \text{(B.13)}$$

This result equals the formula (B.9), which was derived using a different approach.

The difference in power spectra between the switching schemes presented in [114] and [116] is in general *not* negligible, as illustrated in Fig. B.8. Effects related to the turn–off instants in [116] cannot be analyzed properly using the single impulse train approach from [114].

As a final case, consider a switching strategy that depends on *three* random variables *in each cycle*. This random pulse modulation scheme is denoted as cascaded random modulation. The following results are also believed to be new.

In the previously described aperiodic modulation example, let the beginning of the on-part of the i–th pulse be displaced by ε_i, where ε_i is independent of τ_i and uniform between $[0, 0.25]$. Thus, a PPM is being superimposed over an aperiodic

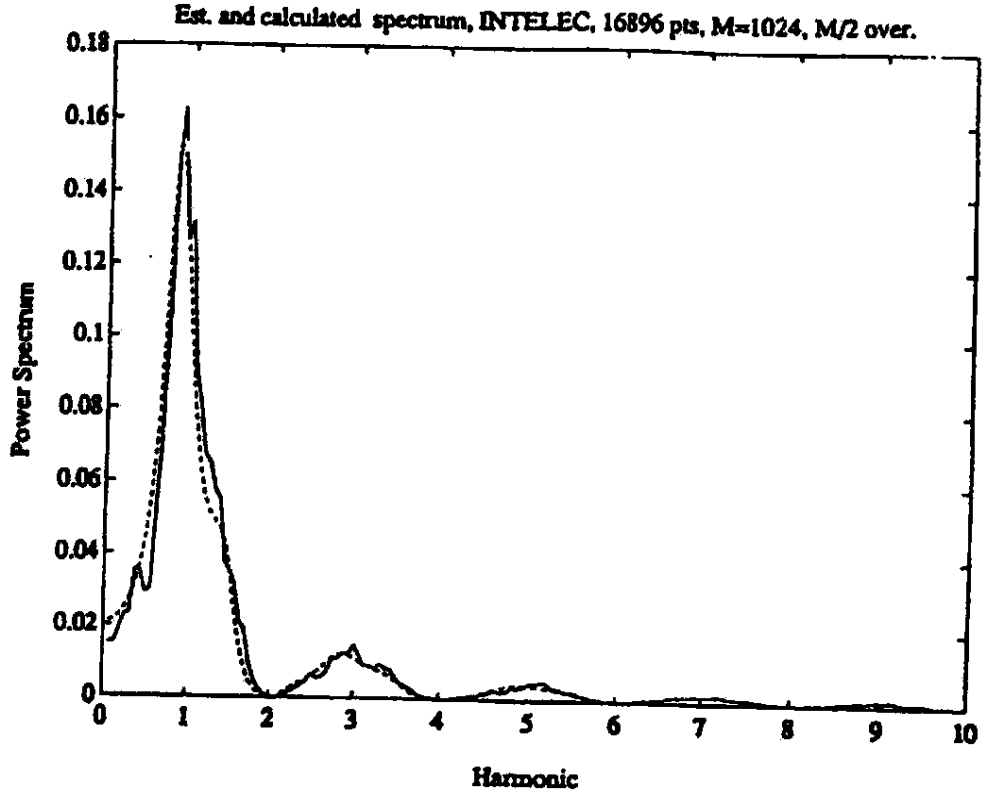


Figure B.6: Simplified Aperiodic Modulation Estimate, Calculated in M=1024 Points, $T_i \in [0.5\ 1.5]$, Uniform, On-pulse 0.5.

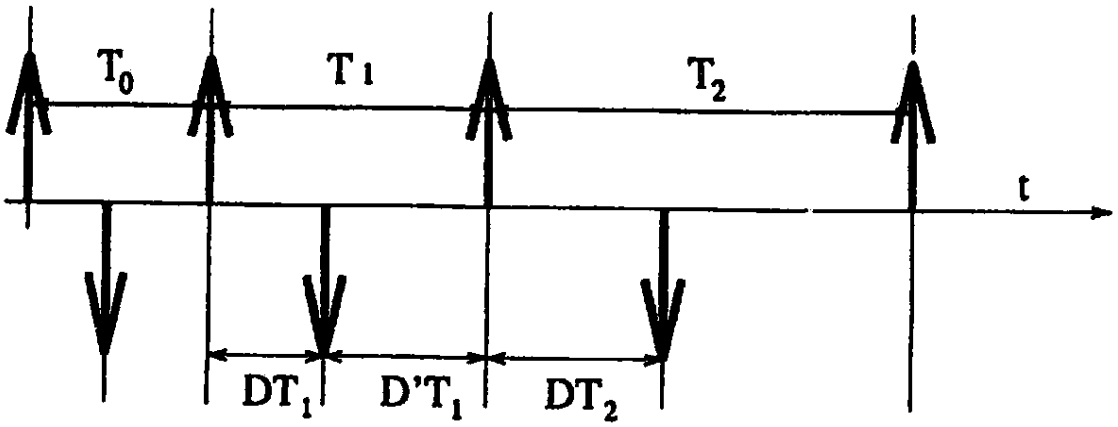


Figure B.7: Impulse Train for Control Circuit II.

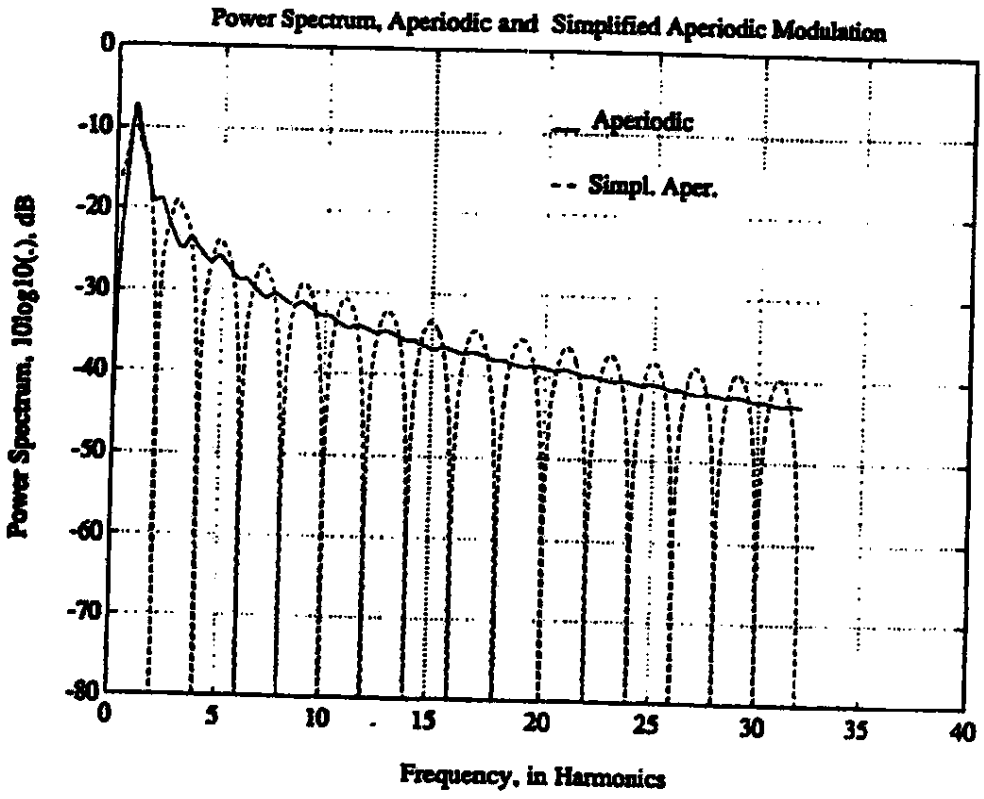


Figure B.8: Power Spectra for Aperiodic Modulation and Simplified Aperiodic Modulation; Aperiodic Modulation $\tau \in [0.5\ 1.5]$, Uniform, $D = .5$; Simplified Aperiodic Modulation with $T_i \in [0.5\ 1.5]$, Uniform, On–pulse 0.5.

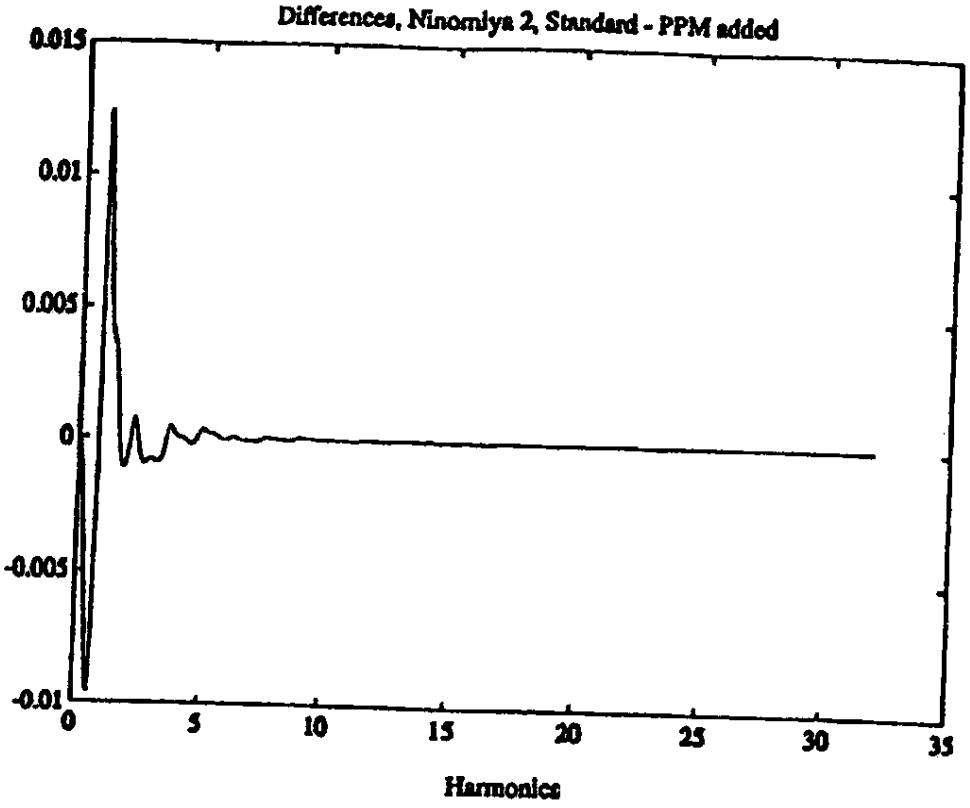


Figure B.9: Differences Between Aperiodic and Aperiodic+PPM Modulation; Aperiodic Modulation $\tau \in [0.5\ 1.5]$, Uniform, $D = .5$; PPM Uniform $\varepsilon \in [0.\ 0.25]$.

modulation, and the overall scheme is denoted as the *cascaded* modulation. Let

$$\hat{h}(f) = E_\varepsilon(e^{i2\pi f\varepsilon}) = e^{i\frac{\pi f}{4}} sinc(\frac{\pi f}{4}) \tag{B.14}$$

Then

$$S_y(f) = \frac{2 - \hat{g}(\frac{f}{2}) - \hat{g}^*(\frac{f}{2})}{(2\pi f)^2} + \frac{2}{(2\pi f)^2} Re\frac{[\hat{g}(f) - \hat{g}(\frac{f}{2})]\hat{h}^*(f)[1 - \hat{g}(\frac{f}{2})]\hat{h}(f)}{1 - \hat{g}(f)} \tag{B.15}$$

Interestingly enough, the resulting spectrum is barely distinguishable from the standard aperiodic switching given in Fig. B.1. The *difference* of the two spectra are shown in Fig. B.9. The spectrum at the lowest frequencies is slightly higher in the cascaded modulation scheme. Evidently the cascaded random modulation is a nonlinear operation and the effects of two combined modulation schemes are *not* predictable by superposition.

The formula for the power spectrum could be derived using a different route. The

effects of an *independent* PPM added to a pulse amplitude modulated pulse train can be observed in equation (4.11), repeated here for convenience:

$$S_y(f) = \frac{|\,U(f)\,|^2}{T_0} \sum_{l=-\infty}^{\infty} E[w_0 w_l] e^{i2\pi f l T_0} \tag{B.16}$$

When a random PPM is added,

$$S_y(f) = \frac{|\,U(f)\,|^2}{T_0} \sum_{l=-\infty}^{\infty} E[w_0 w_l e^{i2\pi f(\epsilon_l - \epsilon_0)}] e^{i2\pi f l T_0} \tag{B.17}$$

Since w and ϵ are assumed independent, the expectation can be factored, and, after adding and subtracting the appropriate term, the PPM formula could be recovered:

$$S_y(f) = \frac{1}{T_0}[|\,U(f)\,|^2 - |\,U(f)P_\epsilon(f)\,|^2 + |\,U(f)P_\epsilon(f)\,|^2 \sum_{l=-\infty}^{\infty} e^{i2\pi f l T_0} \tag{B.18}$$

where $P_\epsilon(f)$ is the Fourier transform of the probability density for ϵ (the characteristic function for ϵ, in probabilistic terms). An application of the Poisson identity yields the PPM formula from Chapter 4:

$$S_y(f) = \frac{1}{T_0}[|\,U(f)\,|^2 - |\,U(f)P_\epsilon(f)\,|^2 + \frac{|\,U(f)P_\epsilon(f)\,|^2}{T_0} \sum_{l=-\infty}^{\infty} \delta(f - \frac{l}{T_0}) \tag{B.19}$$

For distinct pulses, an addition of independent PPM is thus equivalent to $U(f) - U(f)P_\epsilon(f)$. This approach is now applied to aperiodic modulation with PPM added. An important observation is that the + and − impulse within the same cycle are *not* independent, since they are being dithered by the same amount. Formula (B.11) is again used to calculate the autocorrelations and crosscorrelations of the impulse trains, and the following formula for the power spectrum is obtained:

$$\begin{aligned} S_y(f) \;=\; & |\,\frac{Q(f)}{2\pi f}\,|^2 \,[2Re(\frac{P(f)}{1-P(f)}) + 2Re(\frac{P^2(\frac{f}{2})}{1-P(f)}) \\ & -2Re(\frac{P(\frac{f}{2})}{1-P(f)}) - Re(\frac{P(f)P(\frac{f}{2})}{1-P(f)}] + (\frac{1}{2\pi f})^2[2 - 2Re(P(\frac{f}{2}))] \end{aligned} \tag{B.20}$$

which gives the same numerical results as (B.15)

Appendix C

Alternate Modulation and Random Choice of Random Modulation

Consider the case of a pulse train in which we alternate between two different modulation schemes from cycle to cycle. For example, let the first cycle in a pair be a standard pulse of length T_0 and duty ratio D, and let the second cycle be an aperiodically modulated pulse. This scheme is classified as *alternate* modulation. Let P_σ denote the characteristic function for the random variable $T_0 + \tau$, where τ is the random pulse length in the aperiodic modulation.Let U_1 and U_2 denote the Fourier transforms of non–dithered pulses for two consecutive cycles. The standard approach from Chapter 4 is followed, and the main additional difficulty is the need to add terms corresponding to the two classes of alternating pulses in (4.19). It can be shown that the power spectrum of the alternately modulated pulse train is:

$$\begin{aligned} S_y(f) &= U_1 U_1^*(1 + 2Re(\frac{P_\sigma}{1-P_\sigma}) + E[U_1 U_2^*] \\ &\quad +2Re(\frac{E[U_2 e^{i2\pi f\tau}]E[U_2^*]e^{i2\pi f T_0}}{1-P_\sigma}) + 2Re(\frac{U_1 E[U_2^*]}{1-P_\sigma}) \\ &\quad +2Re(\frac{U_1^* E[U_2 e^{i2\pi f\tau}]}{1-P_\sigma}) \end{aligned} \qquad (C.1)$$

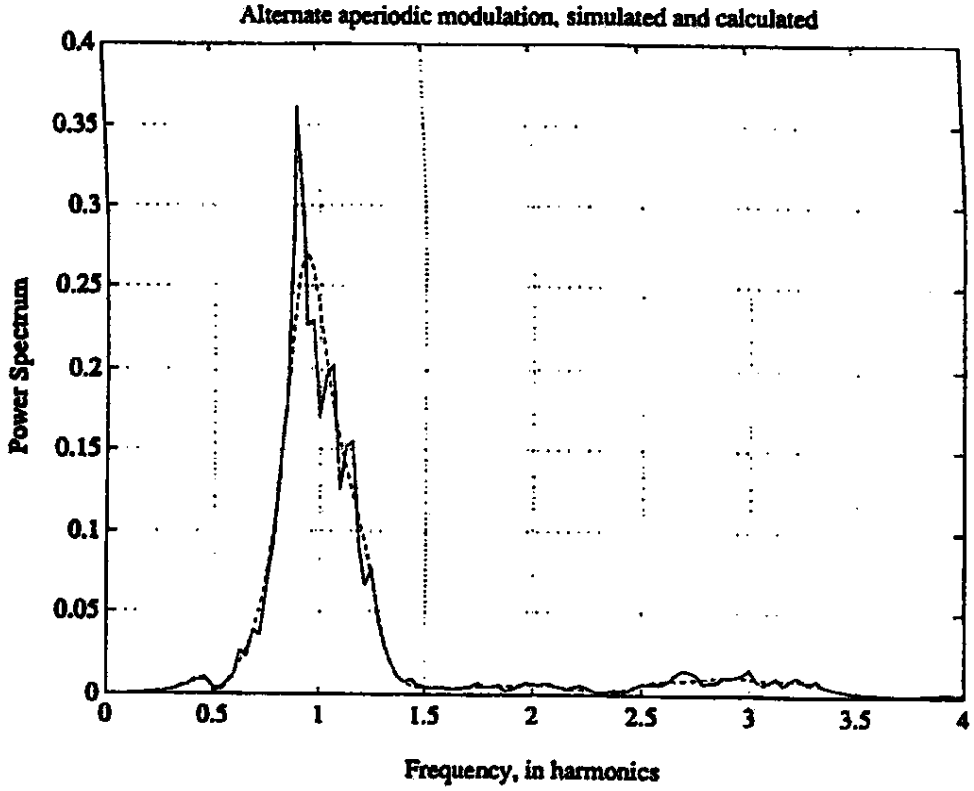


Figure C.1: Simulated and Calculated Spectrum, Alternate Modulation; Standard Pulse $T_0 = 1$, Duty Ratio $D = 0.5$; Aperiodic Modulation $\tau \in [0.5\ 1.5]$, Duty Ratio $D = 0.5$.

Verification results for the preceding formula are given in Fig. C.1, for the standard example (aperiodic modulation with pulse lengths $\in [.5T_0,\ \ 1.5T_0]$, duty ratio .5, $T_0 = 1$).

As a more complicated example. if the pulses in the first cycle of each pair are randomly modulated with PPM and the second is aperiodically modulated, the spectrum is

$$S_y(f) = 2Re\left(\frac{E[U_1 e^{-i2\pi f\tau}]^* E[U_2 e^{i2\pi f\tau}]}{1 - P_\sigma}\right) + 2Re\left(\frac{E[U_1 e^{-i2\pi f\tau}] E[U_2 e^{i2\pi f\tau}]^*}{1 - P_\sigma^*}\right) \quad (C.2)$$

Verification results for the formula (C.2) are given in Fig. C.2, again for the standard example (PPM dither $\in [0\ \ .5T_0]$, aperiodic modulation with pulse lengths

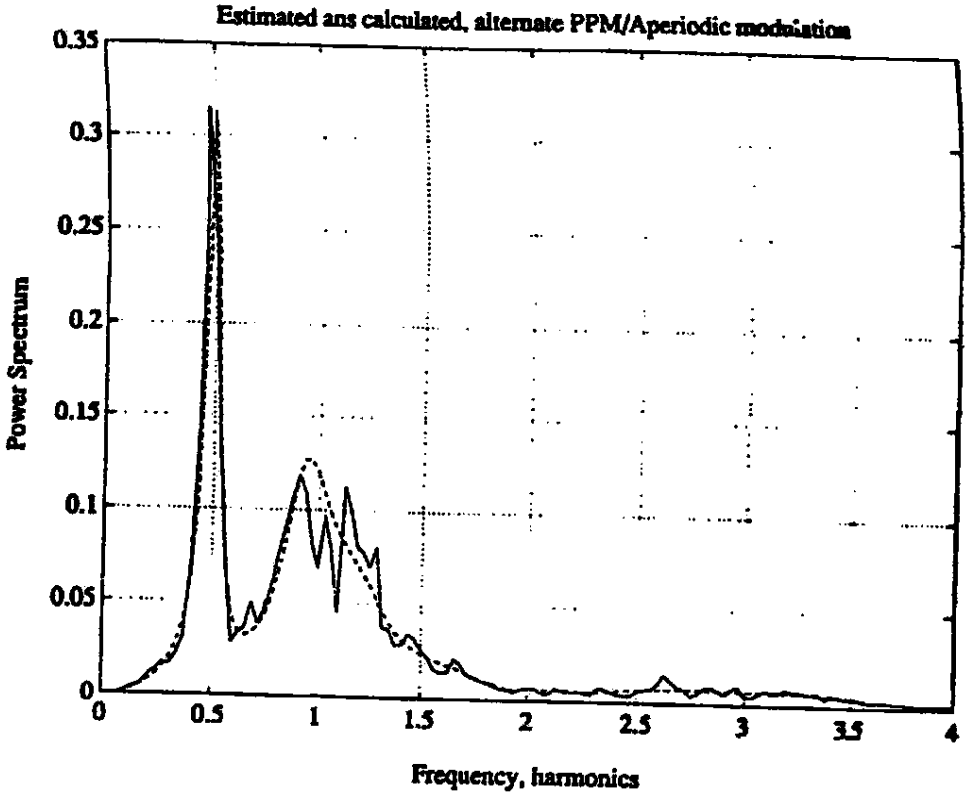


Figure C.2: Simulated and Calculated Spectrum, Alternate Modulation. PPM and Aperiodic Modulation; PPM Uniform $\varepsilon \in [0,\ 0.5]$, Duty Ratio $D = 0.5$; Aperiodic Modulation $\tau \in [0.5\ 1.5]$, Duty Ratio $D = 0.5$.

$\in [.5T_0,\ 1.5T_0]$, duty ratio .5).

The case of a *random choice of random modulation* is considered next. At each cycle, a random choice between random PPM and aperiodic modulation is made, with probabilities p and $q = 1 - p$, respectively. (Other random modulation schemes can be combined using the same approach.) After a choice of modulation is made, another independent experiment is performed to get a value for the associated random parameter(s) (pulse position, or pulse length). The resulting formula for the power spectrum is

$$S_y(f) = E[|\,U(f,\tau,\varepsilon)e^{i2\pi f(\tau-\varepsilon)}\,|^2] + 2Re\left(\frac{E[U(f,\tau,\varepsilon)e^{i2\pi f(\tau-\varepsilon)}]E[U^*(f,\tau,\varepsilon)e^{i2\pi f\varepsilon}]^*}{1-P_\tau^*}\right) \qquad (C.3)$$

where

$$U_1 = \frac{1 - e^{-i2\pi f \frac{T_0}{2}}}{2i\pi f} \tag{C.4}$$

$$U_2 = \frac{1 - e^{-i2\pi f \frac{\tau}{2}}}{2i\pi f} \tag{C.5}$$

$$E[|\, U(f,\tau,\varepsilon)e^{i2\pi f(\tau-\epsilon)}\,|^2] = pE_\varepsilon[|\, U_1\,|^2] + qE_\tau[|\, U_2\,|^2] \tag{C.6}$$

Let

$$P_\tau = E[e^{-i2\pi f\tau}] \tag{C.7}$$

$$P_\varepsilon = E[e^{-i2\pi f\varepsilon}] \tag{C.8}$$

then

$$E[U(f,\tau,\varepsilon)e^{i2\pi f(\tau-\epsilon)}] = pU_1 e^{i2\pi fT_0} P_\varepsilon(f) + q\frac{P_\tau^*(f) - P_\tau^*(\frac{f}{2})}{2i\pi f} \tag{C.9}$$

$$E[U(f,\tau,\varepsilon)e^{i2\pi f\epsilon}] = pU_1^* P_\varepsilon^*(f) + qE[U_2] \tag{C.10}$$

Verification results for the formula (C.3) are given in Fig. C.3, again for the standard PPM and aperiodic modulation example, with $p = q = 0.5$.

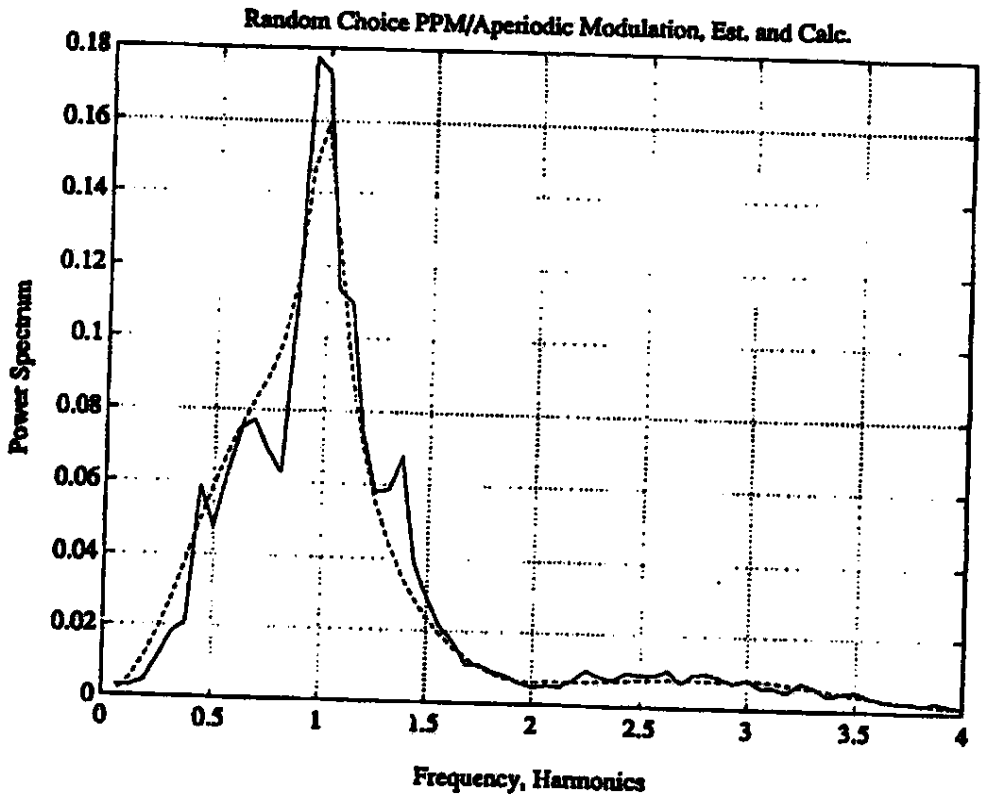


Figure C.3: Simulated and Calculated Spectrum, Random Choice of Random Modulation, Equally Probable Choice Between PPM and Aperiodic Modulation; PPM Uniform $\varepsilon \in [0,\ 0.5]$, Duty Ratio $D = 0.5$; Aperiodic Modulation $\tau \in [0.5\ 1.5]$, Duty Ratio $D = 0.5$.

Appendix D

Experimental Setup

This appendix contains a description of an experimental setup for verification of power spectral formulas for random modulation. The system was designed and built by D.J. Perreault, at MIT Laboratory for Electromagnetic and Electronic Systems.

The block–stationary (inverter) modulation scheme described in Chapter 5 has been verified with the circuit shown in Fig. D.1, with a fundamental switching frequency of 250 Hz. Spectral formulas for other random modulation schemes, described in Chapter 6 and in Appendix A, have been verified with the down converter circuit shown in Fig. D.2. The fundamental switching frequency in this circuit is 10 kHz. In both circuits, the switching of the transistor is controlled by a microprocessor, which is in turn connected to a personal computer. The main role of the personal computer is to facilitate development of the microcode for random switching. A block diagram of the experimental system is shown in Fig. D.3.

D.1 Block–Stationary Random Modulation Example

In the verification of the power spectral formula for the block–stationary random modulation example, described in Chapter 5. Figs. 5.4 and 5.5, the continuous part of the spectrum is clearly visible. This is a consequence of the relatively wide fre-

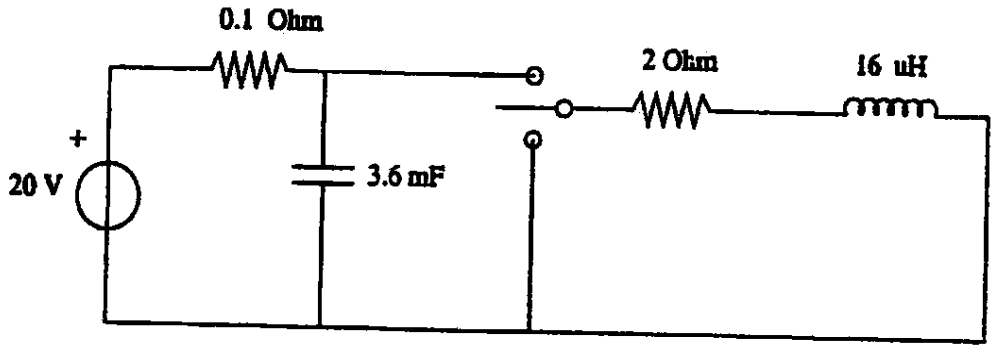


Figure D.1: Inverter Circuit Used in Verification of Power Spectral Formulas in Block Stationary Modulation.

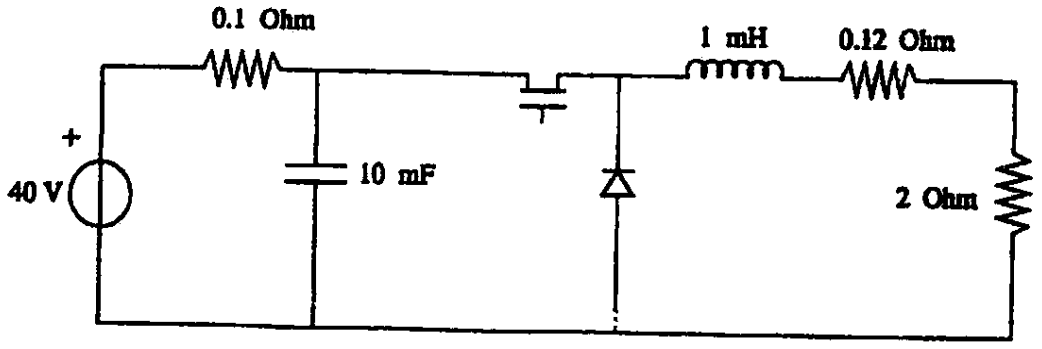


Figure D.2: Down Converter Used in Verification of Power Spectral Formulas for Stationary and Markov Modulation.

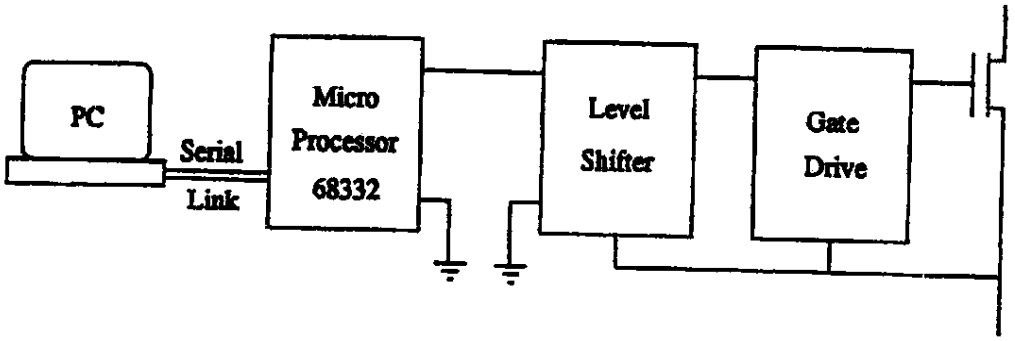


Figure D.3: Block Diagram of the Experimental Setup for Verification of Power Spectral Formulas in Random Modulation.

quency windows corresponding to each estimated or measured point ($\frac{1}{8}$ and $\frac{1}{5}$ of the switching frequency, respectively). If the windows are made narrower, the signal power contributed by the continuous spectrum (which is the integral of the continuous spectral component) will decrease, while the discrete harmonics remain the same, as illustrated in Figs. D.4 and D.5 with frequency windows $\frac{1}{64}$ and $\frac{1}{42}$, respectively.

Thus, if the number of estimated or measured points per unit frequency in the spectrum is increased, then the continuous part of the spectrum becomes less visible. This might explain the remarks made in some references where drastic reductions of discrete harmonics (compared to conventional switching) were observed, when random modulation was applied, but the "filling in" of the continuous spectrum was not noticed.

D.2 Example of Random Modulation Based on a Markov Chain

A verification of the Markov chain example considered in Section 6.2.1 is presented next. If, in the standard four-state Markov chain, the transition probabilities are

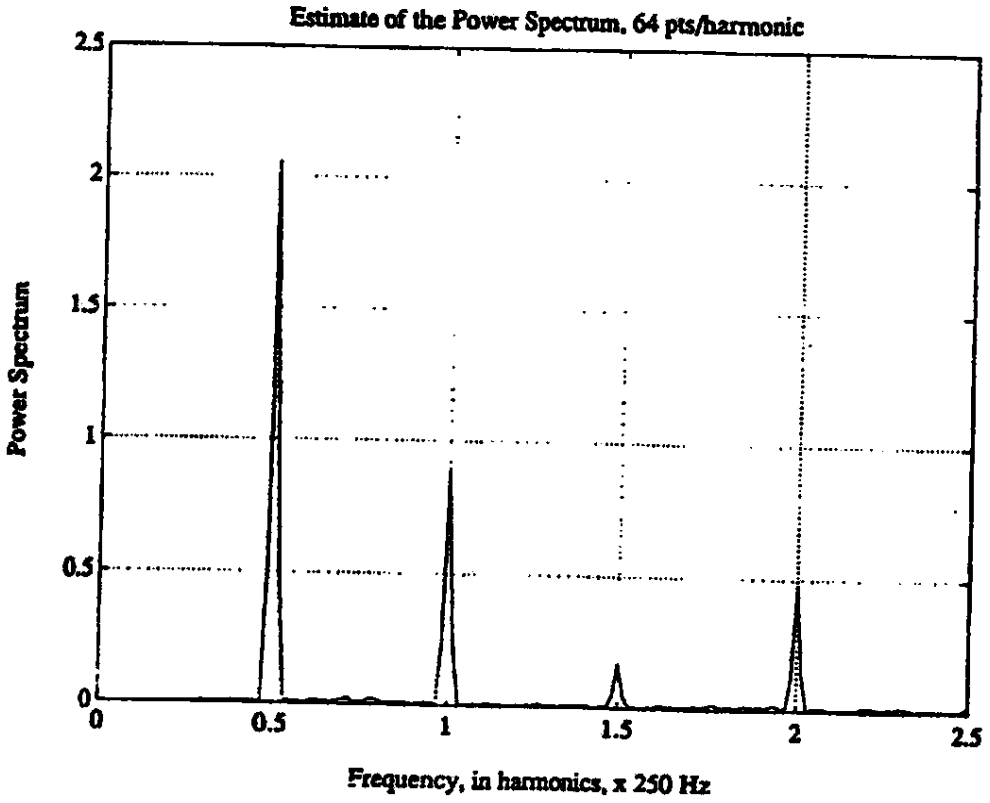


Figure D.4: Estimated Spectrum in the Example of Block–Stationary Random Modulation, Narrow Frequency Segments.

altered. so that $q_{12} = q_{43} = 1$, $q_{11} = q_{44} = 0$, then sequences of three or more pulses of the same kind (long or short) are prevented from occurring. The corresponding calculated power spectrum is shown in Fig. D.6, and the experimentally measured power spectrum is shown in Fig. D.7.

D.3 Time–Domain Performance of Markov Random Modulation

The time–domain performance of both stationary and Markov random modulation is verified in a sequence of four experiments. using the circuit shown in Fig. D.2. The horizontal axis in Figs. D.8 and D.9 is the inductor current ripple (1 A/div), and the vertical axis is the capacitor voltage ripple (0.5 V/div). The exposure time was set to $\frac{1}{4}$ seconds, which (with the switching frequency of 10 kHz) corresponds to approximately 2500 pulses being traced on the screen. In Fig. D.8 the results of

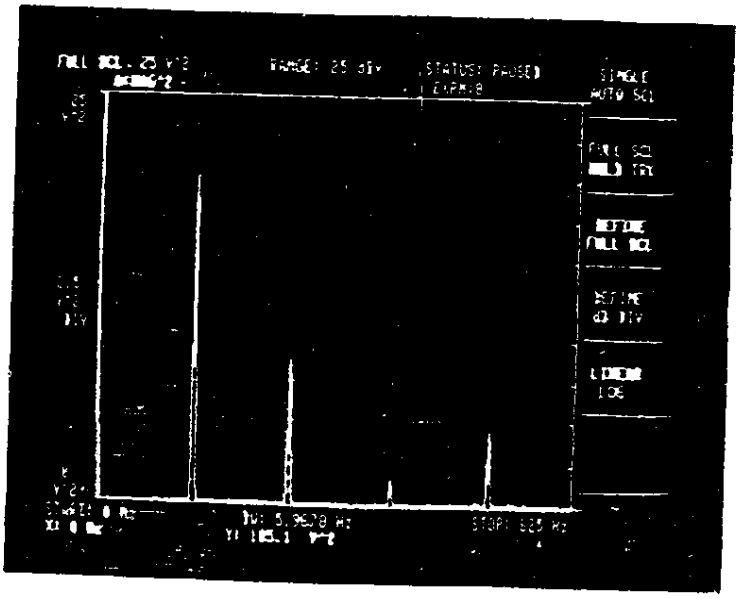


Figure D.5: Measured Spectrum in the Example of Block-Stationary Random Modulation, Narrow Frequency Segments.

conventional switching with the duty ratio $D = 0.5$ is shown. The time waveform obtained when the modulation process is a random choice between $D = \frac{1}{4}$ and $D = \frac{3}{4}$, corresponding to the last example in Appendix A. is shown in Fig. D.9. A sequence of five pulses in succession with $D = \frac{3}{4}$ would account for a current ripple that extends approximately 4.5 divisions to the right of the coordinate origin. Markov modulation is expected to reduce the ripple. and that is indeed the case. We have marked in Fig. D.9 the inductor current ripple obtained with the four-state Markov chain from Chapter 6. (The capacitor voltage ripple is not greatly affected.) The current ripple can be further reduced if the modified Markov chain described in the previous section of this appendix is used, as also marked in Fig. D.9.

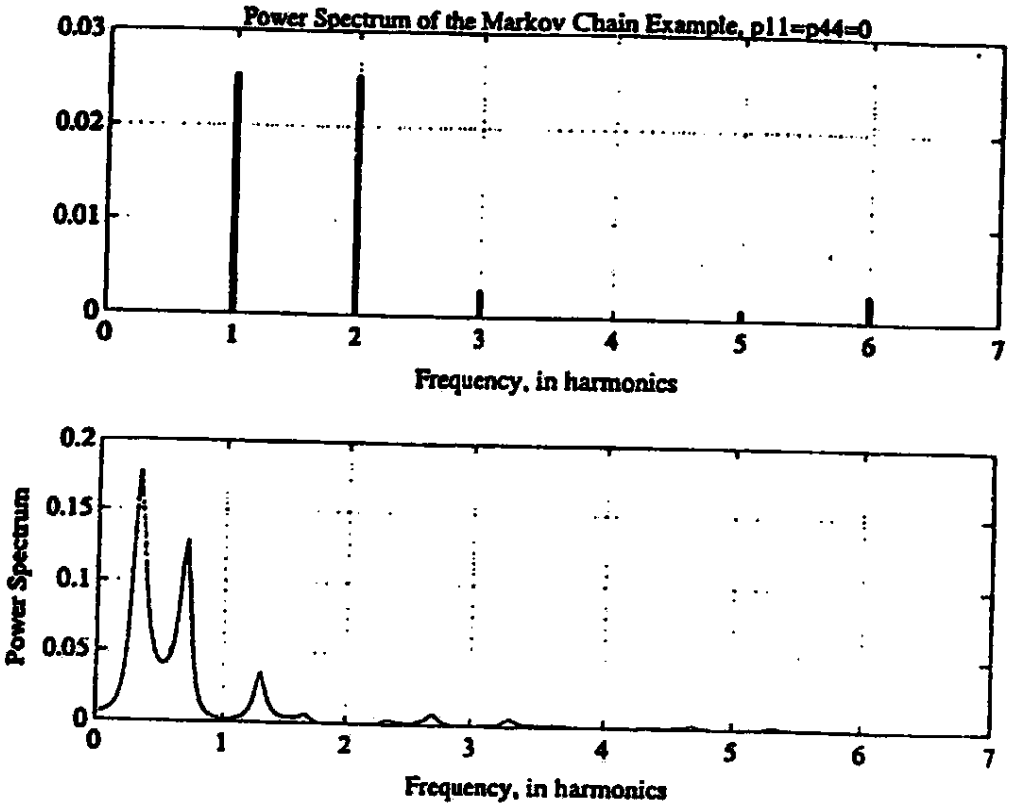


Figure D.6: Calculated Power Spectrum in the Modified Markov Random Modulation Example.

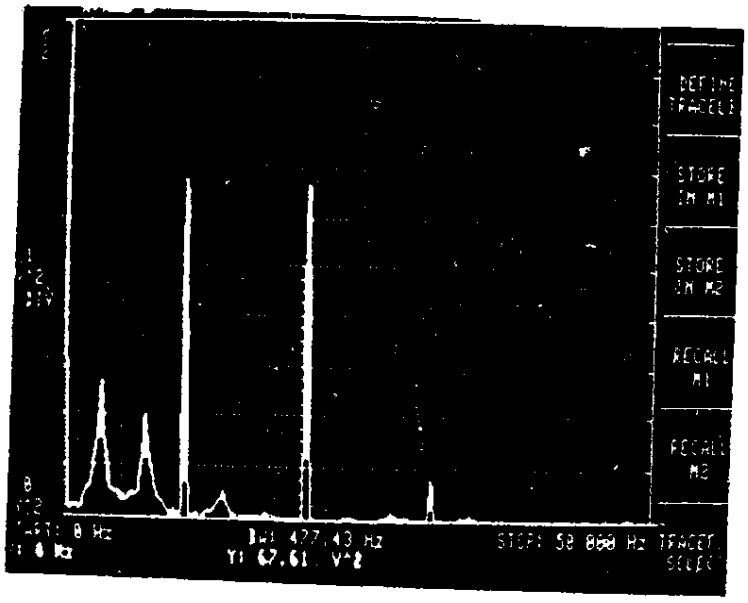


Figure D.7: Experimentally Observed Power Spectrum in the Modified Markov Chain Based Random Modulation Example.

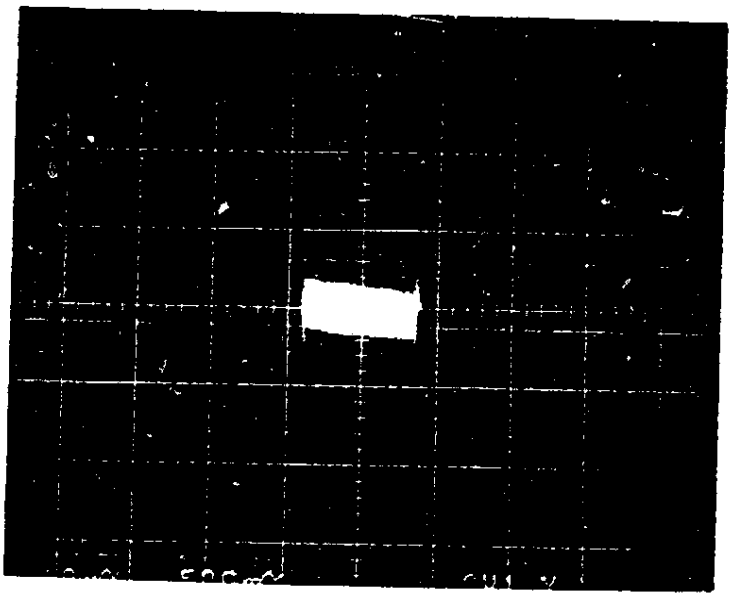


Figure D.8: Experimentally Observed Ripple Waveform of the Conventional Modulation with Duty Ratio $D = 0.5$.

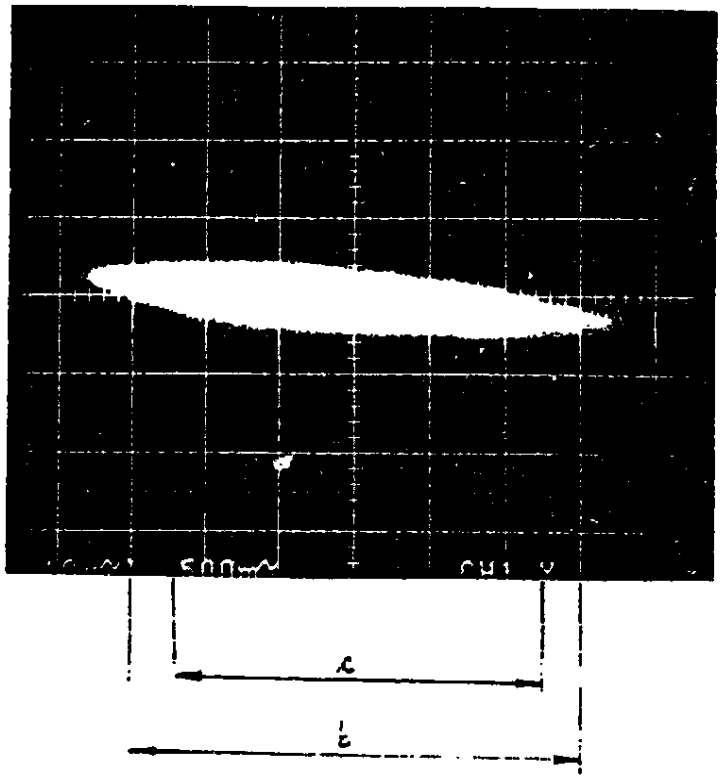


Figure D.9: Experimentally Observed Ripple Waveform of the Independent Random Choice Between the Duty Ratios $D = \frac{1}{4}$ and $D = \frac{3}{4}$; (b) Random Modulation with Standard Markov Chain; (c) Random Modulation with Modified Markov Chain $\bar{P}_{1,1} = \bar{P}_{4,4}=0$

Appendix E

High–Frequency Switching Phenomena

High–frequency phenomena (on the order of a few hundred times the switching frequency) caused by device imperfections have been addressed in [116], [114]. Random modulation can substantially reduce the effects of non–ideal switching, as will be shown now. Suppose that, due to device nonlinearities and the presence of stray (parasitic) inductances and capacitances, at each turn–on instant a high-frequency ringing waveform is added to the switching function. This waveform is assumed to contain frequencies of the order of hundreds of times the switching frequency e.g. tens of MHz in implementations [116], [114]. The turn–off transient can be analyzed analogously. For a regular (ideal) deterministic switching with period T_0, this process is described by a sequence of equidistant impulses (corresponding to turn–on instants) convolved with the ringing turn–on waveform. In the spectral domain, a sequence of equal impulses ($\frac{1}{T_0}$ apart) is multiplied by the square of the Fourier transform of the "on" waveform, yielding the result shown in Fig. E.1 for the case $T_0 = 1$ (so that impulse coefficients are all equal to one). Suppose a random PPM modulation is applied, with a smooth probability density function used for dither, so that its Fourier transform falls off relatively quickly. Then, from (7.1) and (7.6), at high frequencies the discrete component of the spectrum of the dithered impulse train disappears, and the continuous component of the spectrum is 1. Thus the continuous spectrum due to

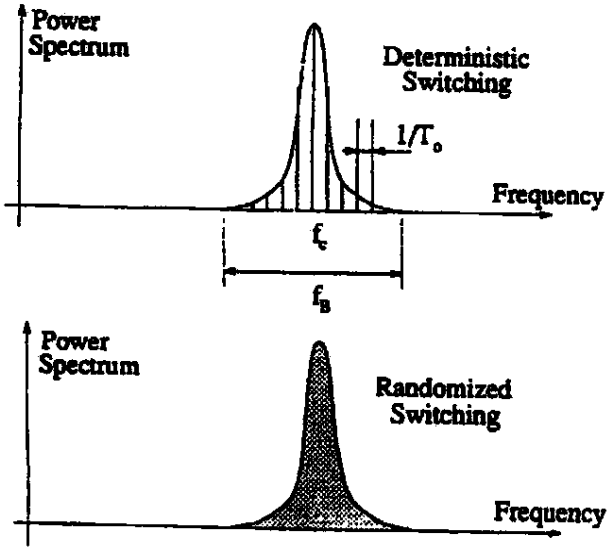


Figure E.1: High Frequency Spectra due to Switching Nonidealities for Conventional and Random PPM Modulation. $T_0 = 1$.

the turn–on transient equals the square of the Fourier transform of the turn–on waveform, as displayed in Fig.E.1. In the case of simplified aperiodic random modulation, the result is the same, thus explaining the significant improvements over conventional switching reported in [114]. If a purely discrete probability density function (or a mixed probability) is used, then less general statements about the spectrum at high frequencies are possible (due to (7.5)). Even in that case, however, it is guaranteed that some reduction of discrete harmonics will be achieved, since the spectra of impulse trains of random PPM or simplified aperiodic modulation are ≤ 1 in the frequency domain.

It is of interest to compare the high frequency power spectra obtained from random modulation and from "practical" conventional switching. It is assumed in this analysis that the conventional (deterministic, periodic) switching is not perfect, and that variations in cycle lengths and duty ratios could be modeled as uniform random PPM. Let the width of the probability density function be $a\ T_0$, where $T_0 = 1$ is the period length. If $a = 0.1\%$, then from power spectral formulas for random PPM it follows that the characteristic function $P(f_1) = 0$ at $f_1 = 1000$, i.e., at a thousand times the switching frequency. If a switching frequency of $100kHz - 1MHz$ is

assumed, then it turns out that the discrete components will dominate the spectrum in the $10 - 100\ MHz$ range, as shown in [116]. On the other hand, if $a = 1\%$, then the discrete harmonics will be zero at $f_1 = 100$, and will largely disappear altogether above 500, due to the decrease of the sinc function. In that case, a broad-band spectrum will be observed in the $10 - 100\ MHz$ range, as shown in the lower part of Fig. E.1.

Appendix F

Closed–Loop Spectral Control

In power electronic applications the primary objective of a spectral controller would be to regulate the power spectra of waveforms of interest, e.g. input currents, or output voltages. Closed–loop operation is the way to compensate for unavoidable deviations, and to reduce the sensitivity to perturbations. A controller for a converter that employs random modulation would use measurements (or estimates) of power spectra to generate the corrections in the modulation process. In one such setup, shown schematically in Fig. F.1, an estimate of the power spectrum $\hat{S}_y$ is compared with the desired (target) spectrum S_y in some appropriate norm, and the difference is fed into the controller K. In the figure, $P(f)$ denotes the Fourier transform of a probability density function used for modulation. $\hat{P}$ is the Fourier transform of an open–loop probability density, and $\tilde{P}$ is a correction generated by the controller K.

Although a variety of issues will need to be addressed for this task, we limit ourselves here to discussing how an on–line spectral estimate may be obtained for use in control. This quantity, denoted as $\hat{S}_y = \hat{S}_y(f,t)$ has to satisfy two main conditions:

- It has to be based on past values of the signal $x(\cdot)$ only. This constraint is often referred to as the "real–time" constraint [89]. Given a likely digital implementation for a power spectrum controller, only finitely many past values of $x(\cdot)$ are available for calculation of $\hat{S}_y$ ("finite data set" constraint),

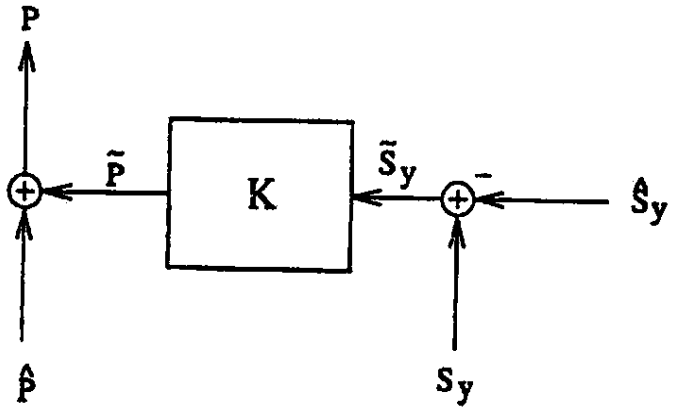


Figure F.1: Closed–Loop Control of a Power Spectrum.

- It has to have a correct "time–marginal", i.e.,

$$\int \hat{S}_y(t,f)dt = S_y(f) \qquad \text{(F.1)}$$

The notion of time–varying spectral density has a long and rich history. It started with the work of Fano [31], which was continued soon thereafter [70]. More recent references on the topic [20], [9], [10], [102], [2], [99], [51] list hundreds of articles and books on the subject. A list of contributors includes researchers in speech, radar and image processing, and statistical physics. The constraints on $\hat{S}_y(t,f)$ in a power electronic setup, however, significantly reduce the list of eligible candidates.

The basic idea is to formulate a function of time and frequency, that will describe the signal energy density simultaneously in time and frequency. The finite data set constraint eliminates the Page distribution from consideration [20], while the real-time constraint makes the Wigner–Ville and Rihaczek ("complex energy spectrum") distributions ineligible [20].

The most promising approach is based on "local autocorrelation methods" [20], and represents a direct descendant of Fano's approach. As a part of the Welch spectral estimation method, described in Section 3.3, the available data record is divided in K segments which are separately windowed, and their periodograms are calculated and averaged. A modification to Welch's procedure suggested here is an averaging

procedure with a forgetting factor. Suppose $\bar{K}$ data segments are available, obtained by possibly allowing overlaps in the original K disjoint segments. Then a weight $a^0 = 1$ is assigned to the most recent segment, the weight a to the preceding segment, and, in general, a weight $a^{\bar{K}-i}$ to the i-th segment, where $0 < a \leq 1$. By setting $a = 1$, the standard Welch method is recovered. As in all recursive procedures with forgetting factors, the smaller the parameter a, the more attention is being paid to more recent samples of the waveform $x(\cdot)$, and the more readily will the variations in S_y be detected. A possible drawback is that the control signal obtained with small values of a might be jittery, i.e., it might oscillate around a long-time trend. The suggested approach is very simple, and in the same spirit as well known methods of Rihaczek, Mark, and Choi and Williams [20].

The variance of the spectral estimate in the modified Welch method is somewhat larger than in the standard method. In the modified method, with $\bar{K}$ data segments available, the variance is reduced K^* times, where

$$K^* = \frac{(1+a)(1-a^{\bar{K}+1})^2}{(1-a^{2(\bar{K}+1)})(1-a)} \tag{F.2}$$

For an example, $\bar{K} = 16$ and $a = 0.9$ yields $K^* = 13.6$, which can be compared with the standard Welch method, where the variance would be reduced $\bar{K} = 16$ times.

A relationship between the proposed spectral estimation procedure and the concept of spectrogram, or Short Time Fourier Transform (STFT) [89], is explored next. Assume for simplicity that K non-overlapping segments of data are available, and consider each segment to be of length L, corresponding to the time interval T_0. The segment windowed with a window $w(\cdot)$ of length L, centered at $\frac{L}{2}$ has the Fourier transform

$$X(\frac{L}{2}, f) = \sum_{m=0}^{L} x(m)w(\frac{L}{2} - m)e^{-i2\pi fm} \tag{F.3}$$

which is a special case of the discrete-time STFT, defined as [89]

$$X(n, f) = \sum_{m=-\infty}^{\infty} x(m)w(n-m)e^{-i2\pi fm} \tag{F.4}$$

Thus, the modified Welch procedure is obtained from a discrete-time STFT by sampling in time. The samples correspond to individual data segments which are of length L (in terms of samples of $x(\cdot)$). When the periodogram $\frac{1}{T_0}\,|X(\frac{L}{2}, f$ is formed, it is the Fourier transform of the short-time autocorrelation, which is defined as

$$r(\frac{L}{2}, m) = [x(m)w(\frac{L}{2} - m)] * [x(-m)w(\frac{L}{2} + m)] \qquad \text{(F.5)}$$

Thus, the short-time autocorrelation is obtained by convolving a windowed signal with its time-reversed windowed version. The STFT is related to other time-frequency distributions, such as complex energy density (Rihaczek distribution), Wigner-Ville distribution and the ambiguity function, through convolutional relationships [89],[20]. The main problem with the modified Welch approach and with STFT is that its time-marginal equals the power spectral density of $x(t)w(t)$, where w is the window used. If a window is not too narrow in the time domain, then the frequency resolution will not be impaired too much, as argued in Section 3.3 on power spectrum verification.

In a closed-loop operation of a power converter employing random switching, it is very important to obtain accurate spectral estimates. One question that arises is whether parametric methods [101] would lead to substantial improvement in spectral estimation for random modulation. Standard parametric methods may be classified into two groups:

- Methods based on modeling the recorded data as the output of a linear system with a rational transfer function, that is driven by a stationary random process, usually a zero mean white noise. In statistics, the same class of models is called ARMA (for auto-regressive moving average), or AR if an all-pole transfer function is used.

- Methods based on eigenanalysis (Pisarenko method, MUSIC and ESPRIT algorithms). The common assumption is that the observed signal comprises finitely many sinusoids corrupted by white noise.

Observe that in the case of random PPM (and in some other random modulation

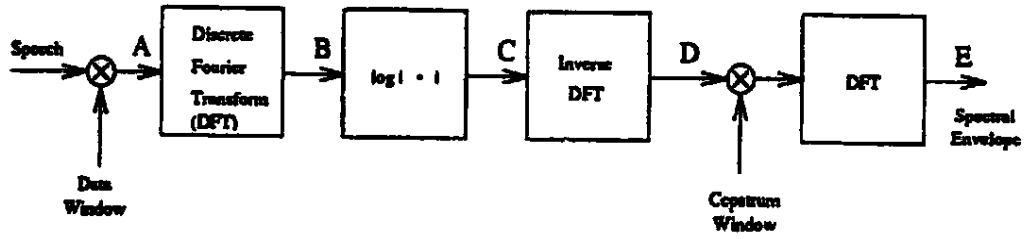


Figure F.2: Homomorphic Processing in Speech Applications.

schemes, e.g. random PWM), the spectrum contains both a continuous part (which can perhaps be modeled well as the output of an ARMA model), and a discrete part (corresponding to distinct sinusoids).

Parametric AR estimation methods tailored to speech processing are described in [81], [107], [103]. These highly successful methods are often labelled as linear prediction methods. A particularly interesting class of selective linear prediction methods [81] concentrates on fitting only a selected portion of a given spectrum. This is similar to the situation in random modulation for power converters, where often only certain parts of the spectrum are important for complying with the regulations.

Homomorphic processing is a nonlinear processing technique, which has originated in speech, and which is useful for spectral estimation [107], [17]. The basic idea is illustrated in Fig. F.2 (adopted from [107]). It is assumed that the input signal is a convolution of the excitation with a filter (representing the vocal tract). The cepstrum D turns out to be an additive combination of the individual cepstra of the excitation and the filter. The two components of interest have disjoint supports in the signal C (logarithm of the magnitude of the DFT), and they can be separated via the last three blocks. The resulting signal E is the power spectrum corresponding to the speech signal, often called the spectral envelope.

Note that the cepstrum is based on the initial computation of a narrow-band spectrum (Short Time Fourier Transform), and the smoothing is done later on a narrow-band log-magnitude spectrum (signal C), instead of STFT. This produces better results than direct methods when the speech spectrum is changing *slowly*. Application of a cepstrum-based spectral estimation to randomly modulated power converters is another interesting research topic.

Appendix G

Piecewise Deterministic Processes

The concept of piecewise deterministic processes has been introduced by Davis in [24], [23]. In imprecise terms, piecewise deterministic processes consist of random jumps and deterministic motion between the jumps. Analysis methods outlined in [24], [23] are directly analogous to those of diffusion theory. Optimal control theory for piecewise deterministic processes has been introduced by Vermes [124].

Piecewise deterministic processes are a natural generalization of piecewise linear processes. Vermes defines piecewise linear process as a two component Markov process

$$(x_t) = (\nu_t, \zeta_t), \quad \nu_t \in \mathbf{Z}, \zeta_t \in [a_n, b_n] \subset \mathbf{R} \tag{G.1}$$

The motion starts at a point $x_0 = (n, z)$ and

$$\nu_t = n, \tag{G.2}$$

$$\zeta_t = z + t \tag{G.3}$$

until the first jump time T_1. Observe that the second component moves uniformly with a constant speed. Jumps are assumed to occur spontaneously in a Poisson-like fashion, with rate $\lambda(x_t)$ and in addition, a jump must occur ("commanded jump") should ζ_t reach the end point of the corresponding interval. In either case, the location of the process at time instant T_i is determined by a probability density p depending on

x_{T_i}. The trajectory is assumed right continuous. After a jump, the motion restarts. A piecewise linear process is specified if the intervals $[a_n, b_n]$, the jump intensity $\lambda(x)$ and the probability density function $p(x)$ for the transitions are given. The additional generality of piecewise deterministic processes is that the second component of the process is determined by an ordinary differential equation, instead of being a uniform motion.

The main characteristics of the piecewise deterministic framework for analysis of random pulse modulation are:

1. As a Markov chain-based approach, it offers the generality needed for the most elaborate switching schemes.

2. During some parts of the basic switching period T_i (which is itself a random variable) both Poisson and commanded transitions can occur. While ordinary differential equations governing the switching function $q(t)$ are very simple, both types of transitions are important:

   - Poisson type (e.g. beginning of a new cycle in an aperiodic scheme, beginning of a pulse in PPM),
   - Commanded (e.g. switching at the end of a fixed on-time interval).

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EXHIBIT 24
(A Comparison of Nondeterministic and Deterministic Switching Methods for DC–DC Power Converters)

A Comparison of Nondeterministic and Deterministic Switching Methods for DC–DC Power Converters

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***Abstract*— An analysis and experimental results of the random pulsewidth modulation (RPWM) and random pulse-position modulation (RPPM) methods for dc–dc converters are presented. The characteristics and performance of power converters under two randomized modulations are evaluated. The theoretical relationships of discrete harmonics, continuous noise, and output-voltage ripple of the RPWM and RPPM schemes are established and compared with those of a standard deterministic pulsewidth modulation (PWM) scheme in a buck converter. Limitations in the randomly switched dc–dc converters, which have not been addressed before, are highlighted. Randomized schemes generally have inherent problems in achieving low-output-voltage ripple due to the low-frequency continuous noise within the passband of the converter filter. The inherent low-frequency noise-induced voltage ripple problems of nondeterministic switching methods for dc converters are confirmed experimentally. The performance of the RPPM method is found to be closer to the standard PWM method than that of the RPWM method. For dc–dc power conversion, the RPPM method offers much better output-voltage performance than the RPWM method.**

I. Introduction

RANDOMIZED modulation technique has recently been recognized as an emerging technology [1]. Various randomized switching techniques have been reported for dc–ac [2]–[14] and dc–dc power conversion [15]–[18]. The basic principle of introducing randomness into standard pulsewidth modulation (PWM) schemes is to spread the harmonic power which exists at well-defined frequencies (discrete harmonics) over a wide range of frequencies so that no harmonic of significant magnitude exists. As a result, discrete harmonics are significantly reduced and the harmonic power is spread over the spectrum as "noise" (continuous spectrum) of insignificant magnitude. Due to the reduction of discrete harmonics, the dc–ac randomized switching methods have been shown to have obvious advantages of acoustic noise reduction and mechanical vibration reduction in electronic drive systems [2], [9], [11], [12]. Various forms of randomized modulation techniques have been successfully implemented. Recently, a new weighted dc–ac random PWM scheme that can be used to alter the degree of structural element in the random PWM switching pattern in order to improve the spectral performance has been proposed [21], [22].

It has been pointed out in two excellent references ([12] and [15]) that many aspects of the randomized switching schemes have not been explored and that the analytical content of existing RPWM literature is limited. Randomized modulation methods for dc–dc power converters have been addressed in several publications [15]–[18]. Stankovic *et al.* [15] have presented an important theoretical foundation on which various dc–dc randomized modulation methods can be analyzed. In standard PWM switching schemes with constant switching frequency, switching harmonics usually occur at fixed and well-defined frequencies and are thus named "discrete harmonics." On the contrary, randomized switching schemes for converters generally produce harmonic spectra consisting of both discrete harmonics and continuous noise. It has been shown [15] that the randorn pulse position modulation (RPPM) and random pulsewidth modulation (RPWM) using a random number generator with uniform distribution have the effect of reducing the magnitude of the discrete harmonics. It was later pointed out in [18] that an RPWM scheme with a binomial distribution could totally eliminate discrete harmonics. While the reduction or elimination of discrete harmonics has the advantage of reducing the filtering efforts for these harmonics, the effect of the continuous noise spectrum in the converter performance has not been addressed in published literature. This aspect of the switching scheme is very important because many power converter applications require tight control of the output-voltage ripple. The continuous noise spectrum, which is a feature of randomized switching schemes, could have undesirable effects for switched mode power supply applications.

This paper presents a comparative study on the performance of the RPWM, RPPM [15], and standard PWM methods. In particular, analyses on the relationship of the output harmonics/noise level and output-voltage ripple of the RPPM and RPWM are established. Finally, advantages and disadvantages of these randomized modulation methods, using the performance of the standard PWM method as a base for comparison, are discussed. Using a buck

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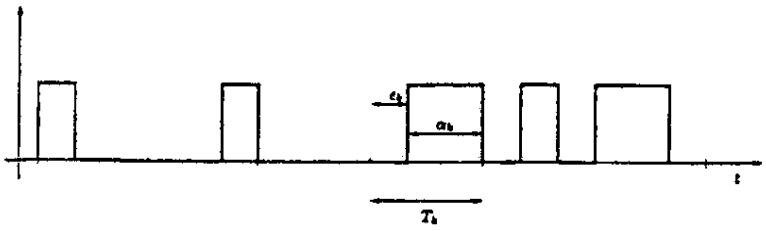

Fig. 1. The switching function $k(t)$

converter, the theoretical predictions of the switching schemes are verified.

II. Classification of Randomized Modulation Under Consideration

A. RPPM and RPWM

Various classifications of randomized modulation schemes have been proposed [12], [15]. The classification described in [15] is adopted here as this approach is more suitable for dc–dc converters than the classification described in [12] (which is more suitable for dc–ac power conversion). RPPM is similar to the traditional PWM method with constant switching frequency. However, the turn-on pulse position is randomized within each switching period instead of always starting at the beginning of each period [13]. RPWM allows the pulse width to vary, but the average pulse width is equal to the required duty cycle. The basic characteristics (Fig. 1) of these two schemes have been summarized in [15], [18] as follows:

RPPM	ε_k changes; T_k, α_k fixed;
RPWM	α_k changes; $\varepsilon_k = 0$; T_k fixed ($T_k = T$)

where T_k is the duration of the kth sampling interval, α_k is the duration of the on-state within the interval (the pulse width), and ε_k is the delay to turn on within the interval. The above two schemes have been tested and compared in [15]. It has been pointed out that "RPWM reduces the fundamental more than RPPM does but RPPM is more efficient at reducing the higher discrete harmonics." The RPWM tested in [15] is a scheme in which α_k changes randomly from one cycle to another. That is, α_k can be any continuous value between 0 and T, where T is the period of each cycle. In the particular implementation reported in [15], random pulse widths have a uniform distribution in the range $[0, T]$ and thus an overall average value of $0.5T$. In general, if the pulse amplitude is A and (average) duty cycle is D, the power of the PWM signal $= \frac{A^2DT}{T} = A^2D$. The output dc power $= \frac{(AD)^2T}{T} = A^2D^2$ as an output of level AD is achieved. The noise power is therefore $A^2D(1-D)$. This noise power has to be distributed in a way so as to reduce switching harmonics and electromagnetic interference (EMI) emission. In [18], we show that if the RPWM scheme is modified for α_k to have a binomial distribution, the discrete switching harmonics can be reduced or eliminated. However, one advantage of a scheme does not guarantee that the method is appropriate for converter implementation. Other aspects have to be considered for a thorough evaluation.

III. Analysis of Randomized Switching Methods

A. Analysis of the RPWM Scheme with Binomial Distribution

1) Probability and Expected Value of Pulse Widths α_k: In this scheme, the switching period is subdivided into N subperiods. Within each sampling period, N random numbers (say, $R_1, \cdots, R_N$) in the range $[0, 1]$ with uniform probability distribution are generated and compared with the desired duty cycle D. D is in the range $[0, 1]$. Let N_S be the number of times $R_i \le D$ for $i = 1, 2, \cdots, N$. Clearly, N_S takes integral values between 0 and N with the following probability density:

$$\Pr\{N_S = l\} = \begin{cases} \binom{N}{l} D^l (1-D)^{N-l}, & \text{for } 0 \le l \le N \\ 0, & \text{otherwise.} \end{cases} \tag{1}$$

This probability function is a binomial distribution. The expectation or mean of N_S is

$$E\{N_S\} = ND \tag{2}$$

and the variance is

$$E\{(N_S - ND)^2\} = ND(1-D). \tag{3}$$

The cumulative distribution function of N_S, $F_N(x)$, is defined as $\Pr\{N_S \le x\}$ and is given by

$$F_N(x) = \begin{cases} 0, & \text{for } x < 0 \\ \sum_{l=0}^{m} \binom{N}{l} D^l (1-D)^{N-l}, & \text{for } m \le x < (m+1) \\ 1, & \text{for } x \ge N \end{cases} \tag{4}$$

and $m = 0, 1, 2, \cdots N-1$.

The pulse width α_k in a switching interval (of length T) in this scheme is defined to be

$$\alpha_k = N_S\left(\frac{T}{N}\right). \tag{5}$$

Equation (5) provides a general expression for the discrete pulse width α_k.

A few important points should be noted.

1) For the particular case of $N = 1$, (1) and (4) can be simplified to

$$\Pr\{N_S = l\} = \begin{cases} (l-D), & \text{for } l = 0 \\ D, & \text{for } l = 1 \\ 0, & \text{for otherwise} \end{cases} \tag{6}$$

and

$$F_1(x) = \begin{cases} 0, & \text{for } x < 0 \\ (1-D), & \text{for } 0 \le x < 1 \\ 1, & \text{for } x \ge 1. \end{cases} \quad (7)$$

This means that $\alpha_k = T$ or 0 in each sampling interval.

2) For the general case where $N > 1$, (say, $N = 3$), $\Pr\{N_S\}$ consists of discrete values and $F_N(x)$ has a staircase characteristic.

3) For large values of N (when $ND(1-D) \gg 1$), according to [19] and [20]

$$\binom{N}{l} D^l (1-D)^{N-l} \approx \frac{1}{\sqrt{2\pi ND(1-D)}} \times \exp\left\{\frac{-(l-ND)^2}{2ND(1-D)}\right\}. \quad (8)$$

Thus, for a large N, α_k seems to take continuous values with the density function

$$F(\alpha_k) = \frac{1}{\sqrt{2\pi}\sigma} \exp\left\{\frac{-(\alpha_k - DT)^2}{2\sigma^2}\right\} \quad (9)$$

where $\sigma^2 = T^2 D(1-D)/N$. Equation (9) is a normal distribution having a mean of DT and a variance of σ^2. Note that $N \to \infty$, $\sigma^2 \to 0$, and the random scheme approaches the deterministic PWM scheme of fixed pulse width DT.

4) For any value of N, the average pulse width is given by $E\{\alpha_k\} = E\{N_S \frac{T}{N}\} = DT$ as desired, and $\text{var}\{\alpha_k\} = \text{var}\{N_S \frac{T}{N}\} = \frac{T^2 D(1-D)}{N}$.

2) Expected Value of RPWM Signal: Let $k(t)$ be the RPWM output function which has the value of either A or 0. Since the pulse width has values that are integral multiples of (T/N) in this discrete RPWM scheme, the expectation $E\{k(t)\}$ is the same for $t \in [nt + \frac{lT}{N}, nT + \frac{(l+1)T}{N})$, where $n = 0, 1, \cdots$ and $l = 0, 1, \cdots, (N-1)$. The expected value of the random RPWM output function $E\{k(t)\}$ can be shown as

$$\begin{aligned} E\{k(t)\} &= \Pr\{k(t) = +A\} \cdot (A) + \Pr\{k(t) = -A\} \cdot (0) \\ &= A \cdot \left\{1 - F_N\left(\left\lfloor \frac{Nt}{T} \right\rfloor - N\left\lfloor \frac{t}{T} \right\rfloor\right)\right\} \\ &= g(t). \end{aligned} \quad (10)$$

It can easily be shown that $g(t)$ is a periodic signal having a period T and thus has a Fourier series representation, i.e., $g(t) = \sum_n c_n \exp(j2\pi nt/T)$. Its dc component c_0 is AD as desired.

3) Expected Power Spectral Density and Harmonics: In order to determine the expected power spectral density of the RPWM waveform, we first define an (time-averaged) autocorrelation function [15]

$$R(\tau) = \lim_{W \to \infty} \frac{1}{2W} \int_{-W}^{W} E\{k(t)k(t+\tau)\}\, dt. \quad (11)$$

The expectation operation $E[\cdot]$ here is taken over the whole ensemble. This definition is suitable for nonstationary RPWM signals under consideration [21], [22]. The autocorrelation function in (11) can be separated into two terms as follows:

$$R(\tau) = R_1(\tau) + R_2(\tau) \quad (12)$$

with

$$R_1(\tau) = \sum_{n=-\infty}^{\infty} |c_n|^2 \exp\left(-j2\pi \frac{n\tau}{T}\right) \quad (13)$$

where c_n's are the Fourier series coefficients of $g(t)$.

It should be noted that $R(\tau)$ defined in (11) is symmetrical about the origin, i.e., $R(\tau) = R(-\tau)$. Equation (13) gives the discrete spectrum. In particular, for $N = 1$, $c_n = 0$ for $n \neq 0$ as $g(t)$ is just a dc signal in this case. So, the theory predicts that there are no discrete harmonics for $N = 1$ in this RPWM scheme. This feature looks very attractive for converter applications. However, it will be shown that other features may indicate otherwise.

The second term $R_2(\tau)$ can be expressed as (14), given at the bottom of the page. Equation (14) provides the information for the general noise spectrum. Doing the integration in (14) an explicit closed form expression for $R_2(\tau)$ can be obtained as

$$\begin{aligned} R_2(\tau) = \left(\frac{A^2}{N}\right) \sum_{k=0}^{\lfloor N - \frac{N|\tau|}{T} \rfloor} &[(1-\delta)F_N(k) \\ &+ \delta F_N(k-1)]\left[1 - F_N\left(\left\lfloor \frac{N|\tau|}{T} \right\rfloor + k\right)\right] \end{aligned}$$

where

$$\delta = \frac{N|\tau|}{T} - \left\lfloor \frac{N|\tau|}{T} \right\rfloor.$$

The power spectral density of the RPWM signal is the Fourier transform of $R(\tau)$. Thus

$$\begin{aligned} S(f) &= \Im[R_1(\tau)] + \Im[R_2(\tau)] \\ &= S_1(f) + S_2(f) \\ &= \sum_{n=-\infty}^{\infty} |c_n|^2 \delta(f + nf_{sp}) + \Im[R_2(\tau)] \end{aligned} \quad (15)$$

where f_{sp} is the sampling frequency. The first term on the right-hand side of (15) gives the information of the discrete spectrum, and the second term gives the continuous noise spectrum. The general expression for c_n is

$$c_n = \frac{A}{N} \text{sinc}\left(\frac{n}{N}\right) \sum_{k=0}^{N-1} [1 - F_N(k)] \times \exp\left(-j\frac{n\pi}{N}(2k+1)\right). \quad (16)$$

$$R_2(\tau) = \begin{cases} \left(\frac{A^2}{T}\right) \int_0^{T-|\tau|} F_N\left(\left\lfloor \frac{N\mu}{T} \right\rfloor\right)\left\{1 - F_N\left(\left\lfloor \frac{N(\mu+|\tau|)}{T} \right\rfloor\right)\right\} d\mu, & \text{for } \tau \in [-T, T] \\ 0, & \text{otherwise} \end{cases} \quad (14)$$

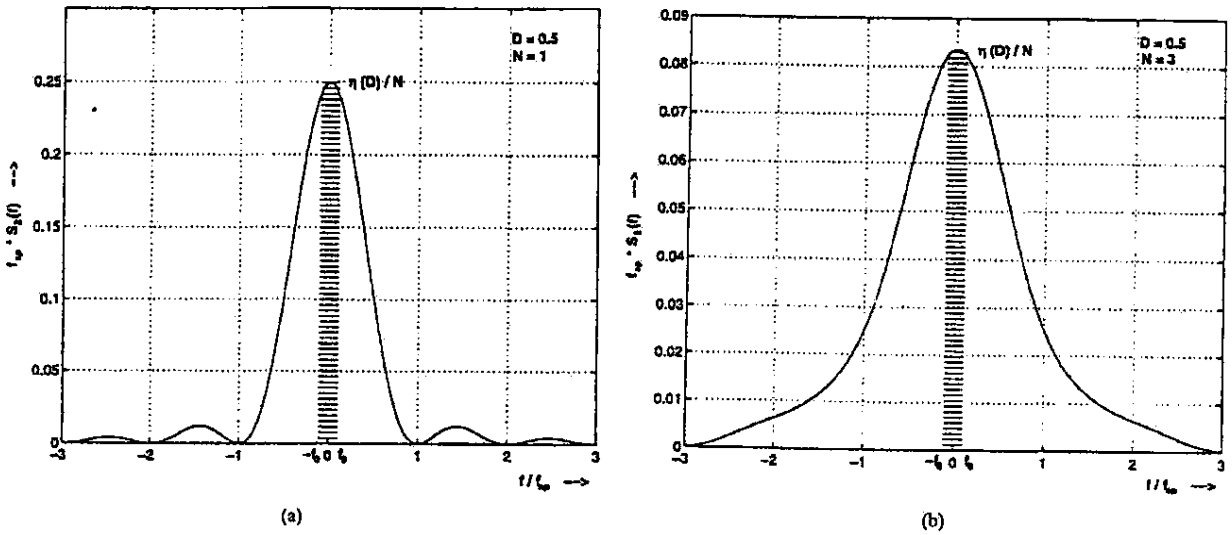

Fig. 2. (a) Typical plot of $f_{sp} \times S_2(f)$ versus the normalized frequency f/f_{sp} for $D = 0.5$ and $N = 1$ under the RPWM scheme. (b) Typical plot of $f_{sp} \times S_2(f)$ versus the normalized frequency f/f_{sp} for $D = 0.5$ and $N = 3$ under the RPWM scheme.

For the special case of $N = 1$, this gives us

$$c_n = A\,\mathrm{sinc}(n)[1 - F_1(0)]\exp(-jn\pi) = \begin{cases} AD, & \text{for } n = 0 \\ 0, & \text{otherwise.} \end{cases}$$

Thus, the discrete spectrum consists of the dc component only, and there are no discrete harmonics. The second term of (15), i.e., the Fourier transform of (14), gives the continuous spectrum. It can be solved numerically and typical plots for $N = 1$ and $N = 3$ at $D = 0.5$ are shown in Fig. 2.

Several important points should be highlighted.

- General continuous noise level is inversely proportional to f_{sp}.
- General continuous noise level is inversely proportional to number of subperiods N.
- To obtain a dc signal, the RPWM signal will be passed through a low-pass filter (e.g., the output filter of a buck converter). For an "ideal" low-pass filter, the noise power (P_{noise}) in the filtered signal is obtained by integrating the noise power spectral density over the filter passband. If the cutoff frequency f_o of the filter is much smaller than the sampling frequency f_{sp}, i.e., $f_o \ll f_{sp}$, then the noise power (P_{noise}) can be approximated by the shaded area of the rectangle in Fig. 2 as

$$P_{noise} \approx \frac{\eta(D)}{N f_{sp}}(2f_o).$$

- The rms value ΔV_{noise} of the voltage ripple in the dc voltage output is then given by

$$\Delta V_{noise} = \sqrt{2P_{noise}} \approx 2\sqrt{\frac{\eta(D) f_o}{N f_{sp}}} \tag{17}$$

where (see Fig. 3)

$$\eta(D) = D(1 - D). \tag{18}$$

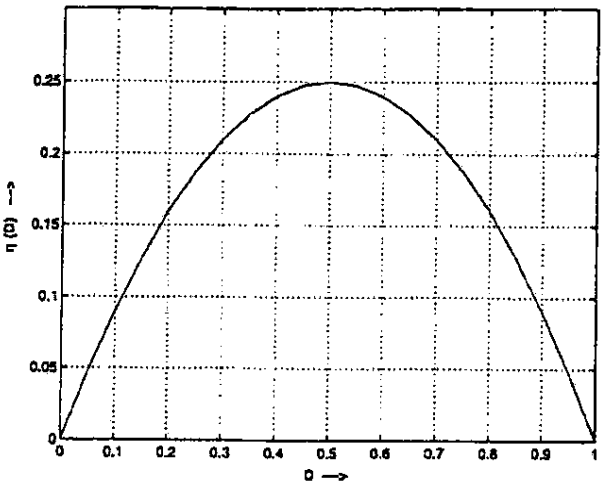

Fig. 3. A plot of $\eta(D)$ versus the duty cycle D under the RPWM scheme.

Equation (17) provides a qualitative dependence of the output-voltage ripple on various parameters. Clearly, the voltage ripple can be reduced by decreasing the ratio f_o/f_{sp} or increasing N. $\eta(D)$ is simply a function of the duty cycle D.

- However, from a practical point of view, a microprocessor or a digital signal processor (DSP) has a limit on its maximum sampling frequency, which restricts the product Nf_{sp}. At the maximum limit of the sampling frequency, an increase in f_{sp} must follow by a corresponding reduction of N. This point will be demonstrated experimentally.

B. Analysis of RPPM Scheme

Unlike the random RPPM scheme reported in [13], which randomly locates the turn-on pulse either at the beginning or the end of the switching period, the RPPM scheme here is

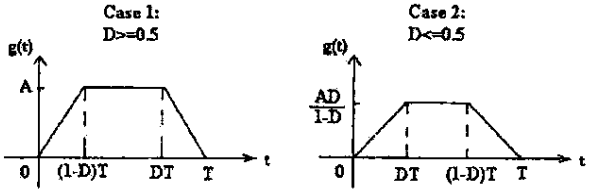

Fig. 4. Typical plot of the expected value $g(t)$ of the RPPM signal.

more general and assumes that the pulses can be randomly located anywhere within the switching interval. A turn-on pulse with a pulse width of DT has a starting instant ϵ_k, where $\epsilon_k \in [0, (1-D)T]$ and has uniform distribution.

1) Expected Value of RPPM Signal: Let $k_p(t)$ be the RPPM signal which takes value of either A or 0

$$k_p(t) = \begin{cases} A, & \text{if } \epsilon_n \in \left(t - \lfloor \frac{t}{T} \rfloor T - DT, t - \lfloor \frac{t}{T} \rfloor T\right] \\ 0, & \text{otherwise.} \end{cases} \quad (19)$$

So, the expected value of $k_p(t)$ is

$$\begin{aligned} &E\{k_p(t)\} \\ &\quad = A \cdot \Pr\left\{\epsilon_n \in \left(t - \left\lfloor \frac{t}{T} \right\rfloor T - DT, t - \left\lfloor \frac{t}{T} \right\rfloor T\right]\right\} \\ &\quad = g_p(t). \end{aligned} \quad (20)$$

Since $(t+T) - \lfloor \frac{t+T}{T} \rfloor T = t - \lfloor \frac{t}{T} \rfloor$, $g_p(t+T) = g_p(t)$. That is, $g_p(t)$ is periodic with period T and has a Fourier series expansion

$$g_p(t) = \sum_{n=-\infty}^{\infty} c_n \exp(j2\pi nt/T)$$

where

$$c_n = \frac{1}{T}\int_0^T g_p(t)\exp(-j2\pi nt/T)\,dt.$$

In particular, the dc component is $c_0 = \frac{1}{T}\int_0^T g_p(t)\,dt$.

The signal $g_p(t)$ consists of trapezoidal pulses. One period of $g_p(t)$ is shown in Fig. 4. For both of the cases of $D \geq 0.5$ and $D < 0.5$, it can be seen that the dc component of the RPPM signal is

$$c_0 = A \cdot D \quad (21)$$

as desired. Fourier series coefficients for general trapezoidal pulses can be shown to be

$$|c_n| = (A \cdot D)|\text{sinc}(nD)\,\text{sinc}[n(1-D)]|. \quad (22)$$

Equation (22) determines the discrete part of the RPPM spectrum. For the RPPM scheme, $c_n \neq 0$ in general, and, thus, discrete harmonics are always present.

2) Expected Power Spectral Density and Output-Voltage Ripple: Similar to the expected power spectral density of the RPWM signal as described in Section III-A3, the noise power spectral density of the RPPM signal can be evaluated using (11). The autocorrelation function for the RPPM scheme is

$$R_P(\tau) = R_{P1}(\tau) + R_{P2}(\tau) \quad (23)$$

with

$$R_{P1}(\tau) = \sum_{n=-\infty}^{\infty} |c_n|^2 \exp\left(-j2\pi\frac{n\tau}{T}\right) \quad (24)$$

where c_n is the Fourier series coefficient of $g_p(t)$. It can be seen that $R_{P1}(\tau)$ consists of the discrete harmonics. $R_{P2}(\tau)$ represents the continuous part of the spectrum and is zero for $|\tau| \geq T$. The power spectral density of $R_P(\tau)$ is thus

$$\begin{aligned} S_{Pk}(f) &= \Im[R_{P1}(\tau)] + \Im[R_{P2}(\tau)] \\ &= \sum_{n=-\infty}^{\infty} |c_n|^2 \delta(f + nf_{\text{sp}}) + \Im|R_{P2}(\tau)|. \end{aligned} \quad (25)$$

The continuous part $R_{P2}(\tau)$ and its Fourier transform can be calculated numerically, and typical plots of $\Im[R_{P2}(\tau)]$ with $D = 0.5$ and $D = 0.75$ are shown in Fig. 5(a) and (b), respectively. Like the duty-cycle-dependent function $\eta(D)$ of (18) for the RPWM scheme, RPPM scheme has a corresponding function $\eta_p(D)$. It is difficult to get a closed-form expression for $\eta_p(D)$, but is can be solved numerically and has a characteristic as shown in Fig. 6.

Several important points should be noted.

- General continuous noise level is inversely proportional to f_{sp} (similar to the RPWM scheme).
- In order to obtain a dc signal, the RPPM signal is passed through a low-pass filter. If an "ideal" low-pass filter is assumed, then the noise power in the filtered signal (P_{noise}) is given by the area of the power spectral density in the passband of the filter. For a cutoff frequency f_o much smaller than the sampling frequency f_{sp}, i.e., $f_o \ll f_{\text{sp}}$, P_{noise} can be approximated by the shaded triangular area (in Fig. 5). This noise power (area of the triangle) is

$$\begin{aligned} P_{\text{noise}} &\approx 2 \cdot \left[\frac{1}{2} f_o \left(\frac{\eta_P(D)}{f_{\text{sp}}} \frac{f_o}{f_{\text{sp}}}\right)\right] \\ &= \eta_P(D)\left(\frac{f_o}{f_{\text{sp}}}\right)^2. \end{aligned}$$

Therefore, the rms value of the noise ripple ΔV_{noise} is approximately

$$\Delta V_{\text{noise}} \approx \sqrt{2 \cdot \eta_P(D)}\frac{f_o}{f_{\text{sp}}}. \quad (26)$$

C. Comparison of ΔV_{noise} in RPWM, RPPM, and Standard PWM Methods

For the standard PWM scheme, the harmonics are discrete. There is no continuous noise spectrum. If the PWM signal is passed through an "ideal" low-pass filter with $f_o \ll f_{\text{sp}}$, the filter signal has theoretically no ripple, i.e., $\Delta V_{\text{noise}} = 0$. For randomized schemes, the part of continuous spectrum within the passband of the filter gives rise to a low-frequency ripple. This is a general feature of all randomized schemes, not just the ones analyzed here. For the schemes analyzed in this paper,

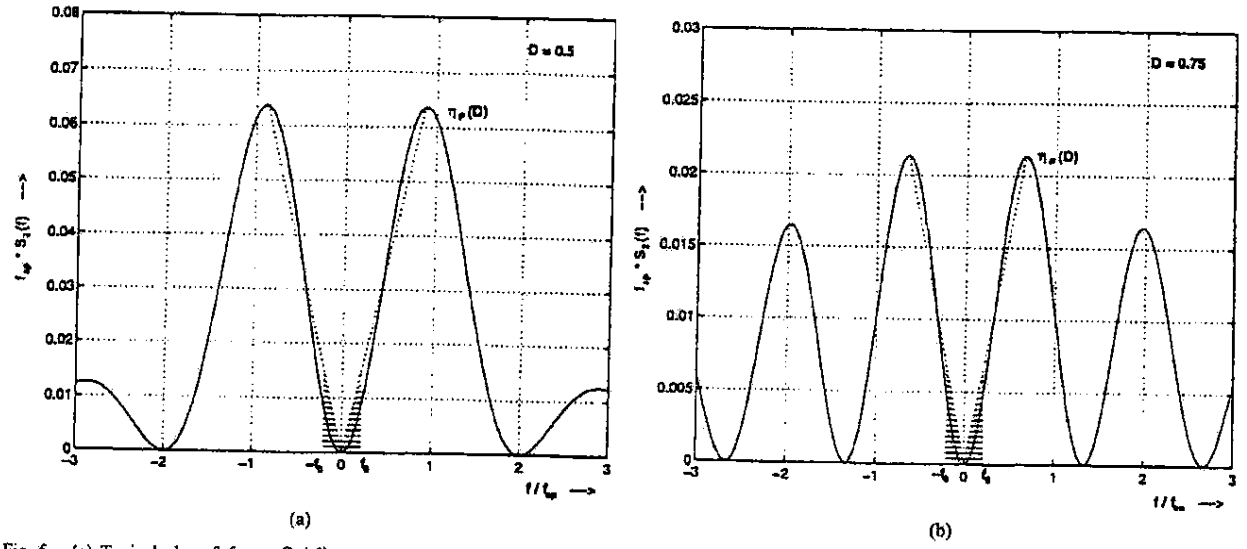

Fig. 5. (a) Typical plot of $f_{sp} \times S_2(f)$ versus the normalized frequency f/f_{sp} for $D = 0.5$ under the RPPM scheme. (b) Typical plot of $f_{sp} \times S_2(f)$ versus the normalized frequency f/f_{sp} for $D = 0.75$ under the RPPM scheme.

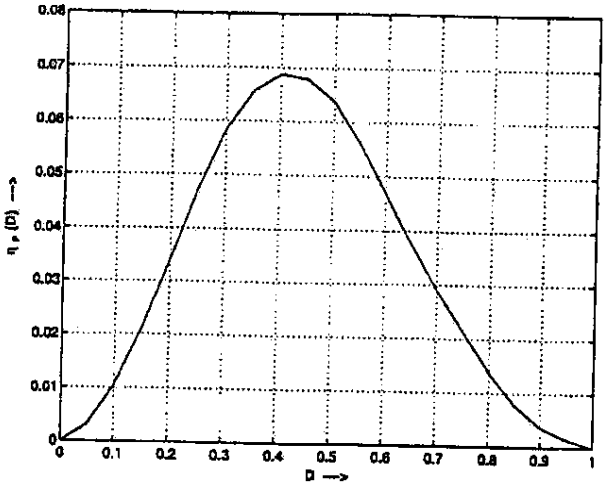

Fig. 6. A plot of $\eta_p(D)$ versus the duty cycle D under the RPPM scheme.

the following qualitative statements can be made:

$$\text{PWM:} \quad \Delta V_{\text{noise}} = 0 \tag{27}$$

$$\text{RPWM:} \quad \Delta V_{\text{noise}} \propto \sqrt{\frac{f_o}{f_{sp}N}} \tag{28}$$

$$\text{RPPM:} \quad \Delta V_{\text{noise}} \propto \frac{f_o}{f_{sp}}. \tag{29}$$

This comparison leads to an important prediction. Randomized switching schemes consist of continuous noise content which leads to inherent extra noise-induced ripple in the filtered signal. Therefore, in practical dc–dc power converter implementation, the output-voltage ripple of randomized switching schemes is inherently higher than that of the standard deterministic PWM scheme. Reduction of ΔV_{noise} requires an increase of the ratio f_o/f_{sp}, i.e, increasing the filtering effort and/or the sampling frequency. In practical terms, this implies a higher implementation cost because of the need for larger

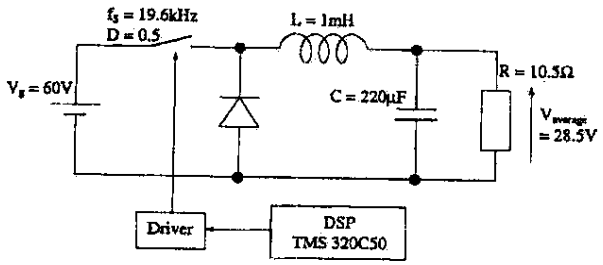

Fig. 7. Schematic of a dc–dc buck converter under test.

filter components and faster DSP. For the two randomized schemes under consideration, the RPPM scheme has a better (smaller) output-voltage ripple than the RPWM scheme because its ΔV_{noise} is proportional to f_o/f_{sp} rather than $\sqrt{f_o/f_{sp}}$. (Note: for $f_o/f_{sp} < 1$, $f_o/f_{sp} < \sqrt{f_o/f_{sp}}$.) Note that for the RPPM scheme, the average switching frequency f_{sw} is approximately the same as f_{sp} since the probability of successive pulses joining together is very low. A similar qualitative statement can be made for RPWM schemes having a large N. However, for the RPWM scheme having $N = 1$, the probability of successive pulses joining together is significant. This leads to a reduction in the average switching frequency. It can be shown that for RPWM schemes, the average $f_{sw} = (1 - D^N)[1 - (1 - D)^N]f_{sp}$.

IV. Practical Evaluation of PWM and Randomized Modulation

A buck converter has been built and tested. Experiments were carried out in an open-loop manner under steady-state conditions so that the influence of the type of controller is irrelevant. The RPWM, RPPM, and standard deterministic PWM schemes were examined in the same converter load system. Fig. 7 shows the schematic of the experimental setup. The firing signal is provided by a TMS320C40 digital signal processor. The practical parameters of the buck converter are

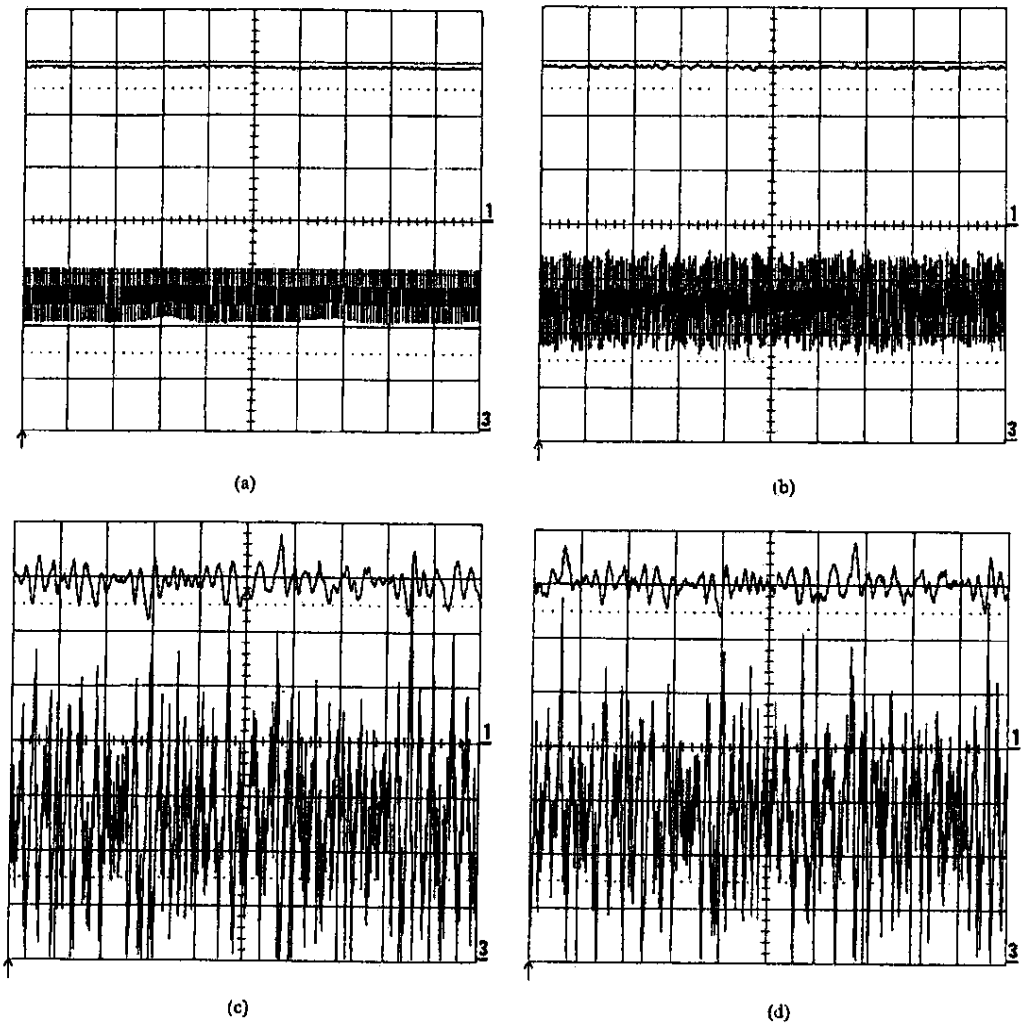

Fig. 8. (a) Measured output voltage (upper) and inductor current (lower) of buck converter under the standard PWM scheme (10 V/div., 1 A/div., 10 ms/div.). (b) Measured output voltage (upper) and inductor current (lower) of buck converter under the RPPM scheme (10 V/div., 1 A/div., 10 ms/div.). (c) Measured output voltage (upper) and inductor current (lower) of buck converter under the RPWM scheme with $N = 16$ (10 V/div., 1 A/div., 10 ms/div.). (d) Measured output voltage (upper) and inductor current (lower) of buck converter under the RPWM scheme with $N = 1$ (10 V/div., 1 A/div., 10 ms/div.).

filter inductor $L = 1$ mH, filter capacitor $C = 220$ μF, and load resistor $R = 10.5$ Ω. The input voltage is 60 V. The average dc output voltage is about 28.5 V. The duty cycle D was set at 0.5 for all schemes under consideration.

A. Converter's Output Voltage and Inductor Current

Fig. 8(a) shows typical measured waveforms of the converter output voltage (upper trace) and inductor current of the buck converter under a standard PWM switching scheme. As expected, the output voltage has a dc-voltage component together with a high-frequency ac switching voltage ripple (of 19.6 kHz). There is no observable low-frequency voltage ripple. Measured waveforms of converter output voltage and inductor current of the buck converter under the RPPM scheme are included in Fig. 8(b). Similar to the standard scheme, the output voltage consists of a dc component and some ac-voltage ripple. However, it can be seen that the voltage ripple of the RPPM scheme is slightly larger than that of the standard PWM scheme, although their magnitudes are close to each other. The low-frequency voltage ripple of the RPPM scheme cannot be seen easily in this figure and will be examined closely in enlarged figure later.

Measured waveforms of the converter's output voltage and inductor current of the RPWM scheme with $N = 16$ and $N = 1$ are shown in Fig. 8(c) and (d), respectively. Unlike those of the standard PWM and RPPM schemes, the output voltage and inductor current of RPWM scheme has significantly larger ripple. The output voltage comprises both low- and high-frequency ripple.

B. Comparison of Output-Voltage Ripple

Under the assumption of an ideal low-pass filter, the voltage ripple induced by the continuous noise in the three switching schemes are given in (27), (28), and (29). The output voltage of the converter was monitored and recorded. It should be noted that the practical output-voltage ripple actually consists of two

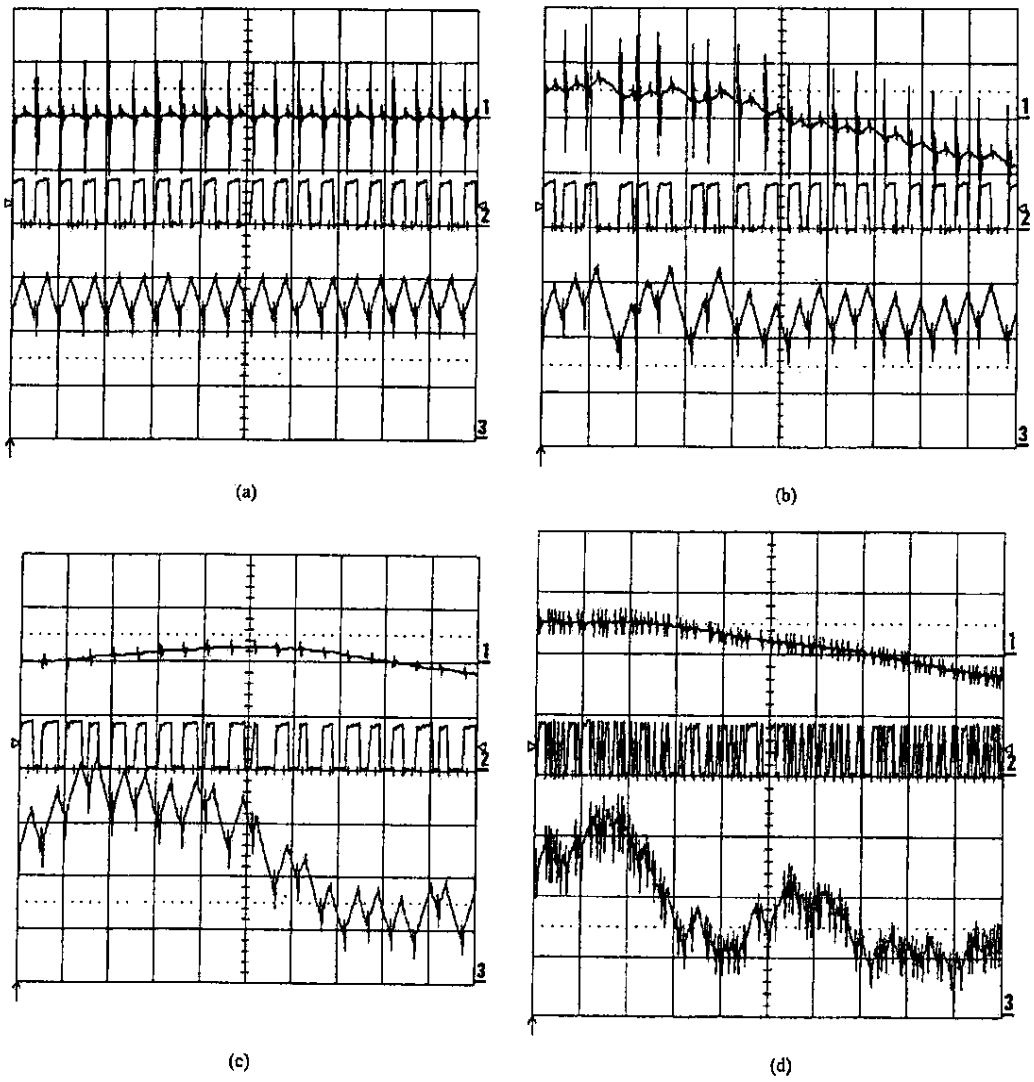

Fig. 9. (a) Measured output-voltage ripple (upper: 0.5 V/div), gating signal (middle: 5 V/div.) and inductor current (lower: 1 A/div.) of buck converter under the standard PWM scheme (time: 0.1 ms/div.). (b) Measured output-voltage ripple (upper: 0.5 V/div), gating signal (middle: 5 V/div.), and inductor current (lower: 1 A/div.) of buck converter under the RPPM scheme (time: 0.1 ms/div.). (c) Measured output-voltage ripple (upper: 5 V/div), gating signal (middle: 5 V/div.), and inductor current (lower: 1 A/div.) of buck converter under the RPWM scheme with $N = 16$ (time: 0.1 ms/div.). (d) Measured output-voltage ripple (upper: 5 V/div), gating signal (middle: 5 V/div.), and inductor current (lower: 1 A/div.) of buck converter under the RPWM scheme with $N = 1$ (time: 0.1 ms/div.).

components in general. Because of the nonideal nature of the low-pass filter, voltage ripple due to the switching harmonics ($\Delta V_{\text{harmonics}}$) does exist. The output voltage ΔV_o is therefore

$$\Delta V_o = \Delta V_{\text{harmonics}} + \Delta V_{\text{noise}} \tag{30}$$

where $\Delta V_{\text{harmonics}}$ and ΔV_{noise} contribute to the high-frequency and low-frequency ripple, respectively.

In order to examine the voltage ripple closely, the switching waveforms were recorded and displayed in a smaller time frame (0.1 ms instead of 1 ms per division as in Figs. 8). The voltage signal was monitored with ac coupling so that the voltage ripple could be observed clearly. Fig. 9(a) shows the measured converter output voltage, gating signal, and inductor current of the standard PWM scheme. The scale of the Y axis for the voltage is 0.5 V per division. The output voltage consists of some switching transients and some high-frequency (19.6 kHz) voltage ripple. This voltage ripple is due to the use of nonideal low-pass filter, i.e., the switching harmonic component is significantly attenuated, but not totally eliminated, by the low-pass filter. However, no low-frequency voltage ripple is observed because there is no continuous noise-induced voltage ripple in the standard PWM scheme.

The measurements of the output-voltage, gating signal, and inductor current under the RPPM scheme are shown in Fig. 9(b). It can be seen that the RPPM scheme has a slightly larger voltage ripple than the PWM scheme. The inductor current ripple in the RPPM scheme is also higher than

that in the PWM scheme. Besides the high-frequency voltage ripple (19.6 kHz), some low-frequency voltage fluctuation of approximately 1 V (peak to peak) is also observed in the output voltage. This observation confirms the prediction that the continuous noise within the passband of the filter causes some low-frequency voltage ripple in the RPPM.

The RPWM scheme is then tested with $N = 16$ and $N = 1$. With $N = 16$, the measurements are shown in Fig. 9(c). It should be noted that the time frame is still 0.1 ms per division as in Fig. 9(a) and (b), but the Y scale for the voltage is increased from 0.5 V per division to 5 V per division. It is obvious that the low-frequency voltage ripple observed is significantly larger than that of the RPPM. This observation agrees with the predictions that, under the same switching frequency (19.6 kHz in PWM, RPPM, and RPWM with $N = 16$) and filtering conditions.

1) Randomized switching dc–dc power conversion schemes have an inherently larger voltage ripple than the deterministic PWM scheme (because of the extra noise-induced voltage ripple caused by the continuous noise spectrum within the passband).
2) The RPPM scheme has a much smaller voltage ripple than the RPWM scheme. The RPWM scheme was also tested with $N = 1$. That is, the pulse is either one or zero in the entire switching period. The sampling frequency is now set at 16 × 19.6 kHz ($f_{sp} = 313.6$ kHz). For $N = 1$, the switching becomes asynchronous and the average switching frequency is given by $f_{sw} = D(1 - D)f_{sp}$. For $D = 0.5$, $f_{sw} = f_{sp}/4$. Fig. 9(d) shows the corresponding measurements. It can be seen that these measurements are similar to that of the RPWM scheme with $N = 16$. Although the average switching of RPWM with $N = 1$ is approximately four times that of RPWM with $N = 16$, the magnitudes of the voltage ripple for $N = 1$ and $N = 16$ are essentially the same. This result confirms the prediction in (17) that the noise ripple in RPWM scheme depends on the product of Nf_{sp} instead of f_{sp}.

In addition, other observations that confirm the theoretical predictions are as follows.

- The PWM scheme has no low-frequency voltage ripple (some switching ripple is present because the filter is not ideal).
- The RPPM has both low-frequency and some high-frequency ripple.
- The RPWM ($N = 1$) has low-frequency ripple only as predicted earlier and in [18].

The presence of the low-frequency ripple is due to the low-frequency part (within the passband of the low-pass filter) of the continuous spectrum in the randomized schemes.

C. Comparison of the PWM, RPPM, and RPWM Schemes

In summary, a standard PWM scheme with constant switching frequency for dc–dc power conversion has discrete harmonics at the switching frequency and its multiples. RPPM has both discrete harmonics and continuous noise. Since the power of the discrete harmonics and noise remains constant, the magnitude of the discrete harmonics in the RPPM scheme is smaller than that in the standard PWM scheme. Because the pulse width in the RPPM is as deterministic as that of the PWM scheme, the voltage ripple in the RPPM converter output is only slightly larger than that in the standard PWM converter. This implies that the noise level in the RPPM scheme is also small (as most of the noise power is associated with the discrete harmonics rather than the continuous noise). However, such a feature leads to small noise-induced voltage harmonics as predicted and observed. Among the three schemes tested, the RPWM scheme is the most inferior method in terms of the output-voltage ripple. The fact that the discrete harmonics can be greatly reduced or even totally eliminated in the RPWM scheme means that most of or all the noise power is associated with the continuous noise. This leads to high-noise-induced low-frequency voltage ripple. In addition, although the mean duty cycle is the same as the desired value, the continuous variation of the duty cycle results in large low-frequency voltage ripple.

V. Conclusions and Discussions

A detailed analysis on the RPWM and RPPM schemes for dc–dc power converters is presented. The theory developed in this paper shows that randomized schemes, because of the presence of the continuous noise, have an inherent noise-induced low-frequency voltage ripple problem when compared with the deterministic PWM method. The main reason for this is the continuous noise spectrum within the passband of the low-pass filter. The possible effect of such continuous low-frequency components includes extra fluctuation of the converter output voltage. The relationship of the noise and the resulting extra voltage ripple is established in this paper. These predictions arising from the theoretical analysis are confirmed by measurements obtained from a buck converter. The open-loop results obtained in this study highlight the low-frequency voltage ripple problem in the RPWM dc–dc converters. Research on the suppression of the voltage ripple using closed-loop control is being conducted.

The advantages of randomized modulation [1]–[14] are more obvious in dc–ac electronic drives than in dc–dc switched mode power supply. The key difference lies in the requirements of each application. The tight control in the voltage level of an inverter is not as important as that in a switched mode power supply. For motor drives, a slight fluctuation of voltage may be acceptable. The randomness introduced in the inverter's PWM switching spreads some or all of the discrete harmonics over the spectrum as continuous noise as in the dc–dc randomized switching schemes. The reduction of discrete harmonics has the advantage of lowering acoustic noise emission from and mechanical vibration in the motor. Normal operating switching frequency of many low-power dc–dc switched mode power supplies is in the hundreds of kilohertz or above. Thus, they cannot take advantage of acoustic noise reduction unless the power converter is employed in some high-power applications (such as high-power dc drives) with switching frequency in the audio frequency range.

Due to space constraints, the detailed proofs have been omitted. They can be obtained by contacting the authors.

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S. Y. (Ron) Hui (SM'94), for a photograph and biography, see this issue, p. 1045.

Yash Shrivastava (S'90–M'92), for a photograph and biography, see this issue, p. 1045.

S. Sathiakumar, for a photograph and biography, see this issue, p. 1045.



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EXHIBIT 25
(Spread Spectrum Clock Generation for the Reduction of Radiated Emissions)

Spread Spectrum Clock Generation for the Reduction of Radiated Emissions

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Abstract : A method is presented for reducing the radiated emissions of an electronic device by frequency modulating (FM) the system clock. This method, referred to as Spread Spectrum Clock Generation, or SSCG, is applicable to most microprocessor based systems. A unique waveform used to frequency modulate a digital clock signal results in a spectrum with sideband harmonics that are nearly uniform in amplitude when measured with an EMI receiver. This has the effect of spreading the energy of a discrete frequency harmonic over a wider bandwidth, thereby reducing the amplitudes of the harmonics. Attenuation as high as 13 dB is presented using an experimental setup, an actual SSCG integrated circuit, and theoretically computed results.

Introduction

In today's electronic products, the need for greater performance and throughput often dictates the need for higher operating frequencies. The fundamental operating frequencies of microprocessors in use today has exceeded 50 MHz and, with advances in solid state technology, these frequencies will continue to increase. However, along with this increase in frequency often comes increases in electromagnetic interference (EMI). When clock signals or any signals derived from the clock such as data and address buses contribute significantly to the radiated emissions of the system, filters may be used to increase the rise and fall times of the signals, thus reducing the amplitudes of higher order harmonics. This method can be effective provided few signals need to be filtered. Filtering more than a few signals can be difficult since space to locate additional components on printed circuit boards (PCB) is often scarce. This is compounded further with 32-bit microprocessors where data and address buses consume the majority of wiring channels.

This paper discusses a technique to simultaneously reduce the emissions from all signals synchronized with a clock signal. This technique intentionally broadbands a signal which is normally narrowband, spreading the energy contained within the signal over a bandwidth wider than the receiver bandwidth. This technique, hereinafter referred to as *Spread Spectrum Clock Generation*, or *SSCG* [1], is analogous to spread spectrum techniques used in communications [2] in that the energy of the intended signal is spread over a wider bandwidth.

The spreading of the energy in the clock signal is accomplished by frequency modulating (FM) the clock signal with a unique modulating waveform. This is demonstrated in Figure 1, where a harmonic of a clock signal is shown. In the frequency domain, the *nth* harmonic of a clock signal is represented by a delta function centered at a frequency of *n* times the fundamental frequency of the clock signal . With SSCG, the energy at each of these harmonics is spread over a wider bandwidth, thereby reducing the peak amplitude. In addition, the bandwidth over which each harmonic is spread increases linearly with frequency so that the attenuation provided by SSCG also increases linearly with frequency. The resulting attenuation, in dB, of a 20 MHz clock signal is shown in Figure 2. The attenuation of the *nth* clock harmonic is defined as the ratio of the amplitude of the *nth* harmonic of the non-modulated clock signal to the amplitude of the *nth* harmonic of the modulated clock signal. As seen in Figure 2, the initial value of the attenuation provided by SSCG is approximately 2 dB at the third clock harmonic, increasing to approximately 10 dB at 400 MHz!

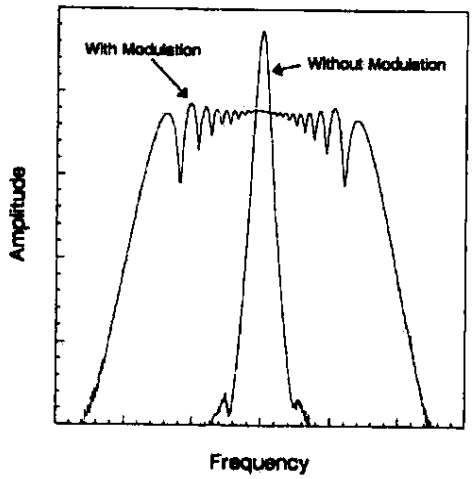

Figure 1. Frequency domain representation at a harmonic of a trapezoidal clock signal with and without SSCG.

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Discussion

As previously stated, SSCG reduces the amplitude of the harmonics of a clock by frequency modulating the signal. Frequency modulation is defined as that type of modulation in which the instantaneous frequency of the signal to be modulated is equal to the constant frequency of the signal plus a time-varying component that is proportional to the magnitude of the modulating signal [3]. A simple example is frequency modulation of a sinusoidal signal $F(t)$, given by

$$F(t) = A\sin\theta(t) \qquad (1)$$

where $\theta(t)$ is the phase angle which is varied as a result of the modulation. The instantaneous frequency of this signal is given by

$$2\pi f_i(t) = \frac{d}{dt}\theta(t) = 2\pi f_c + KV(t) \qquad (2)$$

where f_c is the constant frequency of the non-modulated signal, $V(t)$ represents the modulating signal, and K is a proportionality constant. The frequency of the modulating signal $V(t)$ is given by f_m. The peak frequency deviation Δf_c represents the plus or minus peak variation from the frequency f_c of the modulated signal and, when $V(t)$ is symmetrical, is given by

$$\Delta f_c = \frac{1}{2\pi}K\left[V(t)\right]_{max} \qquad (3)$$

As a result of the frequency modulation, sideband harmonics with a spacing of f_m will be introduced and concentrated around the harmonics of the signal which is being modulated. Analytical expressions for the frequency spectrum of the sinusoidal modulation of a sinusoid signal are easily obtained and found in most textbooks on communication theory [4]. However, determining analytical expressions for the modulation of more complex signals is much more difficult.

The key to maximizing the attenuation of a clock signal and its harmonics is the modulating waveform. Although much easier to analyze and implement, a sinusoidal modulating waveform does not provide optimum attenuation of the clock harmonics. The energy in the spectrum of the modulated waveform will tend to concentrate at those frequencies corresponding to points in the modulating waveform where the time derivative is small [3]. This is demonstrated in Figure 3 (a) where a sinusoidal signal is used to frequency modulate a clock signal. The resulting spectrum at a harmonic of a clock signal modulated with a sinusoid signal is shown in Figure 3 (b). As expected, the spectrum exhibits a peaking of the amplitude at frequencies where the time derivative of the sine wave is zero. At frequencies corresponding to the zero-crossing of the sine wave in Figure 3 (a), the amplitude is reduced since the time derivative of the sine wave is greatest. Sinusoidal modulation has been proposed for reducing the EMI of a switching power supply but does not provide optimum attenuation in the frequency range 30 -1000 MHz for the receiver bandwidth required [5].

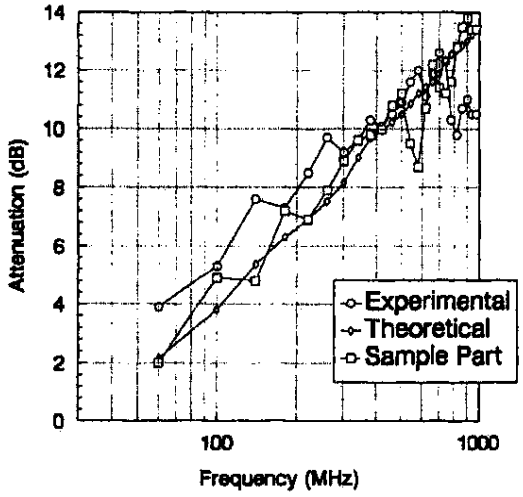

Figure 2. Measured and theoretical values of attenuation provided by SSCG.

Although some attenuation of the amplitudes of the clock signal and its harmonics is obtained with a sinusoidal modulating signal, additional attenuation could be obtained if the two peaks in the amplitudes shown Figure 3 (b) could be reduced. These peaks are reduced when the triangular wave shown in Figure 3 (c) is used to modulate the clock signal . Since the time derivative of the triangular wave at its zero crossing is less than the time derivative of the sine wave of Figure 3 (a), the amplitudes at the center of the spectrum are slightly increased. However, this is offset by a reduction in the amplitudes at the edges of the spectrum. Finally, by decreasing the time derivative at the zero crossing and increasing the time derivative at the peaks of the modulating waveform, such as in Figure 3 (e), a fairly uniform spectrum is obtained, as shown in Figure 3 (f). The modulating waveform shown in Figure 3 (e) was empirically derived given the insight provided by Figures 3 (a) - (d) and was used to obtain the attenuation in Figure 2.

As previously stated, deriving analytical expressions for the spectrum of a clock signal modulated by a signal other than a sine wave is difficult. However, numerical methods can be employed to compute the spectrum provided by a particular modulating waveform. Since the modulated clock signal is periodic, with a period equal to $1/f_m$, the Fourier series of the

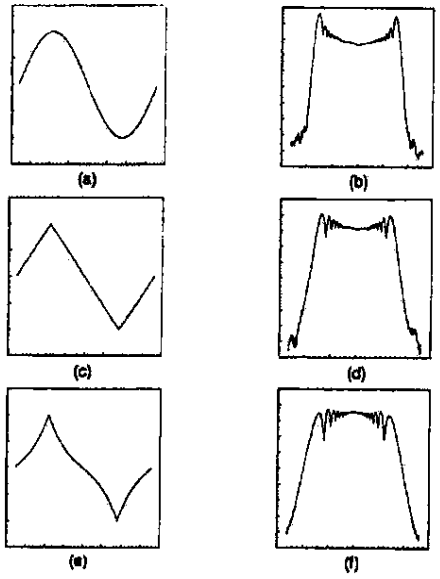

Figure 3. Sinusoidal modulating signal (a) and the resulting spectrum (b), triangular modulating signal (c) and the resulting spectrum (d), and SSCG modulating signal (e) and the resulting spectrum (f).

modulated clock signal can be found. Consider the clock signal shown in Figure 4, represented by $A(t)$. Although greatly exaggerated in Figure 4, the frequency of $A(t)$ varies over the period T of the modulating waveform. Within one period are M intervals where the value of $A(t)$ is +5 volts. The jth interval where the clock signal is non-zero is given by (t_j^-, t_j^+). From Equations 1 and 2, the phase angle of $A(t)$ is given by

$$\theta(t) = \int_{-\infty}^{t} 2\pi f_i(t)dt \tag{4}$$

where $f_i(t)$ is the instantaneous frequency shown in Figure 3 (e). Since $f_i(t)$ is known, this integration can be performed analytically or numerically. The Fourier coefficients of $A(t)$ are given by [6]

$$a_n = \frac{2}{T}\int_{-T/2}^{T/2} A(t)\cos(n2\pi f_m t)dt \tag{5}$$

and

$$b_n = \frac{2}{T}\int_{-T/2}^{T/2} A(t)\sin(n2\pi f_m t)dt \tag{6}$$

where $n = 0, 1, 2, \ldots$. Interestingly, $A(t)$ is either +5 volts or 0, therefore if the intervals over which $A(t)$ is equal to +5 volts can be determined, the integrations in Equations 5 and 6 can be

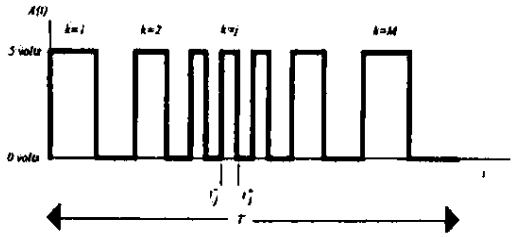

Figure 4. Time domain representation of the modulated clock signal.

performed analytically. Recognizing that $A(t)$ can be represented by the following expression

$$A(t) = \begin{cases} 5 & ; \quad \sin\theta(t) \geq 0 \\ 0 & ; \quad \sin\theta(t) < 0 \end{cases} \tag{7}$$

the intervals (t_j^-, t_j^+) in which the value of $A(t)$ is +5 volts are found by first finding all the zeroes of $\sin\theta(t)$. These intervals will continuously vary depending on the modulating frequency and the modulating waveform. However, once these intervals are found, the Fourier coefficients are given by the following expressions

$$a_n = 5\frac{2}{T}\sum_{k=1}^{M} \frac{\sin(n2\pi f_m t)}{n2\pi f_m}\Bigg|_{t=t_j^-}^{t=t_j^+} \tag{8}$$

and

$$b_n = 5\frac{-2}{T}\sum_{k=1}^{M} \frac{\cos(n2\pi f_m t)}{n2\pi f_m}\Bigg|_{t=t_j^-}^{t=t_j^+} \tag{9}$$

The amplitude of the nth sideband harmonic, represented by C_n, will be given by

$$|C_n| = \sqrt{a_n^2 + b_n^2} \tag{10}$$

In the frequency domain, the modulated clock signal is represented by delta functions at integer multiples of f_m with amplitudes given by Equation 10. Although these harmonics will be continuous, the amplitudes will be maximum around the harmonics of the clock signal being modulated. Therefore, when computing the attenuation provided by SSCG, only those sideband harmonics lying within a bandwidth centered at the harmonics of the clock signal need to be measured. Only those sideband harmonics which lie in a $\pm 3\Delta f_c$ bandwidth have significant amplitudes and need to be considered for accurate values of attenuation. In addition, the receiver bandwidth must be accounted for to correctly compute the measured amplitudes. For example, the 3 dB receiver-bandwidth specified in the frequency

range 30 - 1000 MHz is 100 kHz. Therefore, each sideband harmonic which lies within this 100 kHz bandwidth will contribute to the net amplitude measured by the receiver. Since each sideband harmonic is at a unique frequency, the net amplitude measured by the receiver will be equal to the sum of the amplitudes of all sideband harmonics which lie within the receiver bandwidth, regardless of the phase angle between these harmonics.

Experimental Results

In order to measure the attenuation provided by SSCG, the configuration shown in Figure 5 is used. The unique modulating waveform of Figure 3 (e) is provided by an arbitrary waveform generator, whose output is fed to a frequency synthesizer which provides a frequency modulated sine wave. This sine wave is amplified and converted to a 5-volt square wave by a zero-crossing detection circuit. The resulting modulated clock signal is available at a BNC connector for direct measurement of the attenuation or can be transmitted via fiber optic cable to an actual product under test.

Measured attenuation of the peak amplitudes of the odd harmonics of the clock signal using the setup of Figure 5 are found in Figure 2, labeled experimental data. The non-modulated frequency of the clock signal used in these measurements is 20 MHz with a duty cycle of approximately 50%. The peak deviation of the modulation is ±125 kHz. Also included in Figure 2 are theoretical results computed using the Fourier series expansion of the modulated clock signal given in Equations 8 and 9. Given the unequal duty cycles of each case considered in Figure 2, good agreement is found between the measured and theoretical results. Since the duty cycle of the clock signal is approximately 50%, the amplitudes of the even harmonics will be significantly lower than the amplitudes of the odd harmonics and will not be of concern. Therefore, only the attenuation of the odd harmonics of the clock signal is included in Figure 2.

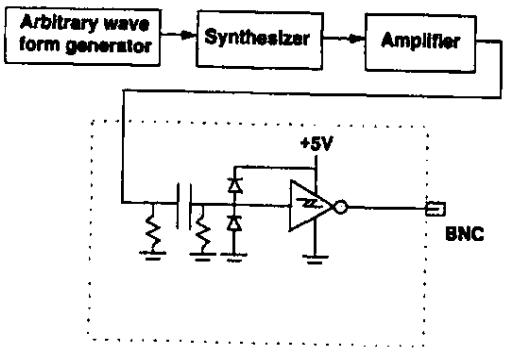

Figure 5. Experimental setup for implementation of SSCG.

Also included in the experimental results of Figure 2 are data measured using an implementation of SSCG in an integrated circuit (IC) package, as shown in Figure 6. This digital implementation of SSCG provides nearly identical attenuation as the experimental setup of Figure 5. This IC has been verified in a product and has good agreement with the attenuation in Figure 2. A crystal or oscillator used to provide the primary clocking signal to a digital system can be easily replaced by this IC package. SSCG can be easily implemented in many electronic products, such as personal computers and printers, reducing the costs associated with EMC compliance. In some cases, modifications to SSCG or system designs may be required, such as limiting the peak deviation or increasing tolerances required by two circuits communicating asynchronously. In other cases, such as video clock circuits, SSCG may not be used due to an observable wavering in the video display.

Conclusions

By frequency modulating a digital clock signal with a unique waveform, the amplitudes of the harmonics of the clock signal and all signals synchronized to it are significantly reduced. This technique is referred to as Spread Spectrum Clock Generation, or SSCG. A modulating waveform was introduced which optimized the attenuation of the harmonics of the clock signal. It was demonstrated with experimental and theoretical data that attenuation of the clock harmonics by as much as 13 dB is achievable with SSCG, with the attenuation increasing with frequency. Even higher values of attenuation are possible with greater peak deviations when allowed by the system design. SSCG can be implemented in a wide array of product applications significantly reducing the cost of EMC compliance.



Figure 6. Photograph of integrated circuit implementation of SSCG (courtesy of International Microcuits Inc.).

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EXHIBIT 26
(Japanese Patent 58-27440 and Translation)

⑲ 日本国特許庁（JP）　⑪ 特許出願公開

⑫ 公開特許公報（A）　昭58—27440

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H 03 L 7/18　6964—5 J

発明の数　1
審査請求　未請求

（全 6 頁）

⑭PLLシンセサイザ

⑳特　願　昭56—125807
㉒出　願　昭56(1981)8月10日
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明　細　書

1. 発明の名称

PLLシンセサイザ

2. 特許請求の範囲

(1) 入力電圧レベルに応じて出力発振周波数が変化する電圧制御発振器と、電圧制御発振器の出力発振周波数を設定値Nで分周した分周周波数を出力するプログラマブルデバイダと、プログラマブルデバイダから出力される分周周波数と基準周波数との位相を比較して位相差に応じた電圧を出力する位相比較器と、位相比較器の出力と電圧制御発振器の入力との間に接続されたローパスフィルタと増幅器とを有し、基準周波数にプログラマブルデバイダの設定値Nを乗じた周波数を電圧制御発振器から出力するようにしたPLLシンセサイザにおいて、電圧制御発振器の出力発振周波数帯域をバンド切換入力に応じて切換自在とすると共に、電圧制御発振器の入力電圧変化に対する出力発振周波数の変化幅をPLLシンセサイザ全体の出力発振周波数の変化幅よりも充分に小さくし、バンド切換入力にプログラマブルデバイダの設定値Nを入力して、プログラマブルデバイダの設定値Nに応じて電圧制御発振器の出力発振周波数帯域を切換自在として成ることを特徴とするPLLシンセサイザ。

3. 発明の詳細な説明

本発明は周波数シンセサイザのうち、特にフェーズロックループ、いわゆるPLLを使用したPLLシンセサイザに関するものである。

第1図は従来の一般的なPLLシンセサイザの回路図を示しており、(1)は位相比較器であり、基準周波数f_Rと分周周波数f_0との位相差に応じた電圧を出力するものである。(2)はローパスフィルタであり、位相比較器(1)の出力から高周波成分やノイズ成分を除去するものである。ローパスフィルタ(2)の出力は増幅器(3)により増幅されて電圧制御発振器(4)に入力される。電圧制御発振器(4)は入力電圧に応じた周波数の信号を発生し、その出力周波数はプログラマブルデバイダ(5)によって1/Nの

周波数に分周されて位相比較器(1)に分周周波数f_oとして入力されるものである。したがってＰＬＬシンセサイザの出力端子(6)からは$f_{out} = f_s \times N$の出力周波数が得られるものである。しかして例えばＰＬＬシンセサイザの出力周波数f_{out}として、第２図(a)に示すように10MHz ～ 20MHzを必要とする場合には基準周波数f_sを10KHzとすると、プログラマブルデバイダ(5)の設定値Ｎは第２図(c)に示すように1000 ～ 2000となり、また電圧制御発振器(4)の発振周波数帯域は第２図(b)に示すように10MHz ～ 20MHzが必要となる。ところがこのように電圧制御発振器(4)の入力電圧の変化に対する発振周波数の変化幅を大きくする際には、キャプチャレンジ、すなわちＰＬＬが最初ロックしていない状態から入力信号を変えて行った場合にその信号にロックできる電圧制御発振器(4)の発振周波数範囲（引込範囲）をも広くする必要があるので、どうしてもローパスフイルタ(2)の時定数τを小さくしなければならず、このために誘導信号除去特性が悪くなるという欠点があつた。

本発明は上述のような点に鑑みて為されたものであり、電圧制御発振器の入力電圧の変化に対する出力周波数の変化幅を広くすることなく、発振周波数帯域自体をプログラマブルデバイダの設定値Ｎに応じてシフトさせることにより、発振周波数帯域が広く、かつ誘導信号除去特性を良好としたＰＬＬシンセサイザを提供することを目的とするものである。

以下本発明の構成を図示実施例について説明する。第３図は本発明の一実施例に係るＰＬＬシンセサイザの構成を示すものであり、位相比較器(1)、ローパスフイルタ(2)、および増幅器(3)については第１図に示す従来例の場合と同様である。プログラマブルデバイダ(5)にはＤＡ変換器04が接続されており、このＤＡ変換器04はプログラマブルデバイダ(5)のデジタル的な設定値Ｎをアナログ信号に変換して電圧制御発振器(4)に供給しているものである。第３図中の破線で囲まれた部分は発振周波数帯域自体をシフトできるようにしたマルチバンド型の電圧制御発振器(4)の構成を示すものであり、Ｐチャンネル型のＭＯＳトランジスタP_1，P_2の各ソース電極は共に正電源V_{DD}に接続されており、また各ゲート電極は互いに同一電位となつているので、一方のＭＯＳトランジスタP_1のソースドレイン間に流れる電流と同じだけの電流が他方のＭＯＳトランジスタP_2のソースドレイン間にも流れてカレントミラー回路(7)を構成するようになっている。N_1はＮチャンネル型のＭＯＳトランジスタであり、そのゲート電極には電圧制御発振器(4)の入力電圧Vinが印加されるようになつている。このＭＯＳトランジスタN_1のソース電極には一端を負電源$-V_{ss}$に接続された抵抗R_1が接続されており、この抵抗R_1に流れる電流は入力電圧Vinに比例した値となり、この電流はＭＯＳトランジスタP_1に流れてＭＯＳトランジスタP_2にも同じだけの電流が流れることになる。ＭＯＳトランジスタP_3，N_3およびＭＯＳトランジスタP_4，N_4はそれぞれゲート電極を結合されて相補接続型のスイッチング回路(8)(9)を構成している。このスイッチング回路(8)(9)の出力には前記カレントミラー回路(7)からの出力電流により充放電されるコンデンサC_1が接続されている。しかしてスイッチング回路(8)(9)のゲート電極はフリップフロップ回路00を構成する一対のNANDゲートG_1，G_2の出力端子に接続されているので、NANDゲートG_1，G_2の出力に応じて交互にコンデンサC_1への充電電流が反転するようになっている。今、一方のNANDゲートG_1の出力がＬレベルであり、他方のNANDゲートG_2の出力がＨレベルであるとすると、ＭＯＳトランジスタP_4およびN_3がオンとなり、反対にＭＯＳトランジスタP_3およびN_4はオフとなる。したがつてコンデンサC_1の端子(11)は負電源$-V_{ss}$の電位となつて、他方の端子側からコンデンサC_1にＭＯＳトランジスタP_2の電流が充電される。しかして端子側の電位が上昇すると、インバータI_3～I_5が反転してフリップフロップ回路00の出力が反転する。すると今度はＭＯＳトランジスタP_3とN_3がオンとなり、反対にＭＯＳトランジスタP_4とN_4はオフとなる。これによつてコンデンサC_1の端子側が負電源$-V_{ss}$の電位と等しくなり、端子(11)にＭＯＳトラ

ンジスタP_2を介してＭＯＳトランジスタP_1の電流が流入してコンデンサC_1が逆方向に充電される。これによって端子(11)の電位が上昇するから、インバータI_1～I_4が反転して再びフリップフロップ回路(10)の出力が反転する。この繰り返し周波数はコンデンサC_1に流入するＭＯＳトランジスタP_2の電流によって変化し、この電流は入力電圧Vinに比例するので、結局出力端子(13)から得られる発振周波数fは入力電圧Vinに比例することになる。なお端子(14)はフリップフロップ回路(10)の発振を起動したり、あるいは停止させたりする発振制御端子である。

ここで入力電圧Vinの変化に対する出力発振周波数fの変化幅は入力電圧Vinの変化に対するＭＯＳトランジスタP_2のソースドレイン間電流の変化幅によって定まるから、抵抗R_1の値を変化させることによって入力電圧変化に対する出力発振周波数の変化幅を考えることができる。またＭＯＳトランジスタN_1のドレイン電極に接続された抵抗R_2は抵抗R_1よりも抵抗値を低く設定してあり、この抵抗R_2の値を変えると、入力電圧Vinが0のときにおける出力発振周波数、すなわちオフセット周波数f_0を変えることができるものである。本実施例においてはこの抵抗R_2と並列に、抵抗R_1と抵抗R_2との中間的な抵抗値を有する抵抗R_3をＮチャンネル型のＭＯＳトランジスタN_2を介して接続してある。このＭＯＳトランジスタN_2のゲート電極にはプログラマブルデバイダ(8)の設定値ＮをＤＡ変換したアナログ的な電圧が印加されており、したがって抵抗R_3に流れる電流はプログラマブルデバイダ(8)の設定値Ｎが増加するにつれて増大するようになっているものである。第４図(a)～(d)はこの動作を説明するものであり、第４図(b)に示すようにプログラマブルデバイダ(8)の設定値Ｎが1000のときにはＤＡ変換器(9)の出力電圧は、第４図(c)に示すように0となり、このために抵抗R_3には全く電流が流れない。したがってカレントミラー回路(7)の出力電流、すなわちコンデンサC_1の充電電流が少なくなるから、フリップフロップ回路(10)の発振周波数fは低くなる。このときの発振周波数fは抵抗R_2の値を適当に選定することにより、第４図(d)に示すように10MHz付近の出力周波数とすることができる。したがって基準周波数f_0が１０KHzであるとすると、ＰＬＬシンセサイザの出力周波数は第４図(a)に示すように正確に10MHzとなる。このとき電圧制御発振器(4)の入力電圧変化に対する出力周波数の変化区域は、第４図(d)に示すように10MHz近傍のみの極めて狭い範囲となっているから、ＰＬＬのキャプチャレンジは拡大する必要はなく、したがってローパスフィルタ(2)の時定数τは充分に大きくすることができるから、妨害信号除去特性を良好にすることができるようになっている。次にプログラマブルデバイダ(8)の設定値Ｎが、第４図(b)に示すように2000となったときには、ＤＡ変換された電圧は第４図(c)に示すように電圧Vmとなり、このときにはMOSトランジスタN_2の内部抵抗はほとんどゼロとなり、したがって抵抗R_3に流れる電流は最大となる。このためにカレントミラー回路(7)の出力電流、すなわちコンデンサC_1の充電電流が多くなるから、フリップフロップ回路(10)の発振周波数fは高くなる。このときの発振周波数fは抵抗値R_2の値を適当に選択することにより、第４図(d)に示すように20MHz付近の出力周波数とすることができる。したがって基準周波数f_0が10KHzであるとすると、ＰＬＬシンセサイザの出力周波数は第４図(a)に示すように正確に20MHzとなる。この場合にも電圧制御発振器(4)の入力電圧変化に対する出力周波数の変化区域は第４図(d)に示すように20MHz付近のきわめて狭い周波数範囲に限られているから、ローパスフィルタ(4)の時定数τは大きく設定しておくことができ、したがって妨害信号除去特性を良好にすることができるものである。さらにプログラマブルデバイダ(8)の設定値Ｎが1000から2000までの任意の整数値であるときには、ＤＡ変換器(9)の出力電圧は第４図(c)に示すように電圧Vmと０ボルトとの間の電圧値Vxとなり、電圧制御発振器(4)の発振周波数範囲は10MHzと20MHzとの間のごく狭い区域にシフトすることになる。したがってプログラマブルデバイダ(8)の設定値Ｎがどのような

値であっても、電圧制御発振器(4)の入力電圧の変化に対する出力周波数の変化幅は小さく、ローパスフイルタ(3)の時定数を大きく設定することができるので、妨害信号除去特性を良好にすることができるものである。なお本実施例においては電圧制御発振器(4)としてMOSICにより構成された回路例を示したが、プログラマブルデバイダ(5)の設定値Nに応じて発振周波数帯域をシフトできるようなものであれば、他の回路構成の電圧制御発振器(4)を使用することもできるものである。

本発明は以上のように構成されており、入力電圧レベルに応じて出力発振周波数が変化し、かつバンド切換入力に応じて出力発振周波数帯域が変化するようにしたマルチバンド型の電圧制御発振器を使用すると共に、この電圧制御発振器のバンド切換入力にプログラマブルデバイダの設定値Nを入力するようにしたものであるから、プログラマブルデバイダの設定値Nに応じて電圧制御発振器の出力発振周波数帯域を切換自在とすることができて、このためにPLLシンセサイザの出力発振周波数帯域幅を広く保ちながら、電圧制御発振器の入力電圧変化に対する出力発振周波数の変化幅を非常に小さく抑えることができ、したがってPLLのキャプチャレンジ（引込範囲）を広くする必要はなくなるからローパスフイルタの時定数τを大きく設定することができて、このために妨害信号除去特性が良好となるという利点を有するものである。

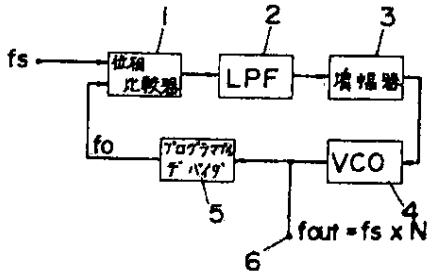
4. 図面の簡単な説明

第1図は従来のPLLシンセサイザのブロック図、第2図(a)(b)(c)は同上の動作説明図、第3図は本発明の一実施例の回路図、第4図(a)(b)(c)(d)は同上の動作説明図である。

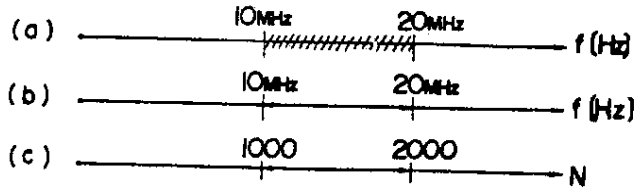
(1)は位相比較器、(2)はローパスフイルタ、(3)は増幅器、(4)は電圧制御発振器、(5)はプログラマブルデバイダ、(6)はDA変換器、R_1は抵抗、N_1はMOSトランジスタである。

代理人　弁理士　石田長七

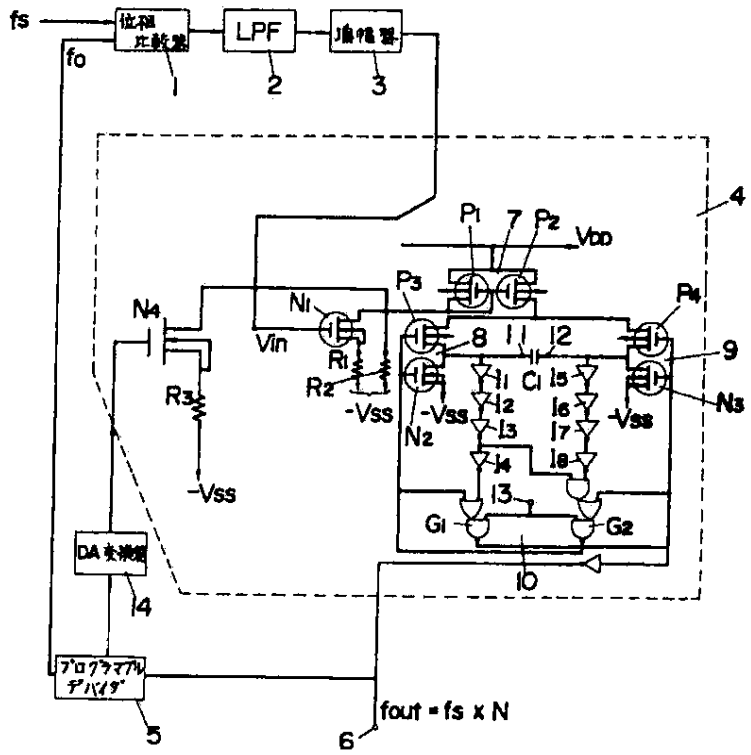
第1図



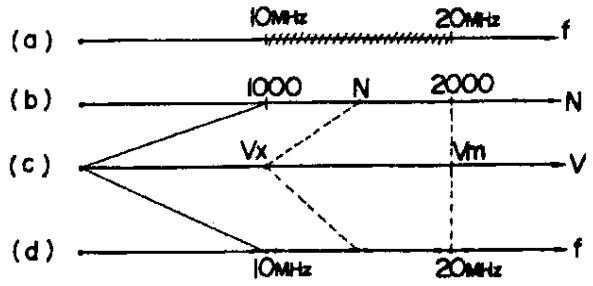
第2図



第３図



第４図



手　続　補　正　書（自発）

昭和５７年１月９日

特許庁長官 殿

1．事件の表示
昭和５６年特許願第１２５８０７号

2．発　明の名称
ＰＬＬシンセサイザ

3．補正をする者
事件との関係　特許出願人
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5．補正命令の日付
自　発

6．補正により増加する発明の数
な　し

7．補正の対象
明細書

8．補正の内容
別紙の通り

特許庁 57. 1. 11

訂　　正　　書

出願番号　　特願昭５６－１２５８０７号

1. 本願明細書第７頁第１９行目乃至第８頁第１行目の「抵抗R_0は抵抗R_1よりも抵抗値を低く設定してあり、この」を削除致します。

2. 同上第８頁第４行目乃至第５行目の「抵抗R_1と抵抗R_2との中間的な抵抗値を有する」を削除致します。

代理人　弁理士　　石　田　長　七

[19] THE PATENT OFFICE OF JAPAN (JP)
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(total 6 pages)

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[54] Title PLL synthesizer

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Specification

1. Title of Invention

PLL synthesizer

2. Scope of Patent Claim

A PLL synthesizer provided with a voltage controlled oscillator that alters the output oscillation frequency as a function of the input voltage level, a programmable divider that outputs the divided frequency following division of the output oscillation frequency of the voltage controlled oscillator by setting value N, a phase comparator that compares the phase of the divided frequency that was output from the programmable divider with the phase of the base frequency and that then outputs voltage in response to the phase difference, an amplifier and a low pass filter connected between the output of the phase comparator and the input of the voltage controlled oscillator, wherein the frequency following multiplication of the base frequency by the setting value N of the programmable divider is output from the voltage controlled oscillator, said synthesizer characterized by the fact that the output oscillation frequency band of the voltage controlled oscillator is set as the switch itself as a function of the band switch input, the fact that the altered width of the output oscillation frequency relative to the input voltage change of the voltage controlled oscillator is set adequately smaller than the altered width of the output oscillation frequency of the entire PLL synthesizer, and the fact that the output oscillation frequency band of the voltage controlled oscillator becomes the switch itself as a function of the setting value N of the programmable divider by the input of setting value N of the programmable divider into the band switch input.

3. Detailed Description of the Invention

The present invention relates to a PLL synthesizer, one type of frequency synthesizer, especially a synthesizer that uses phase lock loops, so-called PLL.

Figure 1 presents a circuit diagram of a conventional generic PLL synthesizer. Reference numeral (1) denotes a phase comparator that outputs voltage in response to the phase difference between the base frequency f_B and the divided frequency f_0. Reference numeral (2) denotes a low-pass filter that removes the high-frequency component and the noise component from the output of phase comparator (1). The output of low-pass filter (2) is amplified by amplifier (3) and is then input to voltage controlled oscillator (4). Voltage controlled oscillator (4) generates a frequency signal in response to the input voltage, and the output frequency is then divided into 1/N frequencies by programmable divider (5) and is input to phase comparator (1) as divided frequency f_0. Accordingly, what is obtained from output terminal (6) of the PLL synthesizer is output frequency

of $f_{out} = f_B \times N$. However, if the base frequency f_B is set at 10 KHz when 10 MHz to 20 MHz as shown in Figure 2 (a) is required as the output frequency f_{out} of the PLL synthesizer, for example, the setting value N of programmable divider (5) would be 1000 to 2000 as shown in Figure 2 (c) and the oscillation frequency band of voltage controlled oscillator (4) would have to be 10 MHz to 20 MHz as shown in Figure 2 (b). However, when increasing the altered width of the oscillation frequency relative to the change in input voltage of voltage controlled oscillator (4) in this manner, the time constant τ of low-pass filter (2) must be decreased since the oscillation frequency range (incoming range) of voltage controlled oscillator (4) that can be locked by signal must also be expanded when the input signal is altered from the capture range, specifically, the initial state unlocked state of PLL. This accounts for the defect of poor removal characteristics of interference signals.

The present invention was devised in light of aforementioned defects. The objective is to provide a PLL synthesizer having a broad oscillation frequency band and good removal characteristics of interference signals by shifting the oscillation frequency band itself as a function of the setting value N of a programmable divider rather than by expanding the altered width of the output frequency relative to change in the input voltage of the voltage controlled oscillator.

Embodiments that show the structure of the present invention are explained below. Figure 3 shows the structure of a PLL synthesizer pursuant to one embodiment of the present invention. Phase comparator (1), low-pass filter (2), and amplifier (3) are identical with those of the conventional example shown in Figure 1. DA converter (14) is connected to programmable divider (5). DA converter (14) is a device that converts digital setting value N of programmable divider (5) into analog signals that are provided to voltage controlled oscillator (4). The section enclosed by broken line in Figure 3 shows the structure of multiband type voltage controlled oscillator (4) that enables shift of the oscillation frequency band itself. Each source electrode of P channel-type MOS transistors P_1 and P_2 is connected to positive power source V_{DD} and each of the gate electrodes adopts the same potential. Thus, current mirror circuit (7) is constructed in which the same current as the current that flows between the source and drain of one MOS transistor P_1 flows between the source and drain of the other MOS transistor P_2. N_1 is an N channel MOS transistor. It is structured so that input voltage V_{in} of voltage controlled oscillator (4) would be applied to the gate electrode. Resistor R_1 in which one terminal is connected to negative power source V_{SS} is connected to the source electrode of this MOS transistor N_1, and the current that flows through this resistor R_1 is proportional to the input voltage V_{in}. This current flows through MOS transistor P_1 and the same current also flows through MOS transistor P_2. MOS transistors P_3, N_2 and P_4, N_3 comprise auxiliary connection type switching circuits (8), (9) that are provided with

gate electrodes. Capacitor C_1 that is charged/discharged by the output current from aforementioned current mirror circuit (7) is connected to the outputs of switching circuits (8), (9). However, the charging current to capacitor C_1 is alternately reversed as a function of the output of NAND gates G_1, G_2 since the gate electrodes of switching circuits (8), (9) are connected to the output terminals of a pair of NAND gates G_1, G_2 that comprise flip-flop circuit (10). Here, MOS transistors P_4 and N_3 turn ON when the output of one NAND gate G_1 is at the L level while the output of the other NAND gate G_2 is at the H level, and MOS transistors P_3 and N_2 turn OFF. Accordingly, terminal (11) of capacitor C_1 adopts the potential of negative power source V_{SS} while capacitor C_1 is charged by the current of MOS transistor P_2 from the other terminal (12). However, when the potential of terminal (12) rises, inverters I_5-I_8 are reversed and the output of flip-flop circuit (10) is reversed. Then MOS transistors P_3 and N_2 turn ON while MOS transistors P_4 and N_3 turn OFF. As a result, terminal (12) of capacitor C_1 adopts the same potential as negative power source V_{SS}, and current of MOS transistor P_2 flows into terminal (11) via MOS transistor P_3 to change capacitor C_1 in the opposite direction. As a result, since the potential of terminal (11) has risen, inverters I_1-I_4 are reversed and the output of flip-flop circuit (10) is reversed again. This repeating frequency is changed by the current of MOS transistor P_2 that feeds into capacitor C_1 and the current is proportional to the input voltage V_{in}. As a result, the oscillation frequency f derived from output terminal (6) becomes proportional to input voltage V_{in}. Terminal (12) is an oscillation control terminal that starts and stops oscillation of flip-flop circuit (10).

The altered width of the output oscillation frequency can be considered relative to change in input voltage due to alteration of the value of resistor R_1 since the altered width of output oscillation frequency f relative to change in input voltage V_{in} is determined by the altered width of source-drain current of MOS transistor P_1 relative to change in input voltage V_{in}. Furthermore, the output oscillation frequency at input voltage V_{in} of zero, specifically, the offset frequency f_a, can be altered when the value of resistor R_2 connected to the drain electrode of MOS transistor N_1 is altered. In this embodiment, resistor R_3 is connected via N channel type MOS transistor N_4 in parallel with this resistor R_2. Analog voltage following DA conversion of the setting value N of programmable divider (5) is applied to the gate electrode of MOS transistor N_4, with the result being an increase in the current flowing to resistor R_3 as the setting value N of programmable divider (5) increases. Figure 4 (a) - (d) explains this action. As shown in Figure 4 (b), when the setting value N of programmable divider (5) is 1000, the output voltage of DA converter (14) becomes zero, as shown in Figure 4 (c) and absolutely no current flows through resistor R_2 as a result. Accordingly, the output current of current mirror circuit (7), specifically, the charging current of capacitor C_1, decreases and the oscillation frequency f of flip-flop circuit (10)

falls. Oscillation frequency f at this time can be the output frequency near 10 MHz, as shown in Figure 4 (d), by selecting a suitable figure for the value of resistor R_2. Accordingly, when the base frequency f_B is 10 KHz, the output frequency of the PLL synthesizer would become exactly 10 MHz as shown in Figure 4 (a). The zone of change of the output frequency of voltage controlled oscillator (4) relative to change of the input voltage would become an extremely narrow range of only 10 MHz, as shown in Figure 4 (d). Consequently, the PLL capture range need not be increased greatly, with the result being that the time constant τ of low-pass filter (2) can be adequately enlarged. Thus, the characteristics of interference signal removal can be improved. Next, when the setting value N of programmable divider (5) is 2000, as shown in Figure 4 (b), the DA converted voltage would become voltage V_m as shown in Figure 4 (c), at which time the internal resistance of MOS transistor N_1 would become virtually zero. As a result, the current flowing to resistor R_2 would be maximized. The oscillation frequency f of flip-flop circuit (10) therefore rises since the output current of current mirror circuit (7), specifically, the charge current of capacitor C_1, increases. Oscillation frequency f can be set at an output frequency close to 20 MHz, as shown in Figure 4 (d), by suitably selecting the value of resistor R_3 at this time. Accordingly, the output frequency of the PLL synthesizer becomes precisely 20 MHz, as shown in Figure 4 (a), when base frequency f_B is set at 10 KHz. In this case as well, the time constant τ of voltage controlled oscillator (4) could be set large since the zone of change of the output frequency of voltage controlled oscillator (4) relative to change of the input voltage would be restricted to the extremely narrow frequency range near 20 MHz, as shown in Figure 4 (d). Accordingly, the characteristics of interference signal removal can be improved. Moreover, when the setting value N of programmable divider (5) is an arbitrary integer from 1000 to 2000, the output voltage of DA converter (14) would be the voltage value V_x between voltage V_m and zero volts, as shown in Figure 4 (c), and the oscillation frequency range of voltage controlled oscillator (4) could be shifted in an extremely narrow zone between 10 MHz and 20 MHz. Accordingly, the altered width of the output frequency relative to change of input voltage of voltage controlled oscillator (4) would be small regardless of the setting value N of programmable divider (5), and the time constant of low-pass filter (2) could be set large. Thus, the characteristics of interference signal removal can be improved. This embodiment is an example in which a circuit comprising MOS IC is structured as voltage controlled oscillator (4), but voltage controlled oscillators (4) having other circuit structures could be used instead if the oscillation frequency band can be shifted as a function of the setting value N of programmable divider (5).

The present invention with aforementioned structure uses a multiband type voltage controlled oscillator that alters the output oscillation frequency as a function of the input voltage level and that alters the output oscillation frequency band as a function of the band switch

input. It also inputs the setting value N of a programmable divider to the band switch input of a voltage controlled oscillator, with the result being that the output oscillation frequency band of the voltage controlled oscillator can be switched as a function of the setting value N of the programmable divider. Accordingly, the output oscillation frequency band width of the PLL synthesizer can be maintained at a wide level and the altered width of the output oscillation frequency relative to change in the input voltage of the voltage controlled oscillator can be held to a very small range. Thus, the PLL capture range (incoming range) need not be expanded greatly, with the result being that the time constant τ of the low-pass filter can be set at a large figure. Thus, the characteristics of interference signal removal can be improved.

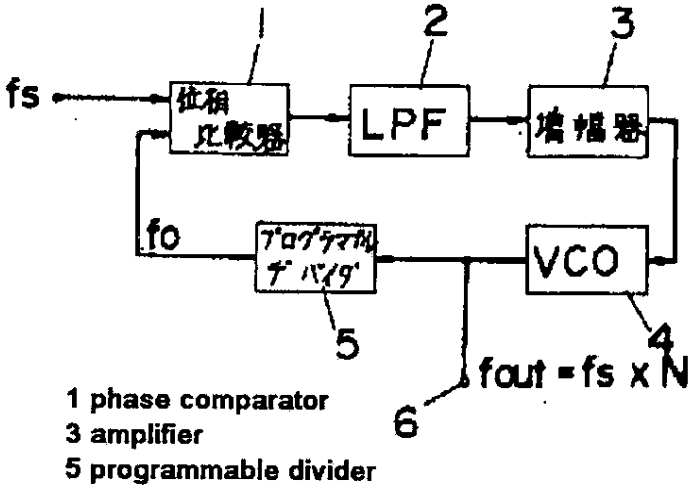
4. Brief Description of Drawings

Figure 1 is a block diagram of a conventional PLL synthesizer. Figure 2 (a) (b) (c) is an operating explanatory diagram thereof. Figure 3 is a circuit diagram of one embodiment of the present invention. Figure 4 (a) (b) (c) (d) is an operating explanatory diagram thereof.

(1) phase comparator, (2) low-pass filter, (3) amplifier, (4) voltage controlled oscillator, (5) programmable divider, (14) DA converter, R_1 resistor, N_4 MOS transistor.

Agent Attorney ISHIDA Choshichi

Figure 1



1 phase comparator
3 amplifier
5 programmable divider

Figure 2

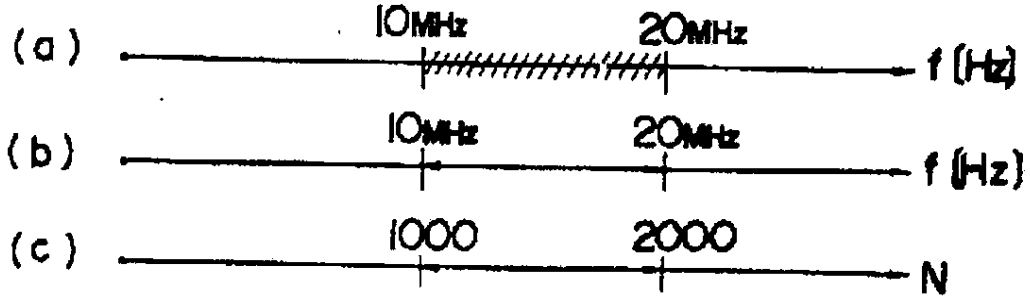


Figure 3

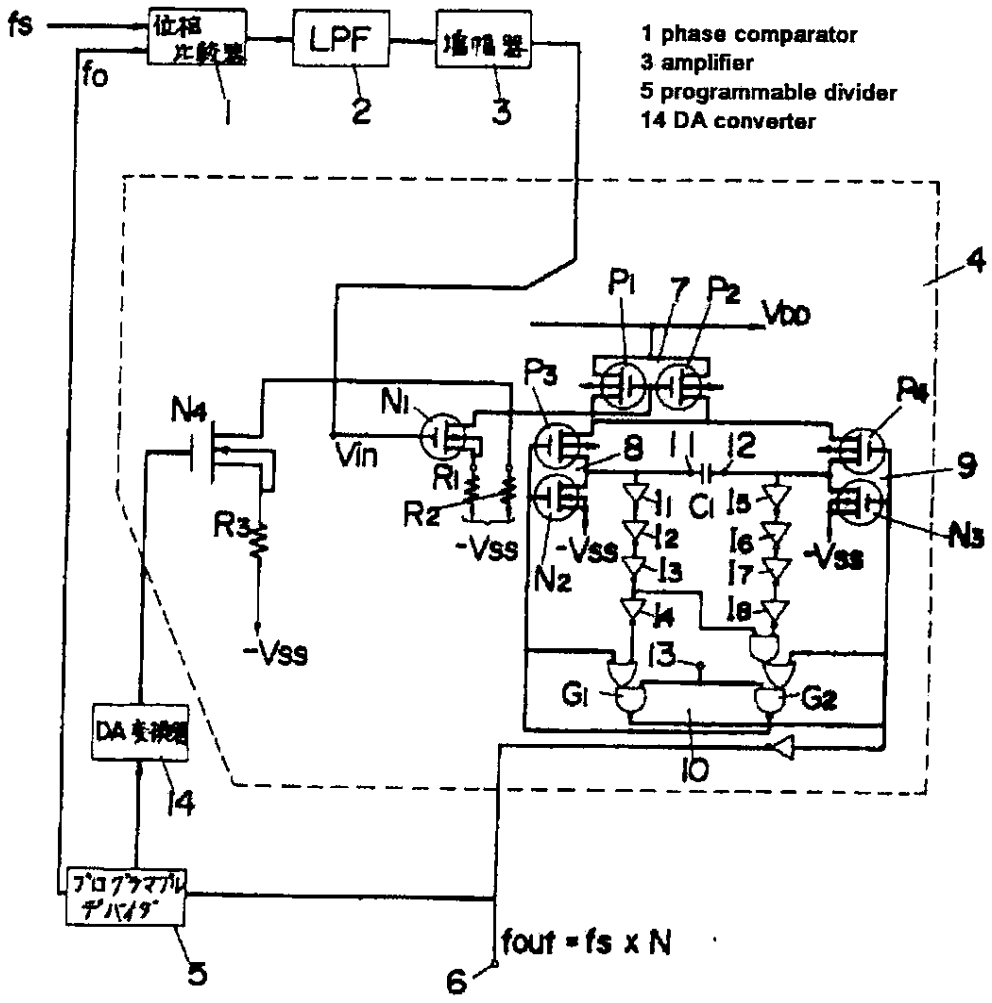

fs
fo
位相比較器
LPF
増幅器
1
2
3
1 phase comparator
3 amplifier
5 programmable divider
14 DA converter
4
P1
7
P2
Vdd
P3
P4
N1
N4
Vin
8
11
12
9
R1
R2
R3
-Vss
I1
Cl
I5
I2
I6
I3
I7
I4
I8
N2
N3
I3
G1
G2
10
DA変換器
14
プログラマブルデバイダ
5
6
fout = fs x N

Figure 4

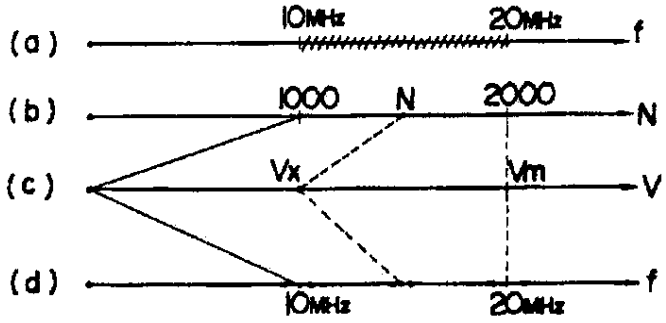


EXHIBIT 27
(USP 5,943,382)

US005943382A

United States Patent [19]

Li et al.

[11] Patent Number: 5,943,382

[45] Date of Patent: Aug. 24, 1999

[54] **DUAL-LOOP SPREAD-SPECTRUM CLOCK GENERATOR WITH MASTER PLL AND SLAVE VOLTAGE-MODULATION-LOCKED LOOP**

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[73] Assignee: **NeoMagic Corp.**, Santa Clara, Calif.

[21] Appl. No.: **08/990,899**

[22] Filed: **Dec. 15, 1997**

Related U.S. Application Data

[63] Continuation-in-part of application No. 08/701,814, Aug. 21, 1996, Pat. No. 5,757,338.

[51] **Int. Cl.**[6] **H03D 3/24**

[52] **U.S. Cl.** **375/376**; 375/200; 375/375

[58] **Field of Search** 375/200, 204, 375/375, 376; 331/7.8; 332/144

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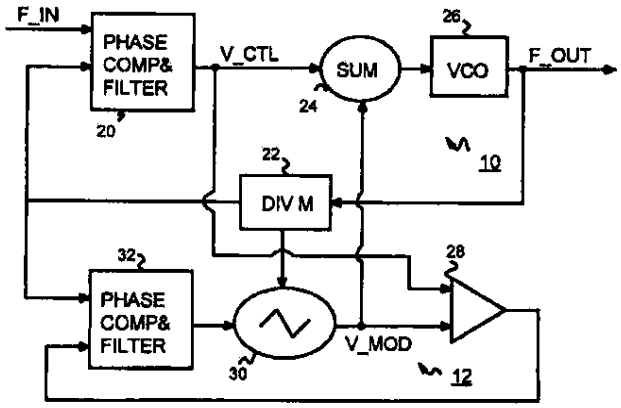
Primary Examiner—Stephan Chin
Assistant Examiner—Chieh M. Fan
Attorney, Agent, or Firm—Stuart T. Auvinen

[57] **ABSTRACT**

A clock generator produces a frequency-modulated clock. A master phase-locked loop (PLL) includes a voltage summer that outputs a voltage to a voltage-controlled oscillator (VCO). The voltage to the VCO determines the frequency of the clock generated. A modulated voltage is subtracted by the voltage summer to produce voltage and thus frequency modulations. This modulated voltage is produced by a second loop that operates as a slave to the master PLL. The slave loop is a voltage-locked loop. The peak amplitude of the modulated voltage is locked to a control voltage of the master PLL. The control voltage is a stable voltage input to the voltage summer that is generated by phase comparisons of the output clock to a reference clock. To overcome the problem of locking to the modulating output clock, phase comparison is performed only at the same point in the modulation cycle, at the beginning of each modulation cycle. Thus modulations do not affect phase comparisons. The modulated voltage is generated by a waveform generator in the slave loop. The waveform generator is controlled by a feedback divider that also controls when phase comparison is performed. The amplitude of the waveform is adjusted to track the control voltage of the master PLL by comparing the control voltage to the modulated voltage, but only at the beginning of the modulation cycle. The modulation amplitude is kept constant over different supply voltages, ambient temperatures, and process corners.

20 Claims, 4 Drawing Sheets



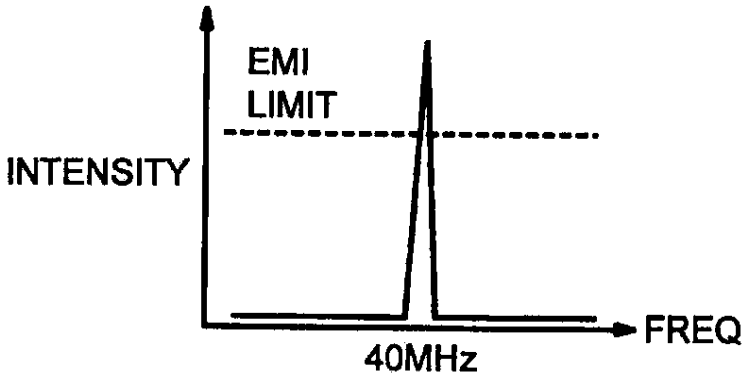


FIG. 1

PRIOR ART

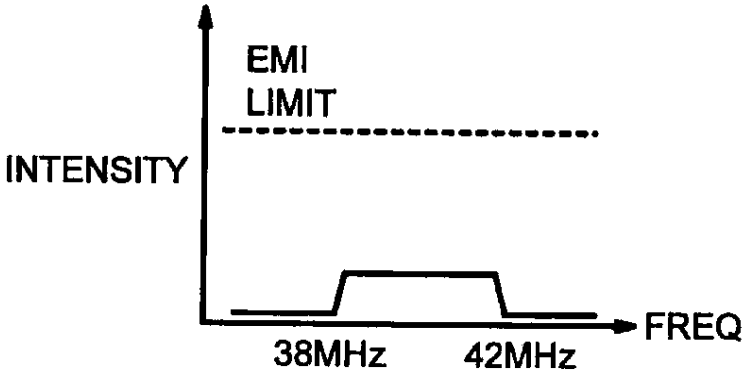


FIG. 2

PRIOR ART

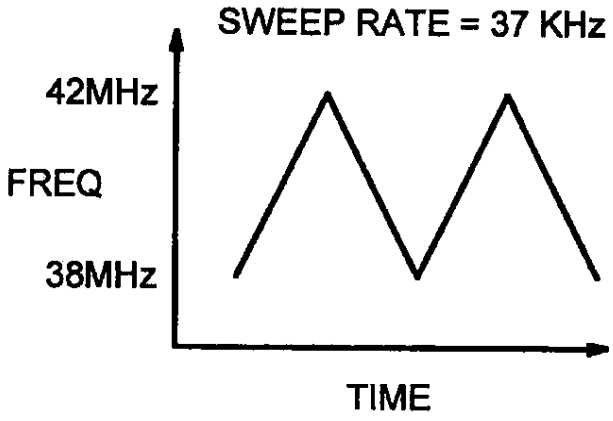


FIG. 3

PRIOR ART

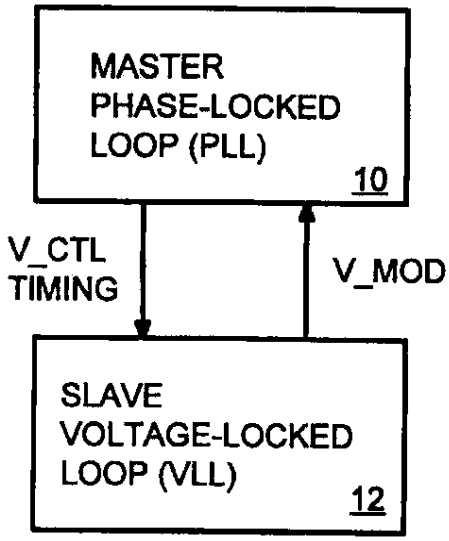


FIG. 4

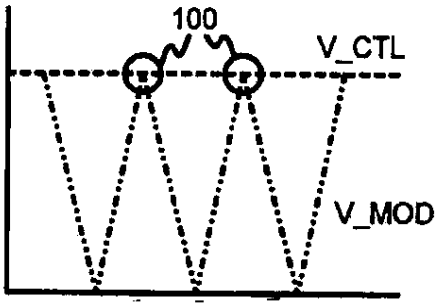


FIG. 5

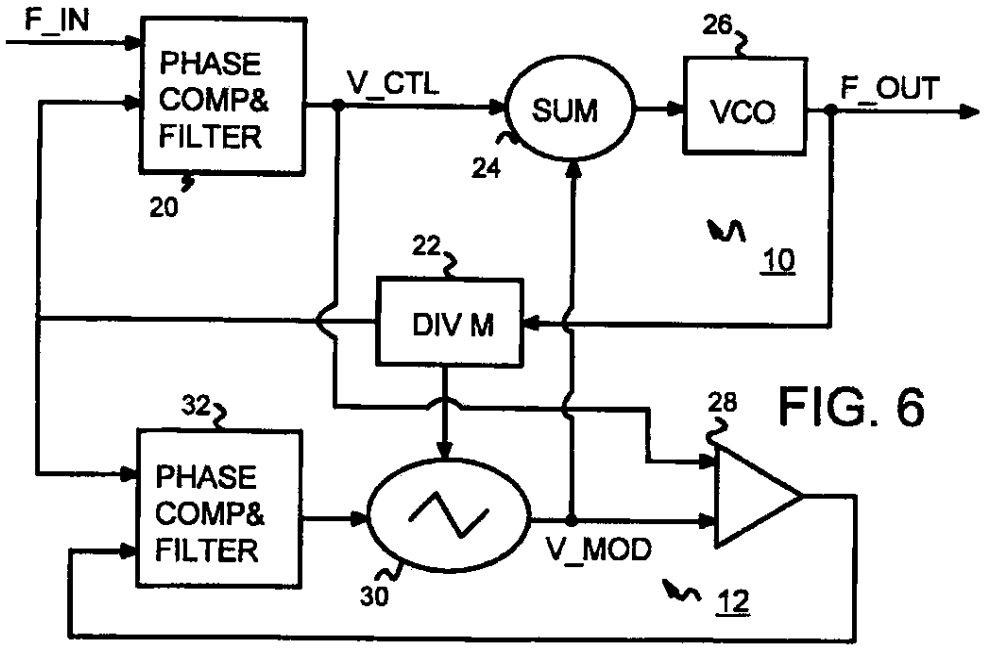


FIG. 6

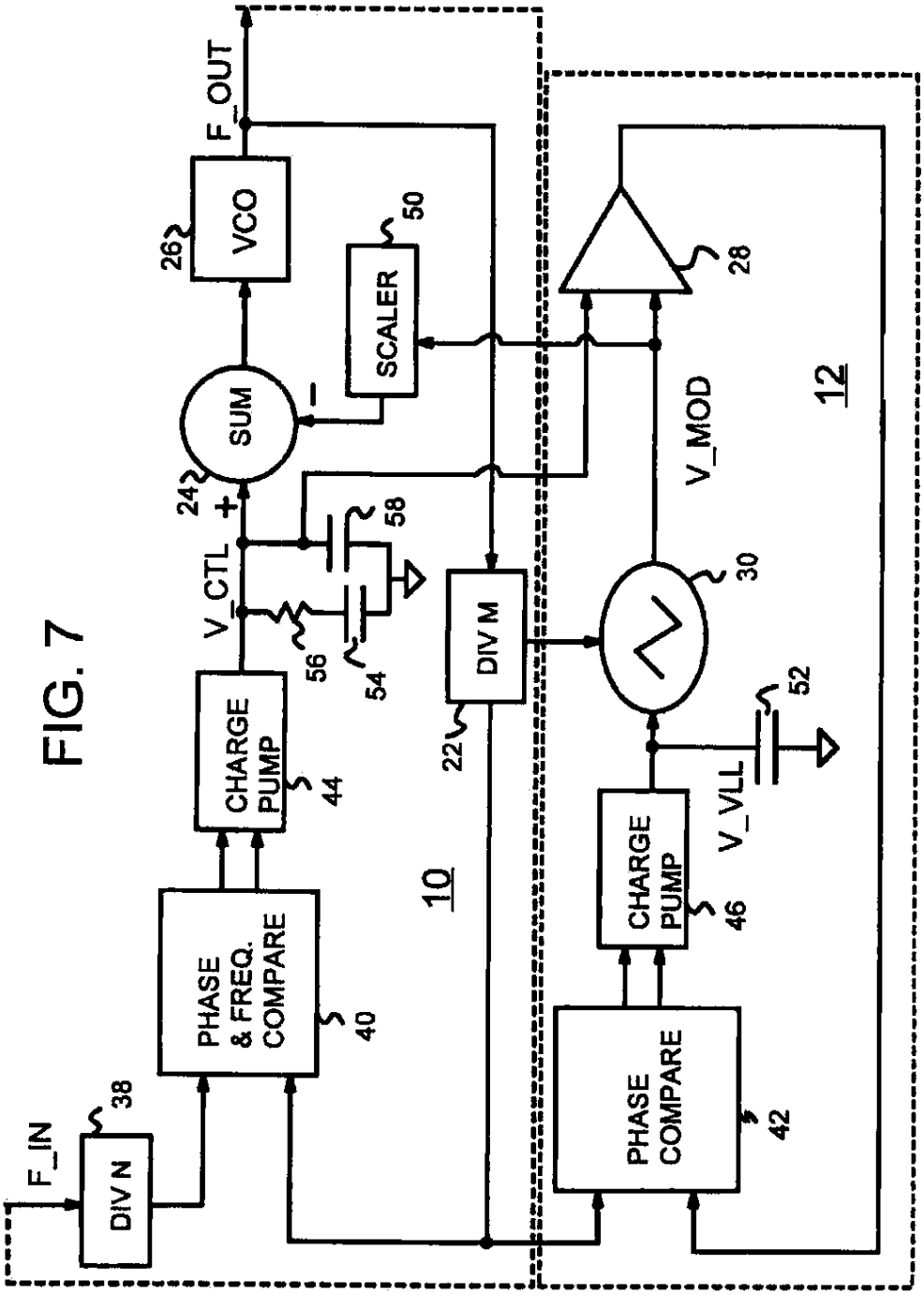

F_OUT
VCO
26
SCALER
50
SUM
24
+
-
V_CTL
58
56
54
DIV M
22
CHARGE PUMP
44
PHASE & FREQ. COMPARE
40
F_IN
DIV N
38
10
12
28
V_MOD
30
52
V_VLL
CHARGE PUMP
46
PHASE COMPARE
42

FIG. 7

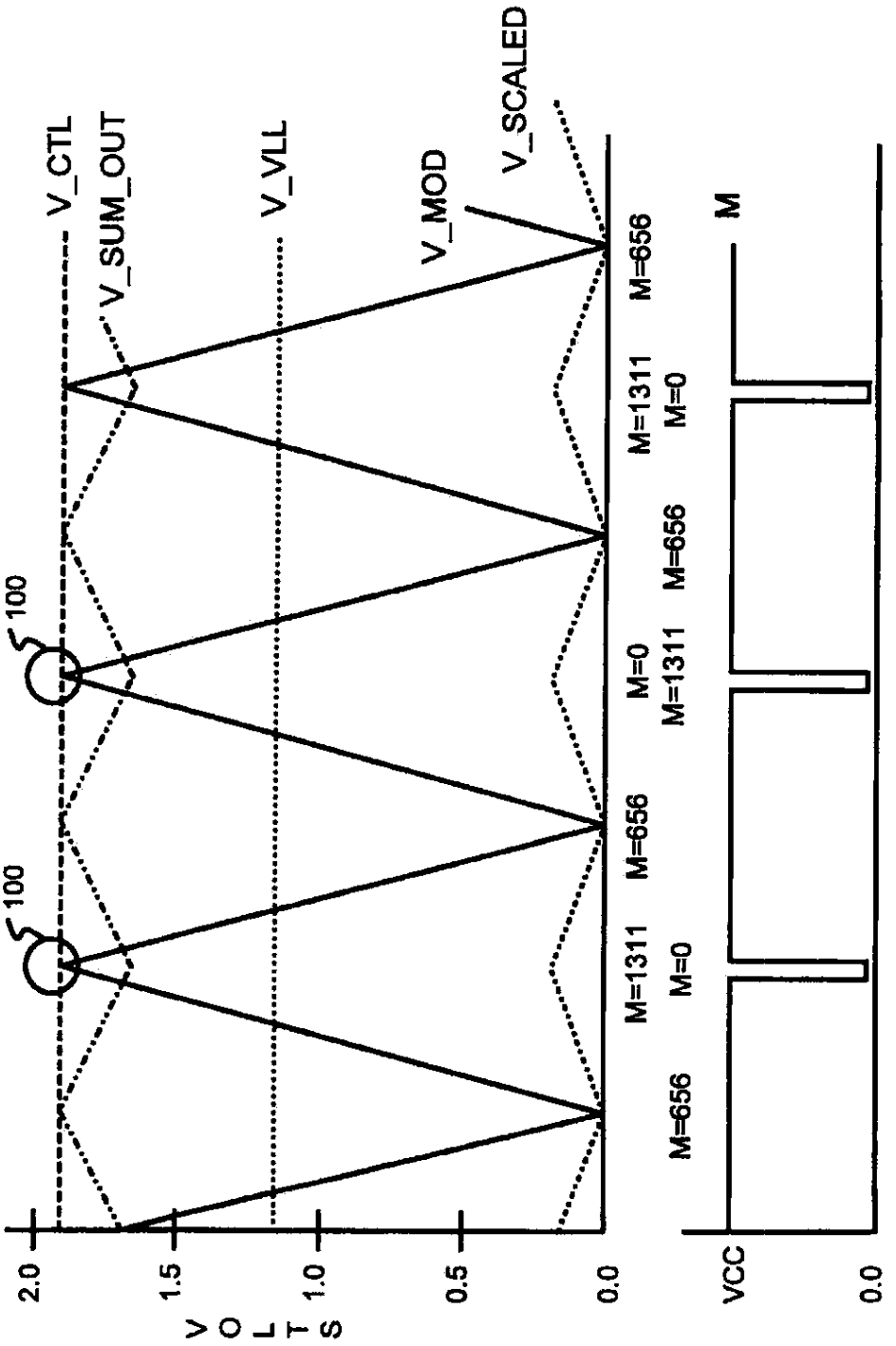

V_CTL
V_SUM_OUT
V_VLL
V_MOD
V_SCALED
100
100
M=1311
M=656
M=0
M=1311
M=656
M=0
M=1311
M=656
M=0
M=656
2.0
1.5
1.0
0.5
0.0
VOLTS
M
VCC
0.0

FIG. 8

DUAL-LOOP SPREAD-SPECTRUM CLOCK GENERATOR WITH MASTER PLL AND SLAVE VOLTAGE-MODULATION-LOCKED LOOP

RELATED APPLICATION

This is a Continuation-in-Part (CIP) of "EMI Reduction for a Flat-Panel Display Controller Using Horizontal-Line-Based Spread Spectrum", U.S. Ser. No. 08/701,814, filed Aug. 21, 1996, now U.S. Patent No. 5,757,338.

FIELD OF THE INVENTION

This invention relates to phase-locked-loop (PLL) circuits, and more particularly to a modulated PLL for reduction of electromagnetic interference (EMI) from computer equipment.

BACKGROUND OF THE INVENTION

Phase-locked loops (PLL's) are widely-used circuits. PLL's have traditionally been used to generate clock signals of desired frequencies from an input reference clock. Some PLL's have employed a second loop to further aid in locking, stabilizing, or quickly acquiring the clock frequency at initialization. See for example U.S. Pat. No. 5,329,250 by Imaizumi et al., assigned to Sanyo Electric Co., and U.S. Pat. No. 5,113,152 by Norimatsu, assigned to NEC Corp. Imaizumi uses two PLL loops, each with their own voltage-controlled oscillator (VCO), while Norimatsu uses a variable loop filter.

A more recent application of PLL's is for generating a modulated clock rather than a stable clock. A slow modulation is intentionally introduced into the output clock. This modulation of the clock's frequency is known as spread spectrum. Two VCO's are used by Hardin in U.S. Pat. No. 5,631,920, assigned to Lexmark International, Inc. Bland in U.S. Pat. No. 5,610,955, assigned to Microclock Inc. of San Jose, Calif., uses a single loop, but with a variable divider in the feedback path.

EMI Interference

Electronic equipment can often generate interference that creates disturbances in other electronic equipment. For example, a portable computer may emit radiation that interferes with a television receiver. Intentional receivers, such as televisions, cellular phones, pagers, and wireless devices, are often affected by unintentional transmitters that emit electromagnetic radiation. As both types of electronic equipment become more common, interference becomes more noticeable to the consumer.

Electromagnetic interference (EMI) is a measure of the amount of interference that an electronic device (the unintentional transmitter) disturbs an intentional receiver. Government agencies such as the Federal Communication Commission (FCC) strictly regulate the amount of radiation or EMI that an electronic device can generate.

Portable devices such as portable personal computers (PC's) are particularly problematic since these portable devices are easily placed near televisions or other receivers. Cramped office and living spaces often force electronic equipment closer together. Since radiation rapidly increases with smaller distances, smaller and more portable equipment often appear to generate more interference.

Improving technology also worsens the EMI problem. Faster clock rates of higher-speed PC's generate more radiation. Higher resolution monitors and displays require that more pixels be transferred to the screen for each screen refresh period; thus a higher clock rate and more interference results.

Traditional techniques to reduce EMI attempt to contain radiation or to reduce the amount of radiation generated. Coax wires and shielded cables are effective at containing radiation, but are expensive, heavy, bulky, and inflexible. The weight and bulk of shielded cables make them undesirable for portable computers. The bulk and relative inflexibility of shielded cables makes it difficult to thread them through the clam-shell hinges connecting the graphics controller in the keyboard-containing base unit with the flat-panel display. Metal chassis with sealed seams are effective for reducing EMI of desktop PC's, but portable PC's are kept light by using plastic. Toxic metal paints are sometimes sprayed on plastic housings for portable PC's to provide shielding.

Lower voltages reduce the intensity of the radiation generated, and the new 3-volt standard has helped reduce EMI at all harmonics. Proper impedance matching and termination of signals reduces ringing and harmonics, and shorter signal traces further reduce radiation. Ground planes on PCB's or ground lines running parallel with signal lines effectively shield signals on boards. Filtering can reduce sharp rise and fall times and reduce radiation by wave shaping since more sinusoidal waves have fewer harmonics than square waves. Of course, filters require additional capacitors, resistors, or inductors, raising the cost. All of these techniques are useful to varying extents.

Frequency Modulation - Spread Spectrum

A newer technique to reduce EMI is to vary or modulate the frequency of clocks in the PC. This technique known as spread spectrum, since the frequency spectrum of the clock is spread out over a wider range of frequencies. FIG. 1 shows a graph of radiation intensity as a function of frequency for an un-modulated clock signal. A sharp spike occurs at a harmonic of the clock's frequency, 40 MHz. Since the clock constantly operates at the rated frequency, all of the energy of the radiation appears in a narrow spike, which has a large amplitude. The spike has an amplitude over the EMI limit set by the FCC. The high intensity of the spike can cause interference in a receiver.

FIG. 2 is a graph of radiation intensity as a function of frequency generated by a modulated clock. The clock's frequency is not constant, but is varied with time over a range of +5% to −5% of the rated frequency. Thus the clock operates at 40 MHz for a period of time, but also operates at other frequencies between 38 MHz and at 42 MHz at other times. Such a clock can be generated by slowly changing the frequency from 38 MHz to 42 MHz and then slowly reducing the frequency back to 38 MHz. A voltage-controlled oscillator (VCO) can be used with the input voltage being slewed back and forth between voltages that generate 38 MHz and 42 MHz oscillations.

Since the modulated clock spends only part of the time at 40 MHz, the intensity of the radiation, averaged over a relatively long time, is reduced. The total energy of the radiation at all frequencies is about the same as for the un-modulated clock of FIG. 1, but the intensity at any particular frequency is greatly reduced. Interference at any one frequency is reduced since receivers generally are tuned to a particular frequency (even FM receivers are tuned to a relatively small range of frequencies).

Thus modulating the clock's frequency reduces the maximum intensity of radiation at any one frequency, although the energy radiated at all frequencies is not reduced. This has the practical effect of reducing interference for receivers tuned to a fixed frequency.

The clock's frequency must not change too rapidly. Rapid variations in clock frequency can cause set-up/hold-time

problems in logic circuits, and in some cases upset phase-locked loops (PLL's) driven by the modulated clock. These PLL's can lose the phase lock and produce erratic outputs. Thus the frequency is modulated slowly. The clock's frequency must not change too slowly, to avoid losing the benefit of EMI reduction.

Graphics controllers in particular have many clocks derived from the input graphics clock. For instance, for SVGA resolution mode a basic clock is multiplied and divided to generate a 40 MHz pixel clock, a 37 KHz HSYNC clock, and a 60 Hz VSYNC clock, and perhaps a 5 MHz character clock. Different resolutions can require that the clock multiplier and divisors be changed to produce signals with the desired timing for that selected resolution.

Phase-locked loops (PLL's) generate a clock by comparing the phase of an input clock to the phase of a generated clock, which is fed back to the phase comparator. The output of the phase comparator is filtered and then input to a voltage-controlled oscillator (VCO). The VCO varies the frequency of the generated clock as the filtered voltage from the phase comparator varies.

The frequency of the generated clock from the VCO does not have to be the same as the frequency of the input clock. The input clock can be divided by a counter to reduce the frequency of the generated clock (clock divisor), while the generated clock fed back to the phase comparator can be divided to increase the frequency of the generated clock (clock multiplier).

These changeable divisors and multipliers can delay phase comparison by many clock periods, resulting in added delays until a modulation in the clock frequency is responded to. For example, a divisor or multiplier of 16 causes the phase comparison to be delayed up to 16 clock periods. The modulated frequency of the PLL will not change until these delayed phase comparisons are made. Normally it takes three to four phase comparisons (depending on the PLL's open loop gain) before the output frequency settles to within 90% of the newly-set frequency. This results in difficulties in finely controlling the modulation, and inaccuracy in the amount of modulation.

Typically the loop filter values in these PLL's are made large to provide low jitter with a stable reference clock. When this reference clock is purposely modulated, the PLL is no longer operating with a stable reference as it was designed for. This can upset the PLL and introduce more jitter than anticipated.

Long Sweep Period of Modulation—FIG. 3

FIG. 3 is a graph of a modulated clock's frequency as a function of time over a few sweep periods. The clock's nominal frequency is 40 MHz. The clock is modulated by +/−5%, from 38 MHz to 42 MHz. The clock's frequency is swept from minimum to maximum frequencies over one or two thousand clock periods so that adjacent clock pulses have a very small variation. A 40 MHz clock with a 25 nanosecond (ns) period is varied from 26.25 ns to 23.75 ns over a sweep period, a variation of +/−1.25 ns. A 37 KHz sweep rate has a sweep period of 27 micro-seconds (μs). A sweep period is 27 μs / 25 ns or 1081 clock periods. The cycle-to-cycle period variation for two adjacent clock periods is thus 5 ns / 1081 or 4.62 pico-seconds (ps). This small cycle-to-cycle variation is needed to prevent PLL's from losing their phase lock. The sweep frequency is typically 15 to 50 KHz.

A related application for "EMI Reduction for a Flat-Panel Display Controller Using Horizontal-Line-Based Spread Spectrum", U.S. Ser. No. 08/701,814, now U.S. Pat. No. 5,757,338, discloses a spread-spectrum PLL that adjusts the feedback divisor. The modulation rate is synchronized with the horizontal refresh rate of the display to eliminate visible distortions.

Intentional Modulation Disturbs PLL Frequency-Lock

While prior-art modulated clock generators exist, often the stability of the generated clock is compromised when an intentional modulation is introduced. Introducing modulation into a PLL disturbs the frequency-lock and stability of the PLL. Often the amount of modulation must be reduced to maintain frequency-lock. Reducing the amount of modulation is undesirable since the amount of EMI reduction is curtailed.

What is desired is a modulated clock-generator circuit. A more stable clock generator is desired for generating modulated clocks. A PLL-based clock generator that locks in the output frequency even though the output frequency is modulated is desirable. A circuit that more effectively isolates the modulation from the frequency-lock is desired.

SUMMARY OF THE INVENTION

A modulated clock generator has a master phase-locked loop (PLL) that receives a reference clock and outputs a modulated clock. The master PLL includes a feedback divider that receives the modulated clock. It generates a pulse after every M cycles of the modulated clock. A phase comparator receives the reference clock and the pulse from the feedback divider. It compares a phase of the reference clock to a phase of the pulse when the pulse is received. The phase comparator outputs a phase-difference signal.

A summer receives the phase-difference signal from the phase comparator. It combines a modulated signal with the phase-difference signal to generate a frequency-determining signal. A frequency generator generates the modulated clock with a frequency determined by the frequency-determining signal from the summer. The frequency varies over time when the modulated signal varies over time.

A slave voltage-locked loop (VLL) has a waveform generator coupled to the feedback divider. It generates the modulated signal to the summer in the master PLL. The modulated signal is synchronized to the pulse from the feedback divider. A slave comparator receives the phase-difference signal from the phase comparator and receives the modulated signal from the waveform generator. It outputs a difference signal when the phase-difference signal has a same voltage as the modulated signal.

A second phase comparator is coupled to supply a level signal to the waveform generator. It compares the difference signal from the slave comparator to the pulse from the feedback divider when the pulse is received. Thus the slave VLL generates the modulated signal for the master PLL.

In further aspects of the invention the phase comparator and the second phase comparator ignore inputs when the pulse from the feedback divider is not received. The phase comparator and the second phase comparator perform phase comparisons only when the pulse is received. The modulated signal and the modulated clock are at a same point in a modulation cycle when the pulse is generated by the feedback divider. One modulation cycle occurs in a period of time between adjacent pulses from the feedback divider. Thus the modulation cycle is synchronized to the feedback divider.

In further aspects, changes in a power-supply voltage or temperature alter the phase-difference signal from the phase comparator. The modulated signal is adjusted by the slave VLL to track the phase-difference signal.

In other aspects the frequency generator is a voltage-controlled oscillator (VCO) that generates the modulated clock with a frequency determined by a voltage of the frequency-determining signal from the summer.

In further aspects of the invention the level signal from the second phase comparator determines a voltage level of the modulated signal but not a timing of the modulated signal. The feedback divider determines a modulation period of the modulated signal. Thus the modulation period is synchronized to the master PLL.

In still further aspects the modulated signal is scaled before is combined by the summer. The summer subtracts the modulated signal from the phase-difference signal from the phase comparator.

In other aspects, M is a total number pixels in a horizontal line of a display.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** shows a graph of radiation intensity as a function of frequency for an unmodulated clock signal.

FIG. **2** is a graph of radiation intensity as a function of frequency generated by a modulated clock.

FIG. **3** is a graph of a modulated clock's frequency as a function of time over a few sweep periods.

FIG. **4** is a diagram of a modulated clock generator with a master PLL and a slave voltage-locked loop (VLL) for generating modulations.

FIG. **5** is a timing diagram showing that the phase comparison for frequency-lock occurs at the start of every modulation sweep cycle.

FIG. **6** is a simplified diagram of a modulated clock generator with a master PLL and a slave VLL for frequency modulation.

FIG. **7** is a detailed schematic of the master PLL and slave VLL for the modulated clock generator.

FIG. **8** is a waveform diagram of the steady-state operation of the modulated clock generator of FIG. **7**.

DETAILED DESCRIPTION

The present invention relates to an improvement in modulated clock generators. The following description is presented to enable one of ordinary skill in the art to make and use the invention as provided in the context of a particular application and its requirements. Various modifications to the preferred embodiment will be apparent to those with skill in the art, and the general principles defined herein may be applied to other embodiments. Therefore, the present invention is not intended to be limited to the particular embodiments shown and described, but is to be accorded the widest scope consistent with the principles and novel features herein disclosed.

Modulation by Slave Loop Isolated from PLL

The inventors have realized that the stability of the frequency-lock of the PLL is disturbed by the intentional introduction of clock modulation. The PLL's stability can be improved if the modulation can be isolated from the frequency-locking portion of the PLL. The inventors separate the modulation from the frequency-lock of the PLL by creating a second or slave loop for modulation. This slave modulation loop generates the modulation signal for the primary or master PLL. The modulation signal from the slave loop is introduced into the master loop after the frequency-locking portion, just before the output frequency is generated. Thus the output clock is modulated, but the frequency-lock is isolated from the modulation.

The slave loop is not a second PLL, since it does not include a voltage-controlled oscillator (VCO). The second loop generates the slow modulation as a varying voltage. This voltage is used to adjust the frequency of the primary PLL loop. The slave loop cannot generate a frequency different from that of the first loop. Instead, the slave loop modulates the adjustment voltage over a cycle (period) equal to the phase comparison period of the primary PLL loop.

Slave Loop Synchronized to PLL

The slave loop is synchronized to the primary PLL loop. The slave loop generates modulation that completes a cycle exactly in step with the frequency-lock of the primary PLL loop. When the primary PLL loop compares the phases of the reference clock and the feedback clock, the modulation is always at the same point in the modulation cycle. Thus the modulation is exactly the same each time the frequency comparison occurs. Since the modulation does not vary when the frequency lock occurs, the modulation is effectively isolated from frequency locking.

Master PLL and Slave Voltage-Locking Loop—FIG. 4

FIG. **4** is a diagram of a modulated clock generator with a master PLL and a slave modulated-voltage-locked loop. Master PLL **10** is a standard PLL that also includes a voltage summer just before a VCO that generates the output clock. A modulated voltage V_MOD is input to this voltage summer to adjust the voltage to the VCO. As V_MOD varies, the voltage to the VCO is varied, and thus the output clock frequency varies (is modulated).

The modulated voltage V_MOD is generated by a second loop, slave voltage-locked loop **12**. This second loop does not include a VCO of its own, but instead receives timing information from the primary loop, master PLL **10**.

Slave voltage-locked loop compares a control voltage V_CTL from master PLL **10** to the modulated voltage V_MOD. Slave voltage-locked loop **12** "locks" these two voltages to each other; thus it is referred to as a voltage-locked loop.

Frequency or phase comparison occurs in both master PLL **10** and slave voltage-locked loop **12** at exactly the same time. The modulation period of V_MOD is exactly synchronized with this phase-comparison period. Although V_MOD varies, it always returns to its starting point when phase comparison occurs. Thus V_MOD and V_CTL are equal at the beginning of the slow modulation cycle, when phase comparison occurs. After phase comparison occurs, V_MOD changes as it cycles through a modulation cycle, returning to its initial voltage just as the next frequency modulation occurs.

Modulation Cycle Matches Phase-Comparison—FIG. 5

FIG. **5** is a timing diagram showing that the phase comparison for frequency-lock occurs at the start of every modulation sweep cycle. The control voltage V_CTL from the master PLL is generated by a phase and frequency comparison that is performed during times **100**. Even though the clock output from the master PLL varies in frequency, the clock output always has the same frequency at times **100** since the modulation cycle begins and ends at times **100**.

The modulated voltage V_MOD generated by the slave voltage-locked loop varies from V_CTL during a modulation cycle. However, the modulation cycle begins and ends at times **100** since the modulation is exactly synchronized to the frequency-lock period of the master PLL loop.

Since the control voltage V_CTL from the master PLL is always equal to the modulated voltage V_MOD from the slave voltage-locked loop at times **100**, the slave loop

remains locked to the primary loop. The primary loop is not disturbed by the modulation because the modulation always finishes by the time phase or frequency comparison occurs, at times **100**.

Voltages Locked

The slave voltage-locked loop compares V_CTL to V_MOD only at times **100**. Should the master PLL adjust its control voltage V_CTL, such as caused by process variations of the wafer fab the slave voltage-locked loop alters its control voltage V_VLL to rematch V_MOD at time **100** to match the new V_CTL. Thus the second loop is a voltage-locked loop (VLL).

Simplified Diagram of PLL-VLL—FIG. **6**

FIG. **6** is a simplified diagram of a modulated clock generator with a master PLL and a slave VLL for frequency modulation. Master PLL **10** is a loop that includes phase comparator **20**, summer **24**, VCO **26**, and divider **22**. An input reference clock F_IN is compared to the feedback from divider **22** by phase comparator **20**. This comparison does not occur continuously but for each pulse from divider **22**. Phase comparator **20** includes a phase and frequency comparator, a charge pump, and a loop filter. The control voltage V_CTL is output from phase comparator **20**. This control voltage remains constant despite frequency modulation.

Voltage summer **24** subtracts the modulation voltage V_MOD from the control voltage V_CTL. The output of summer **24** is a voltage applied to VCO **26**. As V_MOD is changed by slave VLL **12**, the voltage output by summer **24** also varies, causing the frequency generated by VCO **26** to vary.

Divider **22** receives the modulated output clock from VCO **26** and divides it by the constant M. After M pulses of the output clock are received by divider **22**, it outputs one pulse to phase comparator **20**. Thus phase comparison occurs only once for every M pulses of the output clock (F_OUT).

The output from divider **22** is also sent to phase comparator **32** in slave VLL **12**. Thus phase comparison occurs at the same time for both loops, once every M output-clock pulses. Phase comparator **32** includes a phase comparator, a charge pump, and a loop filter. It outputs a stable voltage to waveform generator **30**, providing the desired modulation.

Waveform generator **30** generates a modulation profile, in this case, a sawtooth waveform from phase comparator **32**, synchronized to divider **22**. Divider **22** determines when to begin and end each cycle so that the cycle is exactly the same as M periods of the output clock F_OUT. The voltage amplitude of the waveform is determined by the voltage from phase comparator **32**, while the period is determined by divider **22**.

The waveform from waveform generator **30** is the modulated voltage V_MOD, which is sent to summer **24**. As waveform generator **30** modulates voltage V_MOD, VCO **26** varies the output frequency.

Even though the frequency is modulated, the frequency comparison by phase comparators **20**, **32** occurs at the same time in the modulation cycle, when divider **22** outputs a pulse. This pulse resets waveform generator **30** to begin a new modulation cycle. Since the modulations of voltage V_MOD occur between pulses from divider **22**, these modulations are not compared by comparators **20**, **32**.

Voltage comparator **28** compares the control voltage V_CTL from master PLL **10** to the modulated voltage V_MOD from slave VLL **12**. Although voltage comparator **28** continuously compares these voltages, phase comparator **32** ignores these voltage comparisons in the middle of the modulation cycle, and only phase-compares the output from voltage comparator **28** at the end of the modulation cycle, when divider **22** outputs a pulse and resets waveform generator **30**. Thus phase comparator **32** samples voltage comparator **28** when it compares V_CTL to the initial V_MOD, when V_CTL is nominally equal to V_MOD. Any voltage difference is the result of temperature or other variations in master PLL **10** or slave VLL **12**. These variations are tracked by slave VLL **12** adjusting the initial V_MOD to account for the change in V_CTL. Thus slave VLL **12** is locked to the control voltage from master PLL **10**.

Detailed Schematic of Master PLL and Slave VLL—FIG. **7**

FIG. **7** is a detailed schematic of the master PLL and slave VLL for the modulated clock generator. A reference clock F_IN is optionally divided by N in divider **38** and then applied to phase and frequency comparator **40**. The output clock has a nominal frequency in the ratio of M/N, where M is the divisor for feedback divider **22**. The output clock F_OUT is often further divided, such as in a divide-by-two divider (not shown).

Phase and frequency comparator **40** compares the phase of the divided reference clock from divider **38** to the pulse from divider **22**. The frequency as well as the phase are compared because comparator **40** checks which of the reference and feedback clock signals arrives first. If reference signal arrives first, meaning VCO is running too slow, a UP signal is generated, and vice versa. The Up and Down signals generated from phase and frequency comparator **40** are sent to charge pump **44**, which sources or sinks charge to and from the loop filter on the V_CTL node. As charge is sourced to capacitors **54**, **58**, V_CTL increases, which ultimately increases the voltage input to VCO **26** and increases the frequency to compensate for the phase or frequency difference.

Resistor **56** and capacitors **54**, **58** form a loop filter that slows down the response of master PLL **10**. The loop filter is useful for filtering out high frequency variations. The value of the loop's time constant can be varied by adjusting the capacitive and resistive values of the loop filter.

Summer **24** subtracts a preset scaled V_MOD from the control voltage V_CTL (such as 2%) and outputs a modulated voltage to VCO **26**. VCO **26** generates a clock with a frequency that varies (2%) with the voltage from summer **24**. Since the VLL locks to V_CTL, the amount of modulation (2%) is guaranteed regardless of supply voltage, temperature, and process variations in IC circuits.

The pulse output from divider **22** after every M output clock pulses is also compared by phase comparator **42** in slave VLL **12**. An up and a down signal output from phase comparator **42** controls a current source and a current sink in charge pump **46**, which partially charge or discharge capacitor **52**. This increases or decrease voltage V_VLL, the nominal lock voltage of slave VLL **12**. Voltage V_VLL is relatively constant, as is V_CTL, the control voltage from master PLL **10**. These two voltage are locked together by slave VLL **12**. When V_CTL increases, V_VLL also changes to track it.

VCO **26** introduces a pole (1/s) to convert frequency to phase. Since no VCO is present in VLL **12**, VLL **12** is a single pole (i.e. first-order loop) feedback system. As a result, a full R-C filter is not needed. This simplifies the circuit design and greatly eases the stability constraint, because a first-order negative feedback loop is unconditionally stable.

Waveform generator **30** uses the nominal control voltage V_VLL across capacitor **52** and generates a sawtooth waveform in synch with the M pulse from divider **22**. Thus the period or cycle time of the modulation is set by divider **22**, but the initial and average voltages generated by waveform generator **30** are determined by the voltage from capacitor **52**. Divider may output additional timing signals to waveform generator **30**, such as a mid-cycle signal to reverse the direction of the voltage changes in the middle of the modulation cycle, and M/2. Waveform generator **30** could be programmable for the type of waveform generated and the midpoint.

Waveform generator **30** outputs the modulated voltage V_MOD, which is compared by voltage comparator **28** to the master PLL's control voltage V_CTL. Although V_MOD varies, the voltage comparison from voltage comparator **28** is only sampled by phase comparator **42** at each M pulse output from divider **22**. This occurs at the start and end of the modulation cycle, when V_MOD has returned to its initial value.

The modulated voltage V_MOD is scaled to be subtracted from V_CTL. V_MOD may not be scaled to the desired modulation, so scaler **50** attenuates the modulation voltage to a desired value for input to voltage summer **24**. The amount of frequency modulation is usually small compared to the frequency generated. A 40 MHz output clock may only be modulated by 5%, or 2 MHz. Thus the modulated voltage V_MOD should be scaled to be only 5% or less of the control voltage V_CTL because output frequency F_OUT is directly proportional to V_CTL. Scaler **50** attenuates the modulation voltage V_MOD by 90% or 95%, depending on the amount of frequency modulation desired. A voltage divider can be used for scaler **50**. Comparator **28** outputs a pulse when V_MOD matches V_CTL. This pulse is phase compared with the output from divider **22**. Should there be any difference, then V_VLL is adjusted accordingly to synchronize the modulation sawtooth voltage with the master PLL.

Waveform Diagram—FIG. **8**

FIG. **8** is a waveform diagram of the steady-state operation of the modulated clock generator of FIG. **7**. The feedback divider counts M pulses of the output clock and then outputs a single low-going pulse as signal "M". The feedback counter counts from M=0 to M=1311 for 1024×768 resolution. This count from M=0 to M=1311 is shown on the horizontal axis and defines a modulation cycle. Three complete modulation cycles are shown in FIG. **8**.

The control voltage V_CTL of the master PLL, and the nominal lock voltage V_VLL of the slave VLL remain relatively constant in steady-state operation. During system initialization, these signals rise from ground and fluctuate as the clock is being acquired and locked.

As the feedback divider counts down from M=1131 to 0, waveform generator **30** of FIG. **7** incrementally decreases the modulation voltage V_MOD until M reaches its midpoint, M=656. Then it incrementally increases the modulation voltage until the initial voltage is reached again when the feedback divider reaches M=0, and outputs the M pulse. The waveform generator receives the nominal lock voltage V_VLL, which normally remains constant through the modulation cycle. V_VLL only changes when the steady state is altered and V_CTL has changed. The waveform generator can be another charge pump but with a variable pump-current controlled by the input voltage V_VLL when generating the modulated voltage V_MOD.

The modulated voltage V_MOD is too large in magnitude for the desired frequency modulation, so it must be attenuated. The scaled modulated voltage V_SCALED swings from 0 to 200 mV while V_MOD swings from 0 to about 2.0 volts. Thus the signal is attenuated by 90%.

The scaled modulated voltage V_SCALED is subtracted from the stable control voltage V_CTL by the voltage summer in the master PLL. The result is V_SUM_OUT, which is a modulated voltage sent to the VCO. Since the voltage V_SUM_OUT modulates from about 2.0 volts to 1.8 volts, the frequency generated is also modulated.

The phase comparisons in both the master PLL and slave VLL are performed only during the M pulse, since the M pulse is sent to the phase comparators. Thus the master PLL compares the M pulse to the reference clock when the slave VLL compares the voltages V_CTL to V_MOD. The modulated voltage is at 2.0 volts, about equal to V_CTL, during the M pulse, as shown in times **100**. Thus there is no adjustment to either loop in steady-state. Fluctuations from steady state cause phase or voltage mis-compares, which adjust the level of the control or modulated voltages to compensate.

Divisor Matches Horizontal Period

For a graphics display system, the value of M is preferably equal to or a fraction of the number of pixels in a horizontal line of a display. M can be any number when used in other systems that require a modulated clock. M is the total number of pixels, not just the number of displayed pixels. Thus for 1024×768 resolution, each horizontal line has 1024 displayable pixels. The horizontal time period also includes non-displayed pixels, such as those when a CRT's horizontal re-trace and blanking occurs. Thus for 1024×768 resolution, M is set to **1311**. Of course, many other values of M are possible, even for the same resolutions, depending on the blanking period programmed.

ADVANTAGES OF THE INVENTION

The modulated clock-generator circuit uses a slave loop to lock a modulated voltage with the control voltage of the master PLL that generates the modulated clock. A more stable clock generator is shown for generating modulated clocks. A PLL-based clock generator locks in the output frequency even though the output frequency is modulated. The circuit more effectively isolates the modulation from the frequency-lock. Thus stability of the PLL is improved, even though modulations are introduced that might otherwise upset the frequency lock and stability of the PLL.

The sensitive control node of the master PLL is isolated from the modulations. This prevents the modulations from disturbing the charge stored on the loop filter's capacitors. Stability is thus improved. Power-supply voltages, temperature, process, and clock loading that can affect the PLL are accounted for by the separate voltage-lock of the slave loop that generates the modulations. The slave loop provides a constant modulation in all conditions, since its output tracks the control voltage in the master PLL. The slave's loop filter is simply a capacitor, which results in a simple, one-pole design. The slave's waveform generator can use a charge-pump-type current integrator that results in a very smooth sawtooth-shaped modulation voltage. This simple, first-order, slave loop is unconditionally stable because of the simple filter. In contrast, the VCO in the master loop introduces a second pole. This adds instability to the master loop that is not present in the slave loop. because the phase changes 180 degree (with 2 poles), and combining the negative feedback configuration produces a positive feedback system.

A digital-to-analog converter (DAC) is not needed, eliminating jitter from discrete steps from the DAC. A second

VCO is also eliminated, reducing cost and complexity. Synchronizing the phase comparisons to the modulation cycle has the effect of fooling the master loop into behaving as an un-modulated PLL. The modulations are not seen when the phase comparisons are sampled.

ALTERNATE EMBODIMENTS

Several other embodiments are contemplated by the inventors. For example a sine wave or other kinds of waveforms for modulation can be generated instead of the sawtooth wave described. The voltage comparator and summer can be implemented with op amps or other circuits. The entire circuit is preferably integrated onto a single integrated circuit, such as with a graphics controller.

The clock generator can be applied to other systems besides graphics systems. Polarities of signals can be reversed, and a voltage summer that adds rather than subtracts the scaled, modulated voltage can be substituted. More than one cycle of modulation can occur between each pulse from the feedback divider.

There are digital counterparts of analog PLL's that can be substituted. The charge pump and loop filter can be substituted by an up/down counter, and the VCO replaced by digitally-controlled delay circuits.

The foregoing description of the embodiments of the invention has been presented for the purposes of illustration and description. It is not intended to be exhaustive or to limit the invention to the precise form disclosed. Many modifications and variations are possible in light of the above teaching. It is intended that the scope of the invention be limited not by this detailed description, but rather by the claims appended hereto.

We claim:

1. A modulated clock generator comprising:

a master phase-locked loop (PLL), receiving a reference clock and outputting a modulated clock, the master PLL comprising:

a feedback divider, receiving the modulated clock, for generating a pulse after every M cycles of the modulated clock;

a phase comparator, receiving the reference clock and the pulse from the feedback divider, for comparing a phase of the reference clock to a phase of the pulse when the pulse is received, the phase comparator outputting a phase-difference signal;

a summer, receiving the phase-difference signal from the phase comparator, for combining a modulated signal with the phase-difference signal to generate a frequency-determining signal;

a frequency generator for generating the modulated clock having a frequency determined by the frequency-determining signal from the summer, the frequency varying over time when the modulated signal varies over time; and

a slave voltage-locked loop (VLL) comprising:

a waveform generator, coupled to the feedback divider, for generating the modulated signal to the summer in the master PLL, the modulated signal being synchronized to the pulse from the feedback divider;

a slave comparator, receiving the phase-difference signal from the phase comparator and receiving the modulated signal from the waveform generator, for outputting a difference signal when the phase-difference signal has a same voltage as the modulated signal;

a second phase comparator, coupled to supply a level signal to the waveform generator, for comparing the difference signal from the slave comparator to the pulse from the feedback divider when the pulse is received,

whereby the slave VLL generates the modulated signal for the master PLL.

2. The modulated clock generator of claim **1** wherein the phase comparator and the second phase comparator ignore inputs when the pulse from the feedback divider is not received, the phase comparator and the second phase comparator performing phase comparisons only when the pulse is received.

3. The modulated clock generator of claim **1** wherein the modulated signal and the modulated clock are at a same point in a modulation cycle when the pulse is generated by the feedback divider.

4. The modulated clock generator of claim **3** wherein one modulation cycle occurs in a period of time between adjacent pulses from the feedback divider, whereby the modulation cycle is synchronized to the feedback divider.

5. The modulated clock generator of claim **1** wherein changes in power-supply voltage or temperature alter the phase-difference signal from the phase comparator, and wherein the modulated signal is adjusted by the slave VLL to track the phase-difference signal.

6. The modulated clock generator of claim **1** wherein the frequency generator is a voltage-controlled oscillator (VCO) generating the modulated clock with a frequency determined by a voltage of the frequency-determining signal from the summer.

7. The modulated clock generator of claim **6** wherein the level signal from the second phase comparator determines a voltage level of the modulated signal but not a timing of the modulated signal, and wherein the feedback divider determines a modulation period of the modulated signal,

whereby the modulation period is synchronized to the master PLL.

8. The modulated clock generator of claim **7** wherein the modulated signal is scaled before being combined by the summer.

9. The modulated clock generator of claim **8** wherein the summer subtracts the modulated signal from the phase-difference signal from the phase comparator.

10. The modulated clock generator of claim **9** wherein M is a total number pixels in a horizontal line of a display.

11. A clock generator for generating a frequency-modulated output clock, the clock generator comprising:

a master phase-locked loop (PLL) comprising:

a voltage-controlled oscillator (VCO), receiving a summed voltage, for outputting the output clock having an instantaneous frequency determined by the summed voltage;

a feedback divider, receiving the output clock from the VCO, for dividing a frequency of the output clock to generate a feedback clock;

a master phase comparator, receiving a reference clock having a fixed reference frequency, for comparing a phase of the reference clock to a phase of the feedback clock, the master phase comparator outputting a phase-difference signal;

a loop filter including a capacitor, the loop filter outputting a control voltage;

a master charge pump, receiving the phase-difference signal from the master phase comparator, for charging and discharging the capacitor in the loop filter in response to the phase-difference signal;

a summer, receiving the control voltage from the loop filter and receiving a modulated voltage, for output-

ting the summed voltage as a combination of the control voltage and the modulated voltage; and

a slave voltage-locked loop (VLL) comprising:

a modulation generator, coupled and synchronized to the feedback divider, for generating the modulated voltage having voltage modulations in a modulation cycle;

a voltage comparator for comparing the modulated voltage to the control voltage from the master PLL and outputting a voltage pulse when the modulated voltage is equal to the control voltage;

a slave phase comparator, coupled to the voltage comparator and receiving the feedback clock, for generating a slave phase-difference signal;

a slave loop filter that includes a capacitor, the slave loop filter coupled to the modulation generator;

a slave charge pump, receiving the slave phase-difference signal, for charging and discharging the slave loop filter in response to the slave phase-difference signal;

whereby modulation is isolated from the loop filter of the master PLL by the slave VLL that generated the modulated voltage.

12. The clock generator of claim **11** wherein the slave loop filter outputs a level signal to the modulation generator, the modulation generator generating the modulated voltage having a level determined by the level signal,

whereby the level of the modulated voltage is adjusted by comparison with the control voltage of the master PLL.

13. The clock generator of claim **12** wherein the modulated voltage changes in a modulation cycle, a period of the feedback clock being exactly equal to one or more periods of the modulation cycle.

14. The clock generator of claim **13** wherein the loop filter in the master PLL includes a resistor and a capacitor in series, while the slave loop filter comprises a capacitor without a series resistor, the slave VLL being a first-order loop with a single frequency pole.

15. The clock generator of claim **13** further comprising:

a scaler for attenuating the modulated voltage before the modulated voltage is combined with the control voltage by the summer.

16. The clock generator of claim **13** wherein the modulated voltage is subtracted from the control voltage by the summer.

17. The clock generator of claim **13** wherein the modulation generator outputs the modulated voltage that forms a sawtooth wave between pulses of the feedback clock.

18. The clock generator of claim **13** wherein the master phase comparator compares a phase and a frequency of the reference clock to the feedback clock, but the slave phase comparator compares only a phase of the voltage pulse to the feedback clock.

19. The clock generator of claim **13** wherein the reference clock is generated by an input divider.

20. The clock generator of claim **13** wherein the feedback divider is synchronized to a horizontal period of a horizontal line of pixels for a display.

* * * * *

EXHIBIT 28
(USP 5,757,338)

US005757338A

United States Patent [19]

Bassetti et al.

[11] Patent Number: 5,757,338

[45] Date of Patent: May 26, 1998

[54] **EMI REDUCTION FOR A FLAT-PANEL DISPLAY CONTROLLER USING HORIZONTAL-LINE BASED SPREAD SPECTRUM**

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[73] Assignee: **NeoMagic Corp.**, Santa Clara, Calif.

[21] Appl. No.: **701,814**

[22] Filed: **Aug. 21, 1996**

[51] **Int. Cl.**[6] **G09G 5/00**

[52] **U.S. Cl.** **345/3**; 345/507; 345/204; 315/85; 348/819

[58] **Field of Search** 348/819, 805, 348/806, 820, 511, 540; 345/1, 3, 132, 507, 212, 196, 213, 204, 905; 315/85, 10; 364/708.1; 361/680, 681, 683

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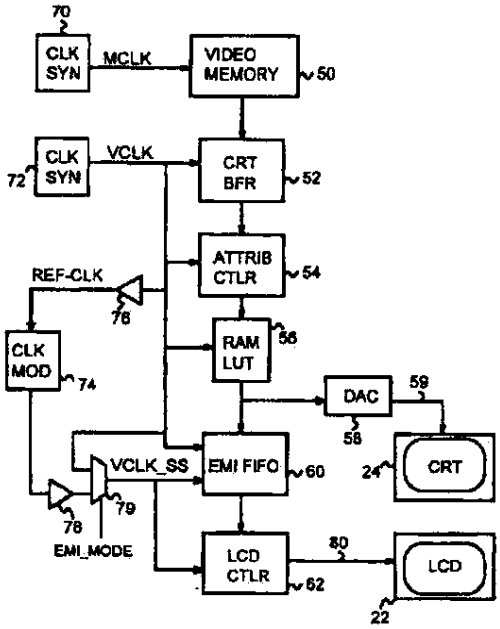
Primary Examiner—Lun-Yi Lao
Attorney, Agent, or Firm—Stuart T. Auvinen

[57] **ABSTRACT**

A graphics controller uses spread-spectrum techniques to modulate the pixel clock over a range of frequencies, reducing the maximum intensity of EMI emissions. When the clock input to the graphics controller is replaced with a modulated clock, the image on a CRT is distorted. Distortion is avoided by only modulating the clock to the flat-panel LCD interface. The vertical and horizontal timing signals for both the CRT and the LCD are generated from the un-modulated clock. Using the un-modulated clock for these critical timing signals ensures that each horizontal line is displayed for the same period of time. Brighter and dimmer lines are thus avoided. A second embodiment modulates the clocks to the CRT and LCD, reducing emissions for both interfaces. Even the timing signals use the modulated clock. The frequency sweep of the modulated clock is reset at the end of every horizontal line. Thus all lines are displayed for the same period, although the transfer of pixels within a line are modulated. Even though the pixel clock is modulated while pixels are written to the displays, the same sequence of modulations is repeated for each line. Thus pixels from different lines are aligned and zig-zag and wiggle distortions seen when simple asynchronous modulation is applied to all clocks is avoided.

7 Claims, 9 Drawing Sheets



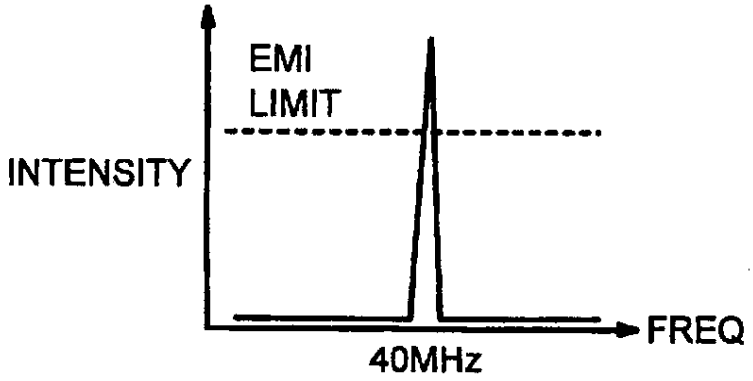


FIG. 1

PRIOR ART

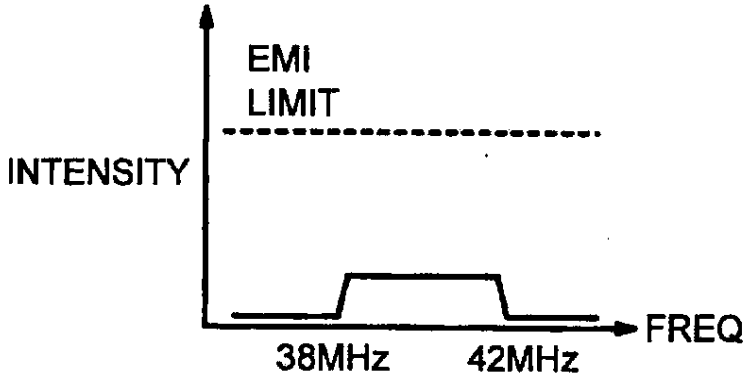


FIG. 2

PRIOR ART

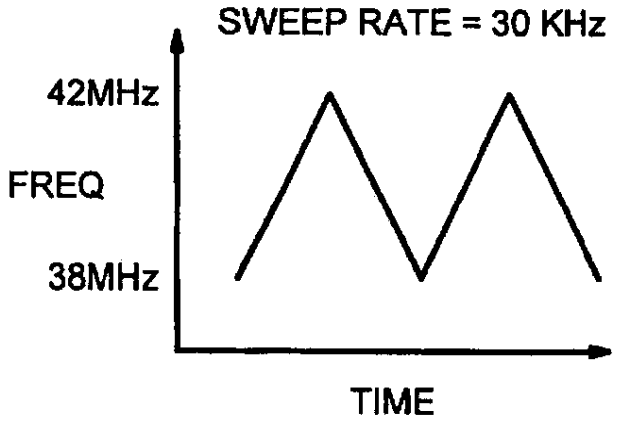


FIG. 3

PRIOR ART

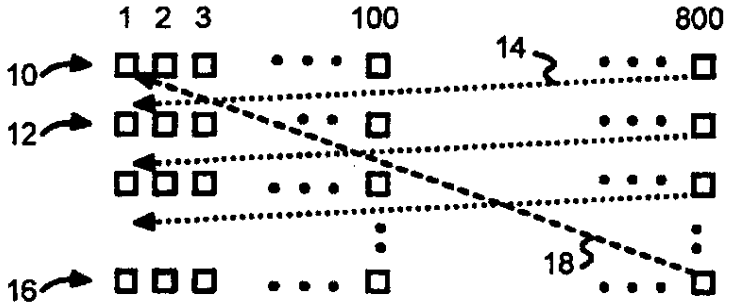


FIG. 4

PRIOR ART

ALL LINES
40 MHz PIXEL
CLOCK

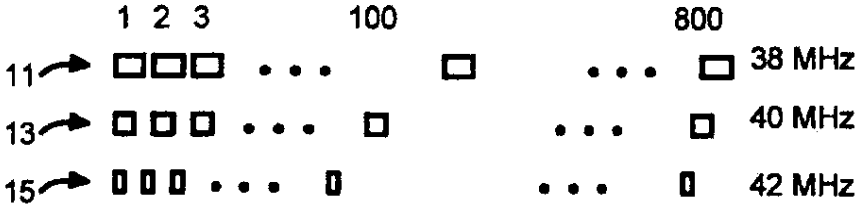


FIG. 5

MODULATED
38-42 MHz
PIXEL CLOCK

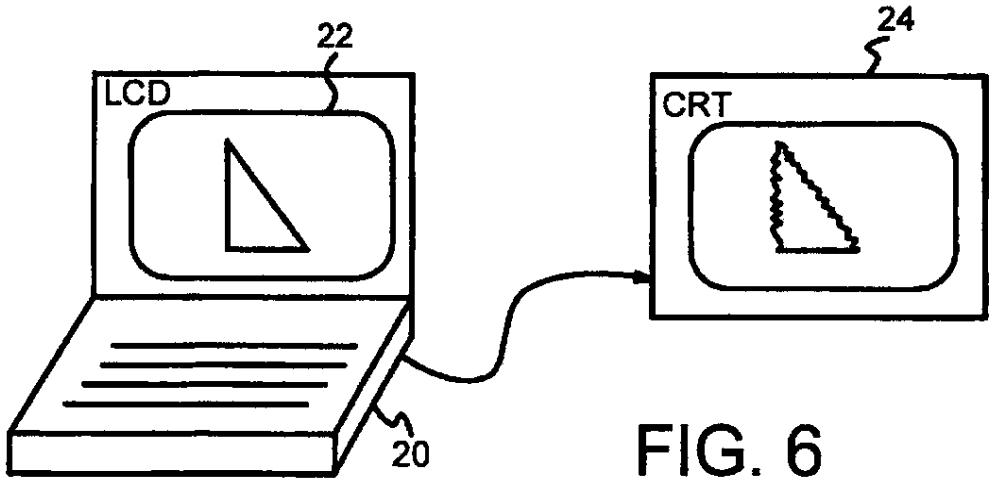


FIG. 6

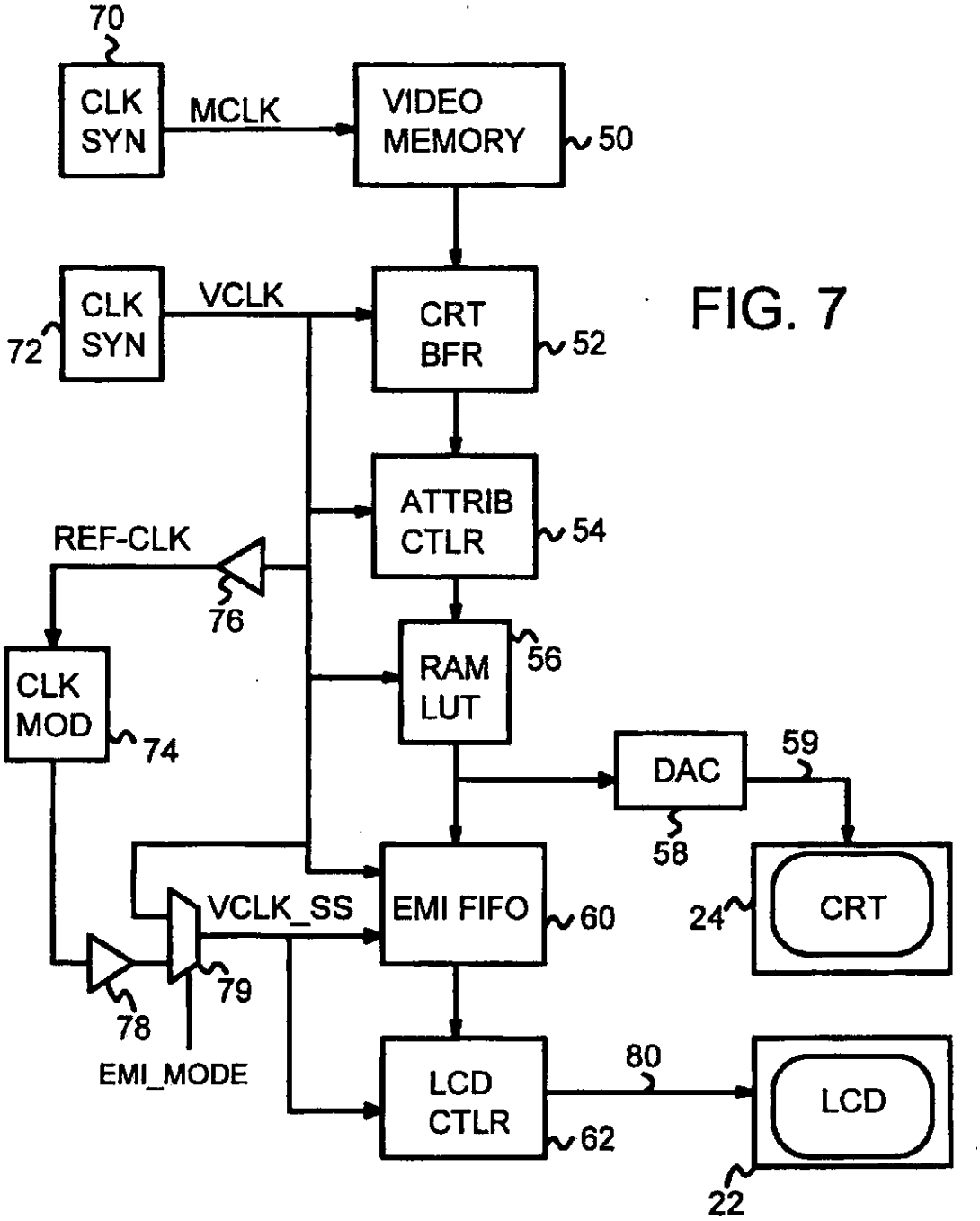

70
CLK SYN
MCLK
VIDEO MEMORY
50
CLK SYN
72
VCLK
CRT BFR
52
ATTRIB CTLR
54
REF-CLK
76
RAM LUT
56
CLK MOD
74
DAC
59
58
VCLK_SS
EMI FIFO
60
24
CRT
79
78
EMI_MODE
LCD CTLR
62
80
LCD
22

FIG. 7

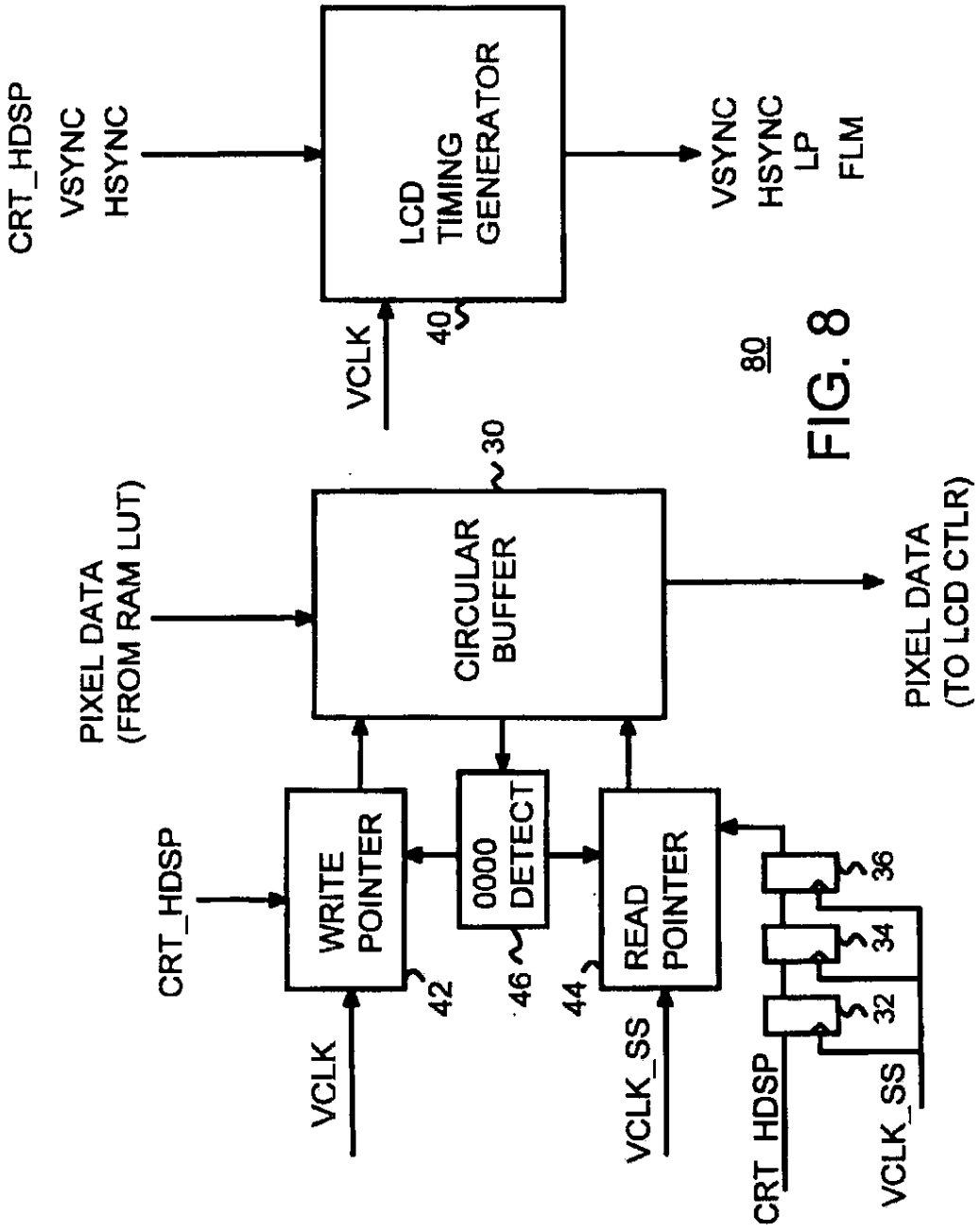

CRT_HDSP
VSYNC
HSYNC
LCD TIMING GENERATOR
VSYNC
HSYNC
LP
FLM
VCLK
40
80
30
PIXEL DATA (FROM RAM LUT)
CIRCULAR BUFFER
PIXEL DATA (TO LCD CTLR)
CRT_HDSP
WRITE POINTER
0000 DETECT
READ POINTER
36
34
32
42
46
44
VCLK
VCLK_SS
CRT_HDSP
VCLK_SS

FIG. 8

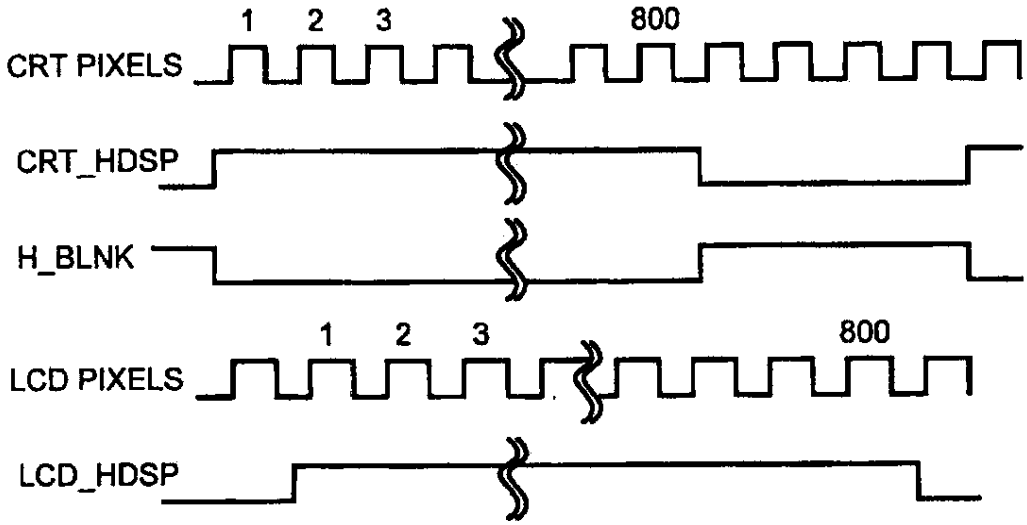

1
2
3
800
CRT PIXELS
CRT_HDSP
H_BLNK
1
2
3
800
LCD PIXELS
LCD_HDSP

FIG. 9

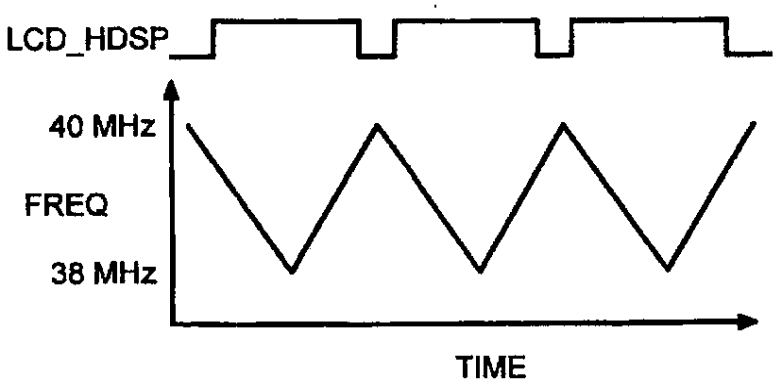

LCD_HDSP
40 MHz
FREQ
38 MHz
TIME

FIG. 10

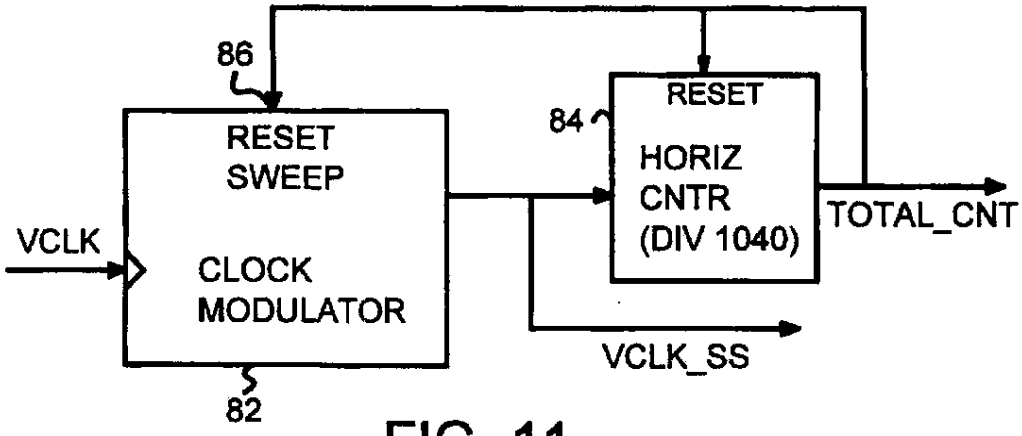

86
RESET
SWEEP
84
RESET
HORIZ
CNTR
(DIV 1040)
TOTAL_CNT
VCLK
CLOCK
MODULATOR
VCLK_SS
82

FIG. 11

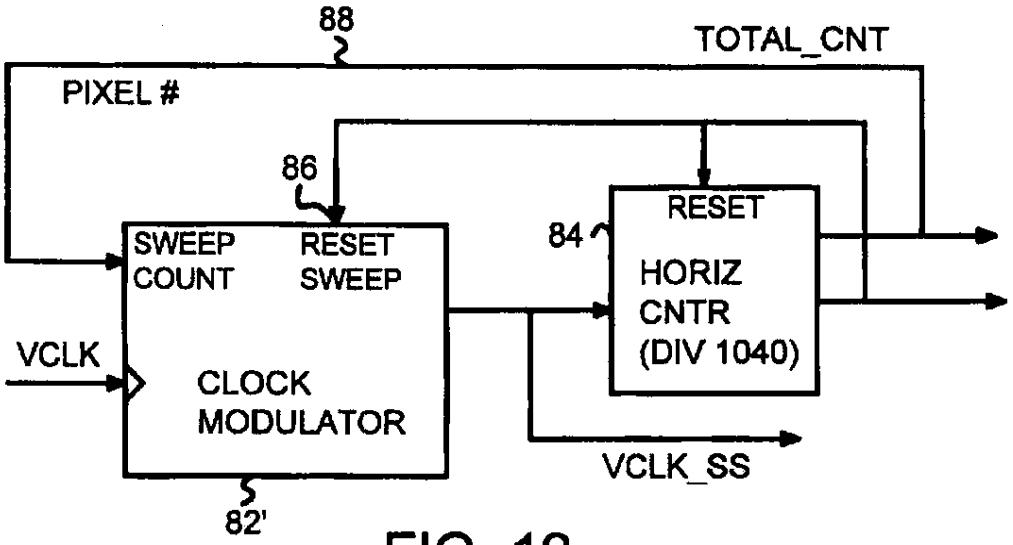

88
TOTAL_CNT
PIXEL #
86
RESET
84
SWEEP
COUNT
RESET
SWEEP
HORIZ
CNTR
(DIV 1040)
VCLK
CLOCK
MODULATOR
VCLK_SS
82'

FIG. 12

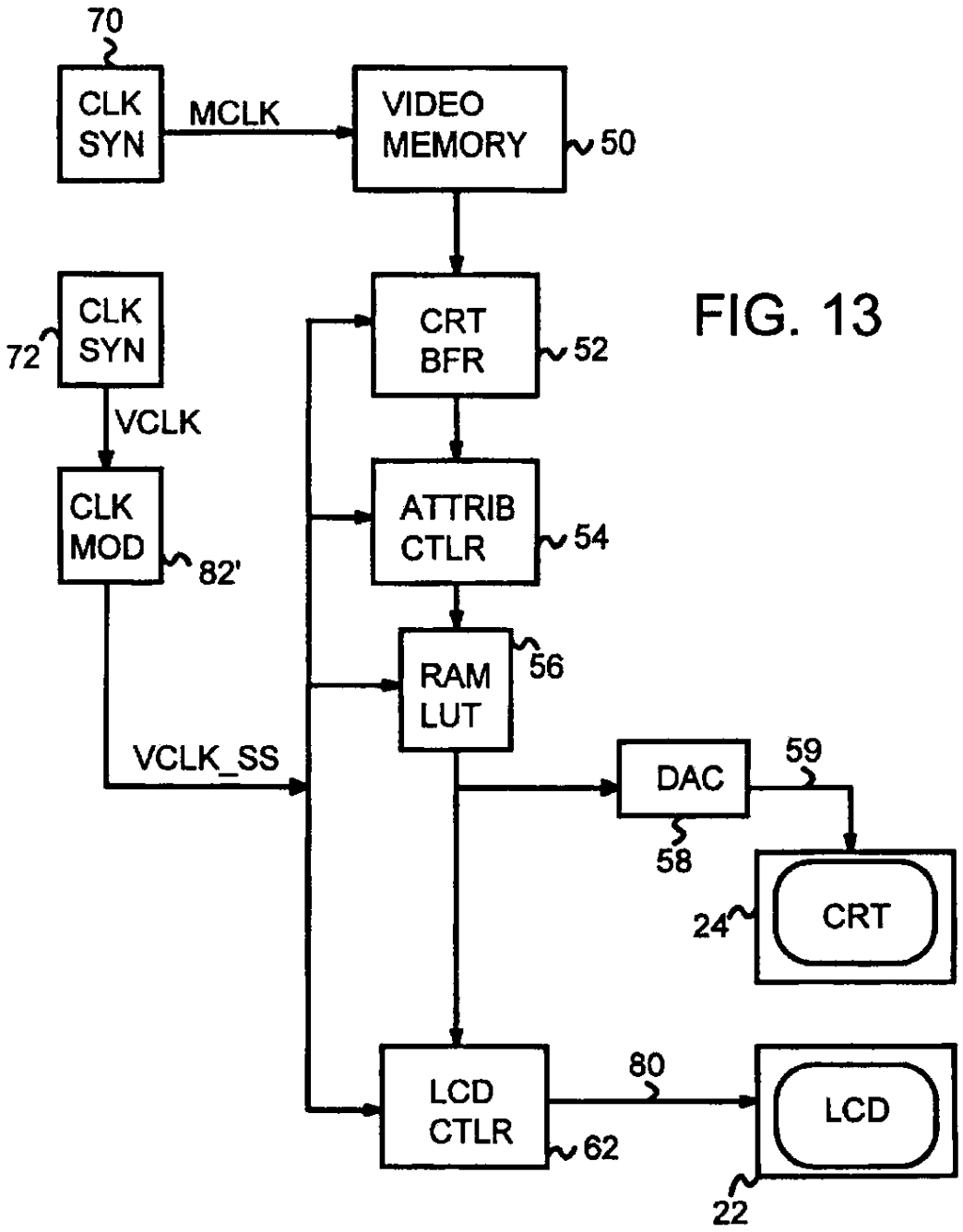

70
CLK SYN
MCLK
VIDEO MEMORY
50
CLK SYN
72
VCLK
CRT BFR
52
CLK MOD
82'
ATTRIB CTLR
54
RAM LUT
56
VCLK_SS
DAC
59
58
24
CRT
LCD CTLR
62
80
LCD
22

FIG. 13

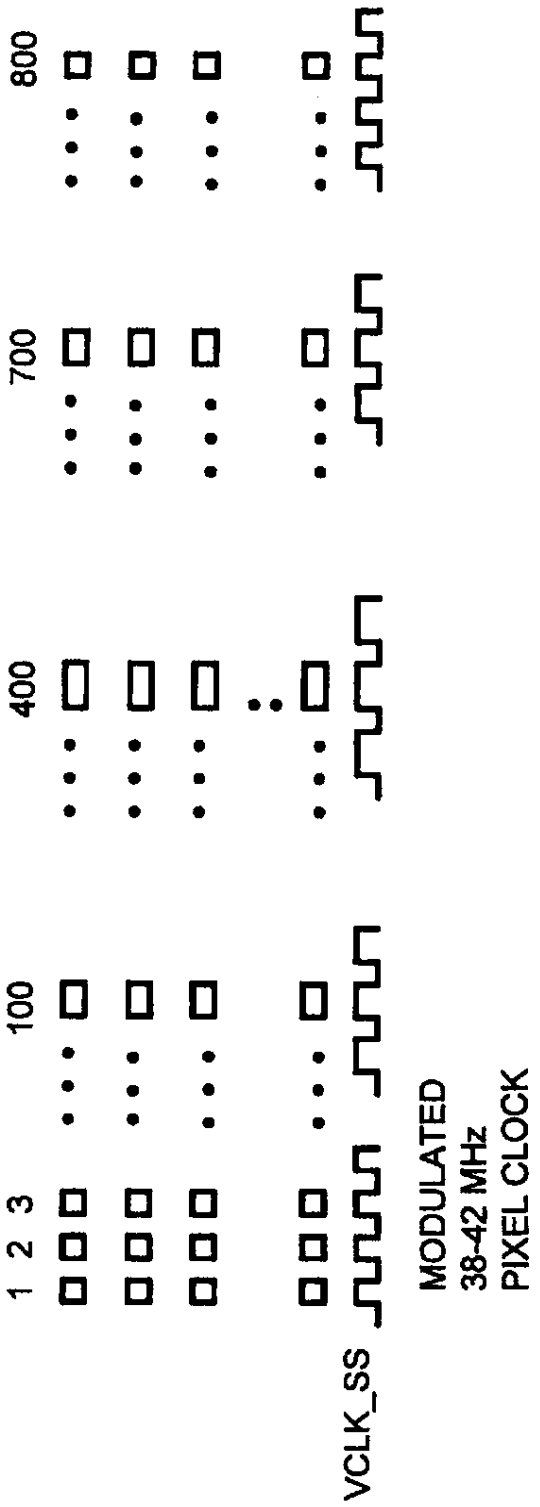


FIG. 14

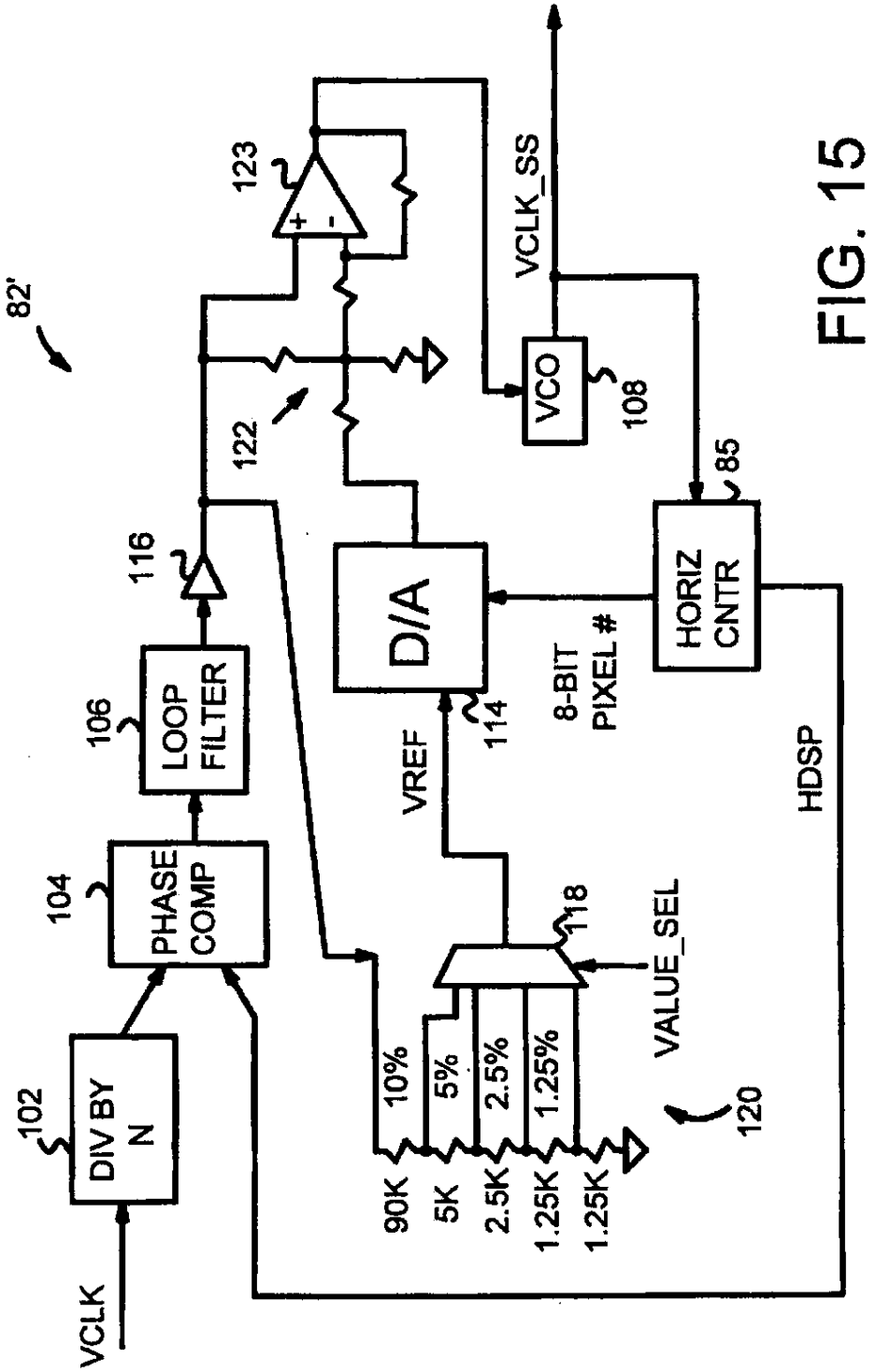

82'
123
VCLK_SS
VCO
108
122
85
116
D/A
HORIZ CNTR
106
LOOP FILTER
8-BIT PIXEL #
114
VREF
HDSP
104
PHASE COMP
118
VALUE_SEL
102
DIV BY N
10%
5%
2.5%
1.25%
120
90K
5K
2.5K
1.25K
1.25K
VCLK

FIG. 15

EMI REDUCTION FOR A FLAT-PANEL DISPLAY CONTROLLER USING HORIZONTAL-LINE BASED SPREAD SPECTRUM

BACKGROUND OF THE INVENTION

Field of the Invention

This invention relates to reduction of electromagnetic interference (EMI) from computer equipment, and more particularly for methods to reduce EMI from a graphics subsystem.

BACKGROUND OF THE INVENTION

Description of the Related Art

Electronic equipment can often generate interference which creates disturbances in other electronic equipment. For example, a portable computer may emit radiation which interferes with a television receiver. Intentional receivers, such as televisions, cellular phones, pagers, and wireless devices, are often affected by unintentional transmitters which emit electromagnetic radiation. As both types of electronic equipment become more common, interference becomes more noticeable to the consumer.

Electromagnetic interference (EMI) is a measure of the amount of interference that an electronic device (the unintentional transmitter) disturbs an intentional receiver. Government agencies such as the Federal Communication Commission (FCC) strictly regulate the amount of radiation or EMI that an electronic device can generate.

Portable devices such as portable personal computers (PC's) are particularly problematic since these portable devices are easily placed near televisions or other receivers. Cramped office and living spaces often force electronic equipment closer together. Since radiation rapidly decreases with distance, smaller and more portable equipment often appear to generate more interference.

Improving technology also worsens the EMI problem. Faster clock rates of higher-speed PC's generate more radiation. Higher resolution monitors and displays require that more pixels be transferred to the screen for each screen refresh period; thus a higher clock rate and more interference results.

Flat-Panel Interface Generates More EMI Than CRT Interface

Traditional cathode-ray-tube (CRT) monitors are connected to PC's by shielded cables to control EMI. CRT's are driven by relatively low analog voltages which farther minimize EMI. Thus although the long cable acts as a good antenna, the shielding and low voltages greatly reduce EMI.

Portable computers typically contain a flat-panel display using technologies such as LCD (liquid-crystal-display) or TFT (thin film transistor). A graphics controller is normally located under the keyboard and is connected to the display through one or more hinges. These hinges are limited in size and thus shielding the cable between the graphics controller and the display is not practical. The flat-panel display is close to the graphics controller, so EMI is reduced since the parasitic antenna length is small. However, the interface between the graphics controller and the display is usually all digital, using 5-volt TTL signals. A large number of signals is required for the interface, perhaps 8 to 36 signals for the pixel data itself. Thus the flat-panel display's interface generates more interference that the CRT interface.

Traditional techniques to reduce EMI attempt to contain radiation or to reduce the amount of radiation generated. Coax wires and shielded cables are effective at containing radiation, but are expensive, heavy, bulky, and inflexible. The weight and bulk of shielded cables make them undesirable for portable computers. The bulk and relative inflexibility of shielded cables makes it difficult to thread them through the clam-shell hinges connecting the graphics controller in the keyboard-containing base unit with the flat-panel display. Metal chassis with sealed seams are effective for reducing EMI of desktop PC's, but portable PC's are kept light by using plastic. Toxic metal paints are sometimes sprayed on plastic housings for portable PC's to provide shielding.

Lower voltages reduce the intensity of the radiation generated, and the new 3-volt standard has helped reduce EMI at all harmonics. Proper impedance matching and termination of signals reduces ringing and harmonics, and shorter signal traces further reduce radiation. Ground planes on PCB's or ground lines running parallel with signal lines effectively shield signals on boards. Filtering can reduce sharp rise and fall times and reduce radiation by wave shaping since more sinusoidal waves have fewer harmonics than square waves. Of course, filters require additional capacitors, resistors, or inductors, raising the cost. All of these techniques are useful to varying extents.

Frequency Modulation—Spread Spectrum

A newer technique to reduce EMI is to vary or modulate the frequency of clocks in the PC. This technique known as spread spectrum, since the frequency spectrum of the clock is spread out over a wider range of frequencies. FIG. 1 shows a graph of radiation intensity as a function of frequency for an un-modulated clock signal. A sharp spike occurs at a harmonic of the clock's frequency, 40 MHz. Since the clock constantly operates at the rated frequency, all of the energy of the radiation appears in a narrow spike, which has a large amplitude. The spike has an amplitude over the EMI limit set by the FCC. The high intensity of the spike can cause interference in a receiver.

FIG. 2 is a graph of radiation intensity as a function of frequency generated by a modulated clock. The clock's frequency is not constant, but is varied with time over a range of +5% to −5% of the rated frequency. Thus the clock operates at 40 MHz for a period of time, but also operates at other frequencies between 38 MHz and at 42 MHz at other times. Such a clock can be generated by slowly changing the frequency from 38 MHz to 42 MHz and then slowly reducing the frequency back to 38 MHz. A voltage-controlled oscillator (VCO) can be used with the input voltage being slewed back and forth between voltages which generate 38 MHz and 42 MHz oscillations.

Since the modulated clock spends only part of the time at 40 MHz, the intensity of the radiation, averaged over a relatively long time, is reduced. The total energy of the radiation at all frequencies is about the same as for the un-modulated clock of FIG. 1, but the intensity at any particular frequency is greatly reduced. Interference at any one frequency is reduced since receivers generally are tuned to a particular frequency (even FM receivers are tuned to a relatively small range of frequencies).

Thus modulating the clock's frequency reduces the maximum intensity of radiation at any one frequency, although the energy radiated at all frequencies is not reduced. This has the practical effect of reducing interference for receivers tuned to a fixed frequency.

The clock's frequency must not change too rapidly. Rapid variations in frequency can upset phase-locked loops (PLLs) driven by the modulated clock. These PLLs can lose the phase lock and produce erratic outputs. Thus the frequency is modulated slowly. The clock's frequency must not change too slowly, to avoid losing the benefit of EMI reduction.

Graphics controllers in particular have many clocks derived from the input graphics clock. For instance, for SVGA resolution mode a basic clock is multiplied and divided to generate a 40 MHz pixel clock, a 37 KHz HSYNC clock, and a 60 Hz VSYNC clock, and perhaps a 5 MHz character clock. Different resolutions can require that the clock multiplier and divisors be changed to produce signals with the desired timing for that selected resolution.

Phase-locked loops (PLL's) generate a clock by comparing the phase of an input clock to the phase of a generated clock, which is fed back to the phase comparator. The output of the phase comparator is filtered and then input to a voltage-controlled oscillator (VCO). The VCO varies the frequency of the generated clock as the filtered voltage from the phase comparator varies.

The frequency of the generated clock from the VCO does not have to be the same as the frequency of the input clock. The input clock can be divided by a counter to reduce the frequency of the generated clock (clock divisor), while the generated clock fed back to the phase comparator can be divided to increase the frequency of the generated clock (clock multiplier). Since the resolutions are programmable and can be changed by older user application programs, the clock multipliers and divisors are often changed to new values.

These changeable divisors and multipliers can delay phase comparison by many clock periods, resulting in added delays until a modulation in the clock frequency is responded to. For example, a divisor or multiplier of 16 causes the phase comparison to be delayed up to 16 clock periods. The output frequency of the PLL can drift between these delayed phase comparisons, resulting in more jitter.

Typically the loop filter values in these PLL's are made large to provide low jitter with a stable reference clock. When this reference clock is purposely modulated, the PLL is no longer operating with a stable reference as it was designed for. This can upset the PLL and introduce more jitter than anticipated.

Long Sweep Period of Modulation—FIG. 3

FIG. 3 is a graph of a modulated clock's frequency as a function of time over a few sweep periods. The clock's nominal frequency is 40 MHz. The clock is modulated by +/−5%, from 38 MHz to 42 MHz. The clock's frequency is swept from minimum to maximum frequencies over one or two thousand clock periods so that adjacent clock pulses have a very small variation. A 40 MHz clock with a 25 nanosecond (ns) period is varied from 26.25 ns to 24.75 ns over a sweep period, a variation of +/−1.25 ns. A 37 KHz sweep rate has a sweep period of 27 micro-seconds (μs). A sweep period is 27 μs/25 ns or 1081 clock periods. The cycle-to-cycle period variation for two adjacent clock periods is thus 1.25 ns/1081 or 1.15 pico-seconds (ps). This small cycle-to-cycle variation is needed to prevent PLL's from losing their phase lock. The sweep period is typically 15 to 30 KHz.

CRT Display Scans Horizontal Lines of Pixels at HSYNC Rate

FIG. 4 is a diagram of a display, which could be a cathode-ray-tube (CRT) video display, or a flat-panel liquid-crystal display (LCD) or other type of display. An image is formed on the display screen by selectively energizing or illuminating small dots or pixels on the screen. In a CRT, a pixel is energized by an electron gun that directs a beam of energizing electrons to a particular point on the screen. The electron beam is scanned from left to right in a horizontal line and pulsed to illuminate some points on the line but not others. The screen is divided into a number of horizontal lines **10**, **12**, **16**, with each line comprising a number of pixels. The pixels in a line are illuminated one-by-one from the left side to the right side of a horizontal lines **10**, **12**, **16**.

Once the entire horizontal line **10**, **12**, **16** has been scanned, the electron beam is disabled or "blanked" so that no pixels are energized and the electron beam is re-traced back to the beginning on the next horizontal line **12**. This horizontal re-trace **14** follows a diagonal path. After re-trace, the blanking is ended and the next horizontal line **12** is scanned. The process of scanning a horizontal line and re-tracing is repeated until all lines are scanned. Once scanning of the last horizontal line **16** is complete, the electron beam is returned to the beginning of the first line **10** by a vertical re-trace **18**. The electron beam is again blanked to prevent any illumination while the electron beam is being retraced to the top of the screen.

Pixels not in a Fixed Location on Screen

One characteristic of a CRT is that the pixels are created on the screen at a location that is not fixed. The location of a certain pixel on the screen is determined by the timing of the lines and pixels being written to the screen. The distance of a pixel from the left of the visible screen, the first pixel at the beginning of the line, is determined by the number of pixels written so far to the horizontal line. Ordinarily the eight-hundredth pixel of each horizontal line appears at about the same distance from the left of the screen. This distance is determined by the number of pixels written in the line, multiplied by the width of each pixel. The width of the pixel is determined by the period of the pixel clock which times the writing of the pixel to the display.

When the pixel clock is not constant, but modulated, then some pixels appear wider than others. A pixel written when the pixel clock is at 38 MHz appears about 10% wider than a pixel written when the pixel clock is 42 MHz. While this difference in pixel width is not noticeable for an individual pixel, the different pixel widths are accumulated over hundreds of pixels until pixels near the middle or end of the horizontal line are visibly displaced.

Visible differences are especially noticeable when one horizontal line is written with a higher pixel-clock rate than an adjacent line. FIG. 5 shows a display using a modulated clock where different lines have pixels displaced relative to pixels in other lines. Horizontal line **11** is written with a 42 MHz pixel clock, while line **13** is written with a 40 MHz pixel clock and line **15** with a 38 MHz pixel clock. While the difference in the width of any individual pixel is slight, when accumulated over 100 pixels, the difference is apparent. The displacement of the one-hundredth pixel of line **11** relative to line **15** is 100×10% or 10 pixels. This is a large, easily noticeable displacement.

As more pixels for a horizontal line are written, the frequency of the pixel clock is swept. Thus line **11** has the first pixel written with the pixel clock at 42 MHz, but later pixels are written with the pixel clock closer to 40 MHz or 38 MHz, depending on the sweep rate and the horizontal line rate. Thus the differences between lines can be lessened as more pixels on the line are written, so that by the time the

last pixel is written, the displacement is smaller. However, some pixels at the end of the line may not be displayed if the horizontal blanking signal turns on early and the last pixel is written too late. Thus some of the pixels at the right edge of the display may be lost.

Sweep Period and Horizontal Sync Period of CRT

FIG. 5 is an idealized case where each line begins at a particular frequency. In reality, each line begins at a frequency which is determined by the sweep rate and the horizontal line rate. This sweep rate, about 30 KHz, is on the order of the horizontal sync rate for many CRT monitors, which typically have HSYNC rates of 30 to 50 KHz.

Other problems using a modulated clock with a graphics subsystem occur when internal PLL's in the graphics controller have a loop delay which is long relative to the change in frequency due to clock modulation. The large loop delay may cause the PLL to not be able to keep track with the modulation sweep, causing erratic behavior.

Image Distortions When Graphics Clock is Modulated—FIG. 6

FIG. 6 shows a portable PC driving a flat panel and a CRT when the graphics clock is modulated. Laptop PC 20 has a flat-panel LCD display 22 built into the portable PC, and a separate CRT which can simultaneously display the same image which is displayed on LCD display 22.

When the graphics clock is modulated with a sweep rate of about 15 to 30 KHz, the standard setting for a commercial clock modulation product, the image is displayed properly on LCD display 22, but the same image on CRT 24 is noticeably distorted. Vertical lines are not straight, although horizontal lines appear correctly. The image on CRT 24 appears to zig-zag and wiggle, since pixels in one horizontal line are displaced relative to pixels in other adjacent horizontal lines. This displacement is caused by different clock frequencies being used when different lines are written.

Since the frequency of the modulated clock is constantly changing, and is not an exact multiple of the horizontal line rate, each time the screen is re-drawn, the pixels on any line move relative to their last position. The PLL's also introduce random jitter, as they are unable to keep up with introduced modulations when the reference clock is divided and phase comparisons are delayed. Thus the wiggle appears to change as each new screen refresh occurs, and the image jumps around. Text is broken and fuzzy and nearly impossible to read. Some data may even be lost off the right edge of the screen.

In sharp contrast, the image on LCD display 22 is not distorted. Pixels on a flat-panel display are not written by an electron beam, but are written by applying voltages to x and y coordinates on a grid making up the display screen. Since the pixel position is determined by the physical grid, the image does not suffer from displacements.

However, some horizontal lines are brighter than other lines. The brightness of a pixel on a flat-panel display is determined by the amount of time that a voltage is applied. Since the clocks are modulated, some lines have longer periods than other lines. This causes some lines to momentarily appear brighter or dimmer than other adjacent lines.

After a period of time, the display is damaged. The display should be driven with A.C. voltages, with the amount of time a negative voltage is driven being equal to the amount of time that a positive voltage is driven. However, clock modulation allows some lines to remain in one polarity longer than in the other polarity. Over time, D.C. voltages build up for some lines and can damage the display grid.

What is desired is to apply spread-spectrum techniques and reduce EMI from a graphics subsystem. It is desired to modulate the graphics clock without distorting the image to a CRT. It is further desired to modulate a graphics clock in a portable computer to reduce radiation. Both the flat-panel and an external CRT monitor should be driven without distortions.

SUMMARY OF THE INVENTION

A graphics controller reduces electromagnetic interference (EMI). A pixel-transfer path has buffering means for buffering pixels from a video memory and pixel processing means for processing pixels. The pixel-transfer path has a pixel output. A flat-panel converter receives pixels from the pixel output of the pixel-transfer path. It converts pixels to a format for transfer to a flat-panel display. The flat-panel converter has a panel-interface output coupled to the flat-panel display.

Video clock means supplies a video clock for synchronizing the transfer of pixels. The video clock has a constant frequency. The video clock is coupled to the pixel-transfer path. A timing generator is coupled to receive the video clock. It generates horizontal and vertical timing signals for synchronizing display of horizontal lines of pixels. The horizontal and vertical timing signals are coupled to the flat-panel display.

Modulated video clock means supplies a frequency-modulated video clock to the flat-panel converter. The flat-panel converter transfers pixels out the panel-interface output to the flat-panel display at a modulated rate proportional to a current frequency of the frequency-modulated video clock. Thus pixels are transferred to the flat-panel display using the frequency-modulated video clock, reducing EMI, but the horizontal and vertical timing signals are generated by the video clock without modulation.

In further aspects of the invention a digital-to-analog converter (DAC) is coupled to receive pixels from the pixel output of the pixel-transfer path. The DAC converts pixels to analog voltages for driving a cathode-ray-tube (CRT) display. The DAC converts pixels to the analog voltages a constant rate proportional to the video clock. The CRT receives the horizontal and vertical timing signals from the timing generator. Thus pixels are transferred to the CRT at the constant rate while pixels are transferred to the flat-panel display at the modulated rate.

In further aspects the CRT is driven with pixels to display a same image as displayed on the flat-panel display. A FIFO is coupled between the pixel output and the flat-panel converter. It receives pixels from the pixel-transfer path in response to a pulse of the video clock, and it outputs pixels to the flat-panel converter in response to a pulse of the frequency-modulated video clock. Thus pixels synchronized to the video clock are buffered by the FIFO to by synchronized to the frequency-modulated video clock, the frequency-modulated video clock is asynchronous to the video clock.

In still further aspects the frequency-modulated video clock sweeps through frequencies less than and equal to the constant frequency of the video clock. Thus pixels are outputted from the FIFO more slowly than pixels are received into the FIFO.

In other aspects a clock modulator receives the video clock and modulates the constant frequency of the video

clock to the current frequency to generate the frequency-modulated video clock. The frequency-modulated video clock is coupled to the modulated video clock means. Thus the frequency-modulated video clock is generated by modulating the current frequency of the video clock. The clock modulator sweeps the current frequency in small increments between a maximum frequency and a minimum frequency so that the current frequency is gradually changed.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 shows a graph of radiation intensity as a function of frequency for an un-modulated clock signal.

FIG. 2 is a graph of radiation intensity as a function of frequency generated by a modulated clock.

FIG. 3 is a graph of a modulated clock's frequency as a function of time over a few sweep periods.

FIG. 4 is a diagram of a display, which could be a cathode-ray-tube (CRT) video display, or a flat-panel liquid-crystal display (LCD) or other type of display.

FIG. 5 shows a display using a modulated clock where different lines have pixels displaced relative to pixels in other lines.

FIG. 6 shows a portable PC driving a flat panel and a CRT when the graphics clock is modulated.

FIG. 7 is a diagram of a CRT and LCD graphics controller using a modulated clock for the LCD portion but not for the CRT portion to reduce EMI for the LCD panel interface.

FIG. 8 is a diagram of a FIFO and timing logic added to the LCD datapath to buffer data for transfer over the panel interface using the modulated clock for EMI reduction.

FIG. 9 is a timing diagram for a graphics controller driving a CRT with un-modulated signals but driving a LCD display with pixels using a modulated clock.

FIG. 10 is a graph of a modulated clock which has the frequency sweep reset during the horizontal blanking time for each horizontal line.

FIG. 11 is a diagram of a clock modulator which is reset by the end of the displayable portion of a horizontal line.

FIG. 12 shows a clock modulator which uses the horizontal counter as the frequency sweep counter.

FIG. 13 is a diagram of an LCD & CRT graphics controller with clock modulation which is reset at the end of each horizontal line.

FIG. 14 shows that the VCLK period for successive pixels slowly increases as the frequency decreases as the line is written, but the same decrease occurs for each line.

FIG. 15 is a diagram of a modulated clock generator 82' which uses the horizontal pixel counter to modulate the clock.

DETAILED DESCRIPTION

The present invention relates to an improvement in EMI reduction in graphics subsystems. The following description is presented to enable one of ordinary skill in the art to make and use the invention as provided in the context of a particular application and its requirements. Various modifications to the preferred embodiment will be apparent to those with skill in the art, and the general principles defined herein may be applied to other embodiments. Therefore, the present invention is not intended to be limited to the particular embodiments shown and described, but is to be accorded the widest scope consistent with the principles and novel features herein disclosed.

As discussed in the background section, modulation cannot simply be applied to the input clock of a graphics controller, since the CRT's image is distorted, while the LCD flat panel experiences brightened and dimmed horizontal lines, and possibly damage from D. C. voltage buildup.

Spread-Spectrum Applied to Flat-Panel Display, but not to CRT

The inventors have realized that the CRT typically uses a shielded cable which conducts low-voltage-swing analog signals. Thus the CRT is not a major EMI radiator. In contrast, the flat-panel interface, although being shorter in length, is a major EMI source since full-voltage-swing digital signals are used, often with parallel data signals. Shielding the flat-panel interface is costly, bulky, and thus undesirable. The inventors have therefore realized that spread-spectrum techniques can be beneficially applied to the flat-panel interface but not to the CRT interface.

Since graphics controller are so complex, many different ways to integrate spread-spectrum into the controller are possible. Many configurations are even possible when the modulated clock is applied to the LCD path and not to the CRT path. A simple implementation is to apply the modulated clock to just the shift clock which shifts a group of pixels into a shift register in the flat panel. However, adding the spread spectrum at this point introduces extra delay. This extra delay can cause the data to not be latched into the panel's shift register with the required set-up time, requiring that an additional set of latches be added. Another problem occurs when the modulated clock causes the pixels to be written more slowly than nominal. Some pixels at the end of the horizontal line may be delayed so much that they are not latched into the shift register before the data in the shift register is transferred to the display grid. Thus some pixels at the end of the line may be lost.

The shift clock and the group of pixels outputted from the graphics controller can be buffered with a FIFO or other buffer at the output of the graphics controller. Unfortunately, power, cost, and board area occupied can increase. But the buffer could also be located at other points in the LCD datapath.

Rather than have two separate datapaths, one for the CRT and a second for the LCD panel, the CRT's datapath is shared with the LCD datapath. Most of the buffering, color mapping, and attributes added for the CRT path also needs to be performed for the LCD path. The CRT's datapath can be tapped off before conversion to analog voltages, and the pixels sent to an LCD controller for gray-scale conversion and other formatting needed for the panel interface. Thus the graphics controller has a partially combined or shared datapath.

FIG. 7 is a diagram of a CRT and LCD graphics controller using a modulated clock for the LCD portion but not for the CRT portion to reduce EMI for the LCD panel interface. A first clock synthesizer 70 is used to generate a memory clock MCLK, which is used to time and sequence accesses to video memory 50. Video memory 50 stores pixels for display on CRT 24 and LCD display 22. The image of the screen stored in graphics memory 50 can be stored either as raw pixels or as characters of text along with a character map for converting text to pixel bitmaps. New images are written by a host processor to video memory, perhaps through a FIFO or buffer (not shown) to synchronize data transferred using the host's clock to the memory clock.

As the screen is refreshed, requests for more pixels are generated to video memory 50, and pixels are copied from video memory 50 to CRT buffer 52 using the memory clock

MCLK to write the pixels into CRT buffer **52**. These pixels are read out of CRT buffer **52** by an asynchronous pixel or video clock VCLK. VCLK is generated by second clock synthesizer **72**. Both first clock synthesizer **70**, generating MCLK, and second clock synthesizer **72**, generating VCLK, can be constructed from PLL's which receive a stable input clock, such as a graphics clock input to the controller chip. A standard 14.318 MHz clock is often used.

Pixels read from CRT buffer **52** are sent to attribute controller **54**, which modifies pixels to add attributes such as blinking or reverse video. Pixels are then clocked to RAM look-up table **56**, which contains a table in memory to re-map the color represented by a pixel. Thus a larger, richer color space can be used than is indicated by the raw number of bits in a pixel.

The re-mapped pixels from RAM look-up table **56** are transferred to digital-to-analog converter (DAC) **58**. DAC **58** converts these pixels from digital values to analog voltages for red, green, and blue (RGB) sub-pixels. These analog voltages drive three signal lines in shielded cable **59** which connects the PC to external CRT **24**. CRT **24** then converts these analog voltages to intensities of a red, green, and blue electron beams which are focused on a point on the screen to display a pixel at the current scan location.

Pixels from RAM look-up table **56** are also sent to LCD display **22** through a second connection to EMI FIFO **60**. EMI FIFO **60** receives pixels from RAM look-up table **56**. These pixels are written to EMI FIFO using video clock VCLK. The pixels are temporarily stored in EMI FIFO **60** and read out to LCD controller **62** using a modulated video clock, VCLK_SS. LCD controller **62** performs formatting of pixels and gray-scale conversion so that the pixels are in a format accepted by LCD display **22**. The formatted pixels are clocked out of LCD controller **62** and to LCD display **22** over panel interface **80**.

Panel interface **80** thus is clocked by a modulated video clock VCLK_SS, or a derivative of this clock. A shift clock SCLK may be generated to shift several pixels over panel interface **80** in a single, slower clock cycle. Using a slower clock for the external interface allow a faster internal clock to be used where delays are smaller. The shift clock is simply a divided-down version of the modulated video clock VCLK_SS. Thus the shift clock is also modulated, reducing EMI radiation from panel interface **80**.

Clock modulator **74** receives video clock VCLK and modulates the clock, producing VCLK_SS, the spread-spectrum video clock. The current embodiment uses an external clock modulator chip for clock modulator **74**, so output buffer **76** and input buffer **78** are needed for buffering the video clock off the controller chip and receiving the modulated video clock as an input on the I/O pins of the controller chip. An external clock modulator chip is sold by International Microcircuits, Inc. of Milpitas, Calif. as the IMISM530 Reduced EMI Clock Modulator Chip.

Multiplexer **79** selects the modulated video clock from clock modulator **74** when the EMI-reduction mode is active, but the normal video clock VCLK is selected by multiplexer **79** as VCLK_SS when EMI mode is disabled. This allows the EMI modulation to be disabled. When EMI mode is disabled, video clock VCLK (or derivatives) clock LCD controller **62** as well as RAM look-up table **56**, attribute controller **54**, and CRT buffer **52**.

Enabling EMI mode selects the modulated video clock, VCLK_SS, for LCD controller **62** and EMI FIFO **60**. This uses modulated signals for panel interface **80**, reducing EMI emissions.

Spread-spectrum clock modulation is thus applied only to the LCD flat-panel interface without modulating clocks in the CRT datapath. Thus no image distortion occurs on the CRT, while EMI emissions are reduced for the flat-panel interface. Since the clock modulation is applied after the internal PLL's, problems with loss of phase lock and jitter are eliminated.

EMI FIFO—FIG. 8

FIG. **8** is a diagram of a FIFO and timing logic added to the LCD datapath to buffer data for transfer over the panel interface using the modulated clock for EMI reduction. EMI FIFO **60** contains circular buffer **30** which stores pixels received from RAM look-up table **56** for buffering to LCD controller **62** of FIG. **7**. Write pointer **42** points to and enables a memory location in circular buffer **30** to receive the next pixel from RAM look-up table **56**. Each pixel is written by a pulse of video clock VCLK, which is not modulated. Write pointer **42** increments with each pulse of VCLK when pixels are being transferred. Horizontal display signal CRT_HDSP is active when pixels are being transferred, but inactive during the horizontal blanking periods of the CRT when the electron beam is being re-traced to the beginning of the next horizontal line. Thus CRT_HDSP can be used to enable write pointer **42** at the beginning of a new horizontal line. Write pointer **42** loops back to zero after the maximum count is reached so that pixels are written to circular buffer **30** in a continuous loop.

Read pointer **44** points to and enables a next location for reading a pixel from circular buffer **30**. Each pixel is read out of circular buffer **30** by a pulse of modulated video clock VCLK_SS, which increments read pointer **44**. Upon reaching the terminal count, read pointer **44** also loops back to zero to continnously count in a loop.

Since the write and read clocks to the FIFO are asynchronous, due to the introduced modulation, the FIFO is a full dual-port FIFO. Reads and writes can be fully asynchronous to each other. A read can occur simultaneously with a write.

Since there is a slight delay before a pixel written to circular buffer **30** may be read out, the reading of the first pixel in a horizontal line must be delayed. Flip-flops **32**, **34**, **36** delay horizontal display signal CRT_HDSP by three periods of VCLK_SS before enabling read pointer **44**. This delay is sufficient to allow the first pixel to be written to circular buffer **30** and ready for reading.

Disabling circular buffer **30** at the end of a horizontal line could be accomplished in a variety of ways. An end-of-horizontal line marker can be used. A pixel is encoded with a special pixel code which indicates the end of the horizontal line. For example, the code "0000" can be encoded into a pixel at the end of each horizontal line to signal that the line is over. This code also indicates that this pixel is not to be displayed. End detector **46** looks at pixels in circular buffer **30** and compares the code for these pixels to the special pixel code "0000". When a match is found with the pixel being written, end detector **46** disables and resets write pointer **42**. When a match is found with the pixel being read, end detector **46** disables and resets read pointer **44**. Thus end detector **46** can compare the pixels being read or written rather than all pixels in circular buffer **30**. An alternative is to only compare the pixel being read, and then reset and disable both write pointer **42** and read pointer **44**, discarding any extra pixels written after the end of the horizontal line. The FIFO is then reset at the end of every horizontal line, during the non-displaying period such as the horizontal blanking period.

A preferred method to detect the end of the horizontal line is to store a flag with the pixel data in the FIFO. The flag is set for pixels in the displayable portion of the line, but cleared for blanking periods. End detector **46** merely reads this flag from circular buffer **30** and disables the read and write pointers when a zero is detected. The flag is simply the CRT_HDSP signal which is set during the displayable portion of the horizontal line. The CRT_HDSP signal is written to circular buffer **30** as an extra bit of the pixel word. Other control signals can also be written to circular buffer **30** in parallel with each pixel and CRT_HDSP.

LCD Timing Signals Don't Use Modulated Clock

LCD timing generator **40** receives the CRT timing signals and generates timing signals for the LCD flat-panel display. The CRT's VSYNC, HSYNC, and CRT_HDSP signals mark the beginning of a new frame or screenfull of lines, the beginning of a new horizontal line of pixels, and when the pixels in a line are being displayed, respectively.

The timing of these signals need to be changed slightly, for instance by advancing the line-pulse (LP) start to meet front and back porch requirements for the panel. Additional signals are needed by the LCD display panel, such as a line-pulse (LP) signal and a first-line marker (FLM) signal. The line-pulse signal is a pulse during the horizontal blanking period at the end of a line which causes the panel to shift all of the pixels for the horizontal line just written from a shift register to the display grid. An entire line of pixels is first shifted into this shift register in the panel assembly and then the shift register dumps all of the pixels to the display grid. Thus instead of scanning individual pixels, the flat-panel display accumulates pixels for a line and then displays the whole line of pixels for the entire horizontal line period.

LCD timing generator **40** uses the un-modulated video clock VCLK to generate these signals. The modulated video clock is not used so that these critical timing signal are always constant and never varied due to clock modulation. Thus the horizontal period does not vary, even through the pixels in the horizontal line are transferred using a modulated clock. The shift register in the panel assembly effectively buffers the pixels transferred in using the modulated clock to the un-modulated horizontal timing signals.

Constant Horizontal Period Despite Modulated Pixel Transfer

Using the un-modulated clock to generate the horizontal timing signals for the flat panel eliminates the problem with brighter and dimmer horizontal lines which occurs then the horizontal signals are generated with a modulated clock, as described in the background section. Each horizontal line has the same display time, and each frame of lines also has the same display time. Thus the panel interface reduces EMI radiation from pixel transfer, while maintaining constant horizontal timing and eliminating dim and bright lines and D.C. buildup of charge caused by variations in how long each horizontal line is displayed.

Full and Empty Flags Not Needed

While full and empty flags could be used to prevent data over- and under-runs, the clock modulation can be set to a "down mode" to sweep through frequencies less than the frequency of the video clock. This guarantees that the modulated video clock VCLK_SS is always equal to or less than the frequency of video clock VCLK. Thus pixels are always read out of circular buffer **30** at a frequency equal to or less than the frequency that pixels are written into circular buffer **30**. Using a slower frequency for reading ensures that circular buffer **30** never becomes empty while the horizontal line is being displayed. Thus an empty flag is not needed.

Circular buffer **30** can be designed to have a storage capacity, or depth, large enough for the largest horizontal line, when the modulated frequency is at its lowest value. Since modulation is typically only 2.5% of the frequency, the data-rate mismatch is small, less than 2.5% of the number of pixels in the horizontal line. For Super VGA, each horizontal line has 800 pixels. Five percent of the pixels is 20 pixels. Thus a relatively small circular buffer may be used.

The clock modulation can also be set to "up-down mode" where the clock modulates both above and below the nominal frequency. The reading of the FIFO is started later than when "down mode" is used and a larger FIFO used to compensate for the modulated clock sometimes being faster than the nominal clock.

LCD Pixels Delayed into Horizontal Blanking Period

FIG. **9** is a timing diagram for a graphics controller driving a CRT with un-modulated signals but driving a LCD display with pixels using a modulated clock. CRT pixels are transferred to the CRT display over a shielded cable using an un-modulated video clock for timing. Each pixel has the same period. For Super-VGA mode, each horizontal line has 800 pixels. After all 800 pixels have been transferred to the CRT, the CRT horizontal display signal, CRT_HDSP, becomes inactive, signaling a horizontal blanking period H_BLNK when pixels are not displayed on the screen. The horizontal blanking period typically lasts for 15% to 30% of the horizontal period. The standard for SVGA is 240 blank pixels.

These CRT pixels are also copied to a LCD path just before being converted to analog voltages by the DAC. Pipeline delays including the delay through the EMI FIFO cause these pixels to be transferred to the LCD panel with a delay relative to the CRT pixels. The LCD pixels are transferred using a modulated clock which sweeps through frequencies less than the nominal pixel or video clock frequency used for CRT pixel transfer. As this frequency changes, the period of the pixels changes. The slower frequency of LCD pixel transfer results in the last LCD pixel being transferred to the LCD display several clock periods after the last CRT pixel was transferred.

If there was no horizontal blanking period, such as when a CRT is not simultaneously displaying the image on the LCD display, then delaying the last pixel could exceed the horizontal period, and the last few pixels would be lost or displayed on the next horizontal line. This loss of pixel data is not acceptable. Fortunately, a relatively large horizontal blanking period is required for a CRT to move its electron beam back to the beginning of a new line. Thus the horizontal blanking period provides ample time to delay the LCD pixels by using a slowed-down modulated video clock.

The LCD timing generator delays the LCD horizontal display signal until the last LCD pixel has been transferred. This can be accomplished by having end detector **46** send a signal to LCD timing generator **40** when the end-of-line code is detected, or by simply programming a larger value for the display time using a programmable register.

LCD panels do not require an extended blanking period, as do CRT's, but smaller front and back porch periods must be met. Large amounts of modulation could delay the last pixel on the horizontal line into the back porch, causing loss

of data. Thus smaller amounts of modulation are desirable. 1% to 2.5% frequency modulation is appropriate.

SPREAD SPECTRUM EMI REDUCTION FOR CRT AND LCD

While today's CRT's have sufficient shielding in their cables to meet EMI requirements, as higher resolutions become standard in the future, faster clock speeds are required to transfer more pixels for each line. These higher clock speeds increase emissions, and thus spread-spectrum techniques are desirable for the CRT interface as well as the LCD panel interface.

The inventors have realized that the CRT's zig-zag and wiggle distortions are caused by two factors:

1. PLL's unable to track modulations in frequency

2. Different horizontal lines have varying pixel timings.

The problems in applying spread spectrum to a graphics controller are not caused by the fact that signals are modulated. Instead the problems arise from secondary effects caused by the modulated clocks, such as variable horizontal timings and interaction with PLL's.

The first factor, interaction with PLL's, can be eliminated by modulating a clock after the PLL, or by integrating the spread-spectrum function within the PLL. Any reference clocks which are input to a PLL should not be modulated, because PLL's require a stable clock.

The second factor is accounted for by ensuring that all horizontal lines have the same timing. Each horizontal line's period must be identical. The relative positions of pixels within each line must be the same as for other lines.

The previously-described embodiment met the first factor by modulating the video clock after it was generated by the PLL. The second factor was met by using the un-modulated video clock to generate the horizontal timing signals. The pixels were transferred to the LCD display using the modulated clock.

The inventors have realized that the second factor can be met even while modulating the video clock to the CRT. If the clock modulation can be synchronized with the horizontal timing, then the problems can be avoided. The frequency sweep for the modulated clock is re-started or reset as part of the horizontal timing of each line.

Sweep Reset By Horizontal Timing—FIG. 10

FIG. **10** is a graph of a modulated clock which resets the frequency sweep as part of the horizontal timing for each horizontal line. At the end of each horizontal line's display period, when the horizontal display HDSP signal goes low (inactive), the frequency sweep is reset. The cycle period of the frequency sweep is equal to the horizontal period. The frequency slowly decrements with each clock cycle or group of clock cycles from the maximum frequency to the minimum frequency. The minimum frequency is reached near the middle of each horizontal line. The sweep then reverses direction and slowly increases with each clock cycle or group of clock cycles from the minimum frequency to the maximum frequency for the second half of the horizontal line.

Since pixels are being transferred to the display as the frequency sweeps down, each pixel has a slightly longer period than the previous pixel. This causes the middle pixel on a line to be wider than the first or last pixels on the line. For a 5% frequency sweep, the middle pixel is 5% wider than the first pixel. This is a small amount of difference, and since the first pixel is not adjacent to the middle pixel, the difference is not noticeable to the viewer. Of course, larger amounts of frequency sweep produce greater differences.

While the prior-art clock modulator chip slowly changed the frequency up and down during the sweep without regard to the horizontal period, this embodiment resets the frequency sweep during each horizontal blanking period. The frequency slowly sweeps to lower frequencies in small decrements during the first half of the display portion of the horizontal line, and then slowly sweeps to higher frequencies in small increments during the second half of the display portion of the horizontal line. The full range of frequencies are swept through during each horizontal line period.

Counters and other logic using the modulated clock are not affected by the shorter clock period as the sweep is reset. Horizontal and vertical timing signals can still be derived from this clock as long as PLL's are not used. Clock dividers to generate horizontal and vertical synchronization and blanking signals can safely use the modulated clock, despite the small frequency changes.

The exact number and range of frequencies that the modulation sweeps through is not important as long as EMI is reduced and the emissions spread out over several frequencies. A 2.5% downward sweep from 40 MHz to 39 MHz rather than the 5% sweep described above may also be used. The drawback to limiting the sweep is that less EMI reduction occurs for shorter lines since the frequency sweeps through a smaller range of frequencies. The sweep rate, or decrement amount, could be changed using a programmable register if this was a concern.

Modulation Frequency Sweep Reset By End of Horizontal Line

FIG. **11** is a diagram of a clock modulator which is reset by the end of the displayable portion of a horizontal line. Clock modulator **82** slowly decreases and then increases the frequency of a clock during a sweep period from a maximum frequency to a minimum frequency and back to the maximum frequency. Clock modulator **82** continues to decrease and then increase the clock's frequency until reset sweep input **86** is asserted. When reset sweep input **86** is asserted, a new frequency sweep cycle begins. The maximum frequency of the output clock VCLK_SS, is equal to the nominal frequency of video clock VCLK input to clock modulator **82**.

The modulated video clock VCLK_SS output from clock modulator **82** is sent to control transfer of CRT and LCD pixels. Horizontal counter **84** also receives this modulated clock, which slowly decreases and then slowly increases in frequency as displayable pixels are transferred to the displays. Horizontal counter **84** is incremented for each pulse of the modulated video clock until the count reaches the total number of pixels in the line, including non-displayable pixels during retrace. The total number of pixels is 1040 pixels for SVGA, including 800 displayable pixels, or 800 pixels for VGA (including 640 displayable), or higher for higher resolutions. The total number varies with the retrace timing. Upon reaching the number of displayable pixels in the line, horizontal counter **84** pulses the horizontal display-enable signal HDSP inactive (high).

After the last displayable pixel has been transferred, horizontal counter **84** drives HDSP high, asserting the signal to sweep reset input **86**. The sweep is reset, causing clock modulator **82** to begin a new frequency sweep, ready for the next horizontal line. This signal may be delayed for a few clock periods, or the resetting of the sweep may be delayed until later in the blanking period.

The sweep decrement and increment may be generated by a sweep counter which slowly increments and decrements a

clock divisor for a PLL in clock modulator **82** to generate the modulated frequency. Alternately horizontal counter **84** may be used as the sweep counter. FIG. **12** shows a clock modulator which uses the horizontal counter as the frequency sweep counter. The numerical count of horizontal counter **84** is also output to clock modulator **82'**. The numerical output is the count value of horizontal counter **84**, which is the pixel number of the current pixel. The pixel number increments from zero or one to the number of pixels in the line for the current resolution. This pixel number is also used to slowly increase the sweep divisor and is input as the sweep count input to clock modulator **82'**. Once the middle count value is reached, the count is used to gradually decrease the sweep divisor and thus raise the frequency. Thus a separate sweep counter is not needed.

GRAPHICS CONTROLLER WITH RESETABLE FREQUENCY SWEEP

FIG. **13** is a diagram of an LCD & CRT graphics controller with clock modulation which is reset at the end of each horizontal line. Many blocks in FIG. **13** were already described in reference to FIG. **7**.

Second clock synthesizer **72** generates an un-modulated video clock, which is immediately input to resetable clock modulator **82'** to generate modulated video clock VCLK_SS. Resetable clock modulator **82'** slowly decrements the frequency while pixels are being written to a first half of a horizontal line, but then slowly increments the frequency while pixels are being written to a second half of the horizontal line. The maximum frequency is reached at the end of a horizontal line during the horizontal blanking portion of the line.

The modulated video clock VCLK_SS is input to the entire CRT path and the LCD path, including CRT buffer **52**, attribute controller **54**, RAM look-up table **56**, and LCD controller **62**. Both shielded CRT cable **59** and panel interface **80** contain frequency-modulated signals, thus reducing the maximum intensity of EMI emissions for both the CRT and the panel interfaces.

The EMI FIFO of FIG. **7** is no longer needed since the CRT and LCD paths use the same modulated clock. The LCD no longer need separate timing signals from the CRT's timing since the LCD pixels are no longer delayed by modulation relative to the CRT pixels. LCD-specific signals such as the line pulse and first line marker still need to be generated.

Pixel Position Fixed Relative to Corresponding Pixels in Other Lines

The horizontal and vertical timings signals for both the CRT and the LCD are both generated from the modulated video clock. No variations occur in either the vertical or horizontal timing signals since the clock modulation are always reset at the end of every horizontal line. Thus while frequency variations occur during a line, variations never occur from one line to another line.

Since the same frequency modulation occurs for every line, all corresponding pixels in different lines have the same timing. Thus the VCLK period which generates the one-hundredth pixel is always the same length of time, even for different lines. Even though the periods of different pixels on a line vary, the periods of corresponding pixels for different lines does not vary. FIG. **14** shows that the VCLK period for successive pixels slowly increases as the frequency decreases as the line is written up to the middle pixel, but the same decrease occurs for each line. Thus line-to-line timings are repeatable. A straight vertical line drawn by the pixels at position **100** appear as a straight line without zig-zags or wiggles, even though the clock is modulated as each line is written. Since the frequency slowly increase back to the maximum frequency during the second half of the line, the last pixel has about the same width as the first pixel, although the middle pixel is wider.

RESETABLE CLOCK GENERATOR

FIG. **15** is a diagram of a modulated clock generator **82'** which uses the horizontal pixel counter to modulate the clock. The un-modulated video clock VCLK is input to counter **102**, which divides VCLK by a numerator N, outputting a pulse to phase comparator **104** after every N cycles of VCLK. Phase comparator **104** outputs a voltage which is proportional to the difference in phase between its inputs. This voltage is filtered by loop filter **106**, which is a simple R-C filter. The voltage from loop filter **106** is buffered by buffer **116**, and modified by voltage divider **120**. The modified voltage is input as the reference voltage to digital-to-analog (D/A) converter **114**. This reference voltage modifies the analog voltage output from D/A converter **114**. The analog voltage from D/A converter **114** is input to voltage summer **122** which sums the analog voltage from D/A converter **114** with the output voltage from loop filter **106**. The summed voltage is applied to the inverting input of unity-gain inverting amplifier **123**. The output from amplifier **123** is then input to voltage-controlled-oscillator (VCO) **108**. VCO **108** generates the modulated video clock VCLK_SS. The frequency of the clock generated by VCO **108** is a function of the input voltage to VCO **108**.

The modulated video clock, VCLK_SS, is used for all pixel-transfer functions, and for generating horizontal and vertical timing as described for FIG. **13**. Horizontal up-down counter **85** receives this modulated video clock VCLK_SS, and counts the number of pixels which have been transferred for the current horizontal line. Horizontal up-down counter **85** divides the modulated video clock VCLK_SS by the total number of pixels in a line, including the non-displayable pixels during the blanking period. Thus for super-VGA, with 800 displayable pixels, the total pixels in each horizontal line is 1040. Horizontal up-down counter **85** first counts up to half the number of pixels in a horizontal line, then counts back down to the end of the line. Thus an up-down rather than an up-only counter is used. Other embodiments are also possible.

The pixel count output from horizontal up-down counter **85** is output as an 8-bit value which is the digital input to D/A converter **114**. This 8-bit digital value is a binary number representing the clock modulation from the nominal frequency. For the first pixel, pixel **0**, the pixel count from horizontal counter is 0, and the 8-bit value is 00 Hex. No modulation adjustment is made, and the frequency output is 40 MHz. Table 1 shows that as the pixels are transferred, the 8-bit value increases until the middle pixel, pixel **520**. Then the 8-bit value decreases as the pixel count increases until the end of the horizontal line. The 8-bit value is converted by D/A converter **114** to an analog voltage which ultimately adjusts the frequency variation generated by VCO **108**.

Horizontal up-down counter **85** can be programmed for different resolutions. Thus while table 1 shows SVGA resolution, with 1040 total pixels (800 displayable pixels), other resolutions are possible such as VGA resolution with 800 total pixels (640 displayable pixels). The middle pixel is actually the middle of the total pixels, rather than the displayable pixels.

TABLE 1

SVGA Sweep		
Pixel Count #	8-bit D/D Output	Frequency
0	00	40 MHz
1	01	39.99 MHz
130	4F	39.5 MHz
260	8F	39 MHz
520	FF	38 MHz
780	8F	39 MHz
1038	01	39.99 MHz
1039	00	40 MHz

Horizontal up-down counter **85** can be used to convert pixel counts for different resolutions to a constant sequence of 8-bit values which control the frequency sweep. Horizontal up-down counter **85** can contain a programmable register with the middle pixel number. Another register is programmed with the step adjustment, which is the maximum 8-bit value of FF Hex, divided by half the number of pixels in a horizontal line for the current resolution. With each increase in pixel count, the 8-bit output is increased by the step adjustment for the first half of the line. A comparator signals when the middle pixel is reached, and the step adjustment is then subtracted with each new pixel count for the second half of the line.

Voltage divider **120** provides voltage steps which produce clock modulation from zero to 10%. Mux **118** applies the amount of modulation voltage to the VREF input of D/A converter **114**. Voltage summer **122** sums the voltage from loop filter **106**, and the desired amount of clock modulation selected by mux **118**. The summed voltage is input to the inverting input of amplifier **123** which modifies the voltage applied to VCO **108**. Thus when higher reference voltages are selected, greater voltage variations are produced as the pixel count increases, and thus more clock modulation is generated.

An alternative is to replace VCLK input to counter **102** with a reference clock such as the 14.318 MHz clock. A stand-alone clock generator for VCLK is then not needed as VCLK_SS is directly generated without the intermediate VCLK.

ADVANTAGES OF THE INVENTION

Spread spectrum techniques reduces the amplitude or intensity of EMI sufficiently that other EMI reduction techniques may be avoided. Adding filters, using metallic cases and shielded cables, and surrounding signals with ground planes and traces all add cost. This added cost can be avoided or reduced with the invention's spread spectrum technique.

Using the un-modulated clock to generate the horizontal timing signals for the flat panel eliminates the problem with brighter and dimmer horizontal lines which occurs then the horizontal signals are generated with a modulated clock, as described in the background section. Thus the panel interface reduces EMI radiation from pixel transfer, while maintaining constant horizontal timing and eliminating dim and bright lines and D.C. buildup of charge caused by variations in how long each horizontal line is displayed.

The EMI FIFO synchronizes the shift clock to the pixels transferred to the LCD flat panel display. Thus set-up time violations do not occur in the panel assembly for pixels written to the panel's shift register.

ALTERNATE EMBODIMENTS

Several other embodiments are contemplated by the inventors. For example other modes of the external clock modulator chip or the internal modulator could be used. Down mode, where the frequencies are swept from the nominal frequency to lower frequencies, was described. A center mode could be used by setting the nominal frequency to be below the nominal video clock frequency, but setting the maximum frequency to be the video clock's nominal frequency. An empty flag could be added to allow the frequency of the read clock to be greater than the nominal frequency of the video clock, rather than delay the FIFO read, or the start of the reading out of the FIFO may be delayed.

The resetable clock modulator is ideally integrated onto the same silicon die as the graphics controller, although other embodiments are possible. When integrating the modulator onto the same die as the graphics controller, the modulator must be protected or isolated from noise generated by the controller. Ground, power, and substrate isolation are useful.

While incrementing a counter for half the number of pixels in a horizontal line has been described, some designers prefer to decrement from half the number of pixels to zero. Decrementing is essentially incrementing by a negative increment rather than a positive increment. Thus incrementing with a negative value accomplishes the equivalent of decrementing.

The frequency sweep was described as being reset during the horizontal blanking period, but the sweep reset could occur at any time during the horizontal period, as long as the sweep is reset at the same point for each line. Thus the sweep could be reset at an arbitrary location, such as at pixel 219 of each line. The sweep could be reset more than once for each line, allowing the sweep to occur several times for each horizontal line. Each reset could simply reverse the direction of the frequency increments, such that the sweep is "reset" at the middle of the line as well as at the end of the line. Thus an even number of direction-reversing "resets" are needed.

The frequency sweep could even be rapidly reset during the blanking period. While the prior-art clock modulator chip slowly changed the frequency up or down during the sweep, this embodiment rapidly changes the frequency during the horizontal blanking period. The frequency slowly sweeps to lower frequencies in small decrements during the display portion of the horizontal line, but then quickly changes from the minimum frequency to the maximum frequency during the horizontal blanking portion. This rapid frequency change would be devastating to any PLL's receiving the modulated clock, and thus such an abrupt frequency change is a surprising departure from prior-art teachings on clock modulation.

Power-down modes are commonly used with flat-panel displays and the graphics adapter can be modified to enable the clock generation circuitry before power is restored to the display when resuming operation after a suspend mode. The sweep generator may require additional time to stabilize before operation can resume. The clocks can be powered-up in a sequence to allow PLL's to stabilize before the clock is used.

The inventors also contemplate having the type or make of panel assembly encoded into some of the signal lines in the panel interface. The graphics BIOS or boot code can read the encoding on these signal lines to determine which panel is connected to the graphics controller. Knowing the type of panel can allow the BIOS to decide how much EMI reduction can be applied for that particular panel.

The foregoing description of the embodiments of the invention has been presented for the purposes of illustration

and description. It is not intended to be exhaustive or to limit the invention to the precise form disclosed. Many modifications and variations are possible in light of the above teaching. It is intended that the scope of the invention be limited not by this detailed description, but rather by the claims appended hereto.

We claim:

1. A graphics controller for reducing electromagnetic interference (EMI) comprising:

a pixel-transfer path, including buffering means for buffering pixels from a video memory and pixel processing means for processing pixels, the pixel-transfer path having a pixel output;

a flat-panel converter, receiving pixels from the pixel output of the pixel-transfer path, for converting pixels to a format for transfer to a flat-panel display, the flat-panel converter having a panel-interface output coupled to the flat-panel display;

video clock means for supplying a video clock for synchronizing transfer of pixels, the video clock having a constant frequency, the video clock coupled to the pixel-transfer path;

a timing generator, coupled to receive the video clock, for generating horizontal and vertical timing signals for synchronizing display of horizontal lines of pixels, the horizontal and vertical timing signals coupled to the flat-panel display;

modulated video clock means for supplying a frequency-modulated video clock to the flat-panel converter, the flat-panel converter transferring pixels out the panel-interface output to the flat-panel display at a modulated rate proportional to a current frequency of the frequency-modulated video clock;

a digital-to-analog converter (DAC), coupled to receive pixels from the pixel output of the pixel-transfer path, for converting pixels to analog voltages for driving a cathode-ray-tube (CRT) display, the DAC converting pixels to the analog voltages a constant rate proportional to the video clock, and

a FIFO, coupled between the pixel output and the flat-panel converter, for receiving pixels from the pixel-transfer path in response to a pulse of the video clock, and for outputting pixels to the flat-panel converter in response to a pulse of the frequency-modulated video clock,

whereby pixels are transferred to the flat-panel display using the frequency-modulated video clock, reducing EMI, but the horizontal and vertical timing signals are generated by the video clock without modulation and whereby pixels are transferred to the CRT at the constant rate while pixels are transferred to the flat-panel display at the modulated rate and whereby pixels synchronized to the video clock are buffered by the FIFO to be synchronized to the frequency-modulated video clock, the frequency-modulated video clock being asynchronous to the video clock.

2. The graphics controller of claim 1 wherein the CRT is driven with pixels to display a same image being displayed on the flat-panel display.

3. The graphics controller of claim 1 wherein the frequency-modulated video clock sweeps through frequencies less than and equal to the constant frequency of the video clock,

whereby pixels are outputted from the FIFO more slowly than pixels are received into the FIFO.

4. The graphics controller of claim 3 further comprising:

reset means for resetting the FIFO after a last displayable pixel is outputted in a horizontal line of pixels,

whereby the FIFO is reset after each horizontal line of pixels.

5. The graphics controller of claim 1 further comprising:

a clock modulator, receiving the video clock, for modulating the constant frequency of the video clock to the current frequency to generate the frequency-modulated video clock; and

coupling means for coupling the frequency-modulated video clock to the modulated video clock means.

whereby the frequency-modulated video clock is generated by modulating the current frequency of the video clock.

6. The graphics controller of claim 5 wherein the clock modulator sweeps the current frequency in small increments between a maximum frequency and a minimum frequency,

whereby the current frequency is gradually changed.

7. The graphics controller of claim 1 wherein the flat-panel display receives converted pixels from the panel-interface output of the flat-panel converter through a panel interface, the panel interface passing through a hinge connecting a base unit of a portable computer, the base unit having a keyboard, the hinge connecting the base unit to the flat-panel display, the hinge for closing the flat-panel display over the keyboard.

* * * * *

EXHIBIT 29
(USP 5,659,587)

US005659587A

United States Patent [19]

Knierim

[11] Patent Number: 5,659,587

[45] Date of Patent: Aug. 19, 1997

[54] **SPREAD SPECTRUM PHASE-LOCKED LOOP CLOCK GENERATOR WITH VCO DRIVEN BY A SYMMETRICAL VOLTAGE RAMP SIGNAL**

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[73] Assignee: **Tektronix, Inc.**, Wilsonville, Oreg.

[21] Appl. No.: **344,267**

[22] Filed: **Nov. 23, 1994**

[51] **Int. Cl.**[6] **H03D 3/24**; H04B 15/00

[52] **U.S. Cl.** **375/376**; 375/200; 375/204; 380/34

[58] **Field of Search** 375/376, 204, 375/373, 371, 340, 322–327; 380/48, 34; 329/345, 346, 360; 331/10, 17

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Primary Examiner—Wellington Chin

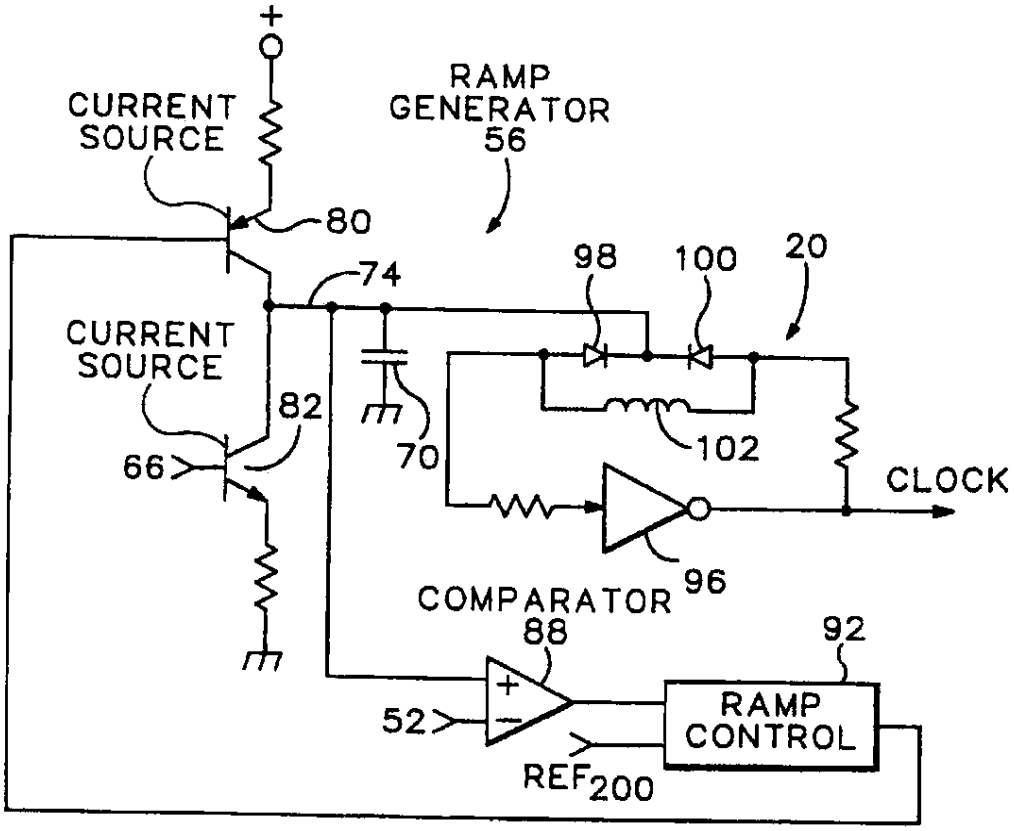
Assistant Examiner—William Luther

Attorney, Agent, or Firm—Ralph D'Alessandro; John Smith-Hill

[57] **ABSTRACT**

A phase-locked loop circuit comprises a VCO and a ramp generator. The ramp generator has an output connected to a control terminal of the VCO. A center frequency control loop is connected between a signal output terminal of the VCO and a first ramp control input of the ramp generator and a spread spectrum control loop is connected between the signal output terminal of the VCO and a second ramp control input of the ramp generator. The signals applied to the ramp control inputs of the ramp generator by the two control loops control respective characteristics of a periodic voltage ramp signal that is generated by the ramp generator at its signal output terminal.

28 Claims, 2 Drawing Sheets



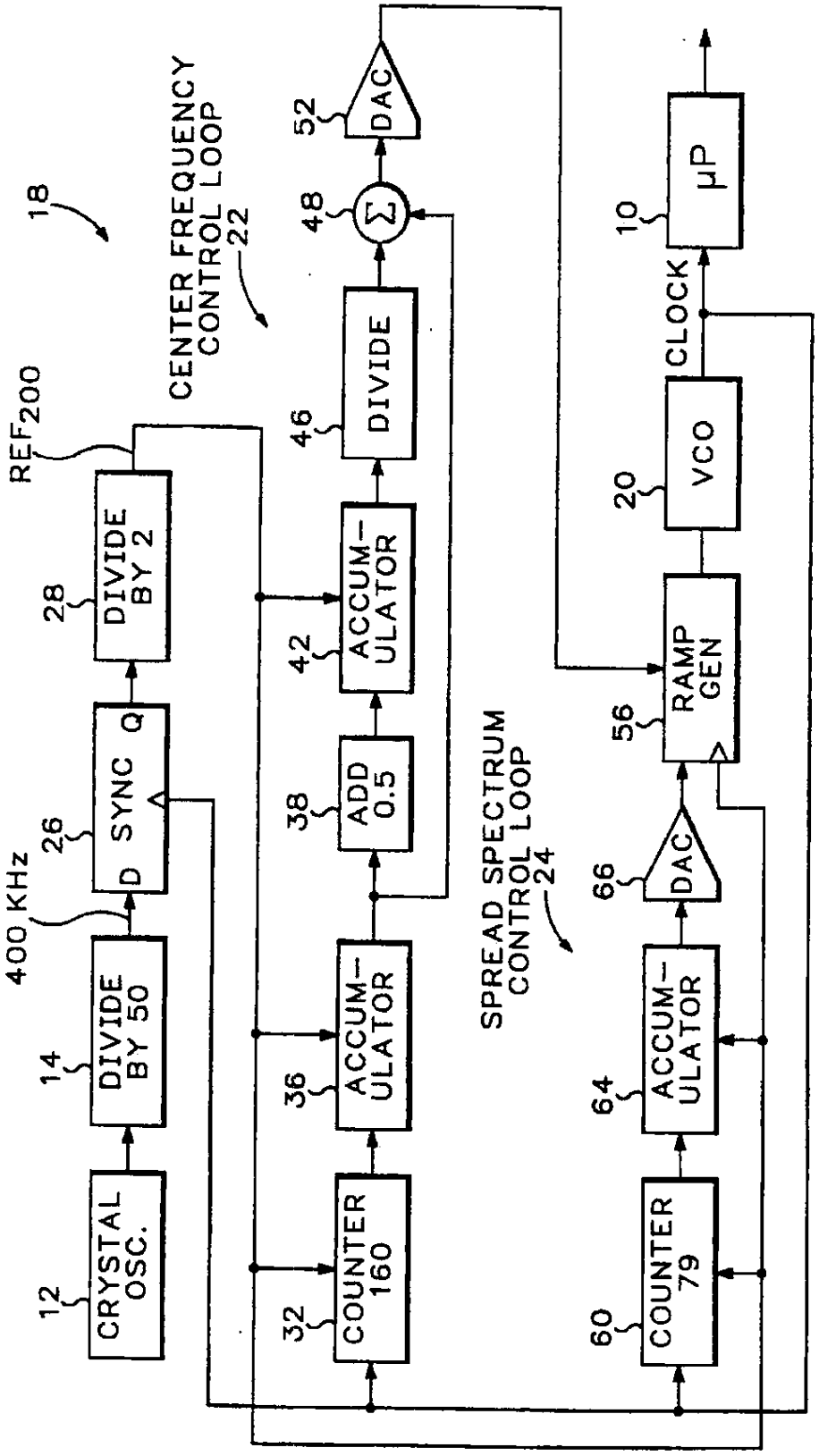

18
CENTER FREQUENCY CONTROL LOOP
22
REF 200
28
DIVIDE BY 2
26
D SYNC Q
400 KHz
14
DIVIDE BY 50
12
CRYSTAL OSC.
42
ACCUM-ULATOR
38
ADD 0.5
36
ACCUM-ULATOR
32
COUNTER 160
46
DIVIDE
48
Σ
52
DAC
SPREAD SPECTRUM CONTROL LOOP
24
56
RAMP GEN
66
DAC
64
ACCUM-ULATOR
60
COUNTER 79
20
VCO
CLOCK
10
μP

FIG.1

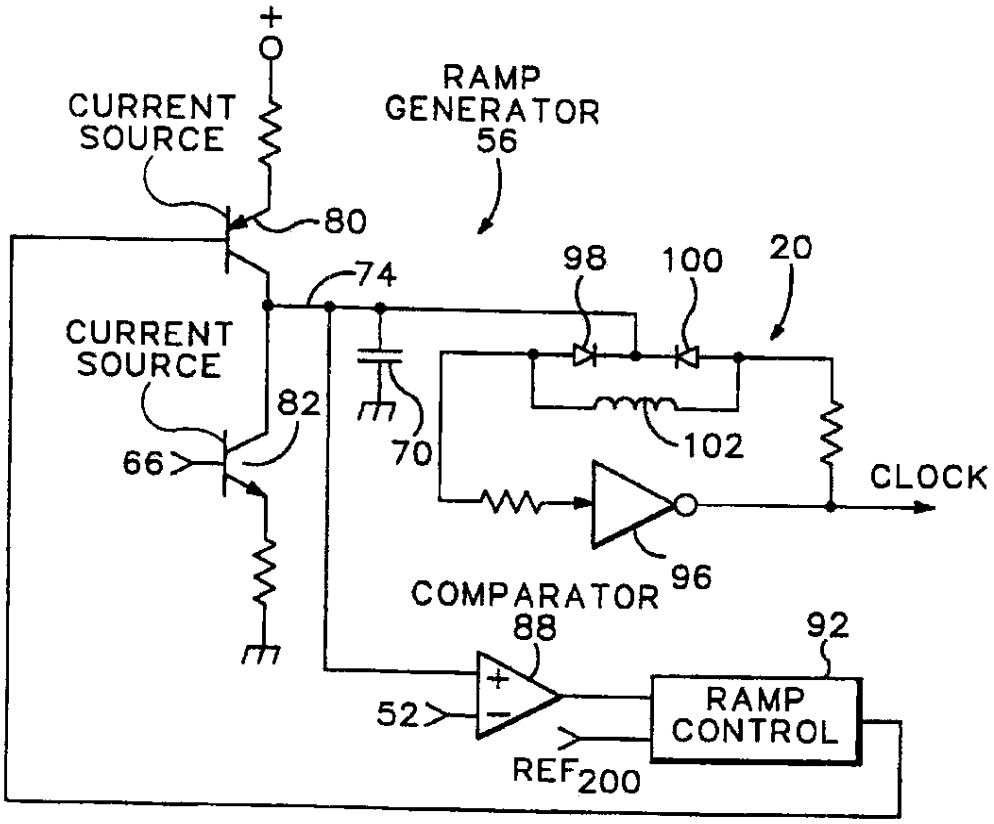

+
CURRENT SOURCE
RAMP GENERATOR 56
80
74
98
100
20
CURRENT SOURCE
82
66
70
102
CLOCK
96
COMPARATOR
88
92
52
RAMP CONTROL
REF200

FIG.2

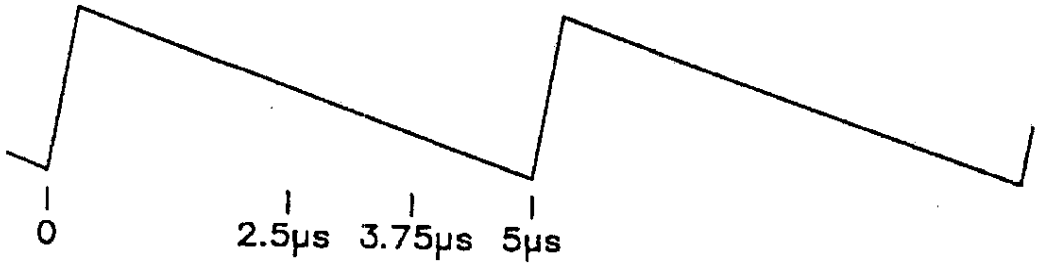

0
2.5μs
3.75μs
5μs

FIG.3

SPREAD SPECTRUM PHASE-LOCKED LOOP CLOCK GENERATOR WITH VCO DRIVEN BY A SYMMETRICAL VOLTAGE RAMP SIGNAL

BACKGROUND OF THE INVENTION

This invention relates to a spread spectrum phase-locked loop clock generator.

Timing control of many electronic devices, such as microprocessors, is provided by a clock signal. Typically, the clock signal has a frequency of several megahertz. The waveform of the clock signal is approximately trapezoidal in form, and the clock signal normally has energy at its fundamental frequency and at each integer multiple of the fundamental frequency.

The clock signal may be generated by a crystal oscillator. The crystal oscillator has the advantage that its oscillation frequency is stable, so that it is relatively easy to guard against the possibility that drift will result in the fundamental frequency of the clock signal exceeding the clock frequency rating of the microprocessor and leading to a malfunction of the microprocessor.

The crystal oscillator has a very high Q value, which results in the energy of the clock signal being concentrated in a narrow fundamental frequency band and harmonics of that band. The concentration of energy at the high frequencies of the harmonics of the clock frequency can lead to emission of electromagnetic interference (EMI) in excess of that permitted under applicable government regulations.

It is known to reduce the level of electromagnetic interference resulting from a microprocessor clock signal by varying the frequency of the clock signal, so that the energy is not concentrated in a narrow fundamental frequency band and the harmonics of that band. For example, the IMISG501 system clock chip sold by International Microcircuits, Inc. of Milpitas, Calif. employs intentional broadbanding to reduce electromagnetic interference.

On first consideration, it might appear attractive to vary the frequency of the clock signal in accordance with a symmetrical triangular waveform composed of two ramps of equal but opposite slope. However, on closer examination, it becomes apparent that this does not provide the optimum solution because at the positive and negative turning points of the waveform there is a region over which the clock frequency varies only slightly. This results in excessive EMI at the two extremes of the range through which the frequency is varied.

SUMMARY OF THE INVENTION

According to a first aspect of the present invention there is provided a phase-locked loop circuit comprising a VCO having a control terminal and a signal output terminal, a ramp generator having an output connected to the control terminal of the VCO and also having first and second ramp control inputs for receiving first and second control signals upon which first and second characteristics of a periodic voltage ramp signal generated by the ramp generator at its signal output terminal respectively depend, and a reset input for receiving a periodic reset signal, a center frequency control loop connected between the signal output terminal of the VCO and the first ramp control input of the ramp generator, and a spread spectrum control loop connected between the signal output terminal of the VCO and the second ramp control input of the ramp generator.

According to a second aspect of the present invention there is provided a spread spectrum clock generator, comprising a VCO having a control terminal and an output terminal, and a ramp generator for generating a periodic voltage ramp signal and applying the periodic voltage ramp signal to the control terminal of the VCO, the periodic voltage ramp signal having a rising segment and a falling segment and the magnitude of the slope of one of the segments being much greater than the magnitude of the slope of the other segment.

According to a third aspect of the present invention there is provided electronic apparatus comprising a timed device that is responsive to input signals to change state on occurrence of a clocking transition at a clock input of the timed device, and a clock generator that generates a clock signal having a succession of clocking transitions at a clock output connected to the clock input of the timed device, and wherein the frequency of the clock signal varies periodically in accordance with a ramp function, each period of the ramp function being composed of a first segment, during which the frequency of the clock signal changes at a first rate, and a second segment, during which the frequency of the clock signal changes at a second rate, the first and second rates being of opposite polarity and the magnitude of the first rate being much greater than the magnitude of the second rate.

According to a fourth aspect of the present invention there is provided a method of operating electronic apparatus that comprises a timed device responsive to input signals to change state on occurrence of a clocking transition at a clock input of the timed device, said method comprising applying a periodic clock signal having a succession of clocking transitions to the clock input of the timed device, and varying the period of the clock signal periodically in accordance with a ramp function, each period of the ramp function being composed of a first segment, during which the period of the clock signal changes at a first rate, and a second segment, during which the period of the clock signal changes at a second rate, the first and second rates being of opposite polarity and the magnitude of the first rate being much greater than the magnitude of the second rate.

BRIEF DESCRIPTION OF THE DRAWINGS

For a better understanding of the invention, and to show how the same may be carried into effect, reference will now be made, by way of example, to the accompanying drawings, in which

FIG. 1 is a block diagram of a spread spectrum clock generator in accordance with the present invention,

FIG. 2 is a partial schematic diagram illustrating part of the clock generator, and

FIG. 3 is a graph illustrating operation of the clock generator.

DETAILED DESCRIPTION

The clock generator illustrated in FIG. 1 is used to generate a clock signal that controls the timing of the operation of a microprocessor **10** having a rated clock frequency of 33.3 MHz. The clock generator comprises a crystal oscillator **12** that generates an output signal at a frequency of 20 MHz and a divider **14** that divides the frequency of the oscillator output signal to 400 kHz. The 400 kHz signal is applied as an external reference to a phase-locked loop circuit **18**, which includes a voltage-controlled oscillator (VCO) **20** and two control loops **22** and **24**. The VCO provides a VCO clock signal at a nominal frequency of 32 MHz to the microprocessor **10**. It will be seen in due course that through operation of the control loops **22** and **24**,

the frequency of the VCO clock signal varies between 31.2 MHz and 32.8 MHz.

The phase-locked loop circuit **18** comprises a synchronizer **26**, whereby the output signal of the divider **14** is synchronized with the VCO clock signal. The synchronizer may comprise a D flip-flop that receives the 400 kHz external reference signal at its D input and the VCO clock signal at its clock input. The Q output of the flip-flop is at the same frequency as the external reference signal but its edges are synchronized to the positive going edges of the VCO clock signal, subject to the delay in the D flip-flop. It is preferred that the synchronizer should contain a second D flip-flop, with its D input connected to the Q output of the first flip-flop and its clock input receiving the VCO clock signal, so as to avoid metastable states in the synchronized reference signal.

The synchronized reference signal is divided by two by a divider **28**, providing a 200 kHz signal REF_{200} in which the falling edges occur halfway between the rising edges, within +/−1 VCO clock. This low frequency reference signal, having a period of 5 μs, is used to control operation of the two control loops **22** and **24**.

The center frequency control loop **22** comprises a counter **32** that counts positive going edges of the VCO clock signal. The first rising edge of the VCO clock signal following the positive going edge of the low frequency reference signal REF_{200} captures the count stored in the counter **32** into a phase error accumulator **36** and also loads the value −159 into the counter **32**. Each subsequent rising edge of the VCO clock signal increments the count stored in the counter by 1. Thus, if 160 VCO clock edges occur between REF_{200} positive going edges, the counter **32** contains the count **0** at the end of its counting period. In general, the count stored in the counter **32** at the end of its counting period is equal to the difference between 160 and the number of consecutive cycles of the VCO clock signal that occurred within the counting period and is proportional to the difference between 32 MHz and the mean frequency of the VCO clock signal over the counting period.

The phase error accumulator **36** adds the count provided by the counter **32** in response to the positive going edge of the signal REF_{200} to the previously accumulated value. The value stored in the phase error accumulator **36** represents phase error of the VCO clock signal. The maximum value that can be stored in the phase error accumulator **36** is limited to prevent overflow.

The value stored in the phase error accumulator **36** is applied to an adder **38**, whereby the phase error is incremented by one-half, and the sum is accumulated into a phase accumulator **42**, which again is updated in response to each positive going edge of the signal REF_{200}. The accumulated value is scaled by a divider **46** and the scaled value is applied to one input of a summation circuit **48**. The output of the phase error accumulator **36** is also applied directly to a second input of the summation circuit **48**, which provides a weighted sum of the outputs of the accumulators **36** and **42** as input to a digital-to-analog converter (DAC) **52**. The DAC **52** is implemented using sigma delta modulation, which provides a digital value that is fed into an accumulator (not shown). The carry output of the accumulator is passed through a single pole low pass filter to provide an analog output signal, which is applied to a peak voltage control input of a ramp generator **56**.

The spread spectrum control loop **24** comprises a counter **60** that counts positive going edges of the VCO clock signal. The first rising edge of the VCO clock signal following the positive going edge of the low frequency reference signal REF_{200} captures the count stored in the counter **60** into a spread spectrum accumulator **64**. The first rising edge of the VCO clock signal following the negative going edge of the signal REF_{200} loads the value −78 into the counter **60**. Each subsequent rising edge of the VCO clock signal increments the count stored in the counter by 1. Thus, the counting period of the counter is the second half of the period of the signal REF_{200}. If 79 VCO clock edges occur before the positive going edge of the signal REF_{200}, the counter **60** contains the count **0** at the end of its counting period. In general, the count stored in the counter **60** at the end of its counting period is equal to the difference between 79 and the number of consecutive cycles of the VCO clock signal that occurred within the counting period and is proportional to the difference between 31.6 MHz and the average frequency of the VCO clock signal during the counting period.

The accumulator **64** adds the count provided by the counter **60** in response to the positive going edge of the signal REF_{200} to the previously accumulated value. The maximum value that can be stored in the accumulator **64** is limited to prevent overflow. The value stored in the accumulator is applied as input to a DAC **66**. The DAC **66** is implemented in similar fashion to the DAC **52**, and the analog output of the DAC **66** is applied to a slew rate control input of the ramp generator **56**.

As shown in FIG. **2**, the ramp generator comprises a capacitor **70** connected between a node **74** and ground, a charging current source transistor **80**, and a discharging current source transistor **82**. The node **74** is connected to the non-inverting input of a comparator **88**. The output of the DAC **52** is connected to the inverting input of the comparator **88**.

The charging current source transistor **80** is responsive to a ramp control circuit **92**, whereas the discharging current source transistor **82** is responsive to the output of the DAC **66**. The ramp control circuit causes the transistor **80** to turn on in response to a rising edge of the signal REF_{200} or when the count in the counter **32** reaches −4, whichever occurs earlier, and to turn off when the voltage at the node **74** exceeds the output voltage of the DAC **52**, as sensed by the comparator **88**.

The VCO **20** comprises an inverter **96** and a feedback loop that includes two variable capacitance diodes **98** and **100** having their cathodes connected to the node **74** and their anodes connected to the input and output respectively of the inverter. An inductor **102** is connected in parallel with the diodes **98** and **100**. The oscillation frequency of the VCO depends on the reactance of the parallel combination of the inducter **102** and the diodes **98**, **100**, which varies in accordance with the voltage to which the capacitor **70** is charged.

In operation of the ramp generator, assuming that the voltage at the node **74** is less than the output voltage of the DAC **52** and the transistor **80** is off, the transistor **82** supplies current to discharge the capacitor **70** at a relatively slow rate, depending upon the output voltage of the DAC **66**. Thus, the voltage at the node **74** declines fairly slowly, and the oscillation frequency of the VCO **20** similarly declines. The voltage at the node **74** continues to decline until a rising edge of the signal REF_{200} occurs. The ramp control circuit **92** then turns on the transistor **80**, which supplies a much larger current than the transistor **82** and rapidly charges the capacitor **70**. The voltage at the node **74** increases rapidly, and when it reaches the output voltage of the DAC **52**, the output of the comparator **88** changes state and the ramp control

circuit turns the transistor **80** off, allowing the transistor **82** to discharge the capacitor **70** once more. The ramp generator **56** therefore generates a periodic voltage ramp signal at the node **74** and consequently the oscillation frequency of the VCO **20** varies in accordance with the asymmetrical sawtooth function shown in FIG. 3. In a practical implementation of the invention, the duration of the rising segment of the ramp signal is about 5 percent of the period of the ramp signal (8 VCO clocks). Since the magnitude of the slew rate over one segment of the ramp signal is much greater than the magnitude of the slew rate over the other segment of the ramp signal, the frequency of the VCO clock signal does not remain in any range for a substantial period of time. Consequently, the EMI emission due to the clock signal is at a much lower level than if the ramp were symmetrical.

The center frequency loop **22** controls the peak voltage at which the comparator **88** switches to end the charging of the capacitor **70**, whereas the spread spectrum loop **24** controls the current supplied by the transistor **82** and therefore the slope of the falling segment of the ramp signal.

The center frequency control loop **22** forces an average phase error of zero. Because the phase-locked loop is digital, and therefore the measured phase error is always an integer number of clock periods, the instantaneous measured phase error will jitter between +0.5 VCO clocks and −0.5 VCO clocks. The scaling of the zero phase error contribution to the summation circuit **48** depends on the loop response: the frequency corresponding to the time taken for the loop to respond to an error in the VCO clock signal and force it back to its proper value. The loop response must be lower than the reference frequency (200 kHz) and is set at about 10 kHz. The actual phase error will jitter somewhat less than +/−0.5 clocks. The amount of the actual phase jitter is just enough for each 160th VCO clock edge to fall on either side of the rising edge of the signal REF_{200} at the end of successive ramp periods. As the phase jitter decreases, the effective gain of quantizing the phase error to +/−0.5 clocks increases. Thus, a phase error of +0.05 clocks has the same effect on the output of the DAC **52** as a phase error of +0.45 clocks. At some point, this increase in gain makes the loop unstable and the jitter increases, reducing the effective gain. The jitter will thus remain at the amplitude resulting in an effective gain that is on the verge of instability. Adding the phase error to the phase accumulation using the summation circuit **48** provides lead compensation. Addition of the value 0.5 by the adder **38** ensures that the amount of time for which the phase error is positive is equal to the amount of time for which the phase error is negative.

The spread spectrum loop **24** forces the slew rate during the declining portion of the ramp to a value such that there will be 79 VCO clock pulses in the second half of each 5 μs period of the ramp signal. This corresponds to an average frequency over the second half of the ramp equal to 31.6 MHz. Since the center frequency loop forces the average frequency to 32 MHz, this implies that during the ramp period, the clock frequency varies from 32.8 MHz to 31.2 MHz if the rising edge of the signal REF_{200} occurs 4 VCO clocks before the center of the rising segment of the ramp. If the rising edge of the signal REF_{200} is not precisely 4 VCO clocks before the center of the rising segment of the ramp, the clock frequency range will be somewhat different from that indicated above.

Whereas the center frequency loop keeps every 160th VCO clock edge jittering across the rising edge of the reference signal REF_{200}, the spread spectrum loop causes the 81st clock edge of each 160 clock edges to jitter across the falling edge of the reference signal. If the spread is slightly small, so that there are 79.1 VCO clocks in the second half of a ramp period, and the center frequency loop phase error is more than 0.1 clocks, the spread spectrum loop will count 79 clocks and not adjust the spread. But the center frequency loop forces the actual phase error to jitter around zero, and before long there will be a ramp period where the center frequency phase error is less than 0.1 clocks. At this point, the spread spectrum loop will count 80 clocks instead of 79 and increase the spread slightly.

If a circuit perturbation causes a reduction in the center frequency of the VCO, the frequency measured by the spread spectrum loop decreases. The spread spectrum loop responds by reducing the spread, and reducing the spread with a given peak frequency increases the average frequency. This helps satisfy the center frequency loop, which requires that the center frequency be increased to compensate for the reduction. Thus, the action of the spread spectrum loop helps stabilize the center frequency loop rather than tending to destabilize it, as would be the case if the spread spectrum loop monitored the frequency during the first half of the negative slope portion of the ramp signal.

By controlling the average frequency and spread so that the maximum frequency is 32.8 MHz, a frequency margin of 0.5 MHz is provided between the maximum clock frequency and the rated clock frequency for the processor **10**. This margin is sufficient to ensure that under normal circumstances the VCO clock frequency will never exceed the rated clock frequency of the processor, causing possible improper operation.

It will be appreciated that the invention is not restricted to the particular embodiment that has been described, and that variations may be made therein without departing from the scope of the invention as defined in the appended claims and equivalents thereof. For example, if the center frequency loop directly controlled the average frequency instead of the peak frequency, there would be no interaction between the center frequency loop and the spread spectrum loop, and the spread spectrum loop could then monitor the number of VCO clock edges in any segment of the ramp whose center was spaced from the center of the ramp, without there being any tendency for the action of one loop to destabilize the other loop. Also, if the difference between the number of clock edges counted by the spread spectrum counter during its portion of the ramp and the average number of clock edges that occur during an interval of that duration were greater, the effect of the correction provided by the spread spectrum loop would be greater, and there would be no need for the zero phase error branch of the center frequency loop. This could by accomplished by operating the VCO at a higher frequency and, if necessary, dividing the VCO output signal to provide the microprocessor clock signal, employing a lower frequency reference signal, so that the period of the ramp signal is longer, or increasing the frequency spread.

I claim:

1. A phase-locked loop circuit comprising:

a VCO having a control terminal and a signal output terminal,

a voltage ramp generator having an output connected to the control terminal of the VCO and also having first and second ramp control inputs for receiving first and second control signals, and a reset input for receiving a periodic reset signal, whereby the voltage ramp generator generates a periodic voltage ramp signal at its output, the voltage ramp signal having a mean magnitude and a peak-to-peak amplitude that depend on said control signals, and the VCO generates an oscillatory

output signal of a frequency that depends on voltage of said periodic voltage ramp signal,

a first control loop connected between the signal output terminal of the VCO and the first ramp control input of the voltage ramp generator, said first control loop generating said first control signal responsive to a first parameter of the VCO output signal, and

a second control loop connected between the signal output terminal of the VCO and the second ramp control input of the voltage ramp generator, said second control loop generating said second control signal dependent on a second parameter of the VCO output signal.

2. A circuit according to claim 1, wherein the peak-to-peak amplitude of the voltage ramp signal is defined between a positive peak voltage and a negative peak voltage and one of said peak voltages depends on said first control signal, and the first control loop comprises a means for measuring phase difference between the VCO output signal and a reference waveform of a predetermined nominal frequency, a means for offsetting the phase difference by a quantity less than one, and a means for integrating the offset phase difference.

3. A circuit according to claim 2, wherein the means for measuring phase difference between the VCO output signal and the reference waveform comprises a means for measuring difference between average frequency of the VCO output signal and said predetermined nominal frequency, and a means for integrating the frequency difference.

4. A circuit according to claim 1, wherein the peak-to-peak amplitude of the voltage ramp signal is defined between a positive peak voltage and a negative peak voltage and one of said peak voltages depends on said first control signal, and the voltage ramp signal has a slew rate that depends on said second control signal.

5. A circuit according to claim 4, wherein the first control loop comprises a means for adjusting the positive peak voltage to achieve a predetermined average frequency and the second control loop comprises a means for adjusting the slew rate to achieve a predetermined frequency spread.

6. A circuit according to claim 4, wherein said first and second ramp control inputs are a positive peak voltage control input and a slew rage control input and the first control loop is connected to the peak voltage control input and the second control loop is connected to the slew rate control input.

7. A circuit according to claim 6, wherein the first control loop comprises a means for monitoring average frequency of the VCO output signal and the second control loop comprises a means for monitoring frequency of the VCO output signal during a portion of the period of the ramp signal.

8. A circuit according to claim 1, wherein the ramp generator comprises a means for controlling the periodic voltage ramp signal so that each period is composed of a first segment, during which the ramp signal has a first slew rate, and a second segment, during which the ramp signal has a second slew rate, the first and second slew rates being of opposite polarity and the magnitude of the first slew rate being much greater than the magnitude of the second slew rate.

9. A spread spectrum clock generator, comprising:

a VCO having a control terminal and an output terminal, and

a ramp generator for generating a periodic voltage ramp signal and applying the periodic voltage ramp signal to the control terminal of the VCO, periodic voltage ramp signal having a rising segment and A falling segment and the magnitude of slope of one of the segments being much greater than magnitude of the slope of the other segment.

10. A spread spectrum clock generator, comprising:

a VCO having a control terminal and an output terminal, and

a ramp generator for generating a periodic voltage ramp signal and applying the periodic voltage ramp signal to the control terminal of the VCO, the periodic voltage ramp signal having a rising segment and a falling segment and magnitude of slope of one of the segments being much greater than magnitude of slope of the other segment, and wherein the ramp generator comprises a capacitor, a first current source for charging the capacitor at a first rate, a second current source for discharging the capacitor at a second rate, responsive to a slew rate control signal, and a ramp control means for selectively turning one of the current sources on and off.

11. A clock generator according to claim 10, wherein the ramp control means comprises a means for turning the first current source on in response to a periodic reference signal and turning the first current source off when ramp magnitude reaches a level that depends on a first operating condition of the VCO, and a means for controlling the second current source to supply a constant current at a level that depends on a second operating condition of the VCO.

12. Electronic apparatus comprising:

a timed device that is responsive to input signals to change state on occurrence of a clocking transition at a clock input of the timed device, and

a clock generator that generates a clock signal having a succession of clocking transitions at a clock output connected to the clock input of the timed device, and wherein frequency of the clock signal varies periodically in accordance with a ramp function, each period of the ramp function being composed of a first segment, during which the period of the clock signal changes at a first rate, and a second segment, during which the period of the clock signal changes at a second rate, the first and second rates being of opposite polarity and magnitude of the first rate being much greater than magnitude of the second rate.

13. Apparatus according to claim 12, wherein the clock generator comprises a phase-locked loop circuit that synchronizes the ramp function to a periodic reference signal.

14. A method of operating electronic apparatus that comprises a timed device responsive to input signals to change state on occurrence of a clocking transition at a clock input of the timed device, said method comprising applying a periodic clock signal having a succession of clocking transitions to the clock-input of the timed device, and varying the period of clock signal periodically in accordance with a ramp function, each period of the ramp function being composed of a first segment, during which the period of the clock signal changes at a first rate, and a second segment, during which the period of the clock signal changes at a second rate, the first and second rates being of opposite polarity and magnitude of the first rate being much greater than magnitude of the second rate.

15. Electronic apparatus comprising:

a timed device that is responsive to input signals to change state on occurrence of a clocking transition at a clock input of the timed device, and

a clock generator that generates a clock sisal having a succession of clocking transitions at a dock output connected to the clock input of the timed device, and

wherein frequency of the clock signal varies periodically in accordance with a ramp function, each period of the ramp function being composed of a first segment, during which period of the clock signal changes at a first rate, and a second segment, during which period of the clock signal changes at a second rate, the first and second rates being of opposite polarity and magnitude of the first rate being much greater than magnitude of the second rate, and wherein the clock generator comprises:

a VCO having a control terminal and a signal output terminal, said signal output terminal being connected to the clock output of the of the clock generator,

a voltage ramp generator having an output connected to the control terminal of the VCO and also having first and second ramp control inputs for receiving first and second control signals, and a reset input for receiving a periodic reset signal, whereby the voltage ramp generator generates a periodic voltage ramp signal at its output, the voltage ramp signal having a mean magnitude and a peak-to-peak amplitude that depend on said control signals, and the VCO generates said dock signal at a frequency that depends on voltage of said periodic voltage ramp signal,

a first control loop connected between the signal output terminal of the VCO and the first ramp control input of the voltage ramp generator, said first control loop generating said first control signal responsive to a first parameter of the VCO output signal, and

a second control loop connected between the signal output terminal of the VCO and the second ramp control input of the voltage ramp generator, said second control loop generating said second control signal dependent on a second parameter of the VCO output signal.

16. Apparatus according to claim 15, wherein the first and second control loops include respective counters for counting transitions of the VCO output signal and generating the first and second ramp control signals in digital form.

17. Apparatus according to claim 16, wherein the counter in the first control loop counts transitions of the VCO output signal during a period of the periodic reset signal.

18. Apparatus according to claim 16, wherein the counter in the second control loop counts transitions of the VCO output signal during an interval that is within the second segment of the period of the ramp function and of which center is offset in time from center of the second segment of the period of the ramp function.

19. A circuit according to claim 1, wherein the voltage ramp generator comprises a capacitor, a first current source for charging the capacitor at a first rate, and a second current source for discharging the capacitor at a second rate, and wherein at least one of said current sources is responsive to a slew rate control signal.

20. A circuit according to claim 1, wherein the voltage ramp generator comprises a capacitor, a first current source for charging the capacitor at a first rate, and a second current source for discharging the capacitor at a second rate, and wherein one of said current sources is responsive to a slew rate control signal and the circuit further comprises a ramp control means for selectively turning the other current source on and off.

21. A circuit according to claim 20, wherein said ramp control means comprises a means for turning the first current source on in response to a periodic reference signal and turning the first current source off when ramp magnitude reaches a level that depends on a first operating condition of the VCO, and a means for controlling the second current source to supply a constant current at a level that depends on a second operating condition of the VCO.

22. A circuit according to claim 1, wherein the first ramp control input of the voltage ramp generator is a slew rate input and the second ramp control input thereof is a peak magnitude input, and the voltage ramp generator generates a periodic voltage ramp signal such that each period is composed of a first segment, during which the ramp signal has a first slew rate that depends on the first ramp control input and attains a voltage level that depends on the second ramp control input, and a second segment, during which the ramp signal has a second slew rate, the first and second slew rates being of opposite polarity.

23. A circuit according to claim 1, wherein said first and second parameters of the VCO output signal each depend on phase of the VCO output signal.

24. A circuit according to claim 1, wherein said first parameter depends on phase of the VCO output signal at a predetermined point in the period of the periodic reset signal.

25. A circuit according to claim 1, wherein said second parameter depends on phase of the VCO output signal at a first point in the period of the periodic reset signal and phase of the VCO output signal at a second point in the the period of the periodic reset signal.

26. A circuit according to claim 1, wherein the first and second control loops include respective counters for counting transitions of the VCO output signal and generating the first and second ramp control signals in digital form.

27. A circuit according to claim 26, wherein the counter in the first control loop counts transitions of the VCO output signal during a period of the periodic reset signal.

28. A circuit according to claim 26, wherein the counter in the second control loop counts transitions of the VCO output signal during an interval that is within the second segment of the period of the ramp function and of which center is offset in time from center of the second segment of the period of the ramp function.

* * * * *

UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO. : 5,659,587
DATED : August 19, 1997
INVENTOR(S) : David L. Knierim

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Column 7, line 42, after "slew" and before "control," delete "rage" and insert --rate--;

Column 7, line 66, after "and" and before "falling," delete "A" and insert --a--;

Column 8, line 23, after "ramp" and before "and" delete "magnitude" and insert --amplitude--;

Column 8, line 65, after "clock" and before "having," delete "sisal" and insert --signal--;

Column 8, line 66, after "a" and before "output," delete "dock" and insert - -clock- -;

Column 9, line 22, after "said" and before "signal," delete "dock" and insert - -clock- -;

Column 10, line 38, after "the" and before "period", delete "the".

Signed and Sealed this

Twentieth Day of January, 1998

Attest:

BRUCE LEHMAN

Attesting Officer

Commissioner of Patents and Trademarks

EXHIBIT 30
(USP 6,294,936)

US006294936B1

(12) **United States Patent**
Clementi

(10) **Patent No.: US 6,294,936 B1**
(45) **Date of Patent: Sep. 25, 2001**

(54) **SPREAD-SPECTRUM MODULATION METHODS AND CIRCUIT FOR CLOCK GENERATOR PHASE-LOCKED LOOP**

(75) Inventor: **Daniel M. Clementi**, Doylestown, PA (US)

(73) Assignee: **American Microsystems, Inc.**, Pocatello, ID (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **09/161,969**

(22) Filed: **Sep. 28, 1998**

(51) **Int. Cl.**[7] **H03D 1/04**
(52) **U.S. Cl.** **327/156**; 327/147
(58) **Field of Search** 327/141, 147, 327/156, 113, 114; 331/78; 375/200

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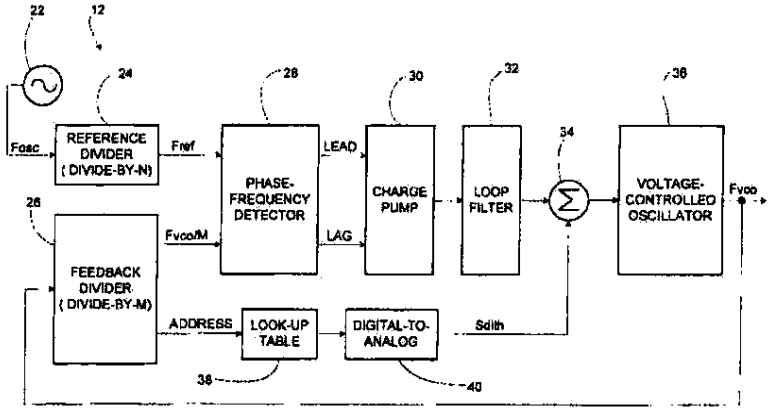
Primary Examiner—Tuan T. Lam
(74) *Attorney, Agent, or Firm*—Renner, Otto, Boisselle & Sklar, LLP

(57) **ABSTRACT**

A spread-spectrum modulation method and circuit for a clock generator phase-locked loop (PLL). A dither signal is injected into a PLL in synchronization with and having the same period or fraction of the same period as the phase comparison performed within the PLL. Over such period, the phase error caused by the modulation will integrate to zero and hence avoid transmitting a disturbance to the loop. A particular embodiment utilizes an output of the reference divider and/or feedback divider within the PLL to generate the dither signal. Such a configuration avoids the need for additional hardware which otherwise would increase the chip area and/or cost of the device. The reference divider and/or feedback divider is made up preferably of a linear feedback shift register (LFSR). One or more stages of the LFSR provide an output which is used to generate the dither signal. In a preferred embodiment, the output from the LFSR exhibits a pseudo-random sequence.

29 Claims, 7 Drawing Sheets



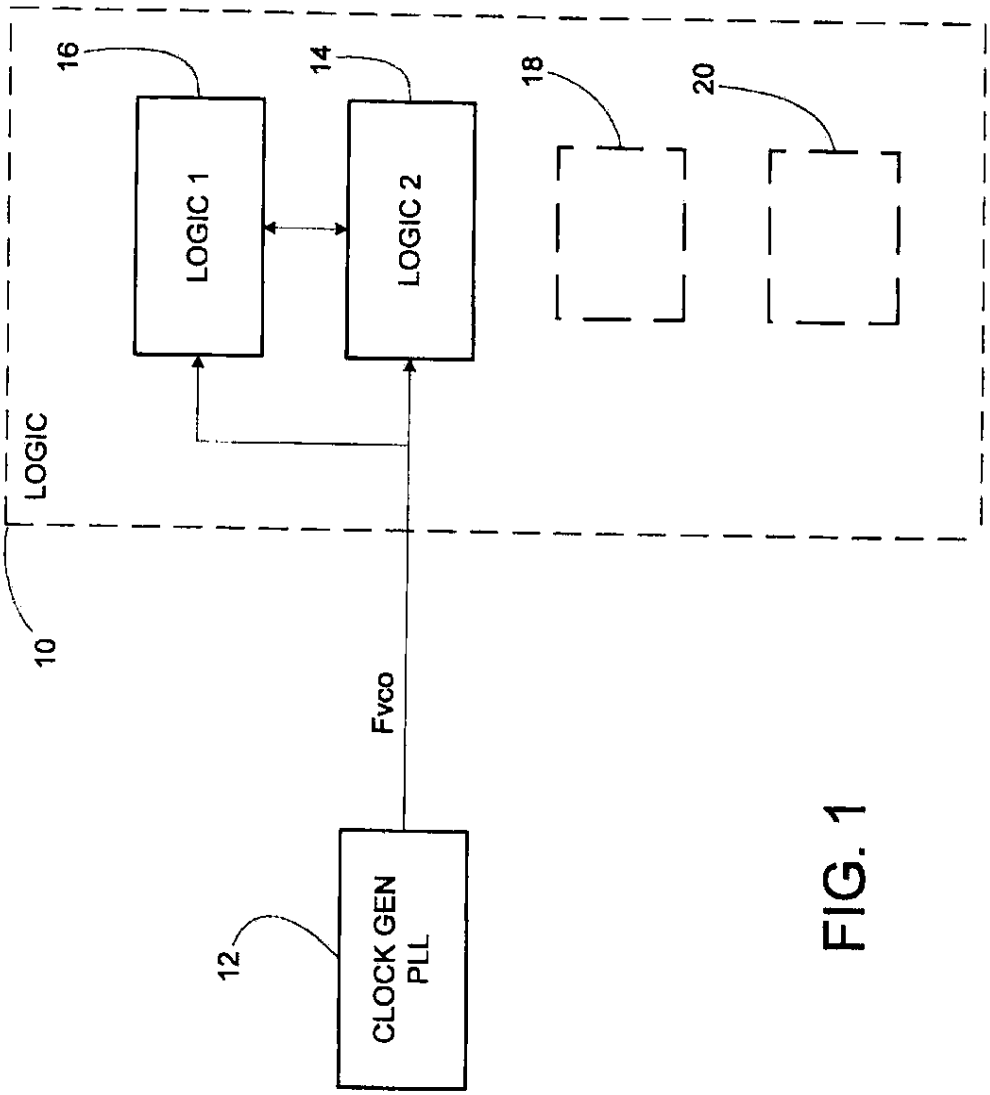


FIG. 1

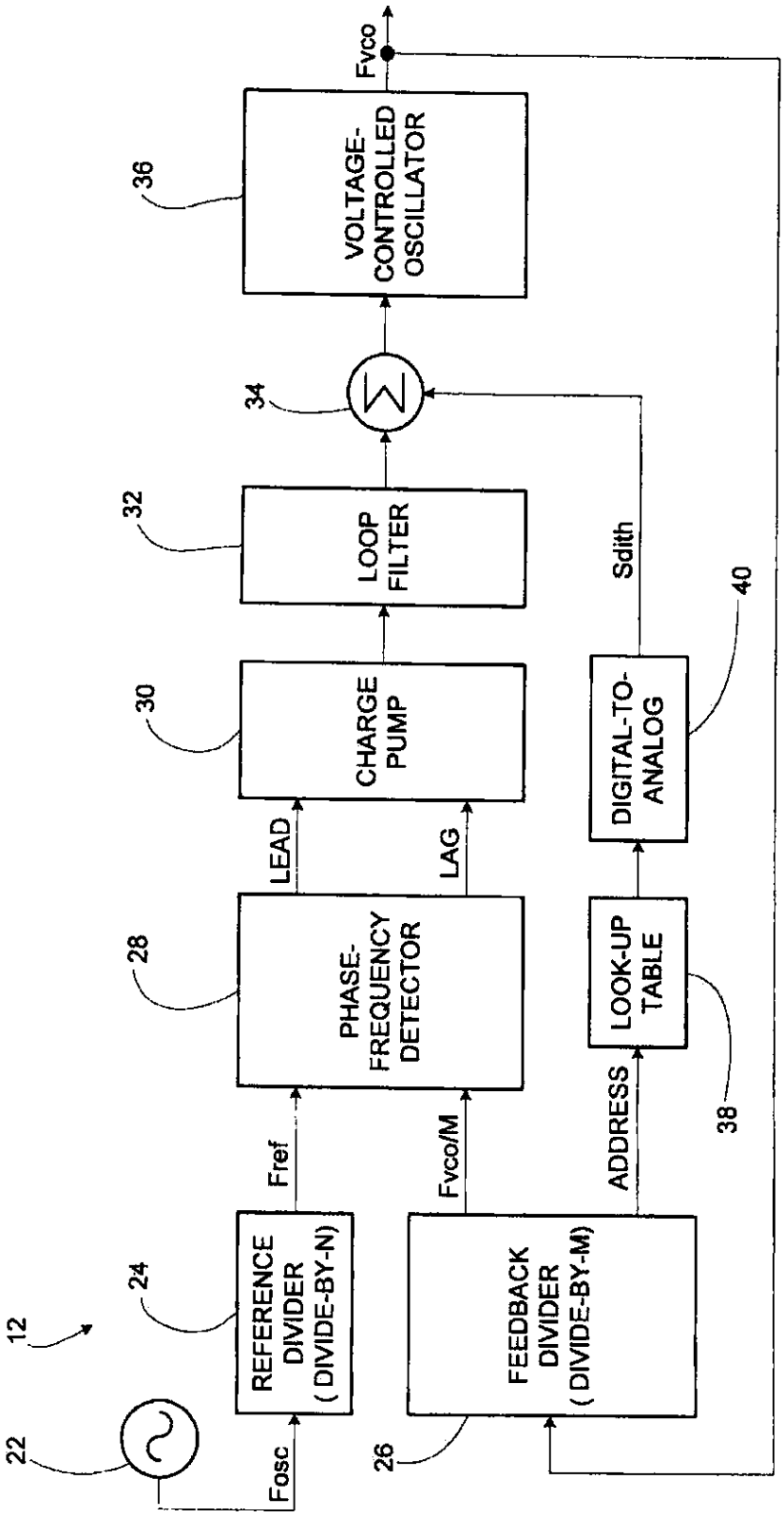
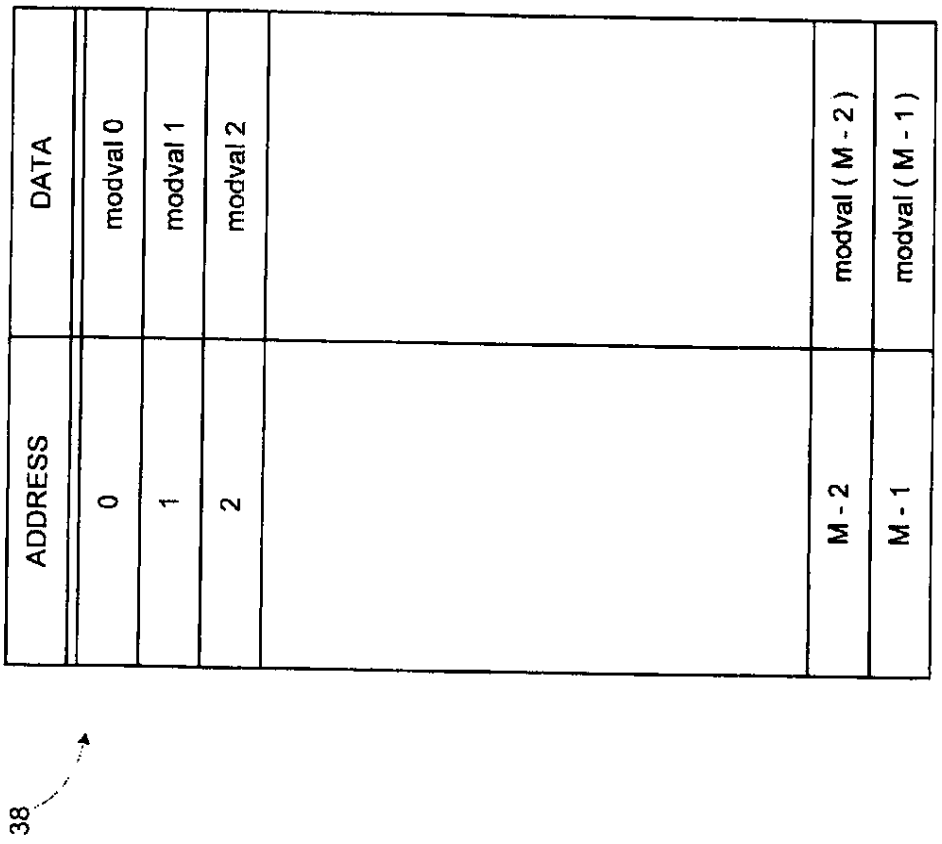

Fvco
VOLTAGE-CONTROLLED OSCILLATOR
36
34
LOOP FILTER
32
CHARGE PUMP
30
LEAD
LAG
PHASE-FREQUENCY DETECTOR
28
Fref
Fvco/M
REFERENCE DIVIDER (DIVIDE-BY-N)
24
12
22
Fosc
FEEDBACK DIVIDER (DIVIDE-BY-M)
26
ADDRESS
LOOK-UP TABLE
38
DIGITAL-TO-ANALOG
40
Sdith

FIG. 2

FIG. 3


ADDRESS
DATA
0
modval 0
1
modval 1
2
modval 2
M - 2
modval (M - 2)
M - 1
modval (M - 1)
38

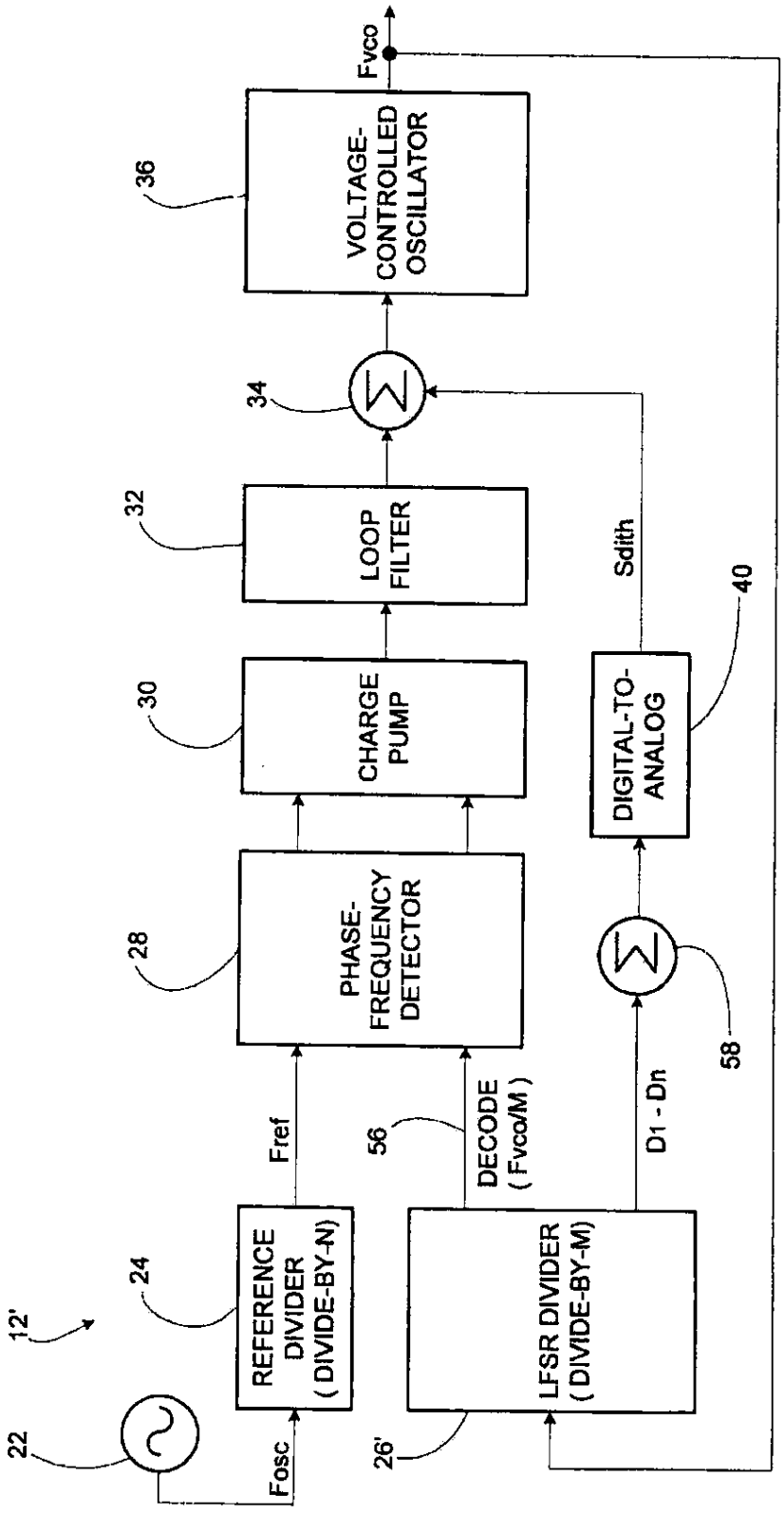

Fvco
VOLTAGE-CONTROLLED OSCILLATOR
36
34
LOOP FILTER
32
CHARGE PUMP
30
PHASE-FREQUENCY DETECTOR
28
REFERENCE DIVIDER (DIVIDE-BY-N)
24
12'
22
Fosc
Fref
56
DECODE (Fvco/M)
LFSR DIVIDER (DIVIDE-BY-M)
26'
D1 - Dn
58
DIGITAL-TO-ANALOG
40
Sdith

FIG. 4

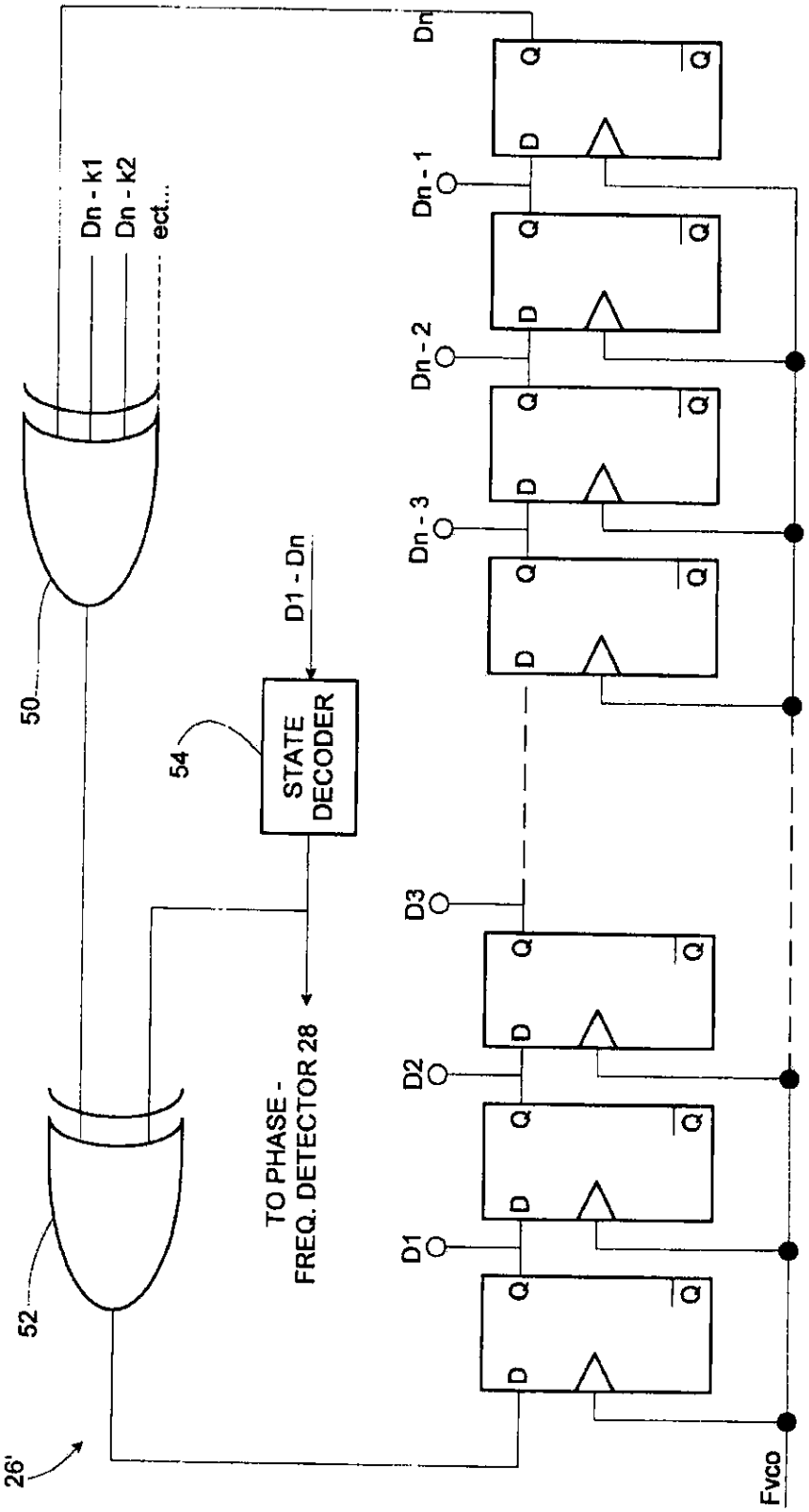

Dn
Dn - 1
Dn - 2
Dn - 3
D3
D2
D1
Dn - k1
Dn - k2
ect...
50
52
54
26'
D1 - Dn
STATE DECODER
TO PHASE - FREQ. DETECTOR 28
Fvco
Q
D

FIG. 5

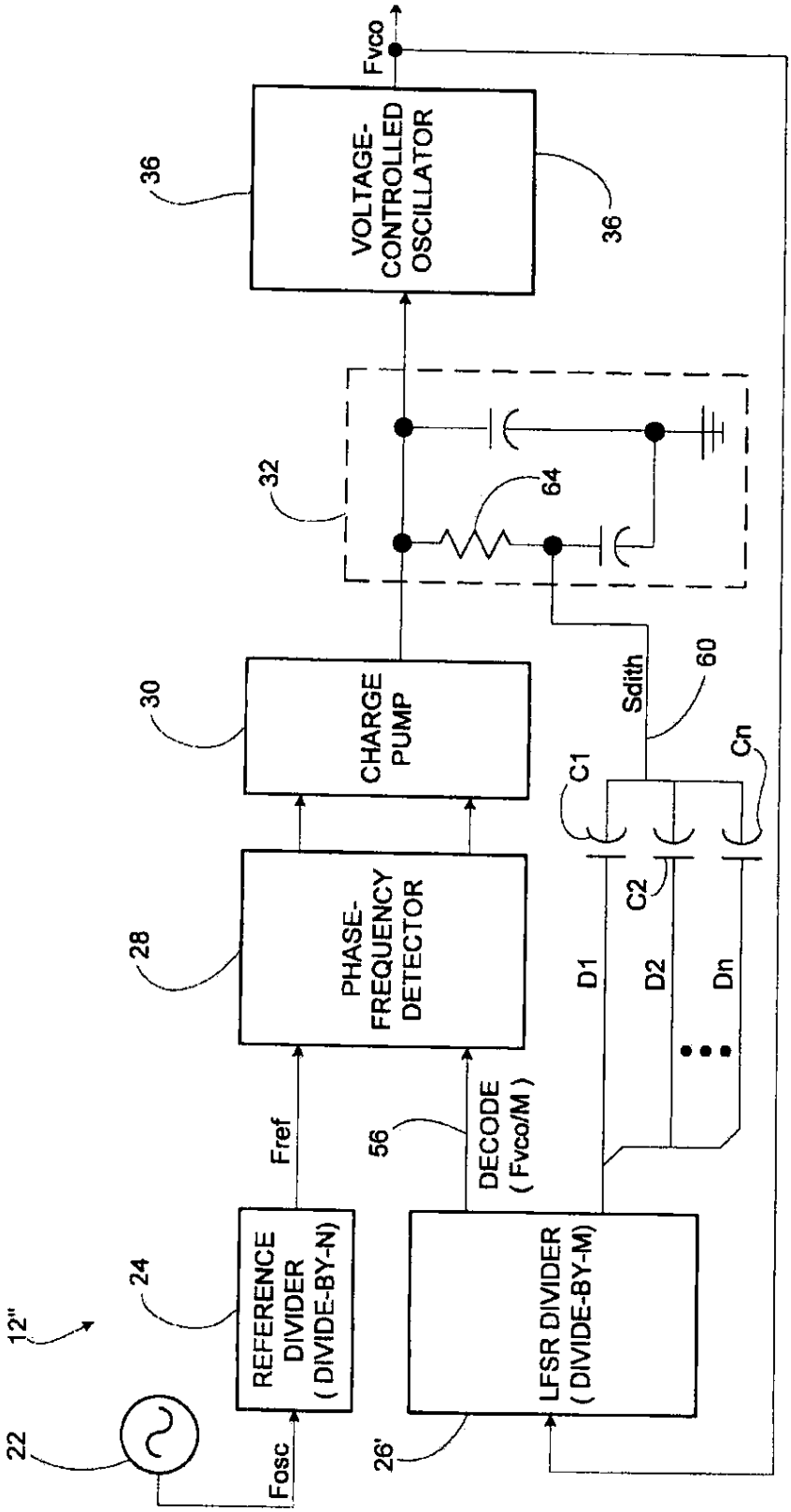

Fvco
VOLTAGE-CONTROLLED OSCILLATOR
36
36
32
64
CHARGE PUMP
30
Sdith
60
C1
Cn
C2
PHASE-FREQUENCY DETECTOR
28
D1
D2
Dn
Fref
56
DECODE (Fvco/M)
REFERENCE DIVIDER (DIVIDE-BY-N)
LFSR DIVIDER (DIVIDE-BY-M)
24
12"
22
Fosc
26'

FIG. 6

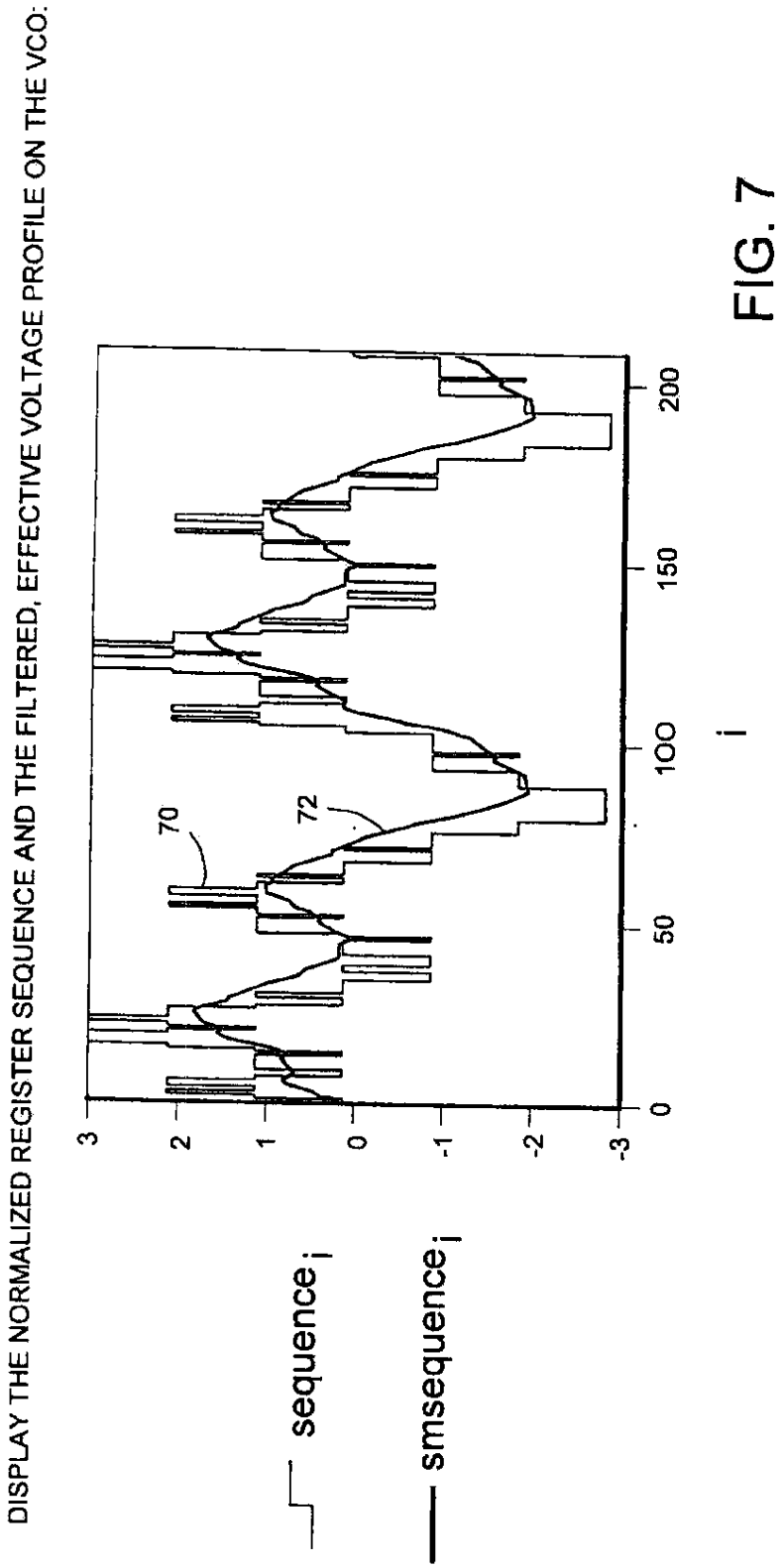

DISPLAY THE NORMALIZED REGISTER SEQUENCE AND THE FILTERED, EFFECTIVE VOLTAGE PROFILE ON THE VCO:
3
2
1
0
-1
-2
-3
0
50
100
150
200
i
70
72
sequence_i
smsequence_i

FIG. 7

SPREAD-SPECTRUM MODULATION METHODS AND CIRCUIT FOR CLOCK GENERATOR PHASE-LOCKED LOOP

TECHNICAL FIELD

The present invention relates to a method and circuit for modulating a clock signal to spread its spectral energy over a band of frequencies.

BACKGROUND OF THE INVENTION

Electronic devices and systems such as microprocessors rely on clock signals to provide timing control. Such clock signals typically are based on a precision reference source such as a crystal oscillator. However, a crystal oscillator has a high Q value which results in the spectral energy of the clock signal being concentrated in a very narrow frequency band. The concentration of the energy at the clock frequency as well as its harmonics can lead to emission of electromagnetic interference (EMI) in excess of that permitted under applicable government regulations.

In certain electronic systems it is possible to dither or modulate the frequency of the clock signal in order to spread its spectral energy over a band of frequencies. The result of this spreading is a reduction of the energy of the clock or harmonics of the clock that might otherwise appear at any particular frequency or band. Such dithering of the clock signal facilitates compliance with the applicable government regulations.

Various approaches have been proposed for dithering a clock signal. For example, Hewlett-Packard has developed a technique for dithering the reference divider of a phase-locked loop (PLL) between values to create a modulation profile. U.S. Pat. No. 5,610,955 is directed to a variation of such technique that dithers both the reference divider and the feedback divider in a PLL in order to spread the resultant clock signal.

Although these approaches are successful in dithering the clock signal, there are however a number of disadvantages. For example, by dithering the feedback divider and/or reference divider the PLL is continually being driven out of lock. This means that the PLL loop dynamics (e.g., unity-gain frequency, damping, etc.) affect the performance of the resulting modulation. If the loop bandwidth is too narrow, the modulating profile is filtered. If the loop bandwidth is set up to be very wide, compromises must be made regarding the precision of the resulting output frequency and step size. As is known, wide loop bandwidths require small integers in the feedback divider path.

Another disadvantage of such conventional approaches is the requirement for significant additional hardware in order to implement clock dithering. For example, additional dividers are oftentimes necessary. Such additional hardware occupies chip area and increases the size and/or cost of the electronic device.

In view of the aforementioned shortcomings associated with conventional approaches, there is a strong need in the art for an improved method and circuit for dithering a clock signal. In particular, there is a strong need for a method and circuit for dithering a clock signal generated by a PLL which avoids continually driving the PLL out of lock. Moreover, there is a strong need in the art for a circuit and method for dithering a clock signal generated by a PLL which does not require significant additional hardware.

SUMMARY OF THE INVENTION

A spread-spectrum modulation method and circuit for a clock generator phase-locked loop is described herein in

accordance with the present invention. In a preferred embodiment, the present invention involves injecting a dither signal into a PLL that is synchronized with and has the same period or fraction of the same period as the phase comparison performed within the PLL. Over such period, the phase error caused by the modulation will integrate to zero and hence avoid transmitting a disturbance to the loop. Consequently, the present invention avoids continually driving the PLL out of lock.

A particular embodiment of the present invention utilizes an output of the reference divider and/or feedback divider within the PLL to generate the dither signal. The dither signal will consequently have the same period or fraction of the same period as the comparison performed by the PLL phase comparator. The PLL phase comparator is a sampled-data system which has a zero in its transfer function for phase modulation at its input where the frequency of such phase modulation is equal to the sampling frequency or multiples thereof.

Moreover, such a configuration avoids the need for additional hardware which otherwise would increase the chip area and/or cost of the device. In a preferred embodiment, the reference divider and/or feedback divider is made up of a linear feedback shift register (LFSR). One or more stages of the LFSR provide an output which is used to generate the dither signal. In a preferred embodiment, the output from the LFSR exhibits a pseudo-random sequence. This tends to spread the frequency of the clock signal more randomly so as to avoid introducing undesirable harmonics.

According to a particular aspect of the present invention, a clock generator phase-locked loop is provided. The phase-locked loop includes a reference frequency source for providing a reference frequency; a phase comparator for producing a control signal based on a periodic comparison of a phase difference between respective signals provided to a first input and a second input of the phase comparator, the reference frequency being operatively coupled to the first input; a voltage-controlled oscillator for generating an output frequency based on the control signal provided by the phase comparator; a feedback divider which receives and divides the output frequency to provide a divider output which is operatively coupled to the second input of the phase comparator; and a modulation circuit for injecting a dither signal within the clock generator phase-locked loop to modulate the output frequency, a period of the dither signal being equal to or an integer fraction of a phase comparison period of the phase comparator.

According to another aspect of the invention, a clock generator phase-locked loop is provided which includes a reference frequency source for providing a reference frequency; a phase comparator for producing a control signal based on a phase difference between respective signals provided to a first input and a second input of the phase comparator, the reference frequency being operatively coupled to the first input; a voltage-controlled oscillator for generating an output frequency based on the control signal provided by the phase comparator; a feedback divider which receives and divides the output frequency to provide a divider output which is operatively coupled to the second input of the phase comparator; and a modulation circuit for injecting a dither signal within the clock generator phase-locked loop to modulate the output frequency, wherein at least one of a reference divider included in the reference frequency source and the feedback divider comprises a linear feedback shift register counter having a plurality of stages, and the modulation circuit comprises an output of at least one of the plurality of stages which is used to produce the dither signal.

In accordance with yet another aspect of the invention, a method is provided for dithering a clock generator phase-locked loop including a reference frequency source for providing a reference frequency, a phase comparator for producing a control signal based on a periodic comparison of a phase difference between respective signals provided to a first input and a second input of the phase comparator, the reference frequency being operatively coupled to the first input, a voltage-controlled oscillator for generating an output frequency based on the control signal provided by the phase comparator, and a feedback divider which receives and divides the output frequency to provide a divider output which is operatively coupled to the second input of the phase comparator. The method includes the step of injecting a dither signal within the clock generator phase-locked loop to modulate the output frequency, a period of the dither signal being equal to or an integer fraction of a phase comparison period of the phase comparator.

According to still another aspect of the invention, a method is provided for dithering a clock generator phase-locked loop including a reference frequency source for proving a reference frequency, a phase comparator for producing a control signal based on a phase difference between respective signals provided to a first input and a second input of the phase comparator, the reference frequency being operatively coupled to the first input, a voltage-controlled oscillator for generating an output frequency based on the control signal provided by the phase comparator, and a feedback divider which receives and divides the output frequency to provide a divider output which is operatively coupled to the second input of the phase comparator, wherein at least one of a reference divider included in the reference frequency source and the feedback divider comprises a linear feedback shift register counter having a plurality of stages. The method includes the step of injecting a dither signal within the clock generator phase-locked loop to modulate the output frequency, the dither signal being based on an output of at least one of the plurality of stages.

To the accomplishment of the foregoing and related ends, the invention, then, comprises the features hereinafter fully described and particularly pointed out in the claims. The following description and the annexed drawings set forth in detail certain illustrative embodiments of the invention. These embodiments are indicative, however, of but a few of the various ways in which the principles of the invention may be employed. Other objects, advantages and novel features of the invention will become apparent from the following detailed description of the invention when considered in conjunction with the drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a block diagram of an exemplary digital logic system utilizing a spread-spectrum clock generator phase-locked loop in accordance with the present invention;

FIG. 2 is a block diagram of a first example of a clock generator phase-locked loop in accordance with the present invention;

FIG. 3 is a look-up table for use in accordance with the example of FIG. 2;

FIG. 4 is a block diagram of a second example of a clock generator phase-locked loop in accordance with the present invention;

FIG. 5 is a schematic diagram of a linear feedback shift register for serving as a reference divider or feedback divider and serving to provide a dither signal in accordance with the present invention;

FIG. 6 is a block diagram of a third example of a clock generator phase-locked loop in accordance with the present invention; and

FIG. 7 is a graphical representation of a normalized register sequence and effective voltage profile of an exemplary dither signal in accordance with the present invention.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

The present invention will now be described with reference to the drawings, wherein like reference numerals are used to refer to like elements throughout.

FIG. 1 illustrates a logic system **10** which utilizes a clock signal Fvco for providing timing control. In accordance with the present invention, a clock generator phase-locked loop (PLL) **12** produces the clock signal Fvco provided to the system **10**. The system **10** includes, for example, digital logic blocks **14** and **16** forming part of a larger logic circuit or the like. The clock signal Fvco is input directly to the logic blocks **14** and **16**. The logic blocks **14** and **16** are designed to use the clock signal Fvco for timing control and/or derive other clock signals therefrom as part of their operation. The system **10** may include various other logic blocks (e.g., **18** and **20**) which may or may not rely directly on the clock signal Fvco for timing control.

The clock generator PLL **12** of the present invention produces a clock signal which has its spectral energy spread over a band of frequencies, thereby avoiding excessive EMI. In addition, any other clock signals derived from the clock signal are spread so as to avoid further excessive EMI.

Moreover, the clock generator PLL **12** is not continually driven out of lock by dithering as has been the case in conventional clock generator PLLs. As is described more fully below in relation to the examples of FIGS. **2** thru **6**, a dither signal is introduced within the clock generator PLL **12** which is synchronized with the phase comparison performed therein. More particularly, the period of the dither signal is equal to or an integer fraction of the period at which phase comparisons are performed by the phase comparator. The phase error which is introduced by the dither signal will integrate to zero as a result, and little or no disturbance is transmitted to the loop. By using the output of a divider/counter included in the clock generator PLL **12** to produce the dither signal, a modulated clock signal can be obtained at relatively low cost as compared to conventional techniques.

FIG. **2** shows a first example of the clock generator PLL **12** in accordance with the present invention. The clock generator PLL **12** receives as an input a reference oscillator frequency Fosc from a reference oscillator **22**. The reference oscillator **22** preferably is a precision oscillator such as a crystal oscillator which provides a stable oscillator frequency Fosc. The oscillator frequency Fosc preferably is a square-wave as is conventional.

The clock generator PLL **12** includes a reference divider **24** and a feedback divider **26**. The reference divider **24** is a divide-by-N divider (where N is an integer) which divides the oscillator frequency Fosc received at an input, and produces a divided reference frequency Fref at its output. The reference divider **24** may be any conventional divider such as a binary counter.

The reference frequency Fref output by the reference divider **24** is input to a first input of a phase detector/comparator **28** also included in the clock generator PLL **12**. The phase comparator **28** can be a standard PLL phase comparator such as a type I or type II phase comparator see,

e.g., P. Horowitz et al., *The Art of Electronics*, pp. 644-646, 2nd Ed., Cambridge University Press (1994)); or a sample/hold type phase comparator (see, e.g., U. Rohde, *Digital PLL Frequency Synthesizers*, pp. 210–213, Prentice-Hall, Inc. (1983)). The phase comparator **28** periodically compares the phase of the reference frequency Fref with that of a feedback signal (discussed below) and produces an output based on the phase difference therebetween. More specifically, the phase comparator **28** compares the phase of the respective input signals responsive to edges of the reference frequency Fref from the reference divider **24** and the output of the feedback divider **26** (Fvco/M). Based on such comparison, the phase comparator **28** produces an output signal representative of the amount by which the phase of the reference frequency Fref leads or lags the feedback signal.

The output from the phase comparator **28** is input to a charge pump **30** (which in some instances is part of the phase comparator **28** itself). The charge pump **30** increases or decreases a control voltage provided at its output based on whether the reference frequency Fref leads or lags the feedback signal. The control voltage from the charge pump **30** is then filtered via a loop filter **32** as is conventional. Specifically, the loop filter **32** is a low pass filter for filtering fluctuations in the output of the charge pump **30**.

In a conventional PLL, the output of the loop filter **32** typically serves as the control voltage provided to a voltage-controlled oscillator (VCO). According to the exemplary embodiment, however, the output of the loop filter **32** is input to an summer **34**. As is discussed in more detail below, the summer **34** is used to modulate the control voltage provided to the VCO. Specifically, the output of the summer **34** provides a voltage control signal which is input to a VCO **36** included within the clock generator PLL **12**. The output frequency Fvco of the VCO **36** is based on the control signal input to the VCO **36** as is conventional. The output frequency Fvco serves a s the output of the clock generator PLL **12** and is input to the electronic system **10** (FIG. 1), for example.

The output frequency Fvco of the VCO **36** is fed back to the input of the feedback divider **26**. The feedback divider **26** is a divide-by-M divider where M is an integer. The value of M may be fixed or programmable according to known techniques. The feedback divider **26** divide s the output frequency Fvco by M and produces a feedback signal Fvco/M which is provided to the feedback input of the phase comparator **28**. As pointed out above, the phase comparator **28** compares the phase of the reference frequency Fref and the feedback signal Fvco/TM s o as to lock in on the desired output frequency Fvco.

The combination of the reference divider **24**, phase comparator **28**, charge pump **30**, loop filter **32**, VCO **36** and feedback divider **26** form what is otherwise known as a conventional PLL. The clock generator PLL **12** differs from such conventional PLLs, however, by the manner in which the output frequency Fvco is dithered or modulated so as to spread the spectral energy over a band of frequencies. Specifically, a dither signal Sdith is injected into the PLL via the adder **34** in order to modulate the output frequency Fvco. The modulating waveform represented by Sdith is synchronized with the phase comparison performed by the phase comparator **28**, and has the same period or fraction of the same period as the phase comparison performed by the phase comparator **28**.

A preferred way for generating a dither signal Sdith which is synchronized with and has the same period or fraction of the same period as the phase comparator **28** is to use the feedback divider **26**, the reference divider **24**, or both to generate the signal. For example, in the embodiment of FIG. **2** the feedback divider **26** is a standard binary counter used as a divider. A first output of the counter changes state once every M cycles of the output frequency Fvco, and is coupled to the input of the phase comparator **28**. Those having ordinary skill in the art will appreciate the manner in which a standard binary counter may be designed to provide such an output.

Additionally, however, the counter forming the feedback divider **26** provides a second output representing the particular value, or state, of the counter. As will be appreciated, the value of the second counter output will be continuously incremented from 0 to M−1 with each cycle of the output frequency Fvco. This second output provides a sequence of addresses from 0 to M−1 to a look-up table **38** included in the clock generator PLL **12**. As is shown in FIG. **3**, the look-up table **38** has stored therein a sequence of modulation values modval0 thru modval(M−1) corresponding respectively to the addresses 0 thru M−1.

The modulation values modval0 thru modval(M−1) are discrete values representing the dither signal waveform Sdith. These discrete values are accessed in synchronization with the output frequency Fvco, and hence in synchronization with the reference frequency Fref and the comparisons performed by the phase comparator **28**. The modulation values accessed from the look-up table **38** are output to a digital-to-analog convertor **40** which converts the discrete values into an analog signal Sdith which is provided to the other input of the summer **34**. Thus, the signal Sdith is added to the output of the loop filter **32** and serves to dither the output of the loop filter **32**. This results in the control voltage applied to the VCO **36** being modulated and hence the output frequency Fvco is dithered.

The particular waveform which is stored in the look-up table **38** can be any desired modulation waveform. Such waveform may be preselected based on the desired profile of the resultant spread output frequency Fvco as will be appreciated. The waveform stored in the look-up table **38** may represent a single cycle, or a plurality of cycles depending on the modulating waveform. Such waveform may be periodic such as a sinewave, a triangle wave, a sawtooth wave, etc. Alternatively, such modulating waveform may represent a pseudo-random variable signal which tends to randomly vary the output frequency Fvco. Symmetry of the modulating waveform, either in time or voltage, may be exploited by storing only a portion of the waveform in the table **38** and repeating its application to the VCO **36** in an appropriate fashion.

The look-up table **38** may be constructed from a read-only memory (ROM) or other type memory. The waveform stored therein may be fixed or programmable as will be appreciated.

FIG. **2** illustrates an embodiment in which the count value of the feedback divider **26** provides the addressing for the look-up table **38**. However, it will be appreciated that the count value of a counter serving as the reference divider **24** instead could be utilized for addressing the look-up table **38** without departing from the scope of the invention. Even further, the combined output values from the dividers **24** and **26** could be utilized. For example, the output value of one of the dividers may serve as the most significant address bits and the output value of the other divider may serve as the least significant address bits. In each case, the values of the dither signal Sdith are injected into the loop in synchronization with the comparisons performed by the phase comparator **28**.

Turning now to FIG. **4**, another example of a clock generator PLL is designated **12'**. The clock generator PLL **12'** is identical to that described above with respect to FIG. **2** with the following exceptions. The feedback divider in the present example is designated **26'** and is made up of a linear-feedback shift register (LFSR). In addition to functioning as a divide-by-M counter, the LFSR produces an output sequence representing a pseudo-random sequence whose properties can be shown to resemble white noise. By direct application of this output sequence to the control signal of the VCO **36**, an effective clock dithering technique can be achieved with very little additional hardware.

As is shown in FIG. **5**, the feedback divider **26'** is represented by an n-stage shift register made up of n D-type flip-flops cascaded together. The Q output of each flip-flop (designated D_1 thru D_n, respectively), with the exception of the last in the sequence, is input to the D input of the next flip-flop. The last, or n-th, flip-flop has its output D_n fed back through exclusive-OR gates **50** and **52** to the D input of the first flip-flop in the sequence. The output frequency Fvco is input to the feedback divider **26'** and serves as the clock signal to each of the flip-flops.

The exclusive-OR gate **50** receives as its other inputs the outputs of one or more of the other flip-flops (i.e., D_1–D_n). The particular outputs which are input to the exclusive-OR gate **50** are preselected based on the desired output sequence, and are designated D_{n-k}, D_{n-k2}, etc. The output of the exclusive OR gate **50** is input to the exclusive-OR gate **52** which exclusive ORs the output with the output of a state decoder **54** included in the feedback divider **26'**. The state decoder **54** receives as inputs each of the outputs D_1 thru D_n from the respective stages. The state decoder **54** represents logic preconfigured to transition through a predefined number of states (e.g., M) to produce an output on line **56** which includes a pulse every M cycles of the output frequency Fvco. In this manner, the LFSR functions as a divide-by-M divider, and the output of the decoder **54** on line **56** is coupled to the feedback input of the phase comparator **28** (FIG. **2**).

Based on which particular outputs D_1 thru D_n are fed back through the exclusive-OR gate **50**, a pseudo-random sequence is output by the LFSR via the outputs D_1 thru D_n. As is known, the counting sequence of an LFSR is non-binary and essentially pseudo-random. This pseudo-random sequence is updated with each Fvco cycle, and is updated in synchronization with the phase comparison performed by the phase comparator **28**.

Referring back to FIG. **4**, the outputs D_1, thru D_n from the respective stages of the LFSR are provided to a digital summer **58**. It can be observed from FIG. **5** that the output of each stage of the LFSR is simply a time shifted copy of the feedback bit D_n. A very simple "boxcar" or moving-average filter can be implemented simply by summing the output of all the shift register outputs together via the summer **58** (e.g., computing the sum of logic "1"s). Such a filter has a sin x/x (low-pass response) and is effective at reducing the high-frequency components present in the pseudo-random data stream presented at the outputs D_1 thru D_n. The filtered sequence is output by the summer **58** and is input to the digital-to-analog convertor **40**. The convertor **40** in turn produces an analog signal which represents the dither signal Sdith used to modulate the output of the loop filter **32** via the summer **34**.

Accordingly, the output frequency Fvco is modulated by a dither signal which represents a pseudo-random sequence produced by the LFSR serving as the feedback divider. Those having ordinary skill in the art of linear feedback shift registers will appreciate the manner in which an LFSR may be configured to operate as a divide-by-M counter for selected value(s) of M as well as to produce a pseudo-random sequence of preselected length. (See, e.g., Xilinx Application Note, *Efficient Shift Registers, LFSR Counters, and Long Pseudo-Random Sequence Generators*, XAPP 052, Jul. 7, 1996). Hence, further detail is omitted herein for sake of brevity.

Although the feedback divider **26'** is shown as incorporating the LFSR, it will be appreciated that the reference divider **24** instead/also may utilize an LFSR as shown in FIG. **5** both to function as a divider and to generate the dither signal. The present invention contemplates each situation.

FIG. **6** represents a third example of the present invention. The third example is the same as the second example of FIGS. **4** and **5** with the following exceptions. In this example, the outputs D_1 thru D_n are each capacitively coupled via a corresponding capacitance C_1 thru C_n to a common line **60**. The summation of the outputs Dthru D_n thus produced on line **60** represents a moving-average, filtered dither signal Sdith which is coupled directly into the loop filter **32**.

The loop filter **32** can be represented by a capacitor **62** and resistor **64** coupled in series. This series combination is arranged in parallel with a capacitor **66**, and the parallel combination is connected between the output of the charge pump **30** and ground as shown to form a low pass filter. The dither signal Sdith on line **60** is coupled to the node between the capacitor **62** and the resistor **64** and functions to modulate the control signal which is input to the VCO **36**. Accordingly, as the value of Sdith changes in accordance with the sequence presented by the outputs Dthru D_n, the output frequency Fvco is modulated so as to spread its spectral energy.

As with the second example, the particular pseudo-random sequence which is output by the LFSR is preselected to provide a desired amount of dithering in the output frequency. In the third example shown in FIG. **6**, the direct capacitive coupling of the LFSR outputs to the loop filter **32** is particularly beneficial in that it permits implementation at extremely small hardware cost. Similar to the previous example, the LFSR may instead be part of the reference divider **24** and may be used to generate the dither signal Sdith in the same manner. As in all of the examples, the modulating waveform Sdith is provided in synchronization with the phase comparison performed by the phase comparator **28**. Consequently, the error signal integrates to zero and is ignored by the loop resulting in the PLL not being driven out of lock as in the conventional techniques.

FIG. **7** illustrates an exemplary normalized register sequence **70** forming Sdith as presented by the capacitively coupled outputs D_1–D_N for a particular configuration of the LFSR. The waveform **72** illustrates the effective voltage profile on the VCO **36** for two complete cycles.

It will therefore be appreciated that the present invention provides for an improved method and circuit for dithering a clock signal. The present invention provides a method and circuit for dithering a clock signal generated by a PLL which avoids continually driving the PLL out of lock. At the same time, the present invention does not require significant additional hardware.

Although the invention has been shown and described with respect to certain preferred embodiments, it is obvious that equivalents and modifications will occur to others skilled in the art upon the reading and understanding of the

specification. For example, the examples of FIGS. 4 and 6 could be modified such that the values of the respective outputs D_1 thru D_n are weighted differently so as to have a different effect on the resultant modulation waveform.

Furthermore, different type reference and/or feedback dividers may be utilized in order to generate the dither signal Sdith. For example, the reference divider **24** or the feedback divider **26** as shown in FIG. **2**, whichever (or both) is utilized to provide the sequence of addresses to the look-up table **38**, could be made of a counter other than a binary counter or an LFSR. Another embodiment of the present invention uses a reference divider **24** and/or feedback divider **26** made up of an accumulator structure. The contents of the accumulator provide the address to the look-up table **38**. By selectively controlling the amount by which the accumulator is incremented on each clock cycle (i.e., by Fvco and Fosc), it is possible to alter the frequency of the resultant dither signal Sdith obtained from the look-up table **38**.

It will be appreciated that the address for the look-up table **38** may be taken from all of the bits of the accumulator or a subset thereof. Upon overflow of the accumulator, simple binary wraparound may be permitted to occur or the accumulator may be reset. If wraparound is permitted, non-integer divisors may occur which can generate disturbances in the PLL which in some circumstances may be acceptable. By resetting the accumulator upon overflow, such disturbances can be avoided.

The present invention includes all such equivalents and modifications, and is limited only by the scope of the following claims.

What is claimed is:

1. A clock generator phase-locked loop, comprising:

a reference frequency source for providing a reference frequency;

a phase comparator for producing a control signal based on a periodic comparison of a phase difference between respective signals provided to a first input and a second input of the phase comparator, the reference frequency being operatively coupled to the first input;

a voltage-controlled oscillator for generating an output frequency based on the control signal provided by the phase comparator;

a feedback divider which receives and divides the output frequency to provide a divider output which is operatively coupled to the second input of the phase comparator; and

a modulation circuit for injecting a dither signal into the control signal provided by the phase comparator to modulate the output frequency, a period of the dither signal being equal to or an integer fraction of a phase comparison period of the phase comparator.

2. The clock generator phase-locked loop of claim **1**, wherein the period of the dither signal is equal to the phase comparison period.

3. The clock generator phase-locked loop of claim **1**, wherein the feedback divider comprises a counter and the modulation circuit comprises a look-up table having modulation values stored therein for producing the dither signal, the value of the counter serving to provide a sequence of addresses to the look-up table for accessing the modulation values.

4. The clock generator phase-locked loop of claim **1**, wherein the feedback divider comprises a counter and an output of the counter is used by the modulation circuit to produce the dither signal.

5. The clock generator phase-locked loop of claim **4**, wherein the counter is a linear feedback shift register counter having a plurality of stages, and an output of at least one of the plurality of stages is used to produce the dither signal.

6. The clock generator phase-locked loop of claim **5**, wherein the output of the at least one of the plurality of stages exhibits a pseudo-random sequence.

7. The clock generator phase-locked loop of claim **1**, further comprising a reference divider for dividing an input reference frequency to produce the reference frequency.

8. The clock generator phase-locked loop of claim **7**, wherein at least one of the reference divider and the feedback divider comprises a counter and the modulation circuit comprises a look-up table having modulation values stored therein for producing the dither signal, the value of the counter serving to provide a sequence of addresses to the look-up table for accessing the modulation values.

9. The clock generator phase-locked loop of claim **7**, wherein at least one of the reference divider and the feedback divider comprises a counter and an output of the counter is used by the modulation circuit to produce the dither signal.

10. The clock generator phase-locked loop of claim **9**, wherein the counter is a linear feedback shift register counter having a plurality of stages, and an output of at least one of the plurality of stages is used to produce the dither signal.

11. The clock generator phase-locked loop of claim **10**, wherein the output of the at least one of the plurality of stages exhibits a pseudo-random sequence.

12. A clock generator phase-locked loop, comprising:

a reference frequency source for proving a reference frequency;

a phase comparator for producing a control signal based on a phase difference between respective signals provided to a first input and a second input of the phase comparator, the reference frequency being operatively coupled to the first input;

a voltage-controlled oscillator for generating an output frequency based on the control signal provided by the phase comparator;

a feedback divider which receives and divides the output frequency to provide a divider output which is operatively coupled to the second input of the phase comparator; and

a modulation circuit for injecting a dither signal within the clock generator phase-locked loop to modulate the output frequency,

wherein at least one of a reference divider included in the reference frequency source and the feedback divider comprises a linear feedback shift register counter having a plurality of stages, and the modulation circuit receives an output of at least one of the plurality of stages which is used to produce the dither signal.

13. The clock generator phase-locked loop of claim **12**, wherein the modulation circuit comprises at least one of a digital-to-analog converter which converts the output to an analog signal which serves to modulate the control signal, and means for capacitively coupling the output to a modulator included within the modulation circuit to modulate the control signal.

14. The clock generator phase-locked loop of claim **12**, wherein the output exhibits a pseudo-random sequence.

15. A method for dithering a clock generator phase-locked loop including a reference frequency source for providing a reference frequency, a phase comparator for producing a control signal based on a periodic comparison of a phase

difference between respective signals provided to a first input and a second input of the phase comparator, the reference frequency being operatively coupled to the first input, a voltage-controlled oscillator for generating an output frequency based on the control signal provided by the phase comparator, and a feedback divider which receives and divides the output frequency to provide a divider output which is operatively coupled to the second input of the phase comparator, the method comprising the step of:

injecting a dither signal into the control signal provided by the phase comparator to modulate the output frequency, a period of the dither signal being equal to or an integer fraction of a phase comparison period of the phase comparator.

16. The method of claim **15**, wherein the period of the dither signal is equal to the phase comparison period of the phase comparator.

17. The method of claim **15**, wherein the feedback divider comprises a counter and the injecting step comprises using a look-up table having modulation values stored therein for producing the dither signal, the value of the counter serving to provide a sequence of addresses to the look-up table for accessing the modulation values.

18. The method of claim **15**, wherein the feedback divider comprises a counter and an output of the counter is used to produce the dither signal.

19. The method of claim **18**, wherein the counter is a linear feedback shift register counter having a plurality of stages, and an output made up of at least one of the plurality of stages is used to produce the dither signal.

20. The method of claim **19**, wherein the output of the at least one of the plurality of stages exhibits a pseudo-random sequence.

21. The method of claim **15**, wherein the clock generator phase-locked loop further comprises a reference divider for dividing an input reference frequency to produce the reference frequency.

22. The method of claim **21**, wherein at least one of the reference divider and the feedback divider comprises a counter and the injecting step comprises using a look-up table having modulation values stored therein for producing the dither signal, the value of the counter serving to provide a sequence of addresses to the look-up table for accessing the modulation values.

23. The method of claim **21**, wherein at least one of the reference divider and the feedback divider comprises a counter and an output of the counter is used to produce the dither signal.

24. The method of claim **23**, wherein the counter is a linear feedback shift register counter having a plurality of stages, and an output made up of at least one of the plurality of stages is used to produce the dither signal.

25. The method of claim **24**, wherein the output of the at lease one of the plurality of stages exhibits a pseudo-random sequence.

26. A method for dithering a clock generator phase-locked loop including a reference frequency source for proving a reference frequency, a phase comparator for producing a control signal based on a phase difference between respective signals provided to a first input and a second input of the phase comparator, the reference frequency being operatively coupled to the first input, a voltage-controlled oscillator for generating an output frequency based on the control signal provided by the phase comparator, and a feedback divider which receives and divides the output frequency to provide a divider output which is operatively coupled to the second input of the phase comparator, wherein at least one of a reference divider included in the reference frequency source and the feedback divider comprises a linear feedback shift register counter having a plurality of stages, the method comprising the step of:

injecting a dither signal within the clock generator phase-locked loop to modulate the output frequency, the dither signal being based on an output of at least one of the plurality of stages.

27. The method of claim **26**, wherein the injecting step comprises using an digital-to-analog converter which converts the output to an analog signal which serves to modulate the control signal.

28. The method of claim **26**, wherein the injecting step comprises capacitively coupling the output to a modulator used to modulate the control signal.

29. The method of claim **26**, wherein the output exhibits a pseudo-random sequence.

* * * * *

EXHIBIT 31
(USP 5,488,627)

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[54] **SPREAD SPECTRUM CLOCK GENERATOR AND ASSOCIATED METHOD**

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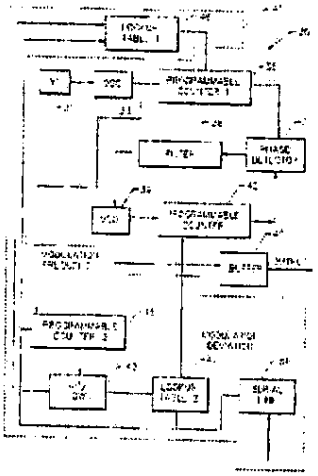
Primary Examiner—Tod R. Swann

Attorney, Agent, or Firm—Bell, Seltzer, Park & Gibson

[57] **ABSTRACT**

A clock circuit includes an oscillator for generating a reference frequency signal, and a spread spectrum clock generator cooperating with the oscillator for generating a spread spectrum clock output signal having a fundamental frequency and reduced amplitude EMI spectral components at harmonics of the fundamental frequency. The spread spectrum clock generator preferably includes a clock pulse generator for generating a series of clock pulses, and a spread spectrum modulator for frequency modulating the clock pulse generator to broaden and flatten amplitudes of EMI spectral components which would otherwise be produced by the clock pulse generator. The spread spectrum modulator frequency modulates the clock pulses with specific profiles of frequency deviation versus the period of the profile. Electronic devices including the spread spectrum clock circuit and associated method are also disclosed.

31 Claims, 7 Drawing Sheets



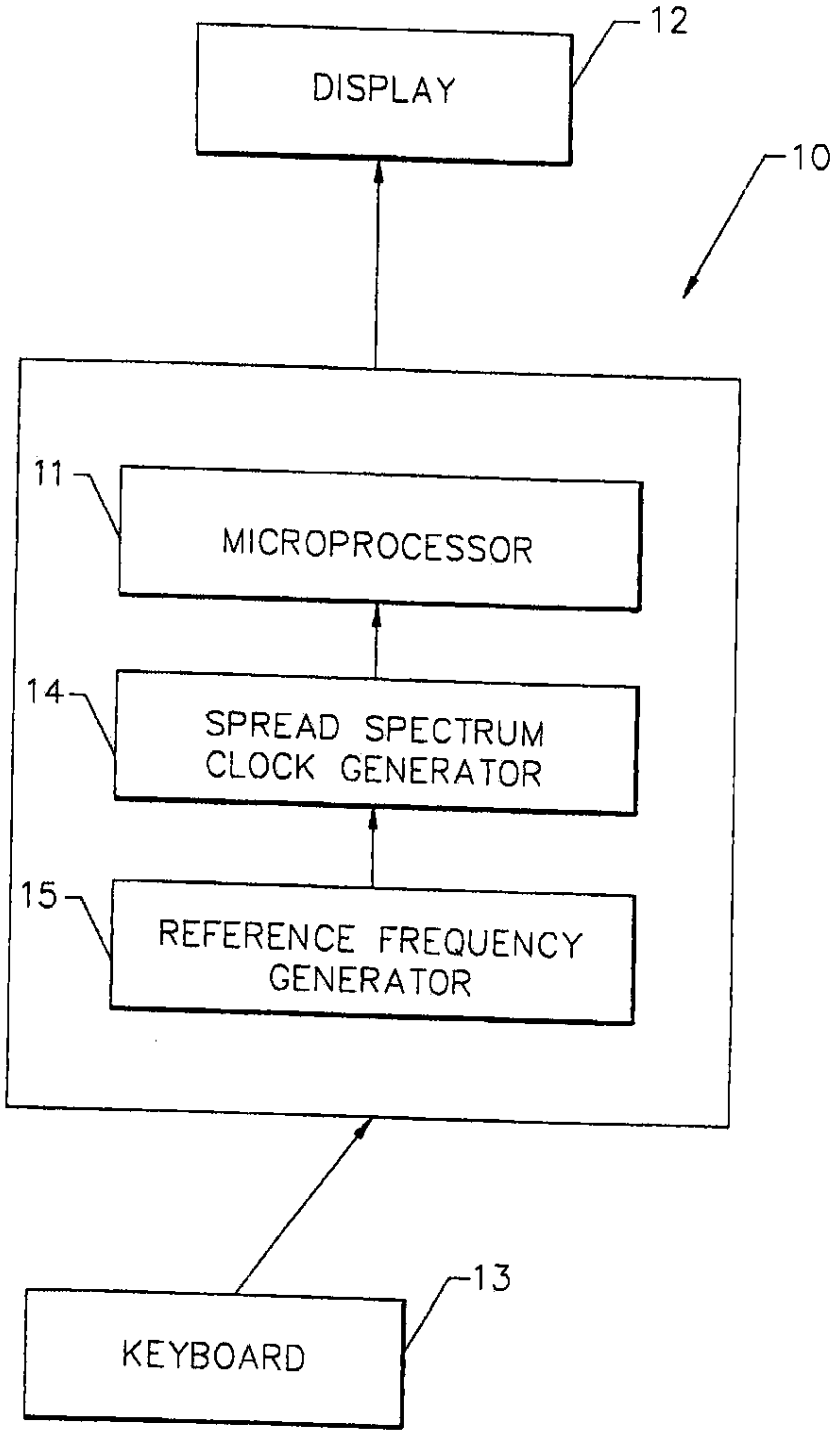

12
DISPLAY
10
11
MICROPROCESSOR
14
SPREAD SPECTRUM
CLOCK GENERATOR
15
REFERENCE FREQUENCY
GENERATOR
13
KEYBOARD

FIG. 1.

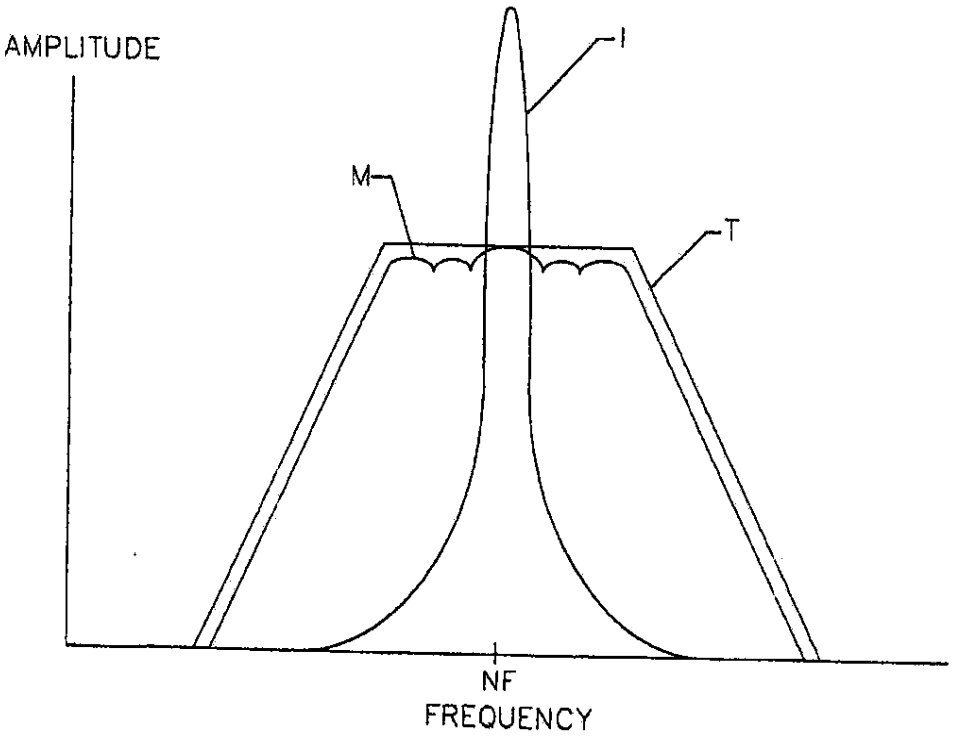

AMPLITUDE
I
M
T
NF
FREQUENCY

FIG. 2.

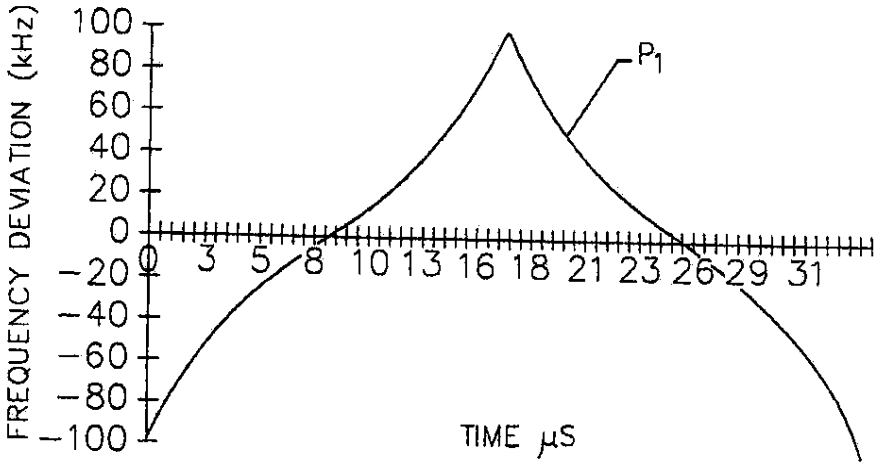

FREQUENCY DEVIATION (kHz)
100
80
60
40
20
0
-20
-40
-60
-80
-100
0 3 5 8 10 13 16 18 21 23 26 29 31
P1
TIME μS

FIG. 3.

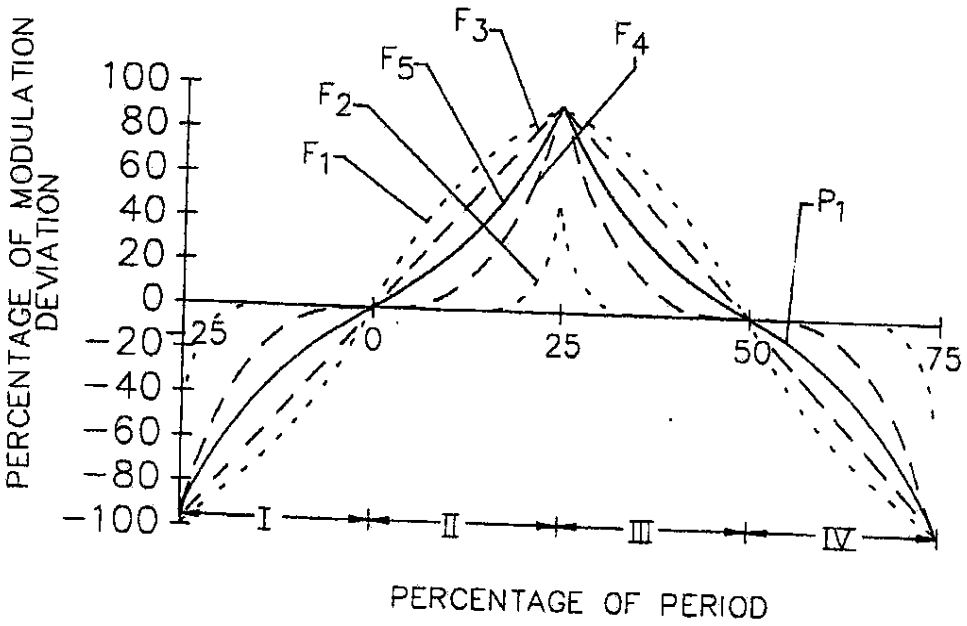

PERCENTAGE OF MODULATION DEVIATION
100
80
60
40
20
0
-20
-40
-60
-80
-100
F1
F2
F3
F4
F5
P1
25
0
25
50
75
I
II
III
IV
PERCENTAGE OF PERIOD

FIG. 4.

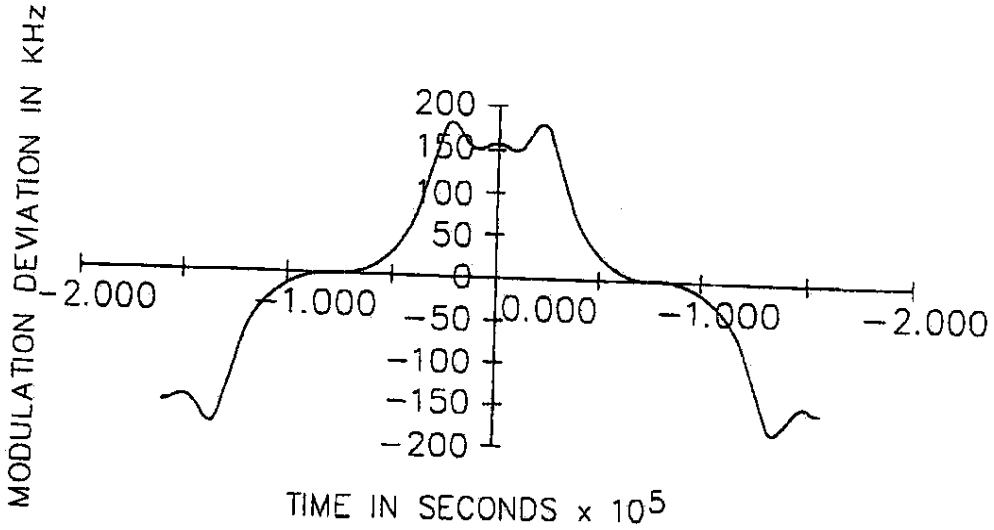

MODULATION DEVIATION IN KHz
200
150
100
50
0
-50
-100
-150
-200
-2.000
-1.000
0.000
-1.000
-2.000
TIME IN SECONDS x 10^5

FIG. 5.

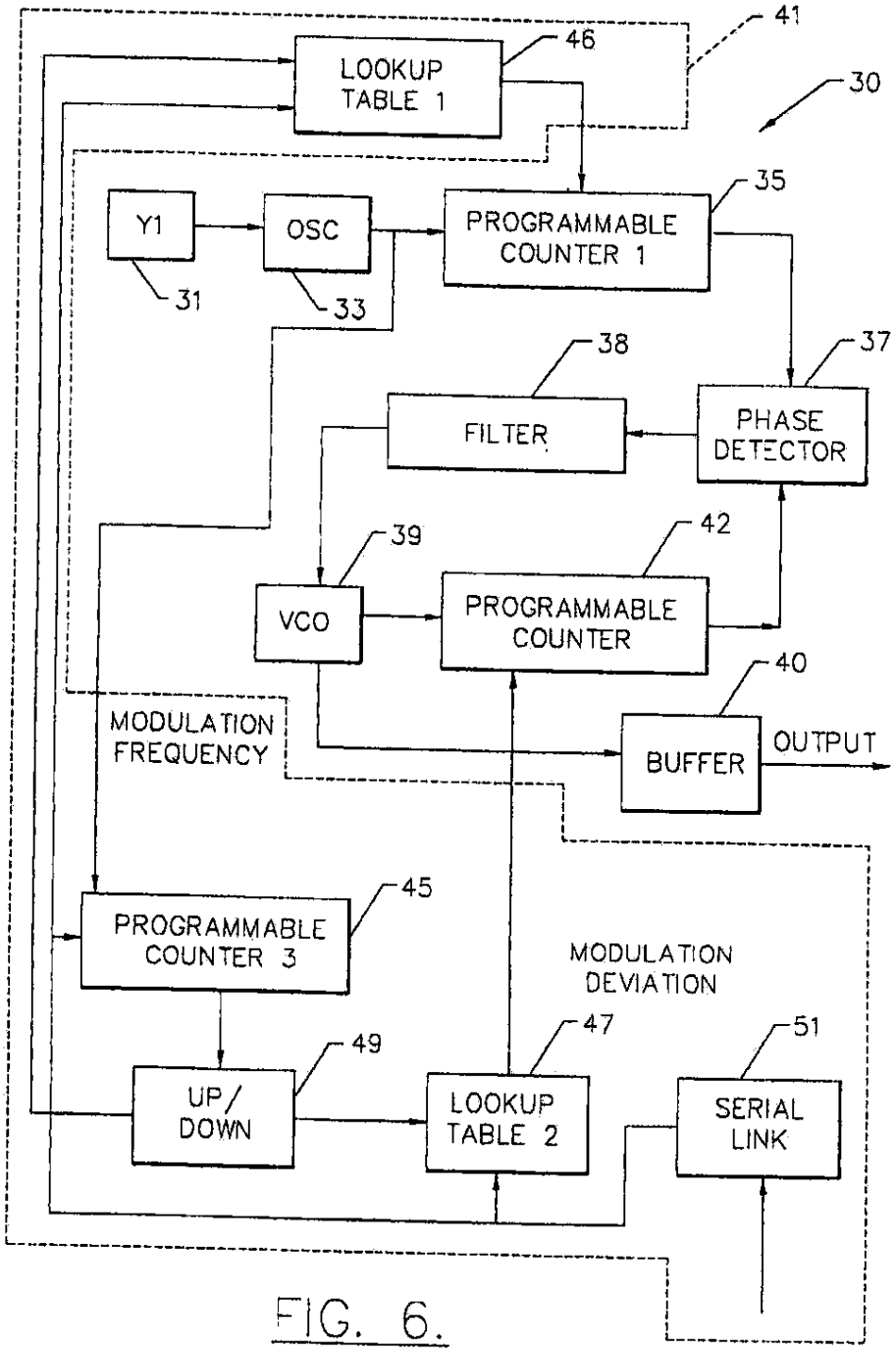

41
46
LOOKUP TABLE 1
30
35
Y1
OSC
PROGRAMMABLE COUNTER 1
31
33
38
37
FILTER
PHASE DETECTOR
39
42
VCO
PROGRAMMABLE COUNTER
40
MODULATION FREQUENCY
BUFFER
OUTPUT
45
PROGRAMMABLE COUNTER 3
MODULATION DEVIATION
49
47
51
UP/ DOWN
LOOKUP TABLE 2
SERIAL LINK

FIG. 6.

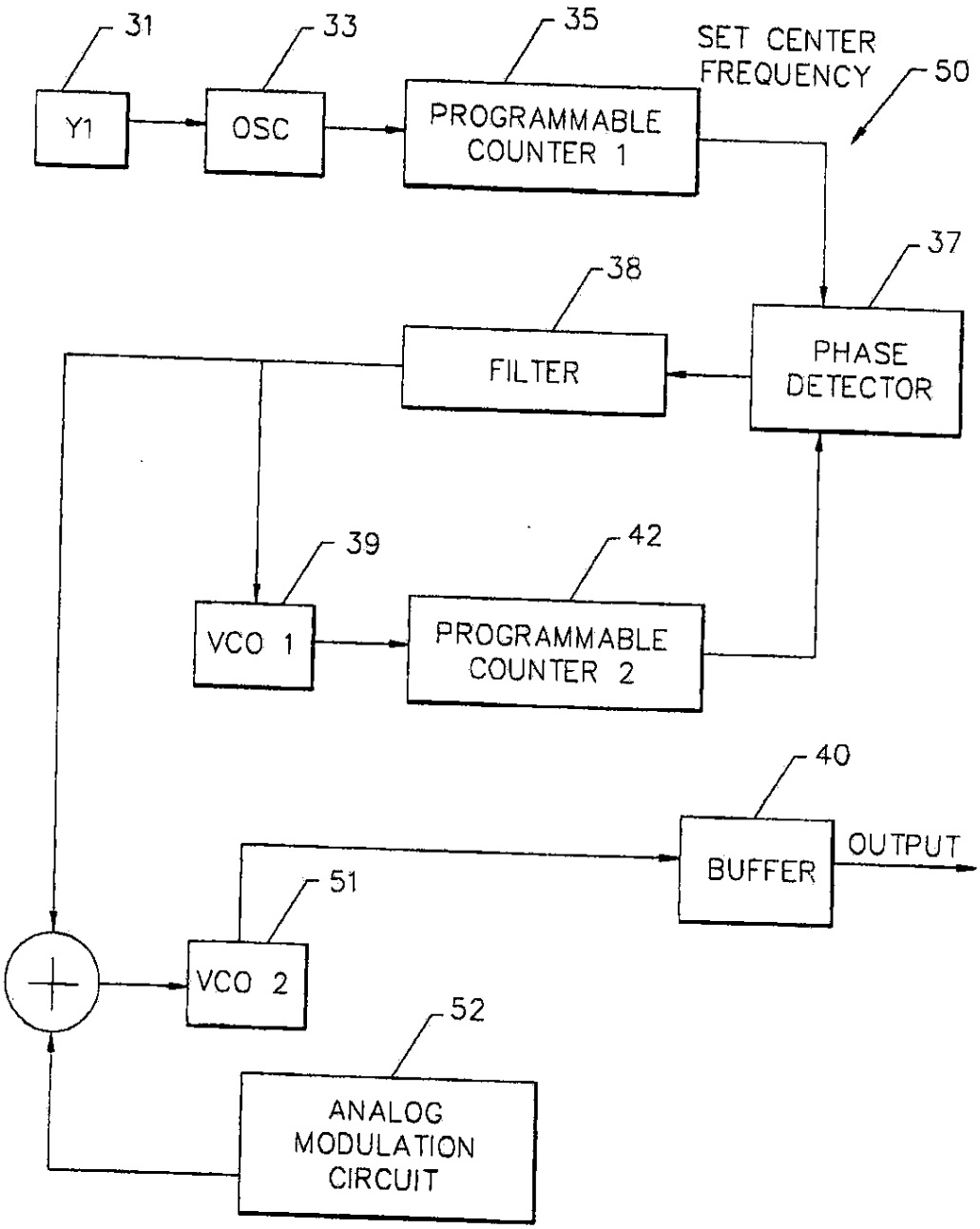

31
33
35
SET CENTER FREQUENCY
50
Y1
OSC
PROGRAMMABLE COUNTER 1
37
38
FILTER
PHASE DETECTOR
39
42
VCO 1
PROGRAMMABLE COUNTER 2
40
BUFFER
OUTPUT
51
VCO 2
52
ANALOG MODULATION CIRCUIT

FIG. 7.

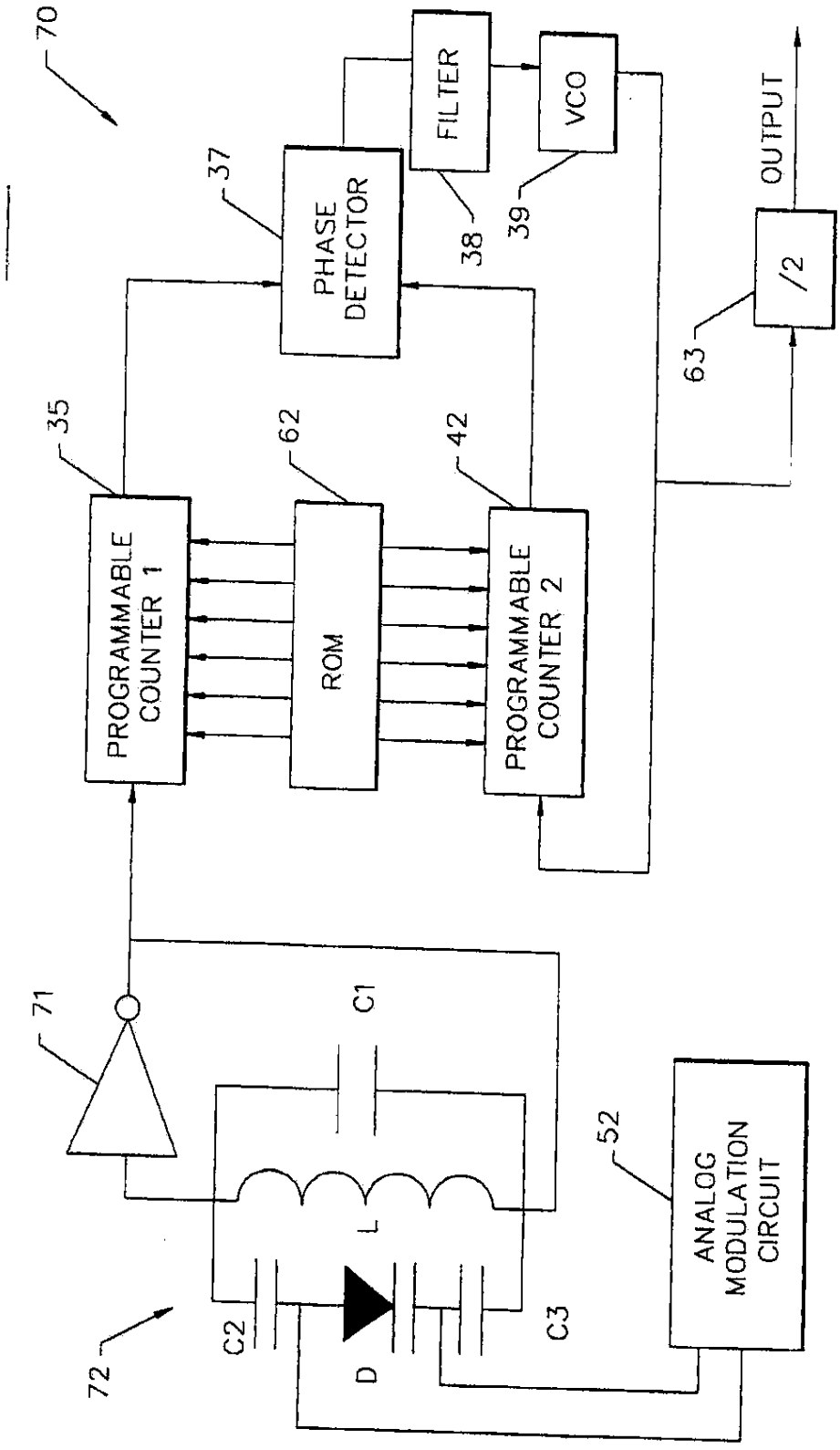

70
FILTER
VCO
OUTPUT
37
PHASE DETECTOR
38
39
/2
63
35
62
42
PROGRAMMABLE COUNTER 1
ROM
PROGRAMMABLE COUNTER 2
71
C1
L
52
ANALOG MODULATION CIRCUIT
C2
D
C3
72

FIG. 8.

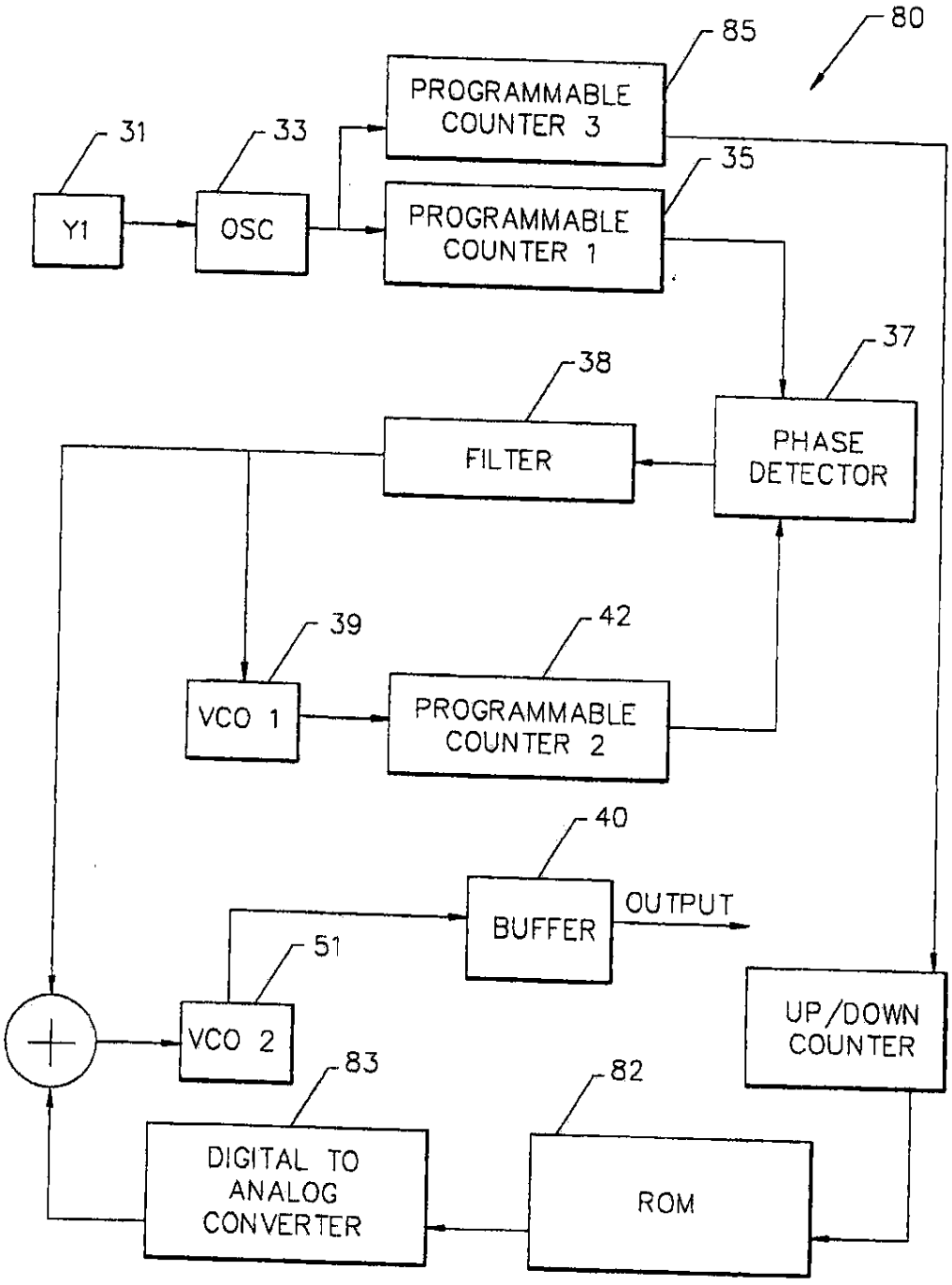

80
85
PROGRAMMABLE COUNTER 3
31
33
35
Y1
OSC
PROGRAMMABLE COUNTER 1
37
38
FILTER
PHASE DETECTOR
39
42
VCO 1
PROGRAMMABLE COUNTER 2
40
BUFFER
OUTPUT
51
VCO 2
UP/DOWN COUNTER
83
82
DIGITAL TO ANALOG CONVERTER
ROM

FIG. 9.

SPREAD SPECTRUM CLOCK GENERATOR AND ASSOCIATED METHOD

FIELD OF THE INVENTION

This invention relates to the field of digital circuits, and more particularly, to a clock circuit having reduced measurable electromagnetic interference (EMI) emissions.

BACKGROUND OF THE INVENTION

Many electronic devices employ microprocessors or other digital circuits which require one or more clock signals for synchronization. A clock signal permits the precise timing of events in the microprocessor, for example. Typical microprocessors may be supervised or synchronized by a free-running oscillator, such as driven by a crystal, an LC-tuned circuit, or an external clock source. Clocking rates up to and beyond 40 MHz are common in personal computers. The parameters of a clock signal are typically specified for a microprocessor and may include minimum and maximum allowable clock frequencies, tolerances on the high and low voltage levels, maximum rise and fall times on the waveform edges, pulse-width tolerance if the waveform is not a square wave, and the timing relationship between clock phases if two-clock phase signals are needed. (See Electronics Engineers' Handbook, by Fink et al., p. 8–111, 1989.)

Unfortunately, high performance, microprocessor-based devices using leading edge, high speed circuits are particularly susceptible to generating and radiating electromagnetic interference (EMI). The spectral components of the EMI emissions typically have peak amplitudes at harmonics of the fundamental frequency of the clock circuit. Accordingly, many regulatory agencies, such as the FCC in the United States, have established testing procedures and maximum allowable emissions for such products. For example, the Commission Electrotechnique Internationale (Comite International Special Des Perturbations Radioelectriques (C.I.S.P.R.)) has guidelines establishing measurement equipment and techniques for determining compliance with regulations. More particularly, for the frequency band of interest to clock circuits, the measured 6 dB bandwidth is a relatively wide 120 KHz.

In order to comply with such government limits on EMI emissions, costly suppression measures or extensive shielding may be required. Other approaches for reducing EMI include careful routing of signal traces on printed circuit boards to minimize loops and other potentially radiating structures. Unfortunately, such an approach often leads to more expensive multilayer circuit boards with internal ground planes. In addition, greater engineering effort must go into reducing EMI emissions. The difficulties caused by EMI emissions are made worse at higher processor and clock speeds.

Power switching circuits also tend to generate EMI emissions due to the rapid switching of high currents and high voltages. EMI noise reduction in such circuits is generally achieved by suppression of the noise source, isolation of the noise coupling path, and filtering or shielding as reported, for example, in Reduction of Power Supply EMI Emission by Switching Frequency Modulation, Lin et al., Virginia Power Electronics Center the VPEC Tenth Annual Power Electronics Seminar, pp. 129–136, Sep. 20–22, 1992. The article further discloses that it is possible to modify the EMI spectrum of the switching power supply circuit to pass regulatory tests by modulating the switching frequency so that side-bands are created thereby smearing the emission spectrum.

In particular the Lin et al. article discloses a switching frequency of 90 KHz that is frequency modulated with a simple sine wave at 400 Hz with the frequency variation selected to be 15 KHz. Improvement of emissions at 90 KHz was reported, which is important because the fundamental frequency EMI determines the amplitude of a required EMI filter for the switching circuit. The article further discloses that from the EMI point of view, a larger frequency variation may be selected and, since there are sideband harmonic frequencies created by the simple sine wave frequency modulation, it is necessary for the switching circuit that these side-bands do not fall within the audible range.

The regulatory requirements for switching power supply circuits fall within a different regulatory category than clock circuits. In particular, as specified by C.I.S.P.R., such switching circuits are only measured for a relatively small 6 dB bandwidth of 9 KHz. Accordingly, approaches described for compliance with such a regulatory test for such a small bandwidth are not adequate to address the difficulties associated with reducing EMI components for high speed digital circuits operating in the tens of megahertz range. The problem associated with lowering measurable EMI emissions is especially difficult where the measured bandwidth is relatively large, such as 120 KHz as in the C.I.S.P.R. regulations which pertain to emissions as generated at typical clock frequencies.

SUMMARY OF THE INVENTION

In view of the foregoing background, it is therefore an object of the present invention to provide a clock circuit and associated method for generating a clock signal, such as for driving a microprocessor or other digital circuit at relatively high frequencies, while reducing the spectral amplitude of EMI components as measured over a relatively large bandwidth.

This and other objects, features, and advantages of the present invention are provided by a clock circuit including an oscillator for generating a reference frequency signal, and spread spectrum clock generating means for generating a spread spectrum clock output signal having a fundamental or center frequency and reduced amplitude EMI spectral components at harmonics of the fundamental frequency. More particularly, the spread spectrum clock generating means preferably includes clock pulse generating means for generating a series of clock pulses, and spread spectrum modulating means for modulating the clock pulse generating means to broaden and flatten amplitudes of EMI spectral components which would otherwise be produced by the clock pulse generating means.

The clock pulse generating means, if unmodulated, would typically produce generally rectangular or trapezoidal electrical pulses which, in turn, would generate corresponding impulse-shaped EMI spectral components at harmonics of the fundamental frequency. The spread spectrum modulating means reduces the peak amplitude of the EMI spectral components that would otherwise be produced. Accordingly, expensive shielding or other EMI suppression techniques may be reduced or eliminated in an electronic device including the spread spectrum clock generating circuit of the present invention. As would be readily understood by those skilled in the art, the spread spectrum clock generating circuit may find wide application in a number of electronic devices, particularly those including a microprocessor or microcontroller, such as a personal computer.

The spread spectrum modulating means preferably includes frequency modulating means for frequency modulating the clock pulse generating means. The frequency modulating means, in turn, preferably includes profile modulating means for frequency modulating the clock pulse generating means with a periodic waveform having a predetermined period and a predetermined frequency deviation profile as a function of the predetermined period. Several preferred or effective ranges for such modulating periodic waveforms are described later herein. In general, the preferred waveforms are more complicated than a simple sine wave in order to thereby reduce the spectral peak of EMI components by broadening and flattening their shape.

The clock pulse generating means preferably includes a phase locked loop as is commonly used in a conventional clock generating circuit. The frequency modulation means may be implemented by several types of circuits including an analog modulating generator or a programmable modulating generator which can produce a predetermined profile for the frequency deviation. In addition, the frequency modulating means is preferably capable of modulating the clock pulse generating means with a periodic waveform having a period of less than about 500 microseconds, that is, the frequency of modulation is desirably greater than about 2 KHz.

A method according to the invention is for generating a clock output signal with reduced amplitude EMI spectral components. The method includes the step of generating a spread spectrum clock output signal having a fundamental frequency and reduced amplitude EMI spectral components at harmonics of the fundamental frequency. The step of generating a spread spectrum clock output signal preferably includes the steps of generating a series of clock pulses, and spread spectrum modulating the series of clock pulses to broaden and flatten amplitudes of EMI spectral components which would otherwise be produced along with the series of clock pulses. The step of spread spectrum modulating the series of clock pulses preferably includes the step of frequency modulating the clock pulses with a periodic waveform having a predetermined period and a predetermined frequency deviation profile as a function of the predetermined period.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** is a schematic block diagram of a personal computer including a spread spectrum clock generating circuit in accordance with the invention.

FIG. **2** is a graph illustrating a reduction of peak spectral amplitude of a harmonic of the clock fundamental frequency produced by the spread spectrum clock generating circuit in accordance with the present invention.

FIG. **3** is a graph illustrating an embodiment of a desired modulation profile for producing a spread spectrum modulated clock signal in accordance with the present invention.

FIG. **4** is a graph illustrating several modulation profile ranges for producing a spread spectrum modulated clock output signal in accordance with the present invention.

FIG. **5** is a graph illustrating yet another embodiment of a desired modulation profile for producing a spread spectrum modulated clock output signal in accordance with the present invention.

FIG. **6** is a schematic block diagram illustrating a first circuit embodiment for producing the spread spectrum modulated clock output signal in accordance with the present invention.

FIG. **7** is a schematic block diagram illustrating a second circuit embodiment for producing the spread spectrum modulated clock output signal in accordance with the present invention.

FIG. **8** is a schematic block diagram illustrating a third circuit embodiment for producing the spread spectrum modulated clock output signal in accordance with the present invention.

FIG. **9** is a schematic block diagram illustrating a fourth circuit embodiment for producing the spread spectrum modulated clock output signal in accordance with the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

The present invention will now be described more fully hereinafter with reference to the accompanying drawings, in which preferred embodiments of the invention are shown. This invention may, however, be embodied in many different forms and should not be construed as limited to the embodiments set forth herein. Rather, applicants provide these embodiments so that this disclosure will be thorough and complete, and will fully convey the scope of the invention to those skilled in the art. Like numbers refer to like elements throughout.

Referring first to FIGS. **1** through **5**, an electronic device incorporating the spread spectrum clock generating circuit and its basic operation are first explained. As shown in FIG. **1**, an electronic device, such as the schematically illustrated personal computer **10**, may benefit by having reduced measurable EMI spectral component emissions provided by the spread spectrum clock generator **14** (SSCG) according to the invention. A reference frequency generator **15**, such as a piezoelectric crystal driven at its resonant frequency by a suitable driver or oscillator circuit, provides a reference frequency for the SSCG **14**. The illustrated personal computer **10** also includes a display **12** and a keyboard **13**.

As would be readily understood by those of skill in the art, a number of electronic devices incorporating microprocessors or other digital circuits requiring a clock signal for synchronization may also desirably incorporate the SSCG **14**. For example, computer printers may also desirably include the SSCG **14**.

The SSCG **14** generates the spread spectrum output clock signal by frequency modulating a typical clock signal including a series of trapezoidal or generally rectangularly-shaped electrical clock pulses. The modulation reduces the spectral amplitude of the EMI components at each harmonic of the clock when compared to the spectrum of the same clocking signal without modulation. FIG. **2** is a schematic representation of this effect where the spectral amplitude versus frequency at a harmonic (NF) is indicated by the plot labelled M. As also shown, the spectrum at the same harmonic of a standard clock signal is given as an impulse function labelled I. The spectrum of the SSCG output clock signal at the same harmonic ideally assumes a trapezoidal shape as illustrated by the plot labelled T.

Although in general the spectral "width" of the spread spectrum output clock signal at a harmonic is greater than the width of the standard non-modulated clock signal, the maximum amplitude for the harmonic is reduced. In an actual implementation, the amplitude of the spread spectrum modulated harmonic will not be uniform, but will exhibit some peaking near the center frequency and at the edges as illustrated by the plot M.

In order to minimize the amplitude of the signal for all frequencies, the modulation of the standard clock signal must be uniquely specified. Accordingly, the SSCG 14 includes profile modulating means for frequency modulating the clock pulse generating means with a periodic waveform having a predetermined period and a predetermined frequency deviation profile as a function of the predetermined period. The modulation profiles described herein produce relatively optimized flat spectral amplitudes at each harmonic. In general, the preferred profiles are more complicated than a simple sine wave in order to thereby reduce the measurable spectral peaks of the EMI components. Stated in other terms, the present invention converts narrow band harmonics into broadband signals that significantly reduce the measured emissions for the FCC and other regulatory bodies worldwide. These emission reductions may permit corresponding cost reductions of about $20 or more per product, as compared to the cost of conventional measures to suppress or shield EMI emissions.

FIG. 3 illustrates a typical profile of the frequency deviation versus time as may be used within the SSCG 14. The maximum deviation illustrated is 100 KHz. This maximum frequency deviation is desirably programmable via a serial link with an upper limit of the maximum deviation being preferably about 250 KHz for typical current applications. However, depending on the application, the maximum deviation may be much greater than 250 KHz as would be readily understood by those skilled in the art. As would be also readily understood by those skilled in the art, a standard, non-modulated clock signal may be obtained by programming the maximum deviation to 0.

The frequency of the signal modulating the profile shown in FIG. 3 is 30 KHz. Significant peak amplitude reduction may also be achieved where the frequency is above 2 KHz, that is, where the period of the modulating waveform or profile is less than about 500 μsec. This frequency is also desirably programmable via the serial link or may be fixed dependent on the application. The modulating profile illustrated is a linear combination of a standard triangular wave and its cubic. The values of the profile are given in Table 1 below for maximum frequency deviations of 100 KHz and 200 KHz. For maximum deviations other than 100 KHz or 200 KHz, values for the modulating signal can be obtained by simply scaling the values found in Table 1 as would be readily appreciated by those skilled in the art.

TABLE 1

Frequency deviation values for maximum frequency deviations of 100 KHz and 200 KHz with a modulating frequency of 30 KHz.

Time (μS)	Deviation (KHz) 100 KHz Maximum	Deviation (KHz) 200 KHz Maximum
0	−100	−200
0.520833	−88.4615	−176.923
1.041667	−76.9231	−153.846
1.5625	−67.3077	−134.615
2.083333	−59.6154	−119.231
2.604167	−51.9231	−103.846
3.125	−44.2308	−88.4615
3.645833	−38.4615	−76.9231
4.166667	−32.6923	−65.3846
4.6875	−26.9231	−53.8462
5.208333	−23.0769	−46.1538
5.729167	−19.2308	−38.4615
6.25	−13.4615	−26.9231
6.770833	−9.61538	−19.2308
7.291667	−7.69231	−15.3846
7.8125	−3.84615	−7.69231
8.333333	0	0
8.854167	3.846154	7.692308
9.375	7.692308	15.38462
9.895833	9.615385	19.23077
10.41667	13.46154	26.92308
10.9375	19.23077	38.46154
11.45833	23.07692	46.15385
11.97917	26.92308	53.84615
12.5	32.69231	65.38462
13.02083	38.46154	76.92308
13.54167	44.23077	88.46154
14.0625	51.92308	103.8462
14.58333	59.61538	119.2308
15.10417	67.30769	134.6154
15.625	76.92308	153.8462
16.14583	88.46154	176.9231
16.66667	98.07692	196.1538
17.1875	88.46154	176.9231
17.70833	76.92308	153.8462
18.22917	67.30769	134.6154
18.75	59.61538	119.2308
19.27083	51.92308	103.8462
19.79167	44.23077	88.46154
20.3125	38.46154	76.92308
20.83333	32.69231	65.38462
21.35417	26.92308	53.84615
21.875	23.07692	46.15385
22.39583	19.23077	38.46154
22.91667	13.46154	26.92308
23.4375	9.615385	19.23077
23.95833	7.692308	15.38462
24.47917	3.846154	7.692308
25	0	0
25.52083	−3.84615	−7.69231
26.04167	−7.69231	−15.3846
26.5625	−9.61538	−19.2308
27.08333	−13.4615	−26.9231
27.60417	−19.2308	−38.4615
28.125	−23.0769	−46.1538
28.64583	−26.9231	−53.8462
29.16667	−32.6923	−65.3846
29.6875	−38.4615	−76.9231
30.20833	−44.2308	−88.4615
30.72917	−51.9231	−103.846
31.25	−59.6154	−119.231
31.77083	−67.3077	−134.615
32.29167	−76.9231	−153.846
32.8125	−88.4615	−176.923
33.33333	−100	−200

Referring now more particularly to FIG. 4, several preferred ranges of profiles of frequency deviation are illustrated. In particular, the profiles are expressed as a percentage of frequency deviation versus a percentage of the period (% Period) of the periodic waveform. The outermost range or envelope is illustrated by the dotted lines labelled F_1, F_2 in the second quadrant II, that is, between 0% and 25% of the period. Straightforward symmetry defines the boundaries in the other indicated quadrants as described. Accordingly, those of skill in the art may readily implement and scale the ranges for a desired application.

The dotted lines may be defined mathematically by predetermined upper and lower bounds for the second quadrant II. The upper bound F_1 is defined by

$$100\%\left[-1+\sqrt{-\left(\frac{\%\ \text{Period}}{25}\right)^2+4\left(\frac{\%\ \text{Period}}{25}\right)+.973}\right],$$

while the lower bound F_2 is defined by

$$50\% \left[\frac{\% \text{ Period}}{25} \right]^{10}.$$

As would be readily understood by those skilled in the art, the boundaries for the other quadrants defined by F_1 and F_2 as follows:

Quadrant I (−25% to 0% Period):

Lower bound=$-F_1$(−% Period),

Upper bound=$-F_2$(−% Period);

Quadrant III (25% to 50% Period):

Lower bound=F_2(50−% Period),

Upper bound=F_1(50−% Period); and

Quadrant IV (50% to 75% Period):

Lower bound=$-F_1$(% Period−50)

Upper bound=$-F_2$(% Period−50).

A more preferred profile range is indicated by the dashed lines indicated in FIG. 4. In quadrant II, this profile is defined by an upper bound F_3 and a lower bound F_4. The upper bound F_3 is defined in quadrant II by

$$100\% \left[\frac{\% \text{ Period}}{25} \right],$$

and the lower bound is defined in quadrant II by

$$100\% \left[\frac{\% \text{ Period}}{25} \right]^{3}.$$

Accordingly, the other boundaries are given by:

Quadrant I (−25% to 0% Period):

Lower bound=$-F_3$(−% Period),

Upper bound=$-F_4$(−% Period);

Quadrant III (25% to 50% Period):

Lower bound=F_4(50−% Period),

Upper bound=F_3(50−% Period); and

Quadrant IV (50% to 75% Period):

Lower bound=$-F_3$(% Period−50)

Upper bound=$-F_4$(% Period−50).

As also shown in FIG. 3, the solid line P_1 of FIG. 4 illustrates the linear combination of a triangular waveform and its cubic. More particularly, this profile is defined in quadrant II by F_5 which is equal to

100% [0.45 (% Period/25)^3+0.55(% Period/25)].

Accordingly, the solid line is defined in the other quadrants as follows:

Quadrant I (−25% to 0% Period): $-F_5$(−% Period);

Quadrant III (25% to 50% Period): F_5(50−% Period); and

Quadrant IV (50% to 75% Period): $-F_5$(% Period−50)

FIG. 5 illustrates yet another embodiment of a profile for the frequency deviation modulation which may be scaled to fit within the outermost profile defined by F_1 and F_2 as would be readily appreciated by those of skill in the art.

The periodic waveforms defined by F_2, F_4, F_5, and those less than F_3 illustrated in FIG. 4, and the waveforms of FIGS. 3 and 5 also may be described in terms of a function having predetermined concavity in each quadrant. More particularly, in view of the generally symmetric nature of a periodic waveform, the waveform may be defined in Quadrant I by a predetermined function which is generally negative, increasing and which defines a concave downward shape; in Quadrant II by a function which is generally positive, increasing and concave upward; in Quadrant III by a function which is generally positive, decreasing and concave upward; and, in Quadrant IV by a function which is generally negative, decreasing and concave downward.

Referring now additionally to FIGS. 6 through 9, preferred circuit embodiments for the SSCG 14 are described. The block diagrams are similar to several conventional phase locked loop (PLL) frequency synthesizer chips; however, a modulation section is added which includes a programmable modulation generator in several embodiments, or an analog modulation generator in other embodiments. The modulation is fed into a voltage controlled oscillator (VCO) or oscillator tank circuit to give the desired modulation index.

The SSCG 14 may desirably be programmable via an I^2C serial bus or select lines to allow variation of the center frequency, maximum frequency deviation and modulation frequency. A single +5V supply, minimal external circuitry and a crystal will produce a TTL and CMOS compatible output with controlled rise and fall times. In addition, all inputs are standard TTL compatible.

The following electrical characteristics (TABLE 2) and switching characteristics (TABLE 3) given below are also desirably met by the embodiments of the SSCG 14 to be compatible with conventional digital circuits or microprocessors clock input requirements.

TABLE 2

Electrical Characteristics

Characteristic	Symbol	Min	Typ	Max	Units
Load Capacitance	C_L	—	30	50	pF
Quiescent Supply Current	I_{CC}	—	—	45	mA

TABLE 3

Switching Characteristics

Characteristic	Symbol	Min	Typ	Max	Units
Output Rise (0.8 to 2.0V) and Fall Time (2.0V to 0.8V)	t_{TLH}, t_{THL}	1	2	3	ns
Maximum Frequency Deviation*	ΔF_{max}	0	100	250	KHz
Modulating Frequency*	F_{mod}	15	30	50	KHz

*Programmable via serial link

Referring first to the schematic block diagram of FIG. 6, a phase locked loop (PLL) implementation of the SSCG indicated generally by reference numeral 30 according to the invention is first explained. Y1 31 is a piezoelectric crystal used with an oscillator circuit 33 to generate a stable clock pulse train or unmodulated clock signal. A first programmable counter 35 divides the unmodulated clock signal by an integer number (M). A voltage controlled oscillator 39 (VCO) generates an output clock signal, output from a buffer 40, that is proportional to the input voltage from the phase detector 37 and filter 38.

A second programmable counter 42 divides the signal from the VCO 39 by an integer number (N). The phase detector 37 and filter 38 generate an analog signal that is proportional to the error in phase between first and second programmable counters 35, 42, respectively. Accordingly, the clock signal output from the buffer 40 is equal to the oscillator frequency times N/M. As would be readily understood by those skilled in the art, when N and M are constant, this circuit operates as a standard (PLL) circuit.

The spread spectrum modulation according to the invention is introduced in this embodiment by the spread spec-

trum modulation means **41** which changes M and N as a function of time. A third programmable counter **45** divides the signal from the oscillator **33** by an integer number (I) which sets the rate that M and N change, or modulation frequency. First and second look-up tables **46**, **47**, respectively, are the stabilized values for M and N which modulate the output clock signal frequency. An up/down counter **49** is used to index successive entries in the look-up tables. A serial link **51**, which is not required for operation, may be used to program different values in the programmable counters or look-up tables to modify modulation characteristics.

Referring now to FIG. **7**, a second embodiment of the SSCG generally designated by reference numeral **50** is described. Elements previously discussed are indicated by like numerals and need not be described further. In this embodiment, the spread spectrum modulation is introduced by a second VCO **51** and an analog circuit **52**. The second VCO creates a clock signal identical to the first VCO **39** when no modulation is present. The second VCO **51** responds to the analog modulation to thereby create the spread spectrum clock output signal.

An embodiment of the analog modulation circuit **52** may include an oscillator to generate the modulation frequency, an integrator to generate a triangle wave function (r(t)), a log anti-log amplifier (alog(3log(r(t)))), and an adder to generate a modulation profile of 0.55r(t)+0.45(alog(3log(r(t)))) as shown by plot P1 in FIG. **3**. An alternative of the illustrated embodiment would be to add the modulation to the first VCO **39** input, as would be readily understood by those skilled in the art.

FIG. **8** illustrates yet another embodiment of the SSCG **70** according to the invention. An inverting amplifier **71** with an inductor L and a capacitor C1 forms a simple oscillator circuit **72** to generate a stable clock signal. Capacitors C1, C3 and varactor diode D are used to change the effective capacitance of C1 which will thereby change the oscillator circuit frequency. The varactor diode changes its junction capacitance proportional to the voltage applied thereacross. The analog modulation circuit **52** is preferably the same as discussed above with reference to FIG. **7**. The output of the inverting amplifier **71** is a spread spectrum clock signal that can be used directly or that may also be scaled to any other frequency by adding a PLL circuit as illustrated. A first programmable counter **35** divides the oscillator signal by an integer number (M), while the VCO **39** generates a clock signal proportional to the input voltage from the phase detector **37** and filter **38**. The second programmable counter **42** divides the VCO signal by an integer number (N). The phase detector **37** and filter **38** output an analog signal that is proportional to the error in phase between the first and second programmable counters **35**, **42**, respectively. The divide by 2 circuit **63** may be used to generate a clock output signal having a 50% duty cycle as would be readily understood by those skilled in the art.

Still another embodiment of an SSCG **80** is illustrated in FIG. **9** and is described as follows. The illustrated embodiment is similar to that shown in FIG. **7**, but the modulation is created by a ROM **82** having stored therein modulation amplitude values that are fed into a digital to analog convertor **83** (DAC). An up/down counter **84** is used to index the values in the ROM **82** while a third programmable counter **85** sets the modulation frequency.

Another embodiment of an SSCG may include a direct digital synthesizer. A crystal and oscillator circuit generate a stable or unmodulated clock signal. As would be readily understood by those skilled in the art, the direct digital synthesizer (DDS) is an accumulator with a phase constant added to the accumulator every clock cycle and which in conjunction with a read only memory (ROM) produces a square wave from the Most Significant Bit (MSB). The frequency of an output square wave can be modulated by changing the phase constant as a function of time. This is preferably accomplished using a programmable up/down counter, and a look-up table similar to those illustrated in FIG. **6**. AVCO generates a clock signal proportional to the input voltage from a phase detector and filter. A programmable counter divides the VCO signal by an integer number (N). The phase detector and filter also output an analog signal that is proportional to the error in phase between programmable counter and the DDS circuit. The spread spectrum modulated clock signal may be output from a divider or buffer.

As would be readily understood by those skilled in the art, in an implementation of any of the circuits described herein in a physical package, several such spread spectrum clock generating circuits (SSCG's) may be found in the same DIP. In addition, a standard phase locked loop frequency synthesizer may also be located in the same DIP to provide standard clock signals, if desired. The SSCG may also be included internally with a microprocessor or any other digital or analog circuit.

A method according to the invention is for generating the spread spectrum clock output signal. The method preferably includes the steps of: generating a series of clock pulses, and spread spectrum modulating the series of clock pulses to broaden and flatten amplitudes of EMI spectral components which would otherwise be produced along with the series of clock pulses. The step of spread spectrum modulating the series of clock pulses preferably includes the step of frequency modulating the clock pulses with a periodic waveform having a predetermined period and a predetermined frequency deviation profile as a function of the predetermined period, as described in greater detail above.

The step of frequency modulating the series of clock pulses preferably includes modulating the series of clock pulses with a periodic waveform having a period of less than about 500 microseconds. The spread spectrum modulation according to the invention causes varying of the clock fundamental frequency, which in turn, may result in a 5–10% reduction in average clock frequency compared to the fixed frequency of a conventional clock circuit. However, for a significant number of applications, the SSCG according to the invention significantly reduces measured EMI emissions without adversely affecting overall electronic device performance.

Many modifications and other embodiments of the invention will come to the mind of one skilled in the art having the benefit of the teachings presented in the foregoing descriptions and the associated drawings. Therefore, it is to be understood that the invention is not to be limited to the specific embodiments disclosed, and that modifications and embodiments are intended to be included within the scope of the appended claims.

That which is claimed is:

1. A clock circuit for generating a clock output signal with reduced amplitude electromagnetic interference (EMI) spectral components, said clock circuit comprising:

oscillator means for generating a reference frequency signal; and

spread spectrum clock generating means cooperating with said oscillator means for generating a spread spectrum clock output signal having a fundamental frequency and reduced amplitude EMI spectral components at

harmonics of the fundamental frequency, said spread spectrum clock generating means comprising

clock pulse generating means for generating a series of generally rectangularly shaped electrical clock pulses; and

spread spectrum modulating means cooperating with said clock pulse generating means for modulating same to broaden and flatten amplitudes of impulse-shaped EMI spectral components which would otherwise be produced by said clock pulse generating means, said spread spectrum modulating means comprising frequency modulating means for frequency modulating said clock pulse generating means, said frequency modulating means comprising profile modulating means for modulating the clock pulse generating means with a periodic waveform having a percentage of frequency deviation profile as a function of percentage of a period (% Period) of the periodic waveform within an envelope defined by predetermined upper and lower bounds, wherein said predetermined upper bound for a second quadrant is defined by F_3 which is equal to

$$100\%\left(\frac{\%\ \text{Period}}{25}\right),$$

wherein said predetermined lower bound is defined by F_4 which is equal to

$$100\%\left(\frac{\%\ \text{Period}}{25}\right)^3;$$

wherein for a first quadrant between −25% to 0% Period the lower bound is equal to $-F_3$(−% Period) and the upper bound is equal to $-F_4$(−% Period); wherein for a third quadrant between 25% to 50% Period the lower bound is equal to F_4(50−% Period), and the upper bound is equal to F_3(50−% Period); and wherein for a fourth quadrant the lower bound is equal to $-F_3$(% Period−50) and the upper bound is equal to $-F_4$(% Period−50).

2. A clock circuit according to claim 1 wherein said profile modulating means further comprises means for modulating said clock pulse generating means with a periodic waveform having a percentage of frequency deviation profile as a function of percentage of a period (% Period) of the periodic waveform defined in a second quadrant by F_5 which is equal to

$100\%(0.45(\%\ \text{Period}/25)^3+0.55(\%\ \text{Period}/25))$;

wherein for a first quadrant between −25% to 0% Period the profile is equal to $-F_5$(−% Period); wherein for a third quadrant between 25% to 50% Period the profile is equal to F_5(50−% Period); and wherein for a fourth quadrant the profile is equal to $-F_5$(% Period−50).

3. A clock circuit according to claim 1 wherein said clock pulse generating means comprises a phase locked loop.

4. A clock circuit according to claim 3 wherein said frequency modulating means comprises an analog modulating generator operatively connected to said phase locked loop.

5. A clock circuit according to claim 3 wherein said frequency modulating means comprises a programmable modulating generator operatively connected to said phase locked loop.

6. A clock circuit according to claim 1 wherein said frequency modulating means comprises means for modulating said clock pulse generating means with a periodic waveform having a period of less than about 500 microseconds.

7. A clock circuit according to claim 1 wherein said oscillator means comprises a crystal having a predetermined resonant frequency.

8. A clock circuit for generating a clock output signal with reduced amplitude electromagnetic interference (EMI) spectral components, said clock circuit comprising:

oscillator means for generating a reference frequency signal; and

spread spectrum clock generating means cooperating with said oscillator means for generating a spread spectrum clock output signal having a fundamental frequency and reduced amplitude EMI spectral components at harmonics of the fundamental frequency, said spread spectrum clock generating means comprising

clock pulse generating means for generating a series of clock pulses, and

profile modulating means for frequency modulating the clock pulse generating means with a periodic waveform having a percentage of frequency deviation profile as a function of percentage of a period (% Period) of the periodic waveform within an envelope defined by predetermined upper and lower bounds, said predetermined upper bound for a second quadrant is defined by F_3 which is equal to

$$100\%\left(\frac{\%\ \text{Period}}{25}\right),$$

and said predetermined lower bound is defined by F_4 which is equal to

$$100\%\left(\frac{\%\ \text{Period}}{25}\right)^3;$$

for a first quadrant between −25% to 0% Period the lower bound is equal to $-F_3$(−% Period) and the upper bound is equal to $-F_4$(−% Period); for a third quadrant between 25% to 50% Period the lower bound is equal to F_4(50−% Period), and the upper bound is equal to F_3(50−% Period); and for a fourth quadrant the lower bound is equal to $-F_3$(% Period−50) and the upper bound is equal to $-F_4$(% Period−50).

9. A clock circuit according to claim 8 wherein said profile modulating means includes means for modulating said clock pulse generating means with a periodic waveform having a percentage of frequency deviation profile as a function of percentage of a period (% Period) of the periodic waveform defined in a second quadrant by F_5 which is equal to

$100\%(0.45(\%\ \text{Period}/25)^3+0.55(\%\ \text{Period}/25))$;

wherein for a first quadrant between −25% to 0% Period the profile is equal to $-F_5$(−% Period); wherein for a third quadrant between 25% to 50% Period the profile is equal to F_5(50−% Period); and wherein for a fourth quadrant the profile is equal to $-F_5$(% Period−50).

10. A clock circuit according to claim 8 wherein said clock pulse generating means comprises a phase locked loop.

11. A clock circuit according to claim 10 wherein said profile modulating means comprises an analog modulating generator operatively connected to said phase locked loop.

12. A clock circuit according to claim 10 wherein said profile modulating means comprises a programmable modulating generator operatively connected to said phase locked loop.

13. A clock circuit according to claim 8 wherein said profile modulating means comprises means for modulating said clock pulse generating means with the periodic waveform having a period of less than about 500 microseconds.

14. A clock circuit according to claim 8 wherein said oscillator means comprises a crystal having a predetermined resonant frequency.

15. A clock circuit for generating a clock output signal with reduced amplitude electromagnetic interference (EMI) spectral components, said clock circuit comprising:

clock pulse generating means for generating a series of clock pulses; and

spread spectrum modulating means cooperating with said clock pulse generating means for modulating same to broaden and flatten amplitudes of EMI spectral components which would otherwise be produced by said clock pulse generating means, said spread spectrum modulating means comprising frequency modulating means for frequency modulating said clock pulse generating means, said frequency modulating means comprising profile modulating means for modulating the clock pulse generating means with a periodic waveform having a percentage of frequency deviation profile as a function of percentage of a period (% Period) of the periodic waveform within an envelope defined by predetermined upper and lower bounds, wherein said predetermined upper bound for a second quadrant is defined by F_3 which is equal to

$$100\% \left(\frac{\% \text{ Period}}{25} \right).$$

wherein said predetermined lower bound is defined by F_4 which is equal to

$$100\% \left(\frac{\% \text{ Period}}{25} \right)^3;$$

wherein for a first quadrant between −25% to 0% Period the lower bound is equal to $-F_3$(−% Period) and the upper bound is equal to $-F_4$(−% Period); wherein for a third quadrant between 25% to 50% Period the lower bound is equal to F_4(50−% Period), and the upper bound is equal to F_3(50−% Period); and wherein for a fourth quadrant the lower bound is equal to $-F_3$(% Period−50) and the upper bound is equal to $-F_4$(% Period−50).

16. A clock circuit according to claim 15 wherein said profile modulating means further comprises means for modulating said clock pulse generating means with a periodic waveform having a percentage of frequency deviation profile as a function of percentage of a period (% Period) of the periodic waveform defined in a second quadrant by F_5 which is equal to

$$100\%(0.45(\%\ \text{Period}/25)^3+0.55(\%\ \text{Period}/25));$$

wherein for a first quadrant between −25% to 0% Period the profile is equal to $-F_5$(−% Period); wherein for a third quadrant between 25% to 50% Period the profile is equal to F_5(50−% Period); and wherein for a fourth quadrant the profile is equal to $-F_5$(% Period−50).

17. An electronic device having reduced amplitude electromagnetic interference (EMI) spectral components, said electronic device comprising:

spread spectrum clock generating means for generating a spread spectrum clock output signal having a fundamental frequency and reduced amplitude EMI spectral components at harmonics of the fundamental frequency, said spread spectrum clock generating means comprising profile modulating means for frequency modulating a series of clock pulses with a periodic waveform having a percentage of frequency deviation profile as a function of percentage of a period (% Period) of the periodic waveform within an envelope defined by predetermined upper and lower bounds, wherein said predetermined upper bound for a second quadrant is defined by F_3 which is equal to

$$100\% \left(\frac{\% \text{ Period}}{25} \right).$$

wherein said predetermined lower bound is defined by F_4 which is equal to

$$100\% \left(\frac{\% \text{ Period}}{25} \right)^3;$$

wherein for a first quadrant between −25% to 0% Period the lower bound is equal to $-F_3$(−% Period) and the upper bound is equal to $-F_4$(−% Period); wherein for a third quadrant between 25% to 50% Period the lower bound is equal to F_4(50−% Period), and the upper bound is equal to F_3(50−% Period); and wherein for a fourth quadrant the lower bound is equal to $-F_3$(% Period−50) and the upper bound is equal to $-F_4$(% Period 50); and

a digital circuit connected to said spread spectrum clock generating means and having a clock input driven by the spread spectrum clock output signal.

18. An electronic device according to claim 17 wherein said spread spectrum clock generating means comprises:

clock pulse generating means for generating a series of clock pulses; and

spread spectrum modulating means cooperating with said clock pulse generating means for modulating same to broaden and flatten amplitudes of EMI spectral components which would otherwise be produced by said clock pulse generating means.

19. A clock circuit according to claim 18 wherein said profile modulating means further comprises means for modulating said clock pulse generating means with a periodic waveform having a percentage of frequency deviation profile as a function of percentage of a period (% Period) of the periodic waveform defined in a second quadrant by F_5 which is equal to

$$100\%(0.45(\%\ \text{Period}/25)^3+0.55(\%\ \text{Period}/25));$$

wherein for a first quadrant between −25% to 0% Period the profile is equal to $-F_5$(−% Period); wherein for a third quadrant between 25% to 50% Period the profile is equal to F_5(50−% Period); and wherein for a fourth quadrant the profile is equal to $-F_5$(% Period−50).

20. An electronic device according to claim 18 wherein said clock pulse generating means comprises a phase locked loop.

21. A method for generating a clock output signal with reduced amplitude electromagnetic interference (EMI) spectral components, said method comprising the steps of:

generating a series of clock pulses; and

spread spectrum modulating the series of clock pulses to broaden and flatten amplitudes of EMI spectral components which would otherwise be produced along with the series of clock pulses by frequency modulating the series of clock pulses with a periodic waveform having a percentage of frequency deviation profile as a function of percentage of a period (% Period) of the periodic waveform within an envelope defined by predetermined upper and lower bounds, wherein the predetermined upper bound for a second quadrant is defined by which is equal to

$$100\%\left(\frac{\%\ \text{Period}}{25}\right),$$

wherein the predetermined lower bound is defined by F_4 which is equal to

$$100\%\left(\frac{\%\ \text{Period}}{25}\right)^3;$$

wherein for a first quadrant between −25% to 0% Period the lower bound is equal to $-F_3(-\%\ \text{Period})$ and the upper bound is equal to $-F_4(-\%\ \text{Period})$; wherein for a third quadrant between 25% to 50% Period the lower bound is equal to $F_4(50-\%\ \text{Period})$, and the upper bound is equal to $F_3(50-\%\ \text{Period})$; and wherein for a fourth quadrant the lower bound is equal to $-F_3(\%\ \text{Period}-50)$ and the upper bound is equal to $-F_4(\%\ \text{Period}-50)$.

22. A method according to claim **21** wherein the step of generating the spread spectrum clock output signal comprises the steps of:

generating a series of clock pulses; and

spread spectrum modulating the series of clock pulses to broaden and flatten amplitudes of EMI spectral components which would otherwise be produced along with the series of clock pulses.

23. A method according to claim **22** wherein the step of frequency modulating the series of clock pulses with a periodic waveform comprises modulating the series of clock pulses with a periodic waveform having a percentage of frequency deviation profile as a function of percentage of a period (% Period) of the periodic waveform defined in a second quadrant by F_5 which is equal to

$100\%(0.45(\%\ \text{Period}/25)^3+0.55(\%\ \text{Period}/25))$;

wherein for a first quadrant between −25% to 0% Period the profile is equal to $-F_5(-\%\ \text{Period})$; wherein for a third quadrant between 25% to 50% Period the profile is equal to $F_5(50-\%\ \text{Period})$; and wherein for a fourth quadrant the profile is equal to $-F_5(\%\ \text{Period}-50)$.

24. A method according to claim **23** wherein the step of frequency modulating comprises modulating the series of clock pulses with a periodic waveform having a period of less than about 500 microseconds.

25. A clock circuit having reduced amplitude electromagnetic interference (EMI) spectral components, said clock circuit comprising:

spread spectrum clock generating means for generating a spread spectrum clock output signal having a fundamental frequency and reduced amplitude EMI spectral components at harmonics of the fundamental frequency;

said spread spectrum clock generating means comprising profile modulating means for frequency modulating a series of clock pulses with a periodic waveform having a percentage of frequency deviation profile as a function of percentage of a period (% Period) of the periodic waveform defined in a first quadrant between −25% to 0% Period by a predetermined function which is generally negative, increasing and has a concave downward shape; wherein the periodic waveform is defined in a second quadrant between 0% to 25% Period by a predetermined function which is generally positive, increasing and has a concave upward shape; wherein the periodic waveform is defined in a third quadrant between 25% to 50% Period by a predetermined function which is generally positive, decreasing and has a concave upward shape; and wherein the periodic waveform is defined in a fourth quadrant between 50% to 75% Period by a predetermined function which is generally negative, decreasing and has a concave downward shape.

26. A clock circuit according to claim **25** wherein said spread spectrum clock generating means comprises clock pulse generating means for generating the series of clock pulses, and wherein said clock pulse generating means comprises a phase locked loop.

27. A clock circuit according to claim **26** wherein said spread spectrum clock generating means comprises an analog modulating generator operatively connected to said phase locked loop.

28. A clock circuit according to claim **26** wherein said spread spectrum clock generating means comprises a programmable modulating generator operatively connected to said phase locked loop.

29. A clock circuit according to claim **25** wherein said spread spectrum clock generating means comprises means for modulating said clock pulse generating means with a periodic waveform having a period of less than about 500 microseconds.

30. An electronic device having reduced amplitude electromagnetic interference (EMI) spectral components, said electronic device comprising:

spread spectrum clock generating means for generating a spread spectrum clock output signal having a fundamental frequency and reduced amplitude EMI spectral components at harmonics of the fundamental frequency;

said spread spectrum clock generating means comprising profile modulating means for frequency modulating a series of clock pulses with a periodic waveform having a percentage of frequency deviation profile as a function of percentage of a period (% Period) of the periodic waveform defined in a first quadrant between −25% to 0% Period by a predetermined function which is generally negative, increasing and has a concave downward shape; wherein the periodic waveform is defined in a second quadrant between 0% to 25% Period by a predetermined function which is generally positive, increasing and has a concave upward shape; wherein the periodic waveform is defined between 25% to 50% Period by a predetermined function which is generally positive, decreasing and has a concave upward shape; and wherein the periodic waveform is defined in a fourth quadrant between 50% to 75% Period by a predetermined function which is generally negative, decreasing and has a concave downward shape; and

a digital circuit connected to said spread spectrum clock generating means and having a clock input driven by the spread spectrum clock output signal.

31. A method for generating a clock output signal with reduced amplitude electromagnetic interference (EMI) spectral components, said method comprising the steps of:

generating a series of clock pulses; and

spread spectrum modulating the series of clock pulses to broaden and flatten amplitudes of EMI spectral components which would otherwise be produced along with the series of clock pulses by frequency modulating the series of clock pulses with a periodic waveform having a percentage of frequency deviation profile as a function of percentage of a period (% Period) of the periodic waveform defined in a first quadrant between −25% to 0% Period by a predetermined function which is generally negative, increasing and has a concave down-

ward shape; wherein the periodic waveform is defined in a second quadrant between 0% to 25% Period by a predetermined function which is generally positive, increasing and has a concave upward shape; wherein the periodic waveform is defined in a third quadrant between 25% to 50% Period by a predetermined function which is generally positive, decreasing and has a concave upward shape; and wherein the periodic waveform is defined in a fourth quadrant between 50% to 75% Period by a predetermined function which is generally negative, decreasing and has a concave downward shape.

* * * * *

UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO. : 5,488,627

DATED : January 30, 1996

INVENTOR(S) : Keith B. Harden; John T. Fessler; Donald R. Bush; James R. Booth

It is certified that error appears in the above-indentified patent and that said Letters Patent is hereby corrected as shown below:

On the cover page, Inventors, "James J. Booth" should be -- James R. Booth --.

On the cover page, References, U.S. Patents, No. 2, "7/1965" should be -- 11/1967 --.

On the cover page, Foreign Patents, No. 1, "Canada" should be -- France --.

On the cover page, Publications, Col 2., last line, after "Converters" insert -- , IEEE, 1989, pp. 500-507 --.

Column 8, line 45, after "link" insert a period (.).

Column 13, line 52, "Fs" should be -- F_s --.

Column 14, line 23, "Period 50" should be -- Period-50 --.

UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO. : 5,488,627

DATED : January 30, 1996

INVENTOR(S) : Keith B. Harden; John T. Fessler; Donald R. Bush; James R. Booth

It is certified that error appears in the above-indentified patent and that said Letters Patent is hereby corrected as shown below:

Column 14, last line, before "which" insert -- F_3 --.

Signed and Sealed this

Eleventh Day of June, 1996

Attest:

BRUCE LEHMAN

Attesting Officer

Commissioner of Patents and Trademarks

EXHIBIT 32
(Claims Chart)

Independent Claims for USP 6,249,876 B1	**Prior Art: Japanese Patent Application No. JP**58-27440
1. A digital frequency jittering circuit for varying the switching frequency of a power supply, comprising:	JP58-27440 discloses a digital circuit for varying the output frequency of an oscillator. *See* Exhibit 26 [English Translation of JP56-125807] at p.2.
an oscillator for generating a signal having a switching frequency, the oscillator having a control input for varying the switching frequency;	FIG. 3 shows an oscillator 4 that generates a signal having a switching frequency and has a control input (e.g., the junction point between the drain of transistors N4 and N1) for varying the switching frequency. *Id.* at p. 8.
a digital to analog converter coupled to the control input for varying the switching frequency; and	FIG. 3 shows a digital to analog converter 14 coupled to the control input for varying the switching frequency. *Id.* at p. 8.
a counter coupled to the output of the oscillator and to the digital to analog converter, the counter causing the digital to analog converter to adjust the control input and to vary the switching frequency.	FIG. 3 shows a counter 5 coupled between the oscillator 4 and the digital to analog converter 14. *Id.* at p. 8.

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EXHIBIT 33
(Claims Chart)

Independent Claims for USP 6,249,876 B1	**Prior Art: US Patent No. 5,943,382**
1. A digital frequency jittering circuit for varying the switching frequency of a power supply, comprising:	The '382 patent teaches a digital circuit for varying or modulating the output frequency of an oscillator. *See* FIG. 6. As disclosed in the BACKGROUND section, the '382 patent is direct to reducing EMI in electronic devices, such as televisions, cellular phones, pagers, and wireless devices. *See* Exhibit 27 at 1:39-48. A power supply is a type of electronic system that experiences EMI.
an oscillator for generating a signal having a switching frequency, the oscillator having a control input for varying the switching frequency;	FIG. 6 shows a voltage controlled oscillator 26 that generates a signal having a switching frequency and has a control input (e.g., the SUM 24) for varying the switching frequency.
a digital to analog converter coupled to the control input for varying the switching frequency; and	The phase comparator 32 and the waveform generator 30 as shown in FIG. 6 are a digital to analog converter. The output of the waveform generator 30 is coupled to the control input of the oscillator.
a counter coupled to the output of the oscillator and to the digital to analog converter, the counter causing the digital to analog converter to adjust the control input and to vary the switching frequency.	The divider 22 is a counter. The divider 22 is coupled to the output of the VCO 26. *See* FIG. 6. The divider 22 is also coupled to the phase comparator 32 and the waveform generator 30. *Id.* The divider 22 causes the digital to analog converter to adjust the control input and to vary the switching frequency. *Id.*

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EXHIBIT 34
(Claims Chart)

Independent Claims for USP 6,249,876 B1	**Prior Art: US Patent No. 5,757,338**
1. A digital frequency jittering circuit for varying the switching frequency of a power supply, comprising:	The '338 patent teaches a digital circuit for varying or modulating the output frequency of an oscillator. *See* FIG. 15. As disclosed in the BACKGROUND section, the '338 patent is directed to reducing EMI in electronic devices, such as televisions, cellular phones, pagers, and wireless devices. *See* Exhibit 28 at 1:20-31. A power supply is a type of electronic system that experiences EMI.
an oscillator for generating a signal having a switching frequency, the oscillator having a control input for varying the switching frequency;	FIG.15 shows a voltage-controlled-oscillator (VCO) 108 that generates a signal having a switching frequency and has a control input (e.g., summer 122) for varying the switching frequency.
a digital to analog converter coupled to the control input for varying the switching frequency; and	FIG.15 shows a digital to analog converter D/A 114 that is coupled to the control input for varying the switching frequency.
a counter coupled to the output of the oscillator and to the digital to analog converter, the counter causing the digital to analog converter to adjust the control input and to vary the switching frequency.	FIG.15 shows a counter (horizontal up-down counter) 85 coupled to the output of the oscillator 108 and to the digital to analog converter 114. The counter 85 causes the digital to analog converter 114 to adjust the control input and to vary the output frequency of the oscillator 108. For example, the specification discloses at 16:48-60: "The pixel count output from horizontal up-down counter 85 is output as an 8-bit value which is the digital input to D/A converter 114. This 8-bit digital value is a binary number representing the clock modulation from the nominal frequency. … The 8-bit value is converted by D/A converter 114 to an analog voltage which ultimately adjusts the frequency variation generated by VCO 108."

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EXHIBIT 35
(Claims Chart)

Independent Claims for USP 6,249,876 B1	**Prior Art: US Patent No. 5,659,587 (Exhibit 29)**
1. A digital frequency jittering circuit for varying the switching frequency of a power supply, comprising:	The '587 patent discloses a digital circuit that uses a spread spectrum technique to reduce EMI in electronic devices. *See* Exhibit 29 at 1:5-48.
an oscillator for generating a signal having a switching frequency, the oscillator having a control input for varying the switching frequency;	The ramp generator 56 and the VCO 20 as shown in FIG. 1 can be considered as an oscillator. The ramp generator 56 has a control input (e.g., the place that receives the signal from DAC 66) for varying the switching frequency.
a digital to analog converter coupled to the control input for varying the switching frequency; and	FIG. 1 shows a digital to analog converter 66 coupled to the ramp generator 56.*
a counter coupled to the output of the oscillator and to the digital to analog converter, the counter causing the digital to analog converter to adjust the control input and to vary the switching frequency.	The counter 79 and the accumulator 64 can be considered as corresponding to the counter in this claim element.** The counter 79 and the accumulator 64 are coupled to the output of the VCO 20 and coupled to the DAC 66. The counter 79 and the accumulator 64 cause the DAC 66 to adjust the control input and to vary the switching frequency.

* The ramp generator can be considered part of either the digital to analog converter or the oscillator.
** The accumulator in FIG. 1 can be considered as part of either the digital to analog converter or the counter.

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EXHIBIT 36
(Claims Chart)

Independent Claims for USP 6,249,876 B1	**Prior Art: US Patent No. 6,294,936 B1**
1. A digital frequency jittering circuit for varying the switching frequency of a power supply, comprising:	The '936 patent teaches a digital circuit for dithering or modulating the output frequency of an oscillator. *See* Exhibit 30 at FIGS. 2, 4, and 6. As disclosed in the BACKGROUND section, the circuit is used to reduce electromagnetic interference (EMI) in electronic devices and systems. *Id.* at 1:10-28. A power supply is a type of electronic system that experiences EMI, and therefore the '936 patent is applicable to a power supply system.
an oscillator for generating a signal having a switching frequency, the oscillator having a control input for varying the switching frequency;	FIG. 4 and FIG. 6 show a voltage controlled oscillator (VCO) 36 that generates a signal having a switching frequency and has a control input (e.g., junction point between the resistor 64 and the charge pump 30 in FIG.6) for varying the switching frequency. For example, the specification discloses "[t]he output frequency Fvco of the VCO 36 is based on the control signal input to the VCO 36 as is conventional." *Id.* at 5:34-36.
a digital to analog converter coupled to the control input for varying the switching frequency; and	The '936 patent discloses a digital to analog converter, for example, digital to analog converter 40 in FIG. 4, or the multiple capacitors C1-Cn and the resistor 64 in FIG. 6. As shown in FIGS. 4 and 6, the digital to analog converter is coupled to the control input of the voltage controlled oscillator 36.
a counter coupled to the output of the oscillator and to the digital to analog converter, the counter causing the digital to analog converter to adjust the control input and to vary the switching frequency.	The '936 patent discloses a counter, for example, the series of flip-flops shown in FIG. 5. The output of the counter is coupled to the digital to analog converter and the output of the oscillator 36 is coupled to the counter. *See e.g.*, FIG. 6. The LFSR DIVIDER 26' and the summer 58 as shown in FIG. 4 can also be considered as a counter.*

* As I explain in my Declaration,, drawing lines around circuit components is somewhat arbitrary, so the counter can include summer 58, or summer 58 can be considered as part of the digital to analog converter.

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EXHIBIT 37
(Claims Chart)

Independent Claims for USP 6,249,876 B1	**Prior Art: US Patent No. 5,488,627 B1**
1. A digital frequency jittering circuit for varying the switching frequency of a power supply, comprising:	The '627 patent teaches a digital circuit using a spread spectrum technique to reduce EMI in electronic devices including power switching circuits. *See* Exhibit 31 at 1:56-2:2.
an oscillator for generating a signal having a switching frequency, the oscillator having a control input for varying the switching frequency;	FIG. 6 shows a voltage controlled oscillator (VCO) 39 that generates a signal having a switching frequency and has a control input (e.g., the place that receives the signal from filter 38) for varying the switching frequency.
a digital to analog converter coupled to the control input for varying the switching frequency; and	The phase detector 37 and filter 38 as shown in FIG. 6 are a digital to analog converter. For example, the specification discloses "[t]he phase detector 37 and filter 38 generate an analog signal that is proportional to the error in phase between first and second programmable counters 35, 42, respectively." *Id.* at 8:58-61.
a counter coupled to the output of the oscillator and to the digital to analog converter, the counter causing the digital to analog converter to adjust the control input and to vary the switching frequency.	The '627 patent discloses a counter, for example, the programmable counter 42. The output of the counter is coupled to the digital to analog converter (the phase detector 37 and the filter 38) and the output of the oscillator 39 is coupled to the counter. *See e.g.*, FIG. 6. The counter causes the digital to analog converter to adjust the control input and to vary the switching frequency. *Id.*

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