IN THE UNITED STATES DISTRICT COURT
FOR THE DISTRICT OF DELAWARE

POWER INTEGRATIONS, INC., a Delaware corporation, Plaintiff, v. BCD SEMICONDUCTOR CORPORATION, a California corporation, and SHANGHAI SIM-BCD SEMICONDUCTOR MANUFACTURING CO., LTD., a China corporation, Defendants.	C.A. No. _____ **JURY TRIAL REQUESTED**

COMPLAINT FOR PATENT INFRINGEMENT

Plaintiff Power Integrations, Inc. hereby alleges as follows:

THE PARTIES

1. Power Integrations, Inc. ("Power Integrations") is incorporated under the laws of the state of Delaware, and has a regular and established place of business at 5245 Hellyer Avenue, San Jose, California, 95138.

2. Upon information and belief, defendant BCD Semiconductor Corporation is incorporated under the laws of the state of California, and has a regular and established place of business at 30920 Huntswood Avenue, Suite D, Hayward, California, 94544.

3. Upon information and belief, defendant Shanghai SIM-BCD Semiconductor Manufacturing Co., Ltd. is incorporated under the laws of the People's Republic of China, with its headquarters located at 800 Yishan Road, Shanghai 200233, China.

4. Defendant BCD Semiconductor Corporation and defendant Shanghai SIM-BCD Semiconductor Manufacturing Co., Ltd. will hereinafter be collectively referred to as the "Defendants."

JURISDICTION AND VENUE

5. This action arises under the patent laws of the United States, Title 35 U.S.C. § 1 *et seq*. This Court has subject matter jurisdiction under 28 U.S.C. §§ 1331 and 1338(a).

6. Upon information and belief, this Court has personal jurisdiction over Defendants because Defendants have purposely availed themselves of the privilege of conducting activities within this State and District.

7. Upon information and belief, venue is proper in this Court pursuant to 28 U.S.C. §§ 1391(b), 1391(c), and 1400 because Defendants are subject to personal jurisdiction in this judicial District.

GENERAL ALLEGATIONS

8. Power Integrations' products include its TOPSwitch®, TinySwitch®, LinkSwitch®, and DPA-Switch® families of power conversion integrated circuit devices which are used in power supplies for electronic devices such as cellular telephones, LCD monitors, and computers. These products are sold throughout the United States, including Delaware.

9. Upon information and belief, Defendants manufacture pulse width modulation ("PWM") controller integrated circuits devices (e.g., devices intended for use in power conversion applications such as off-line power supplies or battery chargers for portable electronics), and directly and through their affiliates, import, sell, and offer to sell the same throughout the United States, including Delaware.

FIRST CAUSE OF ACTION

INFRINGEMENT OF U.S. PATENT NO. 6,107,851

10. The allegations of paragraphs 1-9 are incorporated as though fully set forth herein.

11. Power Integrations is now, and has been since its issuance, the assignee and sole owner of all right, title, and interest in United States Patent No. 6,107,851,

entitled "Offline Converter with Integrated Softstart and Frequency Jitter" ("the '851 patent"), which was duly and legally issued on August 22, 2000. A true and correct copy of the '851 patent is attached hereto as Exhibit A.

12. Upon information and belief, Defendants have been and are now infringing, inducing infringement, and contributing to the infringement of the '851 patent in this District and elsewhere by making, using, selling, offering to sell, and/or importing devices, including PWM integrated circuit devices, covered by one or more claims of the '851 patent, and/or contributing to or inducing the same by third-parties, all to the injury of Power Integrations.

13. Defendants' acts of infringement have injured and damaged Power Integrations.

14. Defendants' infringement has caused irreparable injury to Power Integrations and will continue to cause irreparable injury until Defendants are enjoined from further infringement by this Court.

SECOND CAUSE OF ACTION

INFRINGEMENT OF U.S. PATENT NO. 6,249,876

15. The allegations of paragraphs 1-9 are incorporated as though fully set forth herein.

16. Power Integrations is now, and has been since its issuance, the assignee and sole owner of all right, title, and interest in United States Patent No. 6,249,876, entitled "Frequency Jittering Control for Varying the Switching Frequency of a Power Supply" ("the '876 patent"), which was duly and legally issued on June 19, 2001. A true and correct copy of the '876 patent is attached hereto as Exhibit B.

17. Upon information and belief, Defendants have been and are now infringing, inducing infringement, and contributing to the infringement of the '876 patent in this District and elsewhere by making, using, selling, offering to sell, and/or importing devices, including PWM integrated circuit devices, covered by one or more claims of the

'876 patent, and/or contributing to or inducing the same by third-parties, all to the injury of Power Integrations.

18. Defendants' acts of infringement have injured and damaged Power Integrations.

19. Defendants' infringement has caused irreparable injury to Power Integrations and will continue to cause irreparable injury until Defendants are enjoined from further infringement by this Court.

THIRD CAUSE OF ACTION

INFRINGEMENT OF U.S. PATENT NO. 5,313,381

20. The allegations of paragraphs 1-9 are incorporated as though fully set forth herein.

21. Power Integrations is now, and has been since its issuance, the assignee and sole owner of all right, title, and interest in United States Patent No. 5,313,381, entitled "Three-terminal switched mode power supply integrated circuit" ("the '381 patent"), which was duly and legally issued on May 17, 1994. A true and correct copy of the '381 patent is attached hereto as Exhibit C.

22. Upon information and belief, Defendants have been and are now infringing, inducing infringement, and contributing to the infringement of the '381 patent in this District and elsewhere by making, using, selling, offering to sell, and/or importing devices, including PWM integrated circuit devices, covered by one or more claims of the '381 patent, and/or contributing to or inducing the same by third-parties, all to the injury of Power Integrations.

23. Defendants' acts of infringement have injured and damaged Power Integrations.

24. Defendants' infringement has caused irreparable injury to Power Integrations and will continue to cause irreparable injury until Defendants are enjoined from further infringement by this Court.

PRAYER FOR RELIEF

WHEREFORE, Plaintiff requests the following relief:

(a) judgment against Defendants as to infringement of the '851 patent;

(b) judgment against Defendants as to infringement of the '876 patent;

(c) judgment against Defendants as to infringement of the '381 patent;

(d) a permanent injunction preventing Defendants and their officers, directors, agents, servants, employees, attorneys, licensees, successors, assigns, and customers, and those in active concert or participation with any of them, from making, using, importing, offering to sell or selling any devices that infringe any claim of the '851, '876, or '381 patents;

(e) judgment against Defendants for money damages sustained as a result of Defendants' infringement of the '851, '876, and '381 patents in an amount to be determined at trial;

(f) an accounting for infringing sales not presented at trial and an award by the court of additional damages for any such infringing sales;

(g) costs and reasonable attorneys' fees incurred in connection with this action pursuant to 35 U.S.C § 285; and

(h) such other and further relief as this Court finds just and proper.

JURY DEMAND

Plaintiff requests trial by jury.

Dated: October 15, 2007

FISH & RICHARDSON P.C.

By: _____

William J. Marsden, Jr. (#2247)
Kyle Wagner Compton (#4693)
919 N. Market Street, Suite 1100
P.O. Box 1114
Wilmington, DE 19801
Telephone: (302) 652-5070
Facsimile: (302) 652-0607

Frank E. Scherkenbach
225 Franklin Street
Boston, MA 02110-2804
Telephone: (617) 542-5070
Facsimile: (617) 542-8906

Howard G. Pollack
Michael R. Headley
500 Arguello Street, Suite 500
Redwood City, CA 94063
Telephone: (650) 839-5070
Facsimile: (650) 839-5071

Attorneys for Plaintiff
POWER INTEGRATIONS, INC.

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EXHIBIT
A

US006107851A

United States Patent [19]

Balakirshnan et al.

[11] **Patent Number: 6,107,851**

[45] **Date of Patent: Aug. 22, 2000**

[54] **OFFLINE CONVERTER WITH INTEGRATED SOFTSTART AND FREQUENCY JITTER**

[75] Inventors: **Balu Balakirshnan; Alex Djenguerian,** both of Saratoga; **Leif Lund,** San Jose, all of Calif.

[73] Assignee: **Power Integrations, Inc.,** Sunnyvale, Calif.

[21] Appl. No.: **09/080,774**

[22] Filed: **May 18, 1998**

[51] **Int. Cl.**[7] **H03K 3/017**

[52] **U.S. Cl.** **327/172**; 327/531; 327/544

[58] **Field of Search** 327/172, 173, 327/174, 175, 176, 530, 531, 544

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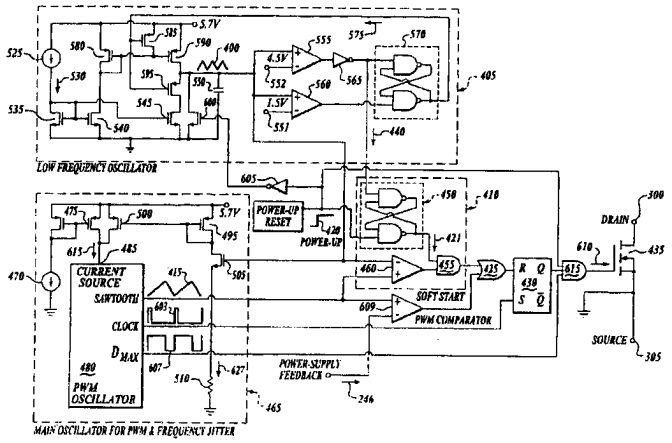
Primary Examiner—Jeffrey Zweizig

Attorney, Agent, or Firm—Blakely, Sokoloff, Taylor & Zafman, LLP

[57] **ABSTRACT**

A pulse width modulated switch comprises a first terminal, a second terminal, and a switch that allows a signal to be transmitted between the first terminal and the second terminal according to a drive signal provided at a control input. The pulse width modulated switch also comprises a frequency variation circuit that provides a frequency variation signal and an oscillator that provides an oscillation signal having a frequency of that varies within a frequency range according to the frequency variation signal. The oscillator further provides a maximum duty cycle signal comprising a first state and a second state. The pulse width modulated switch further comprises a drive circuit that provides the drive signal when the maximum duty cycle signal is in the first state and a magnitude of the oscillation signal is below a variable threshold level.

18 Claims, 9 Drawing Sheets



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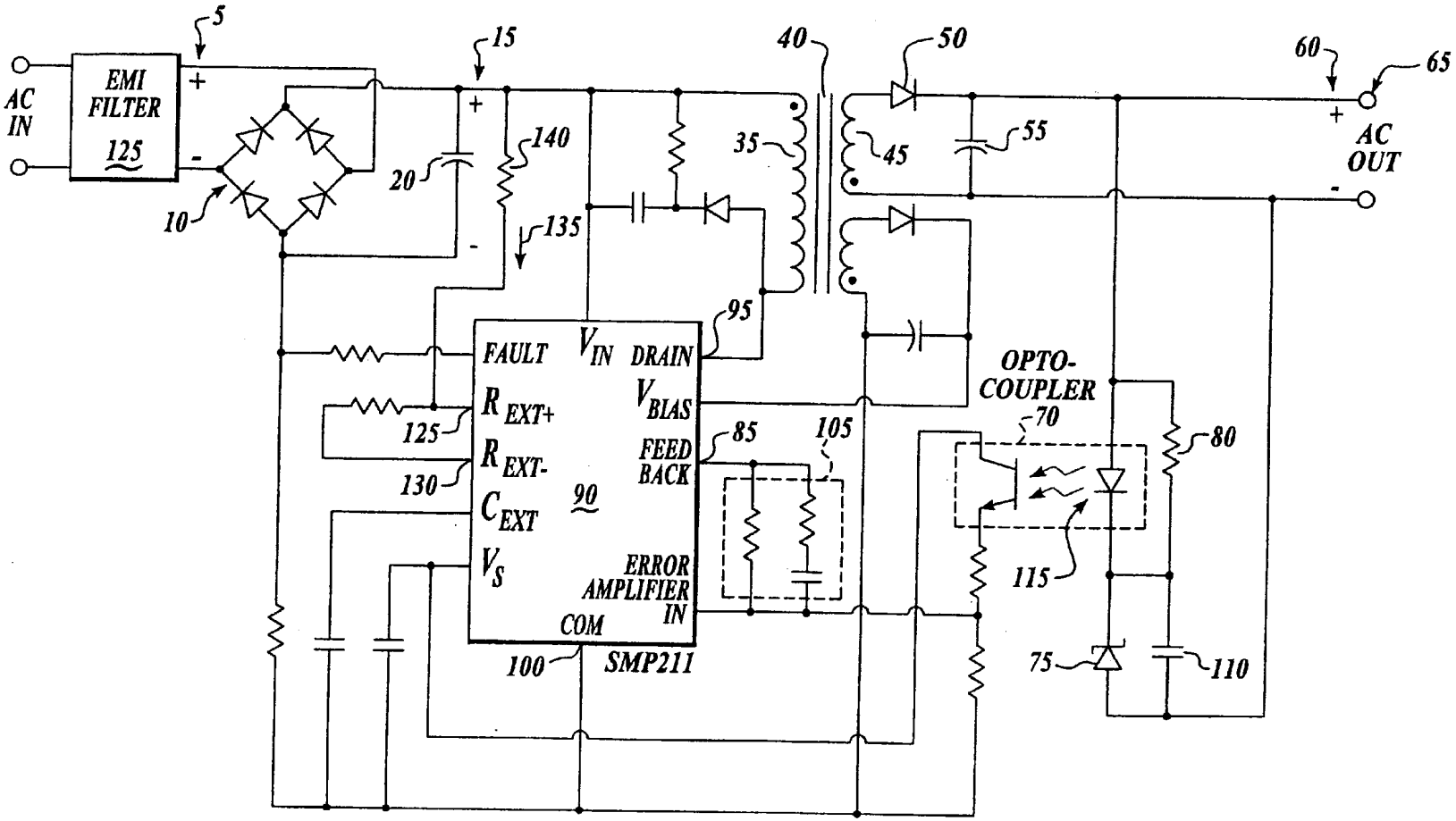


Fig. 1 (PRIOR ART)

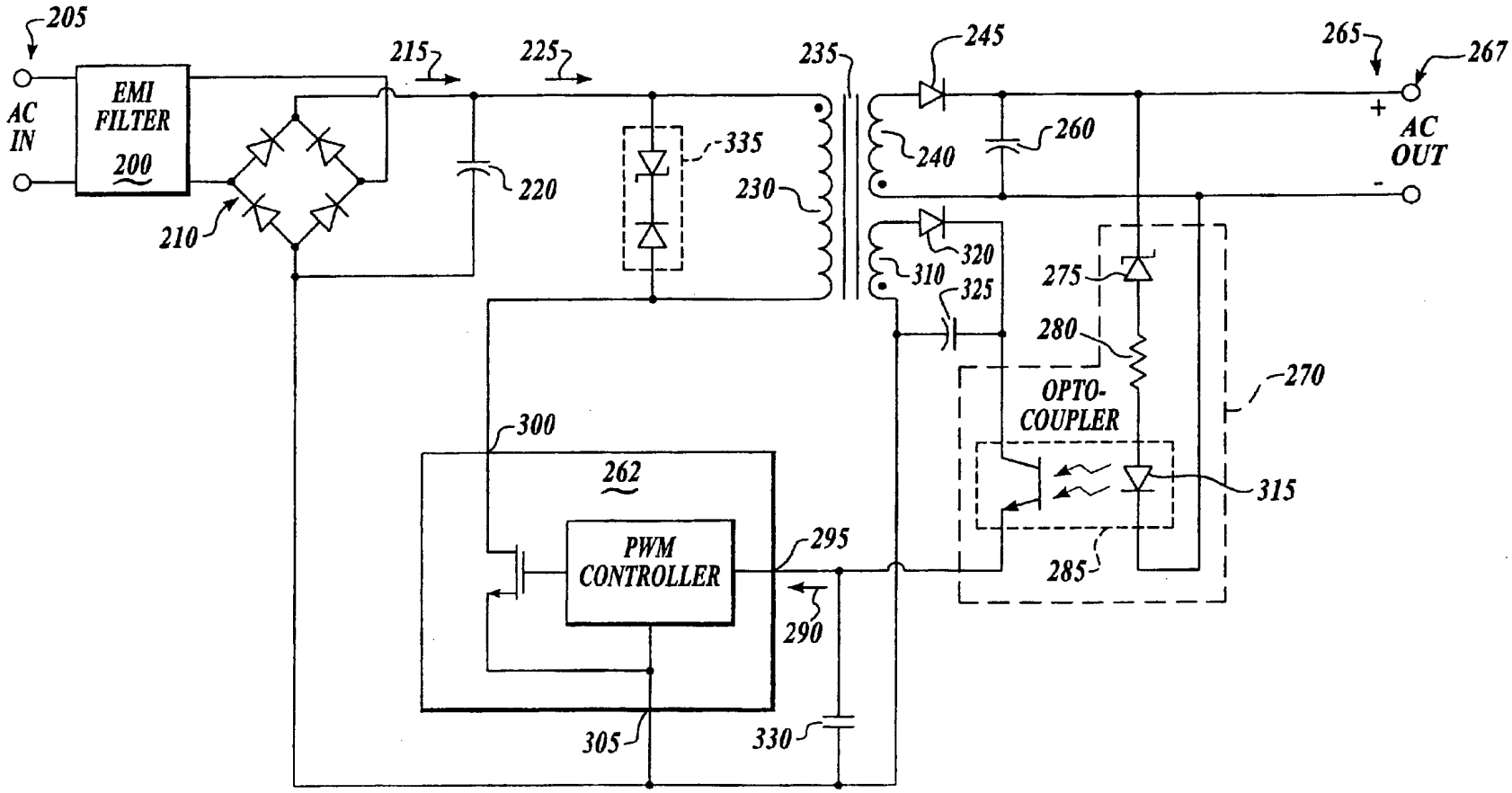
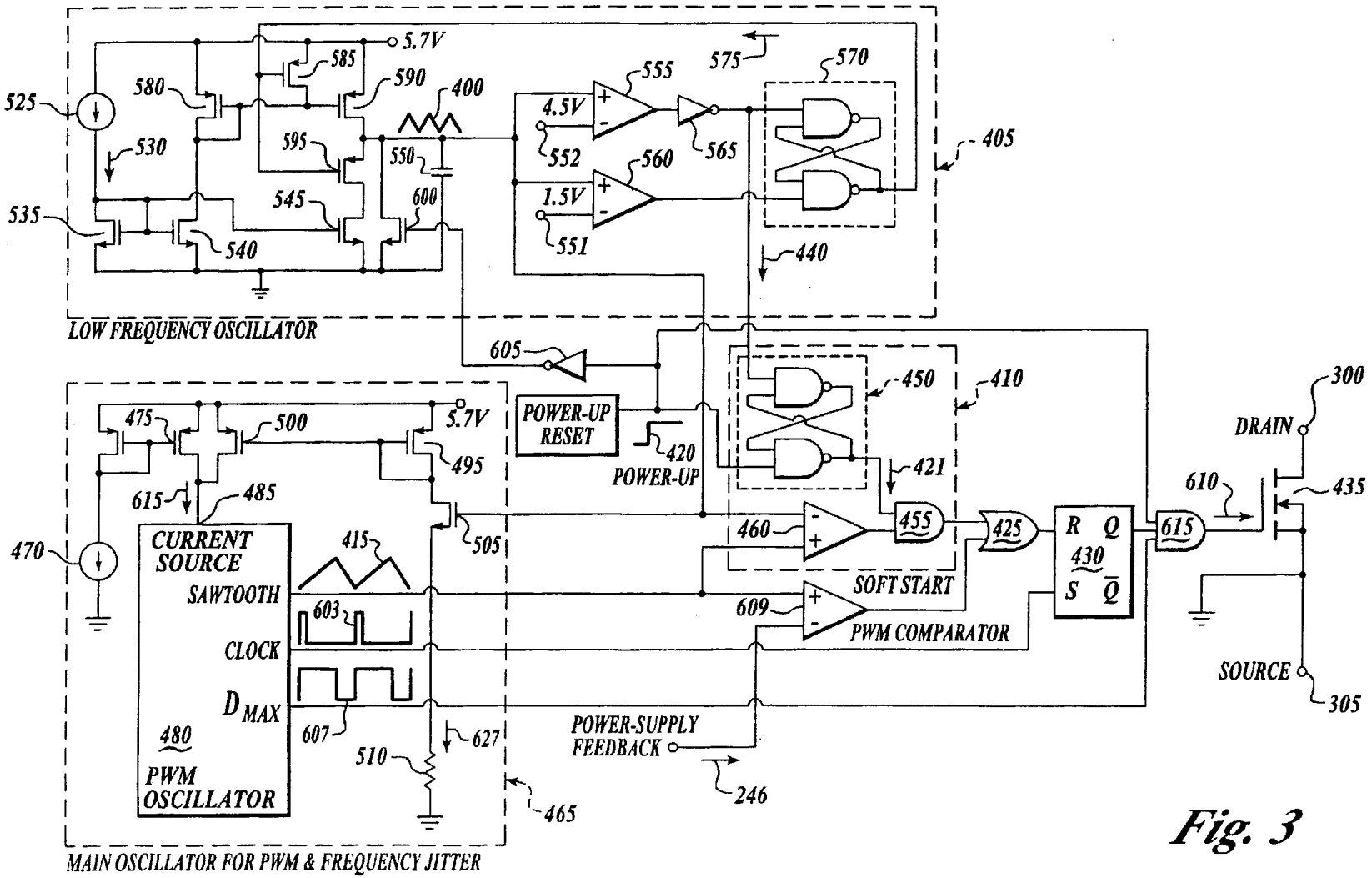

205
AC IN
EMI FILTER
200
210
215
220
225
235
335
230
245
240
260
265
267
AC OUT
+
-
310
320
325
275
280
270
OPTO-COUPLER
315
285
300
262
PWM CONTROLLER
295
290
305
330

Fig. 2


LOW FREQUENCY OSCILLATOR
MAIN OSCILLATOR FOR PWM & FREQUENCY JITTER
5.7V
4.5V
1.5V
POWER-UP RESET
POWER-UP
CURRENT SOURCE
SAWTOOTH
CLOCK
D MAX
PWM OSCILLATOR
SOFT START
PWM COMPARATOR
POWER-SUPPLY FEEDBACK
DRAIN
SOURCE
R Q
S Q
525
530
535
540
545
550
552
551
555
560
565
570
575
580
585
590
595
600
605
610
615
400
405
410
420
421
425
430
435
440
450
455
460
465
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475
480
485
495
500
505
510
603
607
609
627
246
300
305
415

Fig. 3

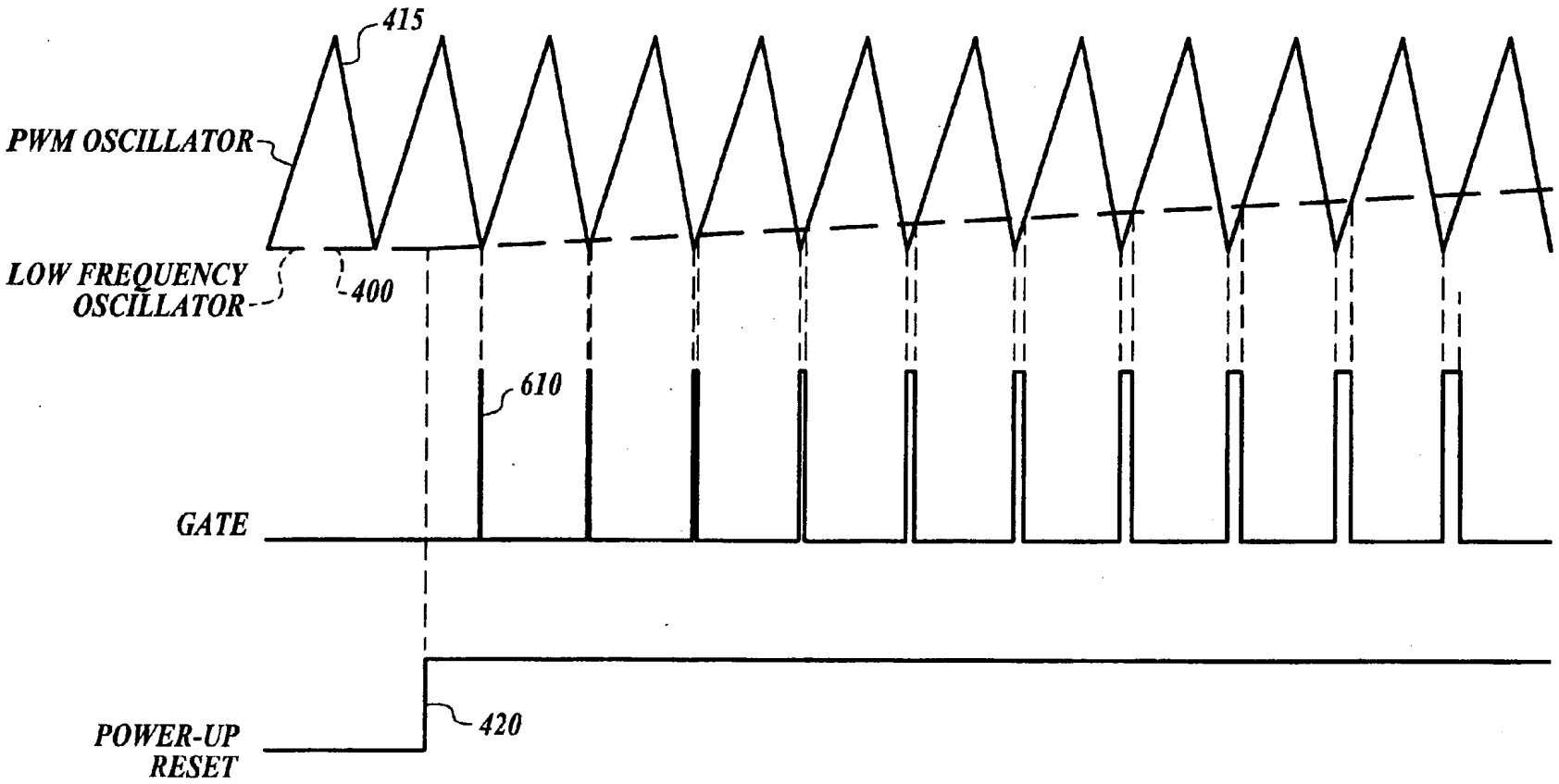

415
PWM OSCILLATOR
LOW FREQUENCY OSCILLATOR
400
610
GATE
420
POWER-UP RESET

Fig. 4

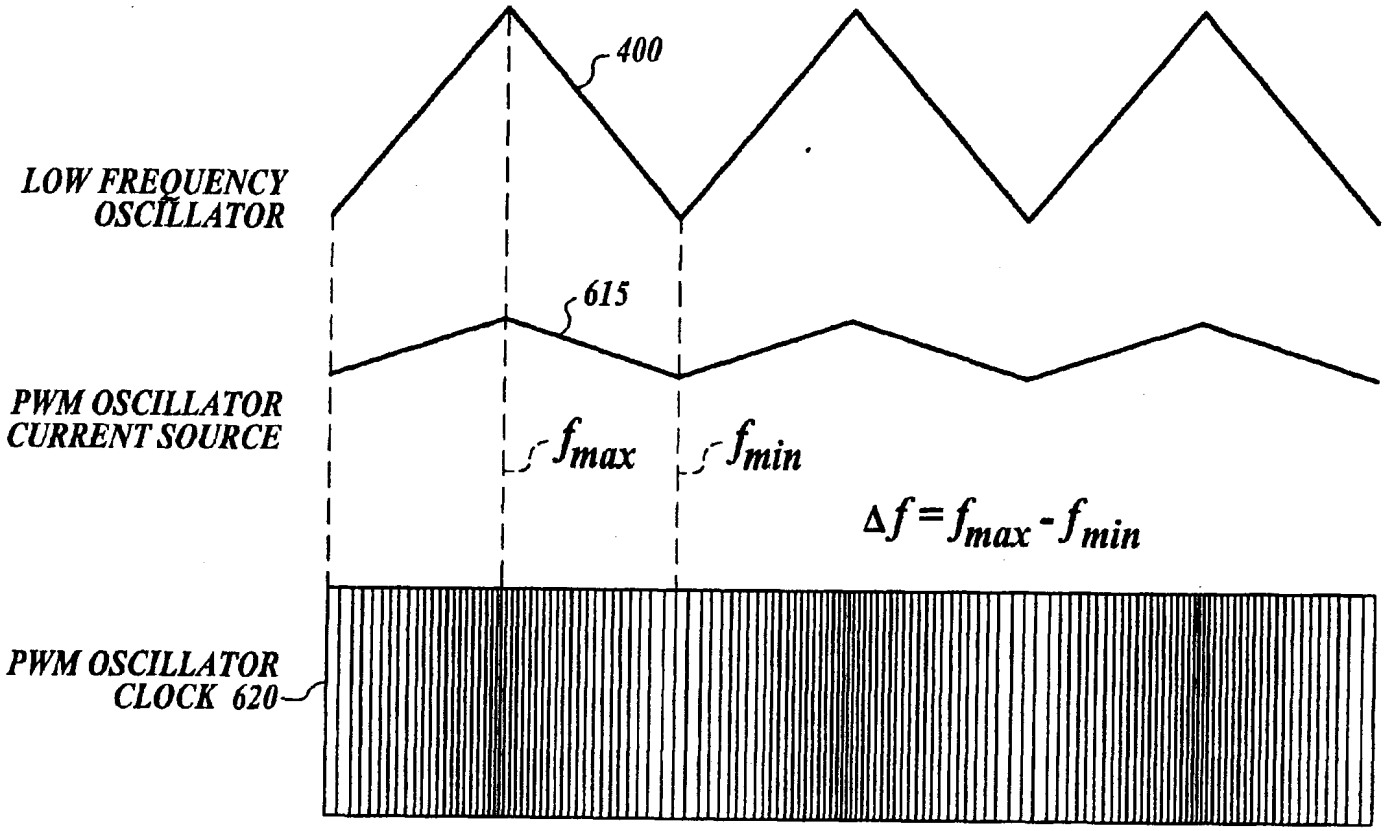
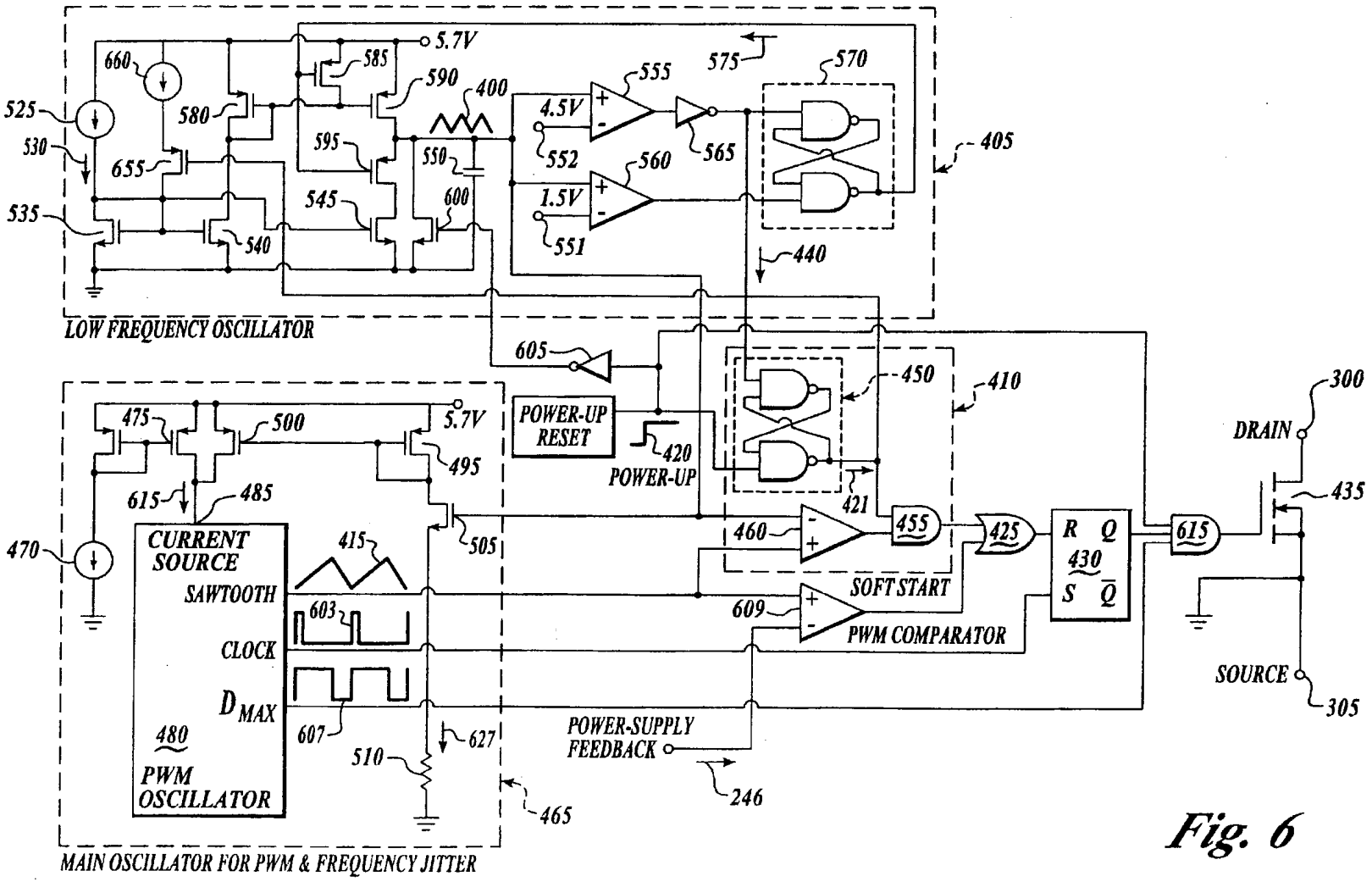

400
LOW FREQUENCY OSCILLATOR
615
PWM OSCILLATOR CURRENT SOURCE
f_{max}
f_{min}
$\Delta f = f_{max} - f_{min}$
PWM OSCILLATOR CLOCK 620

Fig. 5



LOW FREQUENCY OSCILLATOR
MAIN OSCILLATOR FOR PWM & FREQUENCY JITTER
CURRENT SOURCE
SAWTOOTH
CLOCK
D MAX
480
PWM OSCILLATOR
POWER-UP RESET
POWER-UP
POWER-SUPPLY FEEDBACK
SOFT START
PWM COMPARATOR
R Q
430
S Q̄
DRAIN
SOURCE
5.7V
4.5V
1.5V
405
410
415
420
421
425
430
435
440
450
455
460
465
470
475
480
485
495
500
505
510
515
525
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552
555
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565
570
575
580
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615
246
300
305
400

Fig. 6

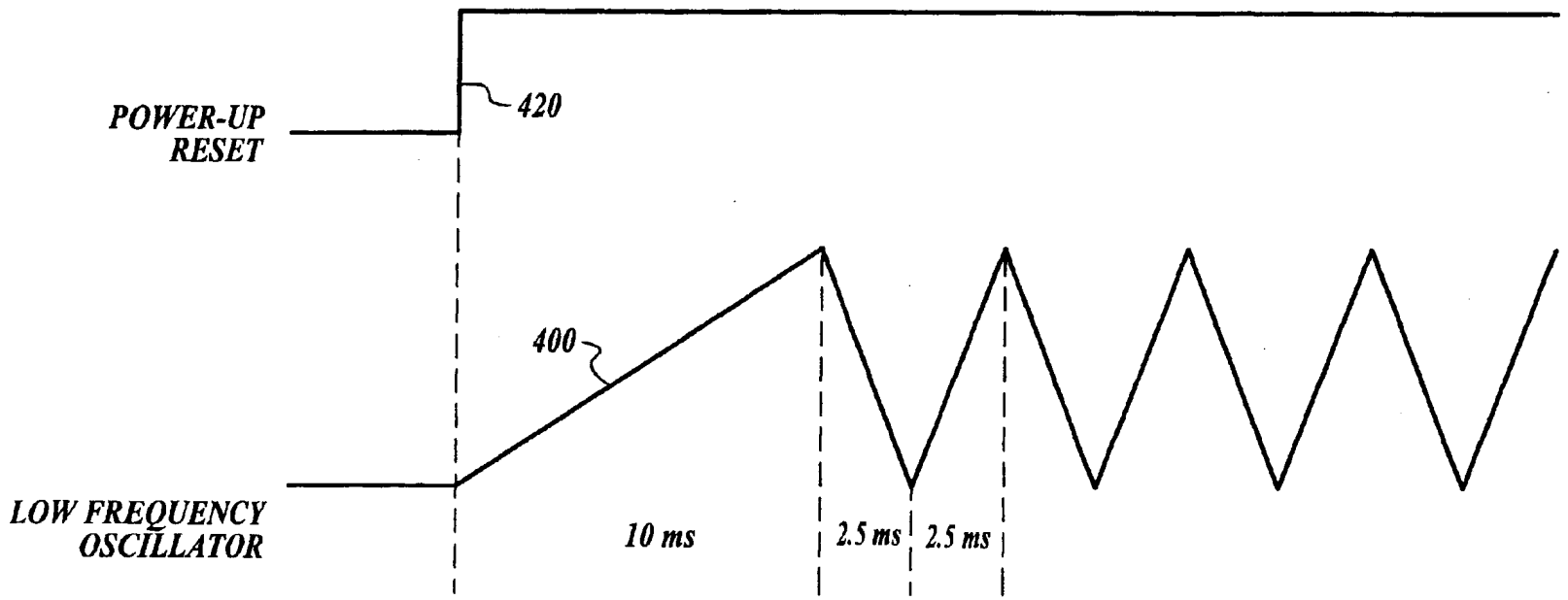
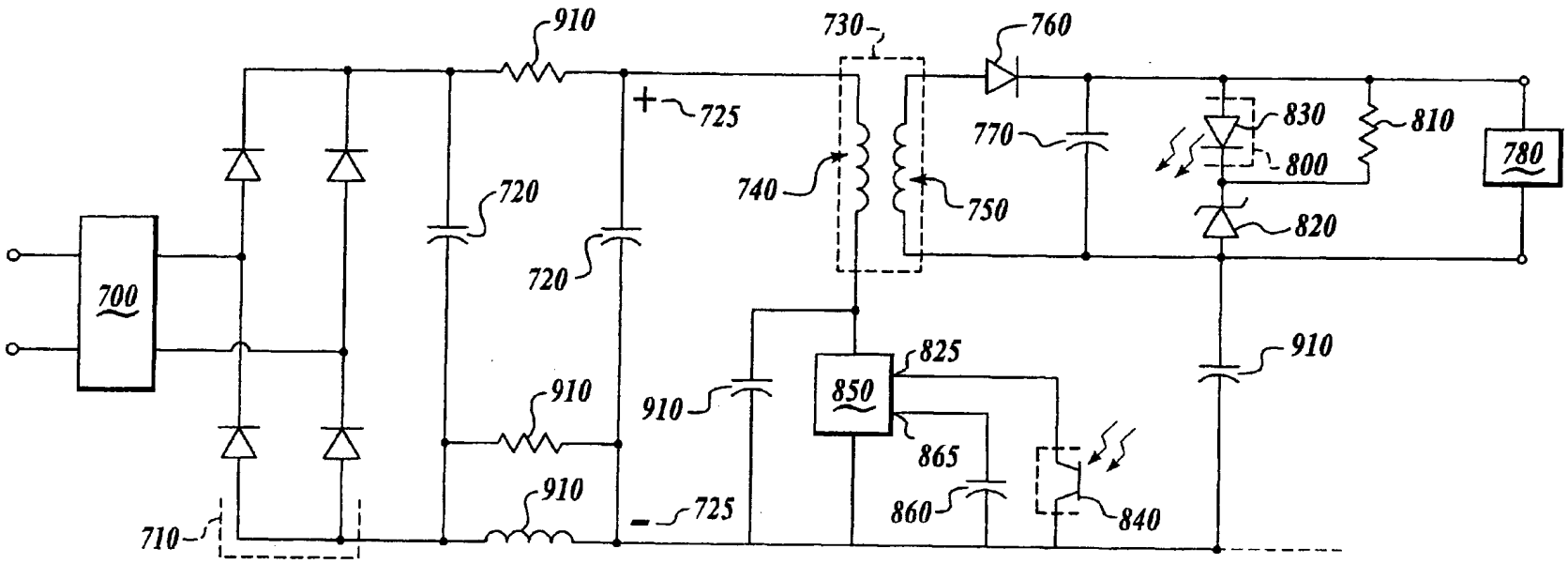

POWER-UP RESET
420
400
LOW FREQUENCY OSCILLATOR
10 ms
2.5 ms
2.5 ms

Fig. 7


910
730
760
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770
830
810
780
800
720
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750
820
700
720
825
910
910
850
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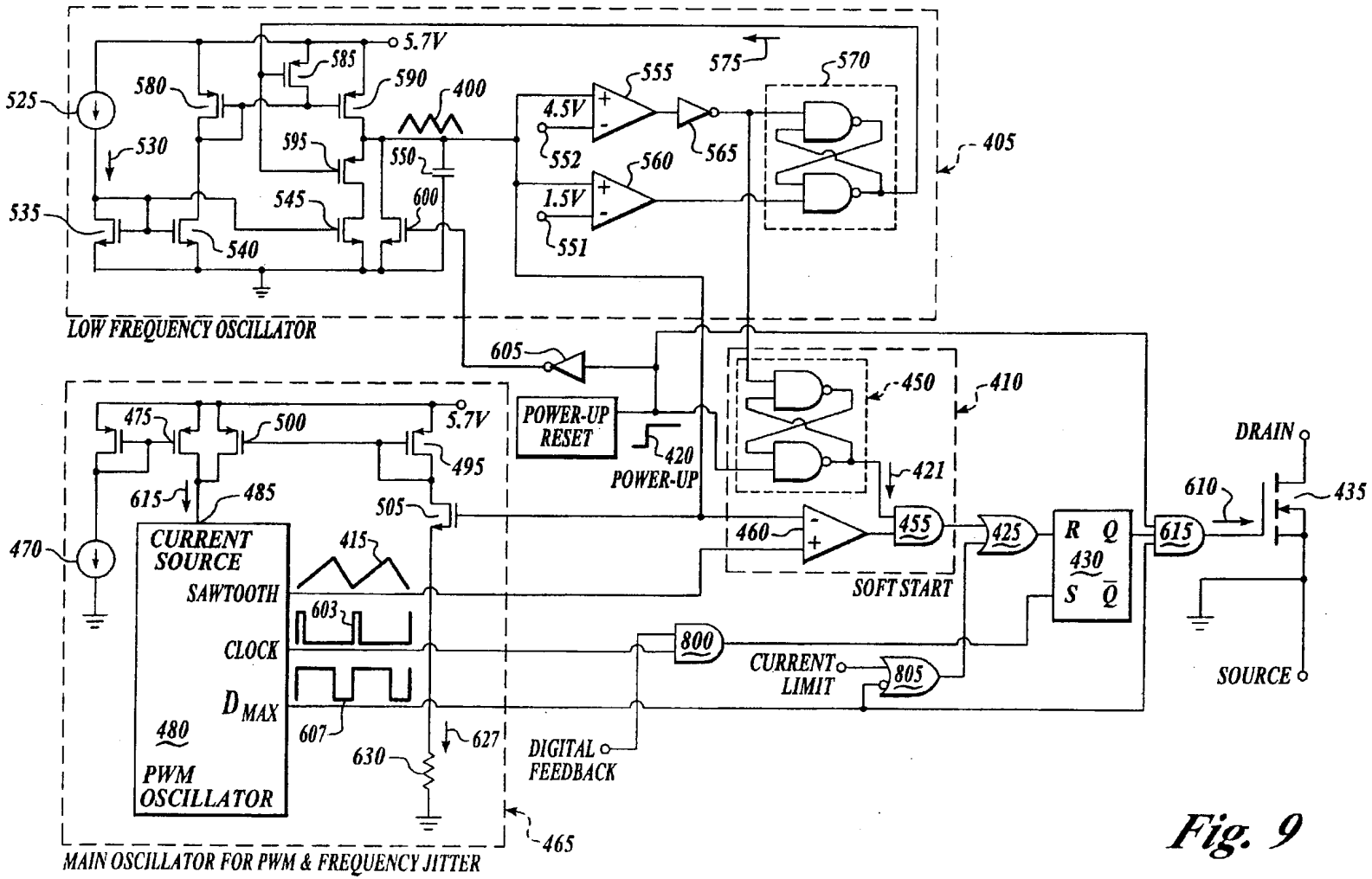
865
910
725
860
840
710

Fig. 8



5.7V
585
590
400
580
525
530
595
550
545
600
535
540
555
575
570
4.5V
552
565
560
1.5V
551
405
LOW FREQUENCY OSCILLATOR
605
POWER-UP RESET
420
POWER-UP
450
410
421
475
500
5.7V
495
615
485
505
470
CURRENT SOURCE
SAWTOOTH
415
603
CLOCK
D MAX
480
PWM OSCILLATOR
607
630
627
465
MAIN OSCILLATOR FOR PWM & FREQUENCY JITTER
460
455
SOFT START
425
R Q
430
S Q̄
615
610
DRAIN
435
SOURCE
800
CURRENT LIMIT
805
DIGITAL FEEDBACK

Fig. 9

OFFLINE CONVERTER WITH INTEGRATED SOFTSTART AND FREQUENCY JITTER

BACKGROUND

1. Field of the Invention

The field of the present invention pertains to the field of power supplies and among other things to the regulation of power supplies.

2. Background of the Invention

Power supplies that convert an AC mains voltage to a DC voltage for use by integrated electronic devices, amongst other devices, are known. The power supplies are required to maintain the output voltage, current or power within a regulated range for efficient and safe operation of the electronic device. Switches that operate according a pulse width modulated control to maintain the output voltage, current, or power of the power supply within a regulated range are also known. These switches utilize an oscillator and related circuitry to vary the switching frequency of operation of the switch, and therefore regulated the power, current or voltage that is supplied by the power supply.

A problem with utilizing pulse width modulated switches is that they operate at a relatively high frequency compared to the frequency of the AC mains voltage, which results in a high frequency signal being generated by the power supply. This high frequency signal is injected back into the AC mains input and becomes a component of the AC mains signal. The high frequency signals are also radiated by the power supply as electromagnetic waves. These high frequency signals add to the Electromagnetic Interference (EMI) of the power supply, and in fact are the largest contributors to the EMI of the power supply. The EMI generated by the power supply can cause problems for communications devices in the vicinity of the power supply and the high frequency signal which becomes a component of the AC mains signal will be provided to other devices in the power grid which also causes noise problems for those devices. Further, the radiated EMI by the power supply can interfere with radio and television transmissions that are transmitted over the air by various entities.

To combat the problem of EMI, several specifications have been developed by the Federal Communications Commission (FCC) in the United States and the European Community (EC) have established specification that specify the maximum amount of EMI that can be produced by classes of electronic devices. Since power supplies generate a major component of the EMI for electronic devices, an important step in designing a power supply is minimizing the EMI provided by the power supply to levels with the acceptable limits of the various standards. Since, a power supply can be utilized in many different countries of the world, the EMI produced should be within the most stringent limits worldwide to allow for maximum utilization of the power supply.

A known way of minimizing the EMI provided by the power supply is by adding an EMI filter to the input of the power supply. An EMI filter generally utilizes at least one inductor, capacitor and resistor in combination. However, the greater EMI produced by the power supply the larger the components that are utilized as part of the EMI filter. The cost of the EMI filter is in large part determined by the size of the inductor and capacitor utilized. The longer the components, the higher the cost of the power supply. Further, simply utilizing an EMI filter does not address the radiated EMI.

Another problem associated with pulse width modulated switches results from operation of the power supply at start up. At start up, the voltage, current and power at the output of the power supply will essentially be zero. The pulse width modulated switch will then conduct for the maximum possible amount of time in each cycle of operation. The result of this is a maximum inrush current into the power supply. The maximum inrush current is greater than the current that is utilized during normal operation of the power supply. The maximum inrush current stresses the components of power supply and switch. Stress is specifically a problem for the switch, or transistor, the transformer of the power supply, and the secondary side components of the power supply. The stress caused by the maximum inrush current decreases the overall life of the power supply and increases the cost of the power supply because the maximum rating of the components used in the power supply to not destruct from the inrush currents will be greater than the maximum rating required for normal operation.

Further, when the pulse width modulated switch conducts for the maximum possible amount of time in each cycle of operation the voltage, current and power at the output of the power supply rise rapidly. Since the feedback circuit of the power supply often does not respond as fast as the operating frequency of the switch, the rapid rise of the voltage, current and power will often result in an overshoot of the maximum voltage in the regulation range which will cause damage to the device being supplied power by the power supply.

Referring to FIG. **1** a known power supply that attempts to minimize EMI and reduce startup stress is depicted. A rectifier **10** rectifies the filtered AC mains voltage **5**, from EMI filter **120**, input by the AC mains to generate a rectified voltage **15**. Power supply capacitor **20** then generates a substantially DC voltage with a ripple component. The rectified voltage **15** with ripple component is provided to the primary winding **35** of transformer **40** that is used to provide power to secondary winding **45**. The output of secondary winding **45** is provided to secondary rectifier **50** and secondary capacitor **55** that provide a secondary DC voltage **60** at the power supply output **65** to the device that is coupled to the power supply.

In order to maintain the secondary DC voltage within a regulate range a feedback loop including an optocoupler **70**, zener diode **75** and a feedback resistor **80** provides a signal indicative of the voltage at the power supply output **65** to feedback pin **85** of pulse width modulated switch **90**. The voltage magnitude at the feedback terminal is utilized to vary the duty cycle of a switch coupled between the drain terminal **95** and common terminal **100** of the pulse width modulated switch **90**. By varying the duty cycle of the switch the average current flowing through the primary winding and therefore the energy stored by the transformer **40** which in turn controls the power supplied to the power supply output **65** is kept within the regulated range. A compensation circuit **105** is coupled to the feedback pin **85** in order to lower the bandwidth of the frequency of operation of the pulse width modulator.

Inrush currents are minimized at start up by use of soft start capacitor **110**. Soft start functionality is termed to be a functionality that reduces the inrush currents at start up. At this instant a current begins to flow through feedback resistor **80** and thereby into soft start capacitor **110**. As the voltage of soft start capacitor **110** increases slowly, current will flow through light emitting diode **115** of optocoupler **70** thereby controlling the duty cycle of the switch. Once the voltage of the soft start capacitor **110** reaches the reverse breakdown voltage of zener diode **75** current will flow through zener diode **75**. The approach described above will reduce the inrush currents into the power supply, however,

it will be several cycles before the light emitting diode **115** will begin conducting. During the several cycles the maximum inrush current will still flow through the primary winding and other secondary side components. During these cycles the transformer may saturate, and therefore the transformer may have to be designed utilizing a higher core size than would be required for normal operation even with the use of soft start capacitor as in FIG. **1**.

To reduce the EMI output by the power supply an EMI filter **120** is utilized. Additionally, pulse width modulated switch **90** is equipped with frequency oscillation terminals **125** and **130**. Frequency oscillation terminal **125** and **130** receive a jitter current **135** that varies according to the ripple component of substantially DC voltage **15**. The jitter current **135** is used to vary the frequency of the saw-toothed waveform generated by the oscillator contained in the pulse width modulated switch **90**. The saw toothed waveform generated by the oscillator is compared to the feedback provided at the feedback pin **85**. As the frequency of the saw toothed waveform varies, so will the switching frequency of the switch coupled between the drain and common terminal. This allows the switching frequency of the switch to be spread over a larger bandwidth, which minimizes the peak value of the EMI generated by the power supply at each frequency. By reducing the EMI the ability to comply with government standards is increased, because the government standards specify quasi-peak and average values at given frequency levels. Varying the frequency of operation of the pulse width modulated switch by varying the oscillation frequency of the oscillator is referred to as frequency jitter.

A problem associated with the EMI reduction scheme described with respect to FIG. **1** is that the ripple component will have variances due to variations in the line voltage and output load. Additionally, since the ripple may vary, design and the component value of EMI resistor **140** is difficult to determine and correspondingly design of the power supply becomes problematic.

SUMMARY OF THE INVENTION

In one embodiment the present invention comprises a pulse width modulated switch comprising a switch that allows a signal to be transmitted between a first terminal and a second terminal according to a drive signal. The pulse width modulated switch also comprises a frequency variation circuit that provides a frequency variation signal and an oscillator that provides an oscillation signal having a frequency that varies within a frequency range according to the frequency variation signal. The oscillator further provides a maximum duty cycle signal comprising a first state and a second state. The pulse width modulated circuit further comprises a drive circuit that provides the drive signal when the maximum duty cycle signal is in the first state and a magnitude of the oscillation signal is below a variable threshold level.

Another embodiment of the present invention comprises a pulse width modulated switch comprising a switch comprising a control input, the switch allowing a signal to be transmitted between a first terminal and a second terminal according to a drive signal. The pulse width modulated switch also comprises an oscillator that provides a maximum duty cycle signal comprising an on-state and an off-state, a drive circuit that provides the drive signal, and a soft start circuit that provides a signal instructing said drive circuit to disable the drive signal during at least a portion of said on-state of the maximum duty cycle.

In an alternate embodiment the present invention comprises a regulation circuit comprising a switch that allows a signal to be transmitted between a first terminal and a second terminal according to a drive signal, a drive circuit that provides the drive signal and a soft start circuit that provides a signal instructing the drive circuit to disable the drive signal.

In yet another embodiment the present invention comprises a regulation circuit comprising a switch that allows a signal to be transmitted between a first terminal and a second terminal according to a drive signal, a frequency variation circuit that provides a frequency variation signal, and a drive circuit that provides a drive signal for a maximum time period of a time duration cycle. The time duration of the cycle varies according to the frequency variation signal.

In the above referenced embodiments the pulse width modulated switch or regulation circuit may comprise a monolithic device.

An object of an aspect of the present invention is directed to a pulse width modulated switch that has integrated soft start capabilities.

Another object of an aspect of the present invention is directed toward a pulse width modulated switch that has integrated frequency variation capabilities.

Yet another object of an aspect of the present invention is directed toward a pulse width modulated switch that has integrated frequency variation capabilities and integrated soft start capabilities.

A further object of an aspect of the present invention is directed toward a low cost regulated power supply that has both soft start and frequency variation capabilities.

This and other objects and aspects of the present inventions are taught, depicted and described in the drawings and the description of the invention contained herein.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** is a known power supply utilizing a pulse width modulated switch, and external soft start, and frequency jitter functionality.

FIG. **2** is a presently preferred power supply utilizing an pulse width modulated switch according to the present invention.

FIG. **3** is a presently preferred pulse width modulated switch according to the present invention.

FIG. **4** is a timing diagram of the soft start operation of the presently preferred pulse width modulated switch according to the present invention.

FIG. **5** is a timing diagram of the frequency jitter operation of the presently preferred pulse width modulated switch according to the present invention.

FIG. **6** is an alternate presently preferred pulse width modulated switch according to the present invention.

FIG. **7** is a timing diagram of the operation of the alternate presently preferred pulse width modulated switch of FIG. **6** according to the present invention.

FIG. **8** is a presently preferred power supply utilizing a regulation circuit according to the present invention.

FIG. **9** is a presently preferred regulation circuit according to the present invention.

DESCRIPTION OF THE PREFERRED EMBODIMENT

Referring to FIG. **2**, EMI filter **200** is coupled to an AC mains voltage **205**. The AC mains voltage **205** is rectified by rectifier **210**. The rectified voltage **215** is provided to power

supply capacitor **220** which provides a substantially DC voltage **225**. The substantially DC voltage **225** is provided to the primary winding **230** of transformer **235** which stores the energy provided to the primary winding **230**. When the primary winding **230** is no longer receiving energy, energy is delivered by the transformer **235** to the secondary winding **240**. The voltage induced across the secondary winding **240** is rectified by rectifier **245** and then transformed into secondary substantially DC voltage **265** by secondary capacitor **260** and provided to the power supply output **267**.

Energy is no longer provided to the primary winding **230** when the pulse width modulated switch **262**, which is coupled to the primary winding **230**, ceases conduction. Pulse width modulated switch **262** is a switch that is controlled by a pulse width modulated signal. Pulse width modulated switch **262** conducts and ceases conduction according to a duty cycle, that is in part determined by feedback from the power supply output **267**. Pulse width modulated switch **262** is a switch that operates according to pulse width modulated control. Feedback to the pulse width modulated switch **262** is accomplished by utilization of feedback circuit **270**, which is presently preferred to comprise a zener diode **275** in series with a resistor **280** and optocoupler **285**. Optocoupler **285** provides a feedback current **290** to feedback terminal **295** of pulse width modulated switch **262**. The feedback current is utilized to vary the duty cycle of a switch coupled between the first terminal **300** and second terminal **305** and thus regulate the output voltage, current or power of the power supply.

Although, it is presently preferred that the output voltage is utilized for feedback, the present invention is also capable of utilizing either the current or power at the power supply output **267** without departing from the spirit and scope of the present invention.

A portion of the current supplied at the feedback terminal **295** is utilized to supply bias power for operation of the pulse width modulated switch **262**. The remainder of the current input at the feedback terminal **295** is utilized to control the duty cycle of the pulse width modulated switch **262**, with the duty cycle being inversely proportional to the feedback current.

A bias winding **310** is utilized to bias optocoupler **285** so that a feedback current can flow when light emitting diode **315** of optocoupler **285** conducts. The power supplied by the bias winding **310** is also used to charge pulse width modulation capacitor **330**, the energy from which is utilized to power the pulse width modulated switch **262**.

Overvoltage protection circuit **335** is utilized to prevent overvoltages from propagating through to the transformer **235**.

Pulse width modulated switch **262** is supplied power during start up of the power supply by current flowing into the first terminal **300**. An embodiment of one type of apparatus and method for designing a configuration for providing power to pulse width modulated switch through first terminal **300** is disclosed in commonly owned U.S. Pat. No. 5,014,178 which is incorporated herein by reference in its entirety.

The drain terminal **300**, source terminal **305** and feedback terminal **295** are the electrical input and/or output points of the pulse width modulated switch **262**. They need not be part of a monolithic device or integrated circuit, unless the pulse width modulated switch **262** is implemented utilizing a monolithic device or integrated circuit.

Pulse width modulated switch **262** also may have soft start capabilities. When the device to which the power supply is coupled is switched on, a power up signal is generated within the internal circuitry of pulse width modulated switch **262**. The power up signal is used to trigger soft start circuitry that reduces the duty cycle of the switch that operates within the pulse width modulated switch **262** for a predetermined period of time, which is presently preferred to be ten (10) milliseconds. Once soft start operation is completed, pulse width modulated switch **262** operates according to its regular duty cycle.

Alternatively, or in addition to soft start functionality, pulse width modulated switch **262** may also have frequency jitter functionality. That is, the switching frequency of the pulse width modulated switch **262** varies according to an internal frequency variation signal. This has an advantage over the frequency jitter operation of FIG. **1** in that the frequency range of the presently preferred pulse width modulated switch **262** is known and fixed, and is not subject to the line voltage or load magnitude variations. At low powers, those less than approximately ten (10) watts, the common mode choke which is often utilized as part of the EMI filter **120** can be replaced with inductors or resistors.

As can be seen when comparing the power supply of FIG. **1** to that of FIG. **2** the number of components utilized is reduced. This reduces the overall cost of the power supply as well as reducing its size.

Referring to FIG. **3**, frequency variation signal **400** is utilized by the pulse width modulated switch **262** to vary its switching frequency within a frequency range. The frequency variation signal **400** is provided by frequency variation circuit **405**, which preferably comprises an oscillator that operates at a lower frequency than main oscillator **465**. The frequency variation signal **400**, is presently preferred to be a triangular waveform that preferrably oscillates between four point five (4.5) volts and one point five (1.5) volts. Although the presently preferred frequency variation signal **400** is a triangular waveform, alternate frequency variation signals such as ramp signals, counter output signals or other signals that vary in magnitude during a fixed period of time may be utilized as the frequency variation signal.

The frequency variation signal **400** is provided to soft start circuit **410**. During operation soft start circuit **410** is also provided with pulse width modulation frequency signal **415** and power up signal **420**. Soft start enable signal **421** goes high at power up and remains high until oscillator signal **400** reaches its peak value for the first time. Soft start circuit **410** will provide a signal to or-gate **425** to reset latch **430** thereby deactivating conduction by the switch **435**, which is presently preferred to be a MOSFET. Soft start circuit **410** will instruct switch **435** to cease conduction when the soft start enable signal **421** is provided and the magnitude of the frequency variation signal **400** is less than the magnitude of pulse width modulation signal **415**. In other words, start up circuit **410** will allow the switch **435** to conduct as long as soft start enable signal is high and the magnitude of the pulse width modulation signal **415** is below the magnitude of frequency variation signal **400** as depicted in FIG. **4**. In this way, the inrush current at startup will be limited for all cycles of operation, including the first cycle. By limiting the inrush current during all cycles of startup operation, the maximum current through each of the components of the power supply is reduced and the maximum current rating of each component can be decreased. The reduction in the ratings of the components reduces the cost of the power supply. Soft start signal **440** will no longer be provided by the frequency variation circuit **405** when the frequency variation signal **400** reaches its peak magnitude.

Operation of soft start circuit **410** will now be explained. Soft start circuit **410** comprises a soft start latch **450** that at

its set input receives the power up signal **420** and its reset input receives the soft start signal **440**. Soft start enable signal **421** is provided to one input of soft start and-gate **455** while the other input of soft start and-gate **455** is provided with an output from soft start comparator **460**. The output of soft start comparator **460** will be high when the magnitude of frequency variation signal **400** is less than the magnitude of pulse width modulation oscillation signal **415**.

The pulse width modulated switch **262** depicted in FIG. **3** also has frequency jitter functionality to help reduce the EMI generated by the power supply and pulse width modulated switch **262**. Operation of the frequency jitter functionality will now be explained. Main oscillator **465** has a current source **470** that is mirrored by mirror current source **475**. Main oscillator drive current **615** is provided to the current source input **485** of PWM oscillator **480**. The magnitude of the current input into current source input **485** of PWM oscillator **480** determines the frequency of the pulse width modulation oscillation signal **415** which is provided by PWM oscillator **480**. In order to vary the frequency of pulse width modulation oscillation signal **415**, an additional current source **495** is provided within main oscillator **465**. The additional current source **495** is mirrored by additional current source mirror **500**. The current provided by additional current source **495** is varied as follows. Frequency variation signal **400** is provided to the gate of main oscillator transistor **505**. As the magnitude of frequency variation signal **400** increases so does the voltage at the source of main oscillator transistor **505**, due to the increasing voltage at the gate of main oscillation transistor and the relatively constant voltage drop between the gate and source of the main oscillation transistor **505**. As the voltage at the source of main oscillation transistor **505** increases so does the current flowing through the main oscillation resistor **510**. The current flowing through main oscillation resistor **510** is the same as the current flowing through additional current source **495** which is mirrored by additional current source mirror **500**. Since, the presently preferred frequency variation signal **400** is a triangular waveform having a fixed period, the magnitude of the current input by additional current source mirror **500** will vary linearly with the magnitude of the rising and falling edges of the frequency variation signal **400**. If the frequency variation signal **400** is a ramp signal, the frequency would linearly rise to a peak and then immediately fall to is lowest value. In this way, the current provided to current source input **485** of PWM oscillator **480** is varied in a known fixed range that allows for easy and accurate frequency spread of the high frequency current generated by the pulse width modulated switch. Further, the variance of the frequency is determined by the magnitude of the current provided by additional current source mirror **500**, which is in turn a function of the resistance of main oscillation resistor **510**.

Frequency variation circuit **405** includes a current source **525** that produces a fixed magnitude current **530** that determines the magnitude of the frequency of the frequency variation signal **400**. Although, the presently preferred current **530** has a fixed magnitude, the frequency variation signal can be generated utilizing a variable magnitude current, if a variable current is generated the frequency spread would not be fixed in time but would vary with the magnitude of current **530**. The fixed magnitude current **530** is fed into first transistor **535**, mirrored by second transistor **540** and fed into third transistor **545**. The frequency variation signal **400** is generated by the charging and discharging of frequency variation circuit capacitor **550**. Frequency variation circuit capacitor **550** is presently preferred to have a relatively low capacitance, which allows for integration into a monolithic chip in one embodiment of the pulse width modulated switch **262**. The frequency variation signal **400** is provided to upper limit comparator **555** and lower limit comparator **560**. The output of upper limit comparator **555** will be high when the magnitude of the frequency variation signal **400** exceeds the upper threshold voltage **552** which is presently preferred to be four point five (4.5) volts. The output of lower limit comparator **560** will be high when the magnitude of frequency variation signal **400** exceeds lower threshold voltage **557** which is presently preferred to be one point five volts (1.5) volts. The output of upper limit comparator **555** is provided to the frequency variation circuit inverter **565** the output of which is provided to the reset input of frequency variation circuit latch **570**. The set input of frequency variation circuit latch **570** receives the output of lower limit comparator **560**. In operation, the output of lower limit comparator **560** will be maintained high for the majority of each cycle of frequency variation signal **400** because the magnitude of frequency variation signal will be maintained between upper threshold **552**, 4.5 volts, and the lower threshold **557**, 1.5 volts. The output of upper limit comparator **555** will be low until the magnitude of frequency variation signal **400** exceeds upper level threshold **552**. This means that the reset input will receive a high signal until the magnitude of the frequency variation signal **400** rises above the upper threshold signal **552**.

The charge signal **575** output by frequency variation circuit latch **570** will be high until the frequency variation signal **400** exceeds the upper threshold limit signal **552**. When the charge signal **575** is high, transistors **585** and **595** are turned off. By turning off transistors **585** and **595** current can flow into frequency variation circuit capacitor **550**, which steadily charges frequency variation circuit capacitor **550** and increases the magnitude of frequency variation signal **400**. The current that flows into frequency variation circuit capacitor **550** is derived from current source **525** because the current through transistor **590** is mirrored from transistor **580**, which is mirrored from transistor **535**.

During power up, when power-up signal **420** is low, the output of inverter **605** is high which turns on transistor **600** causing frequency variation signal **400** to go low. The frequency variation signal **400** is presently preferred to start from its lowest level to perform the soft start function during its first cycle of operation.

Steady-state operation of the pulse width modulated switch **262**, i.e. non start up operation, will now be described. PWM oscillator **480** provides pulse width modulation oscillation signal **415** to pulse width modulation comparator **609**, the output of which will be high when the magnitude of pulse width modulation signal **415** is greater than the magnitude of a feedback signal **296** which is a function of the input provided at feedback terminal **295**. When the output of pulse width modulation comparator **609** is high or-gate **425** is triggered to go high, which in turn resets pulse width modulation latch **430**, removing the on signal from the control input of switch **435**, thereby turning off switch **435**. Pulse width modulation latch **430** is set by clock signal **603**, which is provided at the beginning of each cycle of pulse width modulation oscillator **480**. Drive circuit **615**, which is presently preferred to be an and-gate, receives the output of pulse width modulation latch **430**, power up signal **420**, and maximum duty cycle signal **607**. As long as each one of the signals is high, drive signal **610** is provided to the gate of MOSFET **435**, which is coupled between first terminal **300** and second terminal **305** of the pulse width modulated switch **262**. When any of the output of pulse

width modulation latch **430**, power up signal **420**, or maximum duty cycle signal **607** goes low drive signal **610** is no longer provided and switch **435** ceases conduction.

Referring to FIG. **4**, frequency variation signal **400** preferably has a period, which is greater than that of pulse width modulated oscillation signal **415**. The presently preferred period for frequency variation signal **400** is twenty (20) milliseconds, in order to allow for a smooth start up period which is sufficiently longer than the period of pulse width modulated signal **415** which is presently preferred to be ten (10) microseconds. Drive signal **610** will be provided only when the magnitude of pulse width modulated signal **415** is less than the magnitude of frequency variation signal **400**. Further, frequency variation signal **400** will be preferably initiated starting from low voltage when power up signal **420** is provided.

Referring to FIG. **5**, frequency variation signal **400** which is presently preferred to have a constant period is provided to the main oscillator **465**. The magnitude of the pulse width modulator current **615** will approximately be the magnitude of frequency variation signal **400** divided by the resistance of resistor **510** plus the magnitude of the current produced by current source **470**. In this way the pulse width modulator current **615** will vary with the magnitude of the frequency variation signal **400**. The result is that the frequency of pulse width modulation signal is varied according to the magnitude of this current. It is presently preferred that the pulse width modulator current source produces a constant current having a magnitude of twelve point one (12.1) microamperes, and that frequency variation signal induced current **627** varies between zero (0) and eight hundred (800) nanoamperes. Thereby spreading the frequency of operation of the pulse width modulation oscillator **480** and reducing the average magnitude and the quasi-peak magnitude at all frequency levels of the EMI generated by the power supply.

Referring to FIG. **6**, an alternate presently preferred pulse width modulated switch **262** includes all of the same components as described with respect to FIG. **3**. In addition to these components, a second frequency variation circuit current source **660** and transistor **655** are added to the frequency variation circuit **405**. Transistor **655** is activated only when the output of soft start latch **450** goes low. When transistor **655** is activated the current provided to the frequency variation circuit **405** increases as does the frequency of frequency variation signal **400**. However, transistor **655** will only be turned on when the output of soft start latch **450** goes low, i.e. when the magnitude of frequency variation signal **400** first reaches the upper threshold after power up. The period of frequency variation signal **400** will then increase after its first half cycle. This will decreases the period of the cycle during which the frequency is spread, without decreasing the frequency range. The benefit of the decreased cycle period will further decrease the quasi-peak levels of the EMI due to spending less time at each frequency level.

Referring to FIG. **7**, operation of the frequency variation circuit **405** of FIG. **6** is depicted. Frequency variation signal **400** will preferably have a period often (10) milliseconds for its first half cycle. After that, when the transistor **655** is turned on the period is preferably decreased to five (5) milliseconds. Pulse width modulated switch **262** is presently preferred to be a monolithic device.

Referring to FIG. **8**, a power supply comprises a bridge rectifier **710** that rectifies an input AC mains voltage. Power supply capacitors **720** charge with the rectified AC mains voltage to maintain an input DC voltage **725**. A presently preferred range for input DC voltage **725** is approximately one hundred (100) to four hundred (400) volts to allow for operation based upon worldwide AC mains voltages which range between eighty five (85) and two hundred sixty five (265) volts. The presently preferred power supply also includes harmonic filter components **910** which in combination with capacitors **720** reduce the harmonic current injected back into the power grid. Transformer **730** includes a primary winding **740** magnetically coupled to secondary winding **750**. The secondary winding **750** is coupled to a diode **760** that is designed to prevent current flow in the secondary winding **750** when the regulation circuit **850** is conducting (on-state). A capacitor **770** is coupled to the diode **760** in order to maintain a continuous voltage on a load **780** which has a feedback circuit coupled to it. A presently preferred feedback circuit comprises an optocoupler **800** and zener diode **820**. The output of optocoupler **800** is coupled to the feedback terminal **825** of regulation circuit **850**. The presently preferred regulation circuit **850** switches on and off at a duty cycle that is constant at a given input DC voltage **725**. A regulation circuit power supply bypass capacitor **860** is coupled to and supplies power to regulation circuit **850** when the regulation circuit **850** is in the on-state.

Operation of the power supply will now be described. An AC mains voltage is input through EMI filter **700** into bridge rectifier **710** which provides a rectified signal to power supply capacitors **720** that provide input DC voltage **725** to primary winding **740**. Regulation circuit **850**, which preferably operates at a constant frequency and about constant duty cycle at a given input DC voltage **725**, allows current to flow through primary winding **740** during its on state of each switching cycle and acts as open circuit in its off state. When current flows through primary winding **740** transformer **730** is storing energy, when no current is flowing through primary winding **740** any energy stored in transformer **730** is delivered to secondary winding **750**. Secondary winding **750** then provides the energy to capacitor **770**. Capacitor **770** delivers power to the load **780**. The voltage across the load **780** will vary depending on the amount of energy stored in the transformer **730** in each switching cycle which is in turn dependent on the length of time current is flowing through primary winding **740** in each switching cycle which is presently preferred to be constant at a given input DC voltage **725**. The presently preferred regulation circuit **850** allows the voltage delivered to the load to be maintained at a constant level.

It is presently preferred that the sum of the voltage drop across optocoupler **800** and the reverse break down voltage of zener diode **820** is approximately equal to the desired threshold level. When the voltage across the load **780** reaches the threshold level, current begins to flow through the optocoupler **800** and zener diode **820** that in turn is used to disable the regulation circuit **850**. Whenever regulation circuit **850** is in the off-state the regulation circuit power supply bypass capacitor **860** is charged to the operating supply voltage, which is presently preferred to be five point seven (5.7) volts by allowing a small current to flow from bypass terminal **865** to the regulation circuit power supply bypass capacitor **860**. Regulation circuit power supply bypass capacitor **860** is used to supply power to operate regulation circuit **850** when it is in the on-state.

When the regulation circuit **850** is disabled, an open circuit condition is created in primary winding **740** and transformer **730** does not store energy. The energy stored in the transformer **730** from the last cycle of regulation circuit **850** is then delivered to secondary winding **750** which in turn supplies power to the load **780**. Once the remaining

energy in transformer **750** is delivered to the load **780** the voltage of the load **780** will decrease. When the voltage at the load **780** decreases below the threshold level, current ceases to flow through optocoupler **800** and regulation circuit **850** resumes operation either instantaneously or nearly instantaneously.

The presently preferred regulation circuit **850** has a current limit feature. The current limit turns off the regulation circuit **850**, when the current flowing through the regulation circuit **850** rises above a current threshold level. In this way regulation circuit **850** can react quickly to changes such as AC ripple that occur in the rectified AC mains voltage, and prevents the propagation of the voltage changes to the load. The current limit increases the responsiveness of the regulation circuit to input voltage changes and delivers constant power output independent of the AC mains input voltage.

Although the presently preferred power supply of FIG. **8** utilizes current mode regulation and a feedback circuit that includes an optocoupler and zener diode, the present invention is not to be construed as to be limited to such a feedback method or circuit. Either current or voltage mode regulation may be utilized by the present invention without departing from the spirit and scope of the present invention so long as a signal indicative of the power supplied to the load is supplied to the feedback terminal **825** of the regulation circuit **850**. Additionally, although the presently preferred power supplies both utilize an optocoupler and zener diode as part of feedback circuits other feedback circuits may be utilized by the present invention without departing from the spirit and scope of the present invention.

Regulation circuit **850** also may have integrated soft start capabilities. When the device to which the power supply is coupled is switched on, a power up signal is generated within the internal circuitry of regulation circuit **850**. A power up signal is used to trigger soft start circuitry that reduces the duty cycle of the switch that operates within the pulse width modulated switch **262** for a predetermined period of time, which is presently preferred to be ten (10) milliseconds. Once soft start operation is completed, regulation circuit **850** operates according to its regular duty cycle.

Alternatively, or in addition to soft start functionality, regulation circuit **850** may also have frequency jitter functionality. That is, the switching frequency of the regulation circuit **850** varies according to an internal frequency variation signal. This has an advantage over the frequency jitter operation of FIG. **1** in that the frequency range of the presently regulation circuit **850** is known and fixed, and is not subject to the line voltage or load magnitude variations.

Referring to FIG. **9**, frequency variation circuit **405** and main oscillator **465** function as described with respect to FIG. **3**. In operation it is the variance of the high and low states of maximum duty cycle signal **607** that generates the frequency jitter functionality of the regulation circuit **850**. A presently preferred regulation circuit **850** and its steady-state operation is depicted and described in copending patent application Ser. No. 09/032,520 which is hereby incorporated by reference in its entirety.

The regulation circuit of FIG. **9** can be modified to include a second current source to further increase the period of main oscillation signal **415** which achieves the same result and function as described with respect of FIGS. **6** and **7**.

The soft start functionality of the presently preferred regulation circuit **850** of FIG. **9**, will shorten the on-time of switch **435** to less than the time of the maximum duty cycle signal **607** as long as the soft start enable signal **421** is provided and the magnitude of frequency variation signal **400** is less than the magnitude of main oscillation signal **415**.

The presently preferred regulation circuit **850** preferably comprises a monolithic device.

While the embodiments, applications and advantages of the present invention have been depicted and described, there are many more embodiments, applications and advantages possible without deviating from the spirit of the inventive concepts described herein. Thus, the inventions are not to be restricted to the preferred embodiments, specification or drawings. The protection to be afforded this patent should therefore only be restricted in accordance with the spirit and intended scope of the following claims.

What is claimed is:

1. A pulse width modulated switch comprising:

a first terminal;

a second terminal;

a switch comprising a control input, said switch allowing a signal to be transmitted between said first terminal and said second terminal according to a drive signal provided at said control input;

a frequency variation circuit that provides a frequency variation signal;

an oscillator that provides an oscillation signal having a frequency range, said frequency of said oscillation signal varying within said frequency range according to said frequency variation signal, said oscillator further providing a maximum duty cycle signal comprising a first state and a second state; and

a drive circuit that provides said drive signal when said maximum duty cycle signal is in said first state and a magnitude of said oscillation signal is below a variable threshold level.

2. The pulse width modulated switch of claim **1** wherein said first terminal, said second terminal, said switch, said oscillator, said frequency variation circuit and said drive circuit comprise a monolithic device.

3. The pulse width modulated switch of claim **1** wherein said frequency variation circuit comprises an additional oscillator that provides said frequency variation signal to said oscillator, said frequency of said oscillation signal varying within said frequency range according to said frequency variation signal.

4. The pulse width modulated switch of claim **1** further comprising a soft start circuit that provides a signal instructing said drive circuit to discontinue said drive signal when said magnitude of said oscillation signal is greater than a magnitude of said frequency variation signal.

5. The pulse width modulated switch of claim **4** wherein said additional oscillator provides a soft start signal, and wherein said soft start circuit ceases operation when said soft start signal is removed.

6. The pulse width modulated circuit of claim **5** wherein said additional oscillator further comprises

a comparator that provides a comparator signal when a magnitude of a reference signal is greater than or equal to a magnitude of said frequency variation signal, and

an inverter that receives said comparator signal and provides said soft start signal.

7. The pulse width modulated switch of claim **1** wherein said frequency of said oscillation signal varies within said frequency range with a magnitude of said frequency variation signal.

8. The pulse width modulated switch of claim **1** wherein said oscillator comprises a an input that receives said

frequency variation signal and a current source, wherein said frequency of said oscillation signal is a function of a sum of a magnitude of a current provided by said current source and a magnitude of said frequency variation signal.

9. The pulse width modulated switch of claim **1** further comprising;

a rectifier comprising a rectifier input and a rectifier output, said rectifier input receiving an AC mains signal and said rectifier output providing a rectified signal;

a power supply capacitor that receives said rectified signal and provides a substantially DC signal;

a first winding comprising a first terminal and a second terminal, said first winding receiving said substantially DC signal, said second terminal of said first winding coupled to said first terminal of said switch; and

a second winding magnetically coupled to said first winding.

10. The pulse width modulated switch of claim **1** wherein said variable threshold level is a function of a feedback signal received at a feedback terminal of said pulse width modulated switch.

11. A regulation circuit comprising:

a first terminal;

a second terminal;

a feedback terminal coupled to disable the regulation circuit;

a switch comprising a control input, said switch allowing a signal to be transmitted between said first terminal and said second terminal according to a drive signal provided at said control input;

a frequency variation circuit that provides a frequency variation signal;

an oscillator that provides an oscillation signal having a frequency range, said frequency of said oscillation signal varying within said frequency range according to said frequency variation signal, said oscillator further providing a maximum duty cycle signal comprising a first state and a second state; and

a drive circuit that provides said drive signal when said maximum duty cycle signal is in said first state and said regulation circuit is not disabled.

12. The regulation circuit of claim **11** wherein said frequency variation circuit comprises an oscillator that provides said frequency variation signal.

13. The regulation circuit of claim **11** further comprising a soft start circuit that provides a signal instructing said drive circuit to discontinue said drive signal according to a magnitude of said frequency variation signal.

14. The regulation circuit of claim **13** further wherein said frequency variation circuit provides a soft start signal, and wherein said soft start circuit ceases operation when said soft start signal is removed.

15. The regulation circuit of claim **14** wherein said frequency variation circuit further comprises

a comparator that provides a comparator signal when a magnitude of a reference signal is greater than or equal to a magnitude of said frequency variation signal, and

an inverter that receives said comparator signal and provides said soft start signal.

16. The regulation circuit of claim **11** wherein said first terminal, said second terminal, said switch, said frequency variation circuit, and said drive circuit comprise a monolithic device.

17. The regulation circuit of claim **11** further comprising;

a rectifier comprising a rectifier input and a rectifier output, said rectifier input receiving an AC mains signal and said rectifier output providing a rectified signal;

a power supply capacitor that receives said rectified signal and provides a substantially DC signal;

a first winding comprising a first terminal and a second terminal, said first winding receiving said substantially DC signal, said second terminal of said first winding coupled to said first terminal of said switch; and

a second winding magnetically coupled to said first winding.

18. The regulation circuit of claim **11** further comprising a current limit circuit that provides a signal instructing said drive circuit to discontinue said drive signal when a current received at said first terminal of said regulation circuit is above a threshold level.

* * * * *

EXHIBIT B

US006249876B1

(12) **United States Patent**
Balakrishnan et al.

(10) **Patent No.: US 6,249,876 B1**
(45) **Date of Patent: Jun. 19, 2001**

(54) **FREQUENCY JITTERING CONTROL FOR VARYING THE SWITCHING FREQUENCY OF A POWER SUPPLY**

(75) Inventors: **Balu Balakrishnan**; **Alex Djenguerian**, both of Saratoga; **Leif Lund**, San Jose, all of CA (US)

(73) Assignee: **Power Integrations, Inc.**, San Jose, CA (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **09/192,959**

(22) Filed: **Nov. 16, 1998**

(51) **Int. Cl.**[7] **G06F 1/04**
(52) **U.S. Cl.** **713/501**; 713/300; 713/503
(58) **Field of Search** 713/300, 320, 713/322, 500, 501, 503

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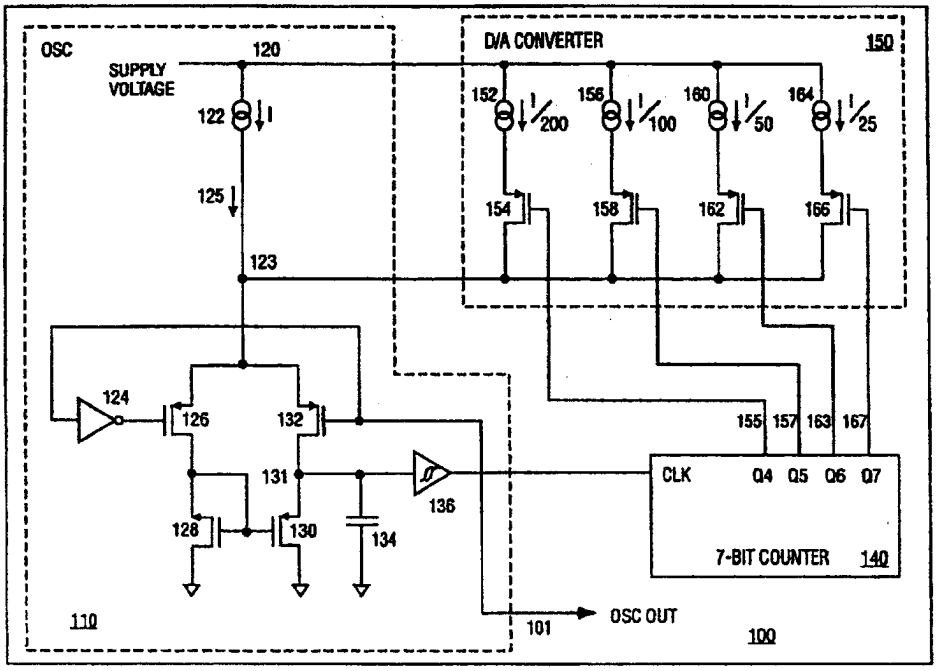
Primary Examiner—Dennis M. Butler
(74) *Attorney, Agent, or Firm*—Blakely, Sokoloff, Taylor & Zafman, LLP.

(57) **ABSTRACT**

EMI emission is reduced by jittering the switching frequency of a switched mode power supply. An oscillator with a control input for varying the oscillator's switching frequency generates a jittered clock signal. In one embodiment, the oscillator is connected to a counter clocked by the oscillator. The counter drives a digital to analog converter, whose output is connected to the control input of the oscillator for varying the oscillation frequency. In another embodiment, the oscillator is connected to a low frequency oscillator whose low frequency output is used to supplement the output of the oscillator for jittering the switching frequency. The invention thus deviates or jitters the switching frequency of the switched mode power supply oscillator within a narrow range to reduce EMI noise by spreading the energy over a wider frequency range than the bandwidth measured by the EMI test equipment.

32 Claims, 6 Drawing Sheets



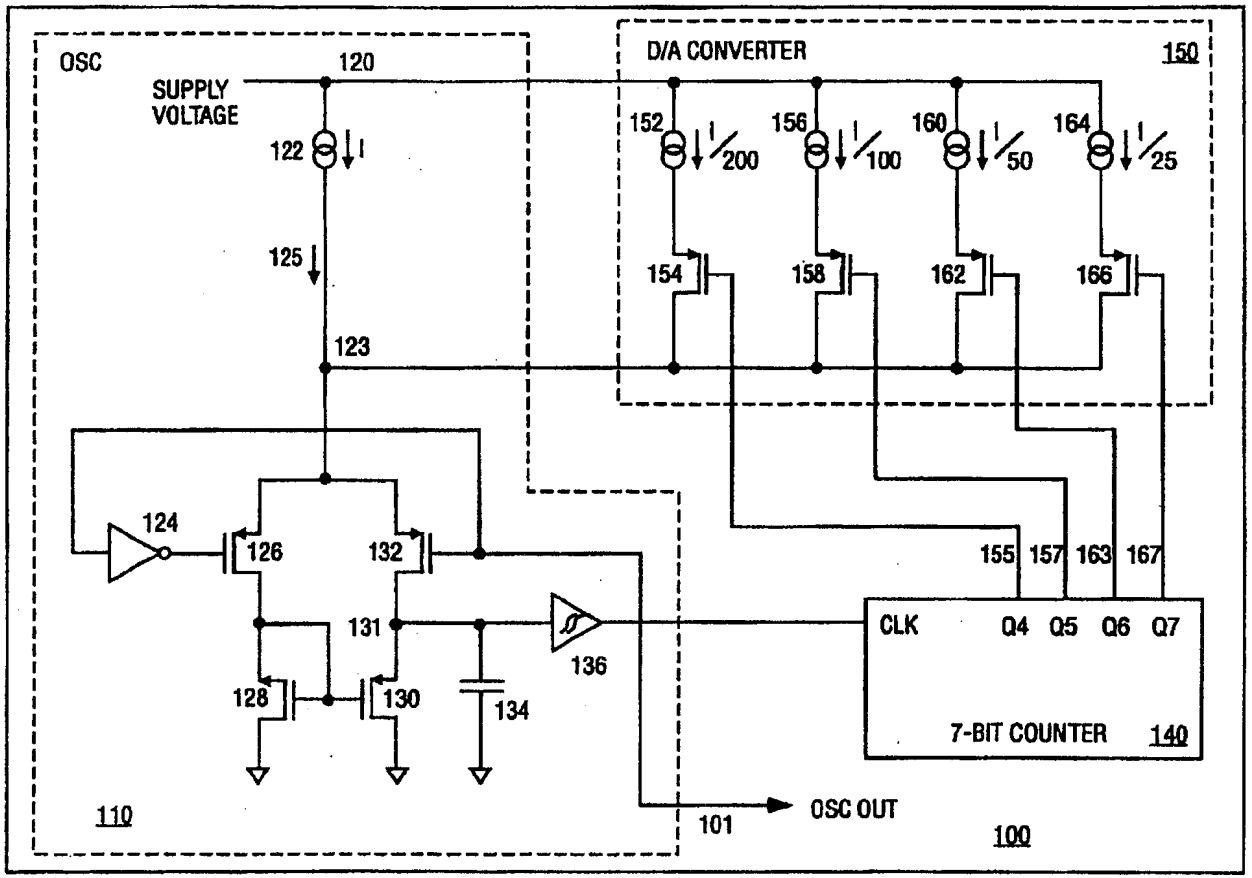
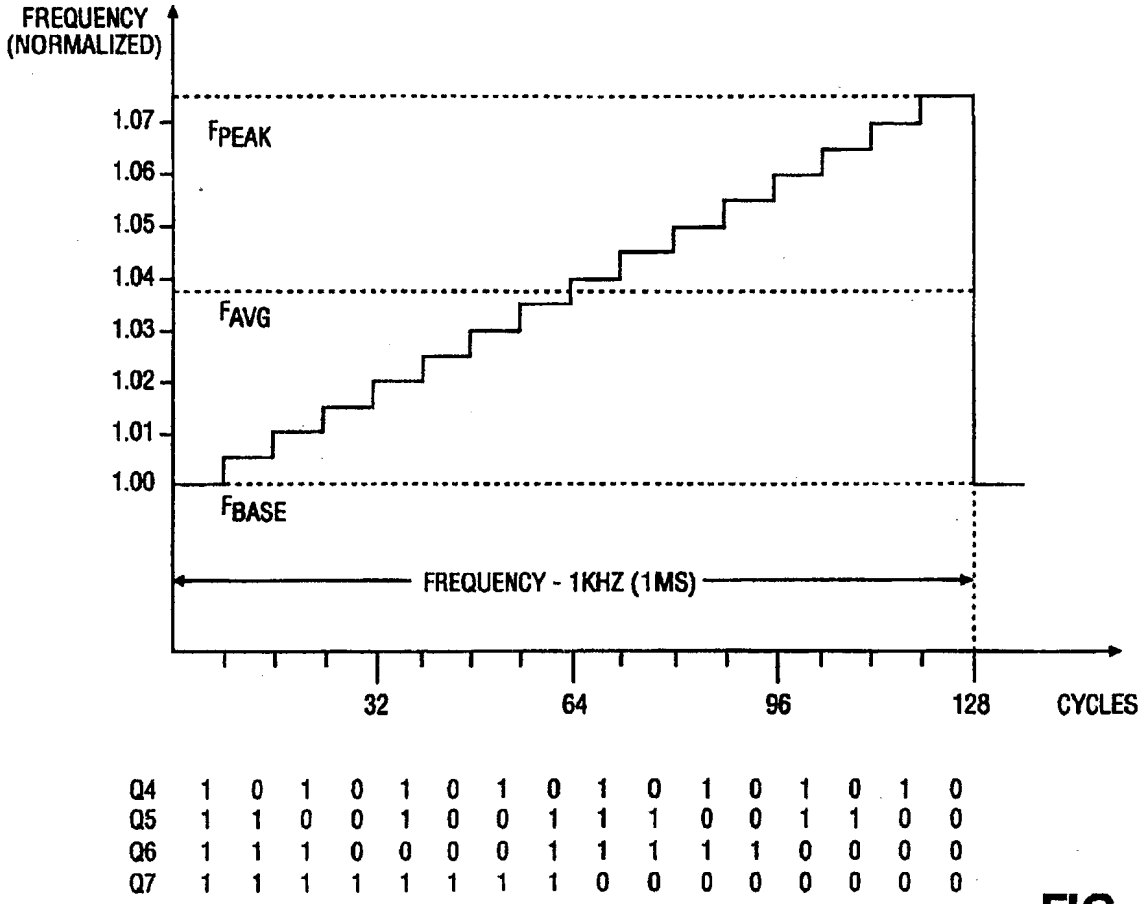

OSC
SUPPLY VOLTAGE
120
122
I
125
123
D/A CONVERTER
150
152
I/200
156
I/100
160
I/50
164
I/25
154
158
162
166
124
126
132
131
136
128
130
134
155
157
163
167
CLK
Q4
Q5
Q6
Q7
7-BIT COUNTER
140
110
101
OSC OUT
100

FIG. 1



Q4	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0
Q5	1	1	0	0	1	0	0	1	1	1	0	0	1	1	0	0
Q6	1	1	1	0	0	0	0	1	1	1	1	1	0	0	0	0
Q7	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0

FIG. 2

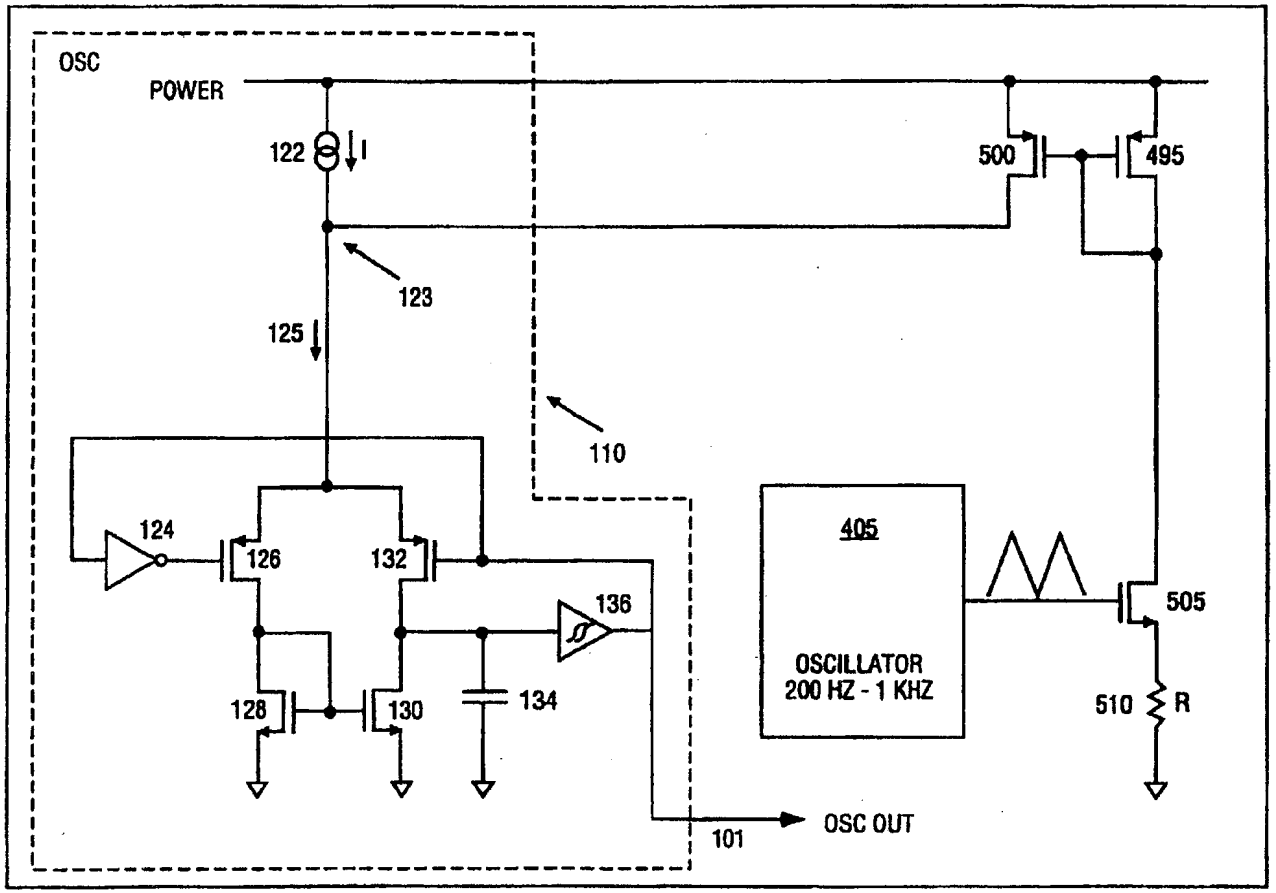

OSC
POWER
122
I
500
495
123
125
110
124
126
132
136
128
130
134
405
OSCILLATOR
200 HZ - 1 KHZ
505
510
R
101
OSC OUT

FIG. 3

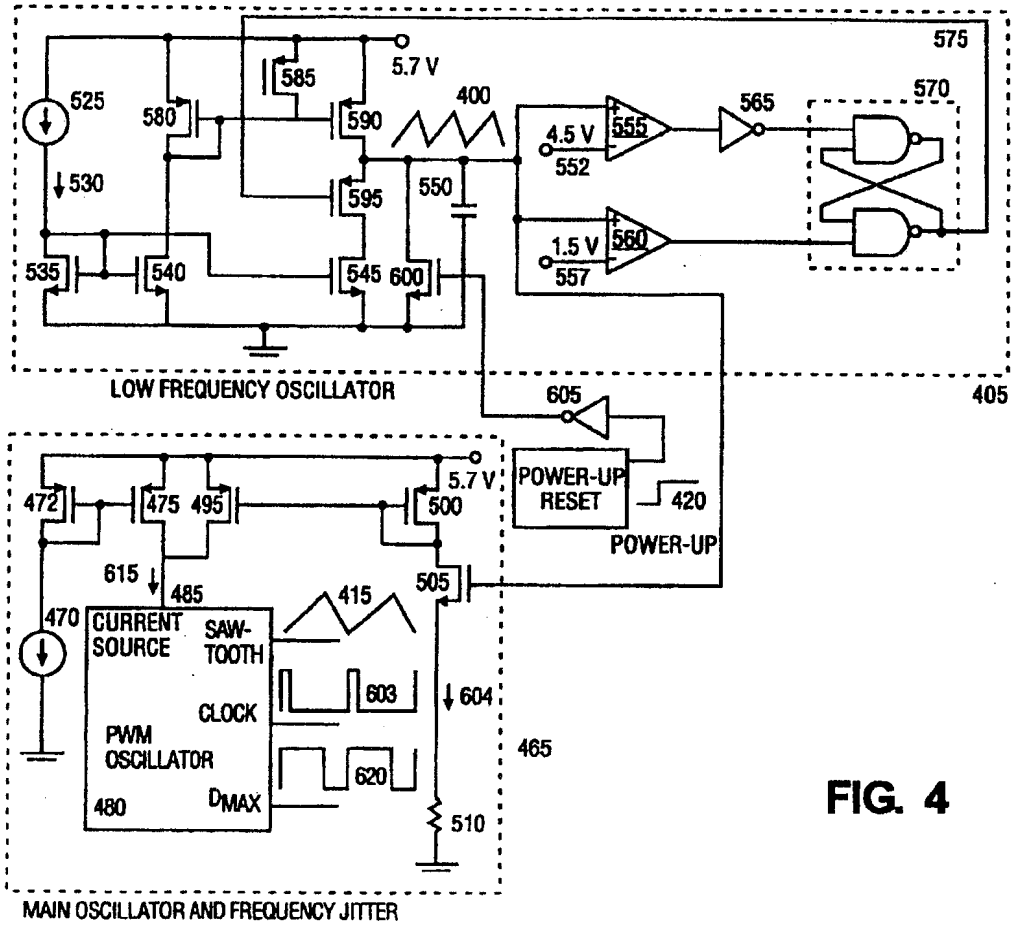

575
5.7 V
585
525
580
590
400
570
565
4.5 V
555
552
530
595
550
1.5 V
560
557
535
540
545
600
LOW FREQUENCY OSCILLATOR
405
605
5.7 V
POWER-UP RESET
420
POWER-UP
472
475
495
500
615
485
505
415
470
CURRENT SOURCE
SAW-TOOTH
603
604
CLOCK
PWM OSCILLATOR
620
465
480
DMAX
510
MAIN OSCILLATOR AND FREQUENCY JITTER

FIG. 4

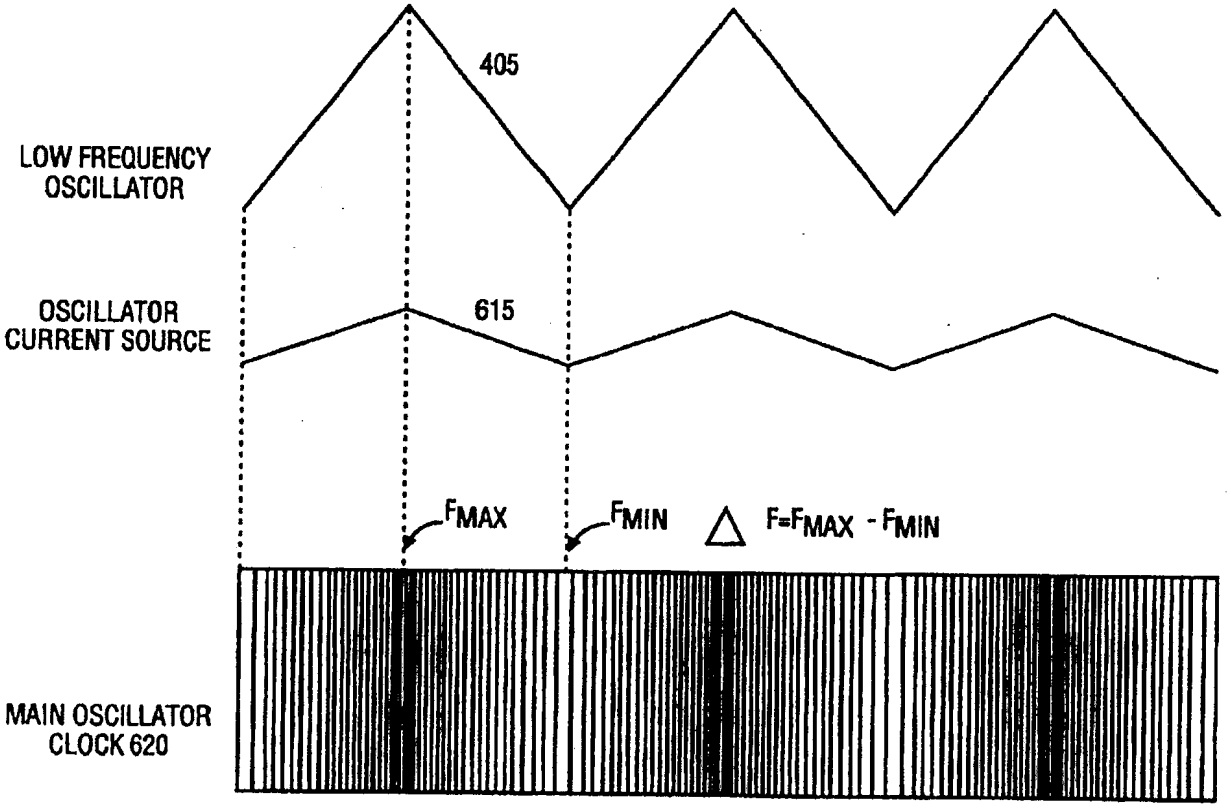
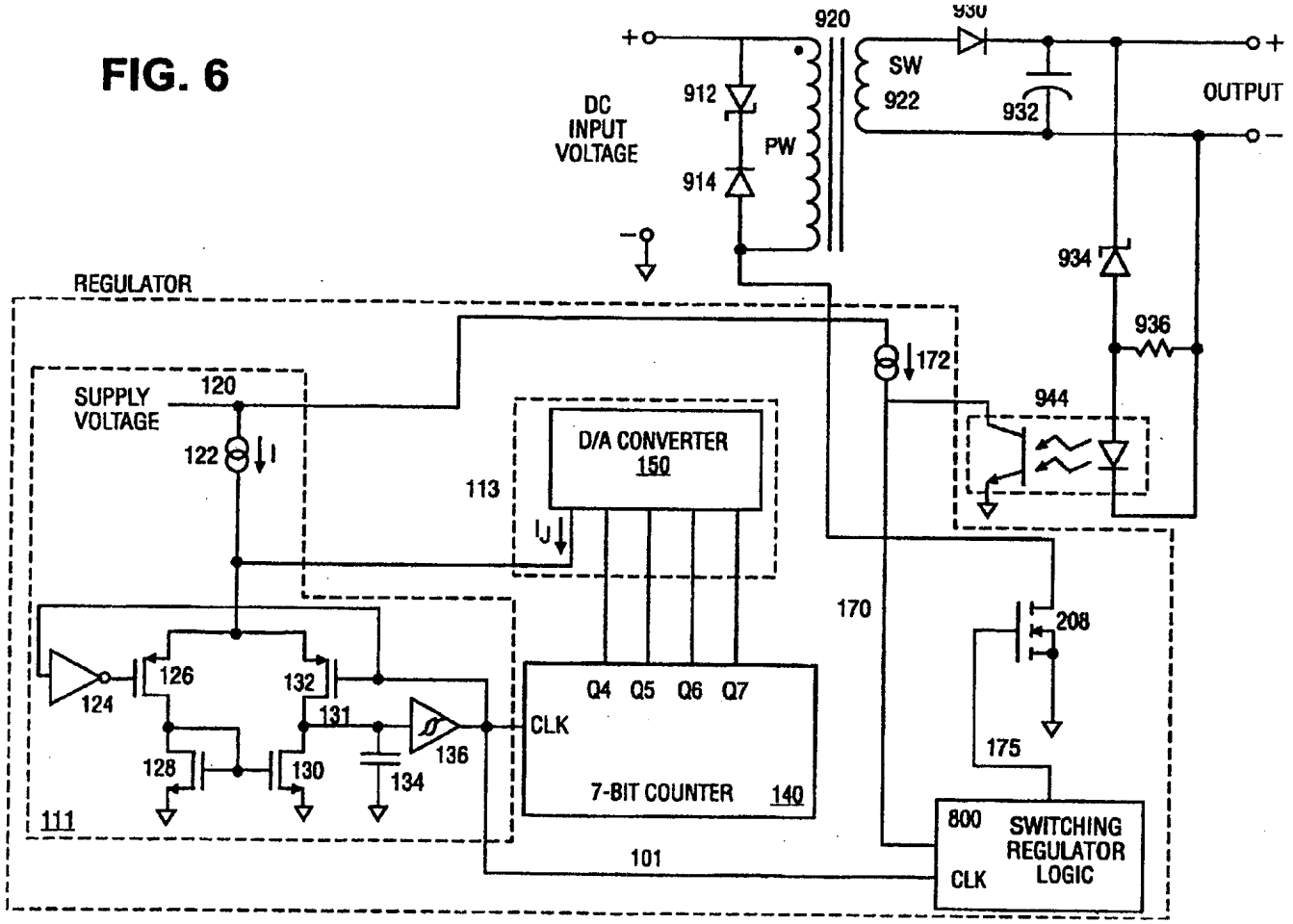

405
LOW FREQUENCY OSCILLATOR
OSCILLATOR CURRENT SOURCE
615
FMAX
FMIN
F=FMAX - FMIN
MAIN OSCILLATOR CLOCK 620

FIG. 5

FIG. 6


920
930
SW
922
912
914
PW
932
OUTPUT
DC
INPUT
VOLTAGE
934
936
944
REGULATOR
172
SUPPLY
VOLTAGE
120
122
I
113
D/A CONVERTER
150
IJ
170
208
126
132
124
131
136
128
130
134
Q4 Q5 Q6 Q7
CLK
7-BIT COUNTER
140
175
111
800
SWITCHING
REGULATOR
LOGIC
CLK
101

FREQUENCY JITTERING CONTROL FOR VARYING THE SWITCHING FREQUENCY OF A POWER SUPPLY

BACKGROUND

The present invention relates to an off-line switched mode control system with frequency jittering.

Many products rely on advanced electronic components to cost-effectively provide the product with the desired functionality. These electronic components require power regulation circuitry to supply them with a clean and steady source of power. The development of switched mode power supply technology has led to power supplies operating at high frequency to achieve small size and high efficiency. Each switched mode power supply typically relies on an oscillator switching at a fixed switching frequency or alternatively a variable frequency (such as in a ringing choke power supply).

Due to the high frequency operation relative to the frequency of an alternating current (AC) power line, switched mode power supplies can exacerbate problems associated with electromagnetic interference (EMI). EMI noise is generated when voltage and current are modulated by the switching power supply. This electrical noise can be transferred to the AC power line.

In addition to affecting the operation of other electronics within the vicinity of the power supply by conduction, EMI induced noise on a power line may radiate or leak from the power line and affect equipment which is not even connected to the power line. Both conducted and radiated electrical noise may adversely affect or interfere with the operation of the electronic equipment. For example, EMI noise generated by the switching power supply can cause problems for communication devices in the vicinity of the power supply. Radiated high frequency noise components may become a part of the AC mains signal and may be provided to other devices in the power grid. Further, power supply radiated EMI can interfere with radio and television transmissions.

To address EMI related interference, several specifications have been developed by government agencies in the United States and in the European Community. These agencies have established specifications that define the maximum amount of EMI that can be produced by various classes of electronic devices. Since power supplies generate a major component of the EMI for electronic devices, an important step in designing such supplies that conform to the specifications is to minimize EMI emission to the acceptable limits of the various specifications.

EMI may be reduced in a power supply by adding snubbers and input filters. These components reduce the noise transferred to the power line and by so doing, also reduce the electric and magnetic fields of noise generated by the power line. While these methods can reduce EMI, they usually complicate the design process as well as increase the production cost. In practice, noise filtering components are added in an ad hoc manner and on a trial-and-error basis during the final design process when EMI is found to exceed the compliance limits specified by the regulatory agencies. This inevitably adds unexpected costs to the products.

Further, extra components can undesirably increase the size and weight of the power supply and thus the resulting product.

SUMMARY OF THE INVENTION

EMI emission is reduced by jittering the switching frequency of a switched mode power supply. In one aspect, a frequency jittering circuit varies the switching frequency using an oscillator for generating a switching frequency signal, the oscillator having a control input for varying the switching frequency. A digital to analog converter is connected to the control input for varying the switching frequency, and a counter is connected to the output of the oscillator and to the digital to analog converter. The counter causes the digital to analog converter to adjust the control input and to vary the switching frequency.

Implementations of the invention include one or more of the following. The oscillator has a primary current source connected to the oscillator control input. A differential switch may be used with first and second transistors connected to the primary current source; a third transistor connected to the first transistor; and a fourth transistor connected to the second transistor at a junction. A capacitor and one or more comparators may be connected to the junction. The digital to analog converter has one or more current sources, with a transistor connected to each current source and to the counter. The primary current source may generate a current I and each of the current sources may generate a current lower than I. The current sources may generate binary weighted currents. The largest current source may generate a current which is less than about 0.1 of I.

In a second aspect, a method for generating a switching frequency in a power conversion system includes generating a primary current; cycling one or more secondary current sources to generate a secondary current which varies over time; and supplying the primary and secondary currents to a control input of an oscillator for generating a switching frequency which is varied over time.

Implementations of the invention include one or more of the following. A counter may be clocked with the output of the oscillator. The primary current may be generated by a current source. If the primary current is I, each of the secondary current sources may generate a supplemental current lower than I and which is passed to the oscillator control input. The supplemental current may be binary-weighted. The largest supplemental current may be less than approximately 0.1 of I.

In another aspect, a method for generating a switching frequency in a power conversion system includes generating a primary voltage; cycling one or more secondary voltage sources to generate a secondary voltage which varies over time; and supplying the primary and secondary voltages to a control input of a voltage-controlled oscillator for generating a switching frequency which is varied over time.

Implementations of the invention include one or more of the following. Where the primary voltage is V, each of the secondary voltage sources may generate a supplemental voltage lower than V which may be passed to the voltage-controlled oscillator. The supplemental voltage may be binary-weighted.

In another aspect, a frequency jittering circuit for varying a power supply switching frequency includes an oscillator for generating a switching frequency signal, the oscillator having a control input for varying the switching frequency; and means connected to the control input for varying the switching frequency.

Implementations of the invention include one or more of the following. The means for varying the frequency may include one or more current sources connected to the control input; and a counter connected to the output of the oscillator and to the one or more current sources. The oscillator may include a primary current source connected to the control

input; and a differential switch connected to the primary current source. The differential switch may have first and second transistors connected to the primary current source; a third transistor connected to the first transistor; and a fourth transistor connected to the second transistor at a junction. A capacitor and a comparator may be connected to the junction. If the primary current source generates a current I, each of the current sources may generate a second current lower than the current I, further comprising a transistor connected to each current source connected to the counter. The means for varying the frequency may include one or more voltage sources connected to the control input; and a counter connected to the output of the oscillator and to the one or more voltage sources. The oscillator may include a primary voltage source connected to the control input; and a differential switch connected to the primary voltage source. The means for varying the frequency may include a capacitor; a current source adapted to charge the capacitor; and means for alternatingly charging and discharging the capacitor. One or more comparators may be connected to the capacitor and the means for alternatingly charging and discharging the capacitor.

In yet another aspect, a power supply includes a transformer, an oscillator for generating a signal having a frequency, the oscillator having a control input for varying the frequency of the signal, the oscillator including a primary current source connected to the control input; a differential switch connected to the primary current source; a capacitor connected to the differential switch; and a comparator connected to the differential switch. The power supply also includes a digital to analog converter connected to the control input, the analog to digital converter having one or more current sources, wherein the primary current source generates a current I and each of the current sources generates a current lower than I. A counter is connected to the output of the oscillator and to the current sources of the digital to analog converter. Further, a power transistor is connected to the primary winding of the transformer so that when the power transistor is modulated, a regulated power supply output is provided.

In another aspect, a power supply includes a transformer connected to an input voltage. The power supply includes an oscillator for generating a signal having a frequency, the oscillator having a control input for varying the frequency of the signal, the oscillator including: a primary current source connected to the control input; a differential switch connected to the primary current source; a capacitor connected to the differential switch; and a comparator connected to the differential switch. A circuit for varying the frequency is connected to the control input, the circuit having a capacitor; a current source adapted to charge and discharge the capacitor; one or more comparators connected to the capacitor to the current source for alternatingly charging and discharging the capacitor. Further, a power transistor is connected to the oscillator and to the primary winding. The power transistor modulates its output in providing a regulated power supply output.

Advantages of the invention include one or more of the following. The jittering operation smears the switching frequency of the power supply over a wide frequency range and thus spreads energy outside of the bandwidth measured by the EMI measurement equipment. By changing the oscillator frequency back and forth, the average noise measured by the EMI measurement equipment is reduced considerably.

Further, the invention provides the required jittering without requiring a large area on the regulator chip to implement a capacitor in a low frequency oscillator. Further, the invention minimizes effects caused by leakage current from transistors and capacitors associated with a low frequency oscillator. Thus, the jittering operation can be maintained even at high temperature which can increase current leakage.

Additionally, the invention reduces the need to add extra noise filtering components associated with the EMI filter. Therefore a compact and inexpensive power supply system can be built with minimal EMI emissions.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a schematic diagram of a digital frequency jittering device.

FIG. 2 is a plot illustrating the operation of the device of FIG. 1.

FIG. 3 is a schematic diagram of an analog frequency jittering device.

FIG. 4 is a schematic diagram of an implementation of the device of FIG. 3.

FIG. 5 is a timing diagram illustrating the operation of the frequency jitter device of FIG. 4.

FIG. 6 is a schematic diagram of a switched mode power supply in accordance with the present invention.

DESCRIPTION

FIG. 1 shows a digital frequency jittering circuit **100**. The digital frequency jittering circuit **100** has a primary oscillator **110** which provides a clock signal to a counter **140**. The primary oscillator **110** typically operates between 100 kHz and 130 kHz. The counter **140** can be a seven bit counter. Each output of counter **140**, when clocked by primary oscillator **110**, represents a particular time interval. The outputs of the counter **140** are provided to a series of frequency jittering current sources **150**. The outputs of the series of frequency jittering current sources **150** are presented to the primary oscillator **110** to vary its frequency, as will be described below.

Primary oscillator **110** contains a primary current source **122** which provides a primary current (denoted as I) to node **123**. Current **125** to the node **123** is provided to the source of MOSFET transistors **126** and **132**. The drain of MOSFET transistor **126** is connected to the drain of an n-channel MOSFET transistor **128**. The source of transistor **128** is grounded, while the gate of the transistor **128** is connected to its drain. The gate of the transistor **128** is also connected to the gate of an n-channel MOSFET transistor **130**. The source of the transistor **130** is grounded while the drain is connected to the drain of the MOSFET transistor **132** at a node **131**. Transistors **126**, **128**, **130** and **132** form a differential switch. The output of comparator **136** is connected to the gate of the transistor **132** and to an inverter **124**. The output of inverter **124** is connected to the gate of transistor **126**. The comparator **136** has an input which is connected to node **131** and to a capacitor **134**. In combination, the transistors **126**, **128**, **130** and **132**, capacitor **134**, inverter **124**, current source **122** and comparator **136** form an oscillator. The output of the comparator **136** is provided as an oscillator output OSC_OUT **101** and is also used to drive the clock input of counter **140**.

Counter **140** has a plurality of outputs Q1–Q3 (not shown) which are not used. The remaining outputs Q4–Q7 are connected to a digital-to-analog (D-to-A) converter **150**, which may be implemented as a series of frequency jittering voltage sources or current sources. A Q4 output **155** is connected to the gate of a p-channel MOSFET transistor

154. A Q5 output 157 is connected to the gate of a p-channel MOSFET transistor 158. The Q6 output 163 is connected to the gate of a p-channel MOSFET transistor 162, and Q7 output 167 is connected to the gate of a p-channel MOSFET transistor 166. When D-to-A converter 150 is viewed as a plurality of current sources, the source of transistor 154 is connected to a jittering current source 152, which provides a current which is 1/200th of the current I generated by the current source 122. The source of MOSFET transistor 158 is connected to a current source 156 which provides a current that is 1/100th of the current I. The source of the MOSFET transistor 162 is connected to a jittering current source 160 which provides a current that is 1/50th of I. Finally, the source of the MOSFET transistor 166 is connected to a jittering current source 164 which provides a current that is 1/25th of the current I. The current sources 152, 156, 160 and 164 are binary-weighted, that is, the current source 164 provides twice the current provided by the current source 160, the current source 160 provides twice the current supplied by the current source 156 and the current source 156 provides twice the current provided by the current source 152.

Further, in one embodiment, the largest current source 164 may supply no more than 10% of the current I provided by the primary current source 122. The drain of transistors 154, 158, 162 and 166 are joined together such that the supplemental frequency jittering current sources of the D-to-A converter 150 can be provided to supplement the primary current source 122.

During operation, at every eight clock cycles, the counter output Q4 on line 155 changes state. Similarly, at every 16 clock cycles, the output Q5 on line 157 changes state and at every 32 clock cycles, the output Q6 on line 163 changes state, and every 64 clock cycles, the output Q7 on line 167 changes state. The entire counting cycle thereafter repeats itself.

Each time the output Q4 on line 155 is low, transistor 154 is turned on to inject current in the amount of I/200 to node 123 so that the total current 125 is 1.005I. Similarly, each time that the output Q5 on line 157 is low, transistor 158 is turned on to inject current in the amount of I/100 to node 123 so that the total current 125 is 1.01I. Further, each time that output Q6 on line 163 is low, transistor 162 is turned on to inject current in the amount of I/50 to node 123 so that the total current 125 is 1.02I. Finally, each time that the output Q7 on line 167 is low, the transistor 166 is turned on to inject current in the amount of I/25 to node 123 so that the total current 125 is 1.04I.

Additionally, when combinations of outputs Q4–Q7 are turned on, the outputs of the respective current sources 152, 156, 160 and 164 are added to the output of current source 122 to vary the frequency of the primary oscillator 110. In this manner, counter 140 drives a plurality of current sources to inject additional current to the main current source 122 such that the frequency of the primary oscillator 110 is varied.

The jittering operation of the embodiment of FIG. 1 is further illustrated in a chart in FIG. 2. A normalized operating frequency is plotted on the y-axis while the counting cycle as shown by the counter outputs Q4–Q7 is plotted on the x-axis. As shown in FIG. 2, as the counter counts upward to the maximum count of 128, the peak switching frequency is achieved. This peak switching frequency is normalized to be about 1.075 times the base switching frequency. Further, on average, the switching frequency is between 1.03 and 1.04 times the base switching frequency. Thus, the embodiment of FIG. 1 deviates the switching frequency of the oscillator within a narrow range. This deviation reduces EMI noise by spreading the energy over a wider frequency range than the bandwidth measured by the EMI test equipment such that the noise measured by the EMI test equipment is reduced considerably.

FIG. 3 shows an analog frequency jittering circuit. More details on the analog frequency jittering device are shown in co-pending U.S. application Ser. No. 09/080,774, entitled "OFFLINE CONVERTER WITH INTEGRATED SOFT START AND FREQUENCY JITTER," filed on May 18, 1998, the content of which is hereby incorporated by reference. In FIG. 3, the primary oscillator 110 provides an oscillator output on line OSC-OUT 101. An analog low frequency oscillator 405 is also provided. Primary oscillator 110 typically operates between a range of 30 to 300 kHz, while the low frequency oscillator 405 typically operates between a range of 5 Hz to 5 kHz. As discussed above, the switching frequency of the primary oscillator 110 is determined by the amount of current the primary oscillator uses to charge and discharge capacitor 134. The low frequency oscillator 405 varies this current within a narrow range to jitter the frequency of the primary oscillator 110.

The output of low frequency oscillator 405 is provided to a MOSFET transistor 505 connected to a resistor 510 and a current mirror including transistors 495 and 500. Transistor 500 is connected to node 123 so that extra current can be added to current source 122 feeding the primary oscillator. In this manner, the frequency of the primary oscillator 110 is shifted around a narrow range to reduce the EMI noise.

FIG. 4 shows a more detailed implementation of FIG. 3. As shown therein, main oscillator 465 has a current source 470 that is mirrored by current mirror transistors 472 and 475. Main oscillator drive current 615 is provided to current source input 485 of oscillator 480. The magnitude of the current input into current source input 485 determines the frequency of the oscillation signal 415 provided by oscillator 480. In order to vary the frequency of the oscillation signal 415, an additional current source 495 is provided within the main oscillator 465. The current source 495 is mirrored by current source mirror 500.

The current provided by current source 495 is varied as follows. Frequency variation signal 400 is provided to the gate of main oscillator transistor 505. As the magnitude of frequency variation signal 400 increases, so does the voltage at the source of main oscillator transistor 505 due to the increasing voltage at the gate of the transistor 505 and the relatively constant voltage drop between the gate and source of the transistor 505. As the voltage at the source of transistor 505 increases, so does the current 604 flowing through the resistor 510. The current flowing through the resistor 510 is the same as the current flowing through additional current source 500 which mirrors transistor 495.

Since the frequency variation signal 400 is a triangular waveform having a fixed period, as shown, the magnitude of the current input by additional current source mirror 500 will vary linearly with the magnitude of the rising and falling edges of the frequency variation signal 400. If the frequency variation signal 400 is a ramp signal, the frequency will linearly rise to a peak and then fall to its lowest value. In this way, the current 615 provided to current source input 485 of the oscillator 480 is varied in a known fixed range that allows for an easy and accurate frequency spread of the high frequency current. Further, the variance of the frequency is determined by the magnitude of the current provided by current source mirror 500, which is a function of the resistance of the resistor 510.

Frequency variation circuit 405 includes a current source 525 that produces a fixed magnitude current 530 that determines the magnitude of the frequency of the frequency variation signal 400. Although the current 530 has a fixed magnitude, the frequency variation signal can be generated utilizing a variable magnitude current. If such variable current is generated, the frequency spread is not fixed in time but varies with the magnitude of current 530. The fixed magnitude current 530 is fed into first transistor 535, mirrored by second transistor 540 and third transistor 545. The frequency variation signal 400 is generated by the charging and discharging of the capacitor 550. Frequency variation circuit capacitor 550 has a relatively low capacitance, which allows for integration into a monolithic chip in one embodiment of low frequency oscillator 405. The frequency variation signal 400 is provided to upper limit comparator 555 and lower limit comparator 560. The output of upper limit comparator 555 will be high when the magnitude of the frequency variation signal 400 exceeds the upper threshold voltage on line 552 which is about 4.5 volts. The output of lower limit comparator 560 will be low when the magnitude of frequency variation signal 400 drops below lower threshold voltage on line 557 which is about 1.5 volts. The output of upper limit comparator 555 is provided to the frequency variation circuit inverter 565 the output of which is provided to the reset input of frequency variation circuit latch 570. The set input of frequency variation circuit latch 570 receives the output of lower limit comparator 560.

In operation, the output of lower limit comparator 560 will be maintained high for the majority of each cycle of frequency variation signal 400 because the magnitude of frequency variation signal will be maintained between the upper threshold on line 552, 4.5 volts, and lower threshold on line 557, 1.5 volts. The output of upper limit comparator 555 will be low until the magnitude of frequency variation signal 400 exceeds upper level thresbold on line 552. This means that the reset input will receive a high signal when the magnitude of the frequency variation signal 400 rises above the upper threshold signal on line 552.

The charge signal 575 output by frequency variation circuit latch 570 will be high until the frequency variation signal 400 exceeds the upper threshold limit signal on line 552. When the charge signal 575 is high, transistors 585 and 595 are turned off. By turning off transistors 585 and 595, current can flow into the capacitor 550, which steadily charges capacitor 550 and increases the magnitude of frequency variation signal 400. The current that flows into the capacitor 550 is derived from current source 525 because the current through transistor 590 is mirrored from transistor 580, which in turn is mirrored from transistor 535.

During power up, when power-up signal 420 is low, the output of inverter 605 is high, which turns on transistor 600, causing frequency variation signal 400 to go low. The frequency variation signal 400 starts from its lowest level to perform a soft start function during its first cycle of operation.

Referring to FIGS. 4 and 5, FIG. 5 shows the operation of the analog frequency jittering device of FIG. 4. In FIG. 5, a frequency variation signal 405 is provided to the main oscillator 465. The magnitude of the current 615 is approximately the magnitude of the frequency variation signal 405, less the threshold voltage of transistor 505, and divided by the resistance of the resistor 510 plus the magnitude of the current produced by the current source 475. The current 615 varies with the magnitude of the frequency variation signal 405. The variation of the current 615 in turn varies the frequency of the oscillator clock.

Referring now to FIG. 6, a switched mode power supply is shown. Direct current (DC) input voltage is provided to a Zener diode 912 which is connected to a diode 914. The diodes 912–914 together are connected in series across a primary winding of a transformer 920. A secondary winding 922 is magnetically coupled to the primary winding of transformer 920. One terminal of the secondary winding 922 is connected to a diode 930, whose output is provided to a capacitor 932. The junction between diode 930 and capacitor 932 is the positive terminal of the regulated output. The other terminal of capacitor 932 is connected to a second terminal of the secondary winding and is the negative terminal of the regulated output. A Zener diode 934 is connected to the positive terminal of the regulated output. The other end of Zener diode 934 is connected to a first end of a light emitting diode in an opto-isolator 944. A second end of the light-emitting diode is connected to the negative terminal of the regulated output. A resistor 936 is connected between the negative terminal of the regulated output and the first end of the light-emitting diode of opto-isolator 944. The collector of the opto-isolator 944 is connected to current source 172. The output of current source 172 is provided to the switching regulator logic 800.

Connected to the second primary winding terminal is the power transistor 208. Power transistor 208 is driven by the switching regulator logic 800. Switching regulator logic 800 receives a clock signal 101 from an oscillator 111. A counter 140 also receives the clock signal 101 from the primary oscillator 111. The outputs of counter 140 are provided to D-to-A converter 150, which is connected to oscillator 111 for jittering the oscillation frequency. Alternatively, in lieu of counter 140 and a D-to-A converter 150, an analog low frequency jittering oscillator may be used.

The foregoing disclosure and description of the invention are illustrative and explanatory thereof, and various changes in the size, shape, materials, components, circuit elements, wiring connections and contacts, as well as in the details of the illustrated circuitry and construction and method of operation may be made without departing from the spirit of the invention.

What is claimed is:

1. A digital frequency jittering circuit for varying the switching frequency of a power supply, comprising:

an oscillator for generating a signal having a switching frequency, the oscillator having a control input for varying the switching frequency;

a digital to analog converter coupled to the control input for varying the switching frequency; and

a counter coupled to the output of the oscillator and to the digital to analog converter, the counter causing the digital to analog converter to adjust the control input and to vary the switching frequency.

2. The circuit of claim 1, wherein the oscillator further comprises a primary current source coupled to the oscillator control input.

3. The circuit of claim 2, further comprising a differential switch, including:

first and second transistors coupled to the primary current source;

a third transistor coupled to the first transistor; and

a fourth transistor coupled to the second transistor at a junction.

4. The circuit of claim 3, further comprising a capacitor coupled to the junction.

5. The circuit of claim 3, further comprising one or more comparators coupled to the junction.

6. The circuit of claim 2, wherein the digital to analog converter has one or more secondary current sources.

7. The circuit of claim 6, further comprising a transistor coupled between each secondary current source and the counter.

8. The circuit of claim 6, wherein the primary current source generates a current I and each of the secondary current sources generates a current lower than I.

9. The circuit of claim 8, wherein the secondary current sources generate binary weighted currents.

10. The circuit of claim 8, wherein the largest secondary current source generates a current which is less than about 0.1 of I.

11. A method for generating a switching frequency in a power conversion system, comprising:

generating a primary current;

cycling one or more secondary current sources to generate a secondary current which varies over time; and

combining the secondary current with the primary current to be received at a control input of an oscillator for generating a switching frequency which is varied over time.

12. The method of claim 11 further comprising the step of clocking a counter with the output of the oscillator.

13. The method of claim 11 wherein the primary current is generated by a current source.

14. The method of claim 11 wherein the primary current is I and each of the secondary current sources generates a supplemental current lower than I, and further comprising passing the supplemental current to the oscillator control input.

15. The method of claim 14 further comprising binary-weighting the supplemental current.

16. The method of claim 14 wherein the largest supplemental current is less than approximately 0.1 of I.

17. A method for generating a switching frequency in a power conversion system, comprising:

generating a primary voltage;

cycling one or more secondary voltage sources to generate a secondary voltage which varies over time; and

combining the secondary voltage with the primary voltage to be received at a control input of a voltage-controlled oscillator for generating a switching frequency which is varied over time.

18. The method of claim 17 further comprising clocking a counter with the output of the oscillator.

19. The method of claim 17 wherein the primary voltage is V and each of the secondary voltage sources generates a supplemental voltage lower than V, further comprising passing the supplemental voltage to the voltage-controlled oscillator.

20. The method of claim 19, wherein the supplemental voltage is binary-weighted.

21. A frequency jittering circuit for varying a power supply switching frequency, comprising:

an oscillator for generating a signal having a switching frequency, the oscillator having a control input for varying the switching frequency; and

means coupled to the control input for varying the switching frequency, including:

one or more current sources coupled to the control input; and

a counter coupled to the output of the oscillator and to the one or more current sources.

22. The circuit of claim 21 wherein the oscillator further comprises:

a primary current source coupled to the control input; and

a differential switch coupled to the primary source.

23. The circuit of claim 22 wherein the oscillator further comprises:

first and second transistors coupled to the primary current source;

a third transistor coupled to the first transistor; and

a fourth transistor coupled to the second transistor at a junction.

24. The circuit of claim 22 further comprising a capacitor and a comparator coupled to the junction.

25. The circuit of claim 22 wherein the primary current source generates a current I and each of said one or more current sources generates a current lower than I.

26. The circuit of claim 22 wherein the primary current source generates a current I and each of said one or more current sources generates a second current lower than the current I, further comprising a transistor coupled to each current source connected to the counter.

27. The circuit of claim 21 further comprising a transistor coupled to each current source and to the counter.

28. The circuit of claim 21 wherein the oscillator further comprises:

a primary voltage source coupled to the control input; and

a differential switch coupled to the primary voltage source.

29. The circuit of claim 21 wherein the means for varying the frequency further comprises:

a capacitor; and

a current source adapted to charge and discharge the capacitor.

30. The circuit of claim 29 further comprising:

one or more comparators coupled to the capacitor; and

means coupled to the capacitor for alternatingly charging and discharging the capacitor.

31. A power supply having a transformer coupled to an input voltage, the transformer having a primary winding, the power supply comprising:

an oscillator for generating a signal having a frequency, the oscillator having a control input for varying the frequency of the signal, the oscillator including:

a primary current source coupled to the control input;

a differential switch coupled to the primary current source;

a capacitor coupled to the differential switch; and

a comparator coupled to the differential switch;

a digital to analog converter coupled to the control input, the digital to analog converter having one or more current sources, wherein the primary current source generates a current I and each of said one or more current sources generates a current lower that I;

a counter coupled to the output of the oscillator and to the current sources of the digital to analog converter; and

a power transistor coupled to the oscillator and to one terminal of the primary winding, the power transistor modulating its output in providing a regulated power supply output.

32. A power supply having a transformer coupled to an input voltage, the transformer having a primary winding, the power supply comprising:

an oscillator for generating a signal having a frequency, the oscillator having a control input for varying the frequency of the signal, the oscillator including:

a primary current source coupled to the control input;

a differential switch coupled to the primary current source;

a capacitor coupled to the differential switch; and

a comparator coupled to the differential switch

a circuit for varying the frequency, the circuit coupled to the control input, including:

a capacitor;

a current source adapted to charge and discharge the capacitor;

one or more comparators coupled to the capacitor and coupled to the current source for alternatingly charging and discharging the capacitor; and

a power transistor coupled to the oscillator and to one terminal of the primary winding, the power transistor modulating its output in providing a regulated power supply output.

* * * * *

UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO. : 6,249,876 B1
DATED : June 19, 2001
INVENTOR(S) : Balakrishnan et al.

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Column 10,
Line 2, please insert -- current -- after "primary".
Line 3, please delete "wherein the oscillator further" and insert -- wherein the differential switch further --.

Signed and Sealed this

Nineteenth Day of February, 2002

Attest:

Attesting Officer

JAMES E. ROGAN
Director of the United States Patent and Trademark Office

EXHIBIT C

US005313381A

United States Patent [19]

Balakrishnan

[11] **Patent Number: 5,313,381**

[45] **Date of Patent: May 17, 1994**

[54] **THREE-TERMINAL SWITCHED MODE POWER SUPPLY INTEGRATED CIRCUIT**

[75] Inventor: **Balu Balakrishnan**, Saratoga, Calif.

[73] Assignee: **Power Integrations, Inc.**, Mountain View, Calif.

[21] Appl. No.: **938,704**

[22] Filed: **Sep. 1, 1992**

[51] **Int. Cl.**[5] **H02M 1/00**

[52] **U.S. Cl.** **363/147**; 363/21; 363/97; 363/131

[58] **Field of Search** 363/20, 21, 97, 131, 363/147

[56] **References Cited**

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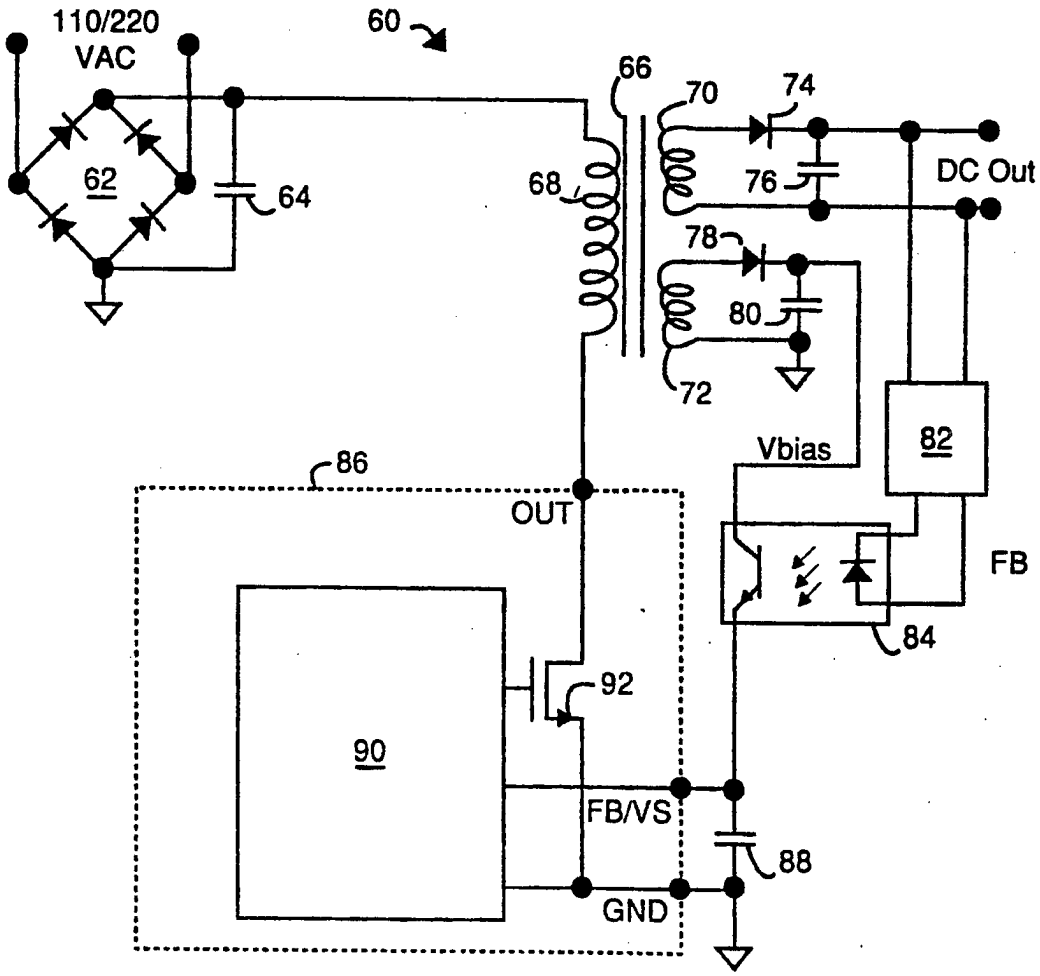
Primary Examiner—Jeffrey L. Sterrett
Attorney, Agent, or Firm—Thomas E. Schatzel

[57] **ABSTRACT**

An embodiment of the present invention is a three-terminal switched mode power supply chip with a signal terminal for accepting a combination of a feedback control signal and bias supply voltage to operate the chip. A feedback extraction circuit separates the feedback signal from the power supply voltage within the chip by sensing the excess current flowing through a shunt regulator.

11 Claims, 3 Drawing Sheets



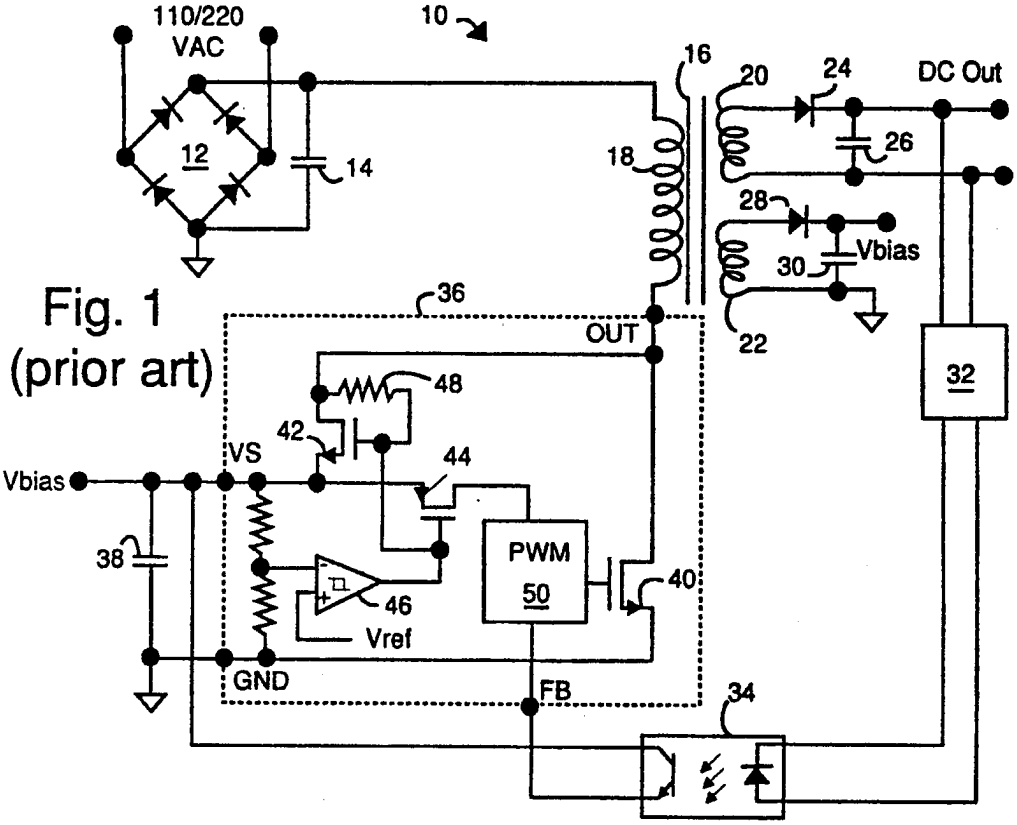


Fig. 1
(prior art)

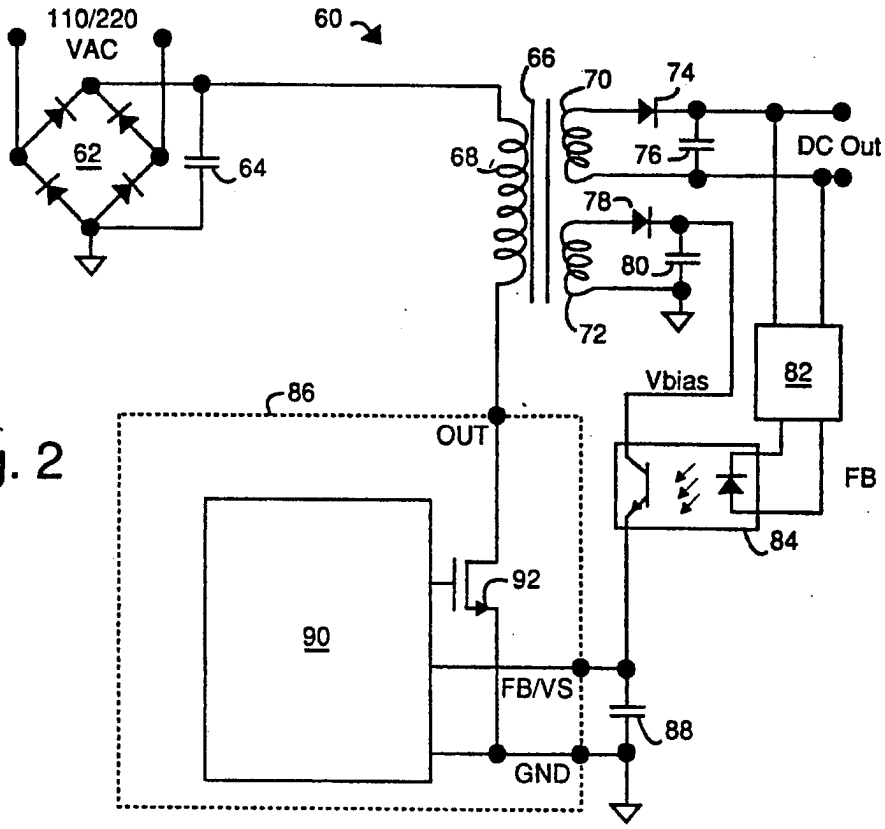
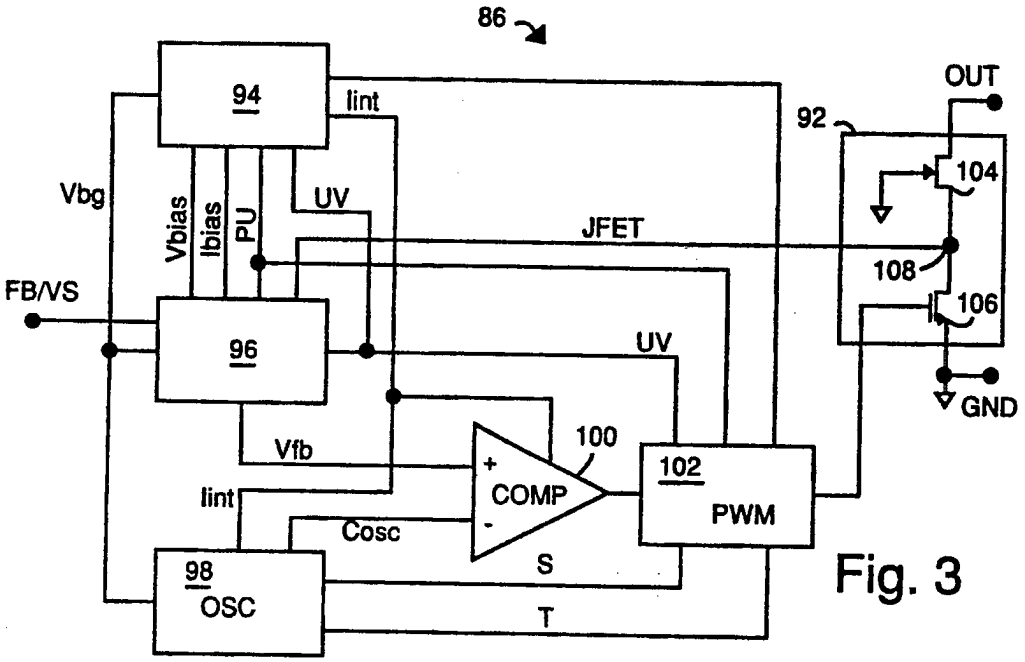


Fig. 2


86
94
Iint
OUT
92
104
Vbg
Vbias
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PU
UV
JFET
108
FB/VS
106
96
UV
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PWM
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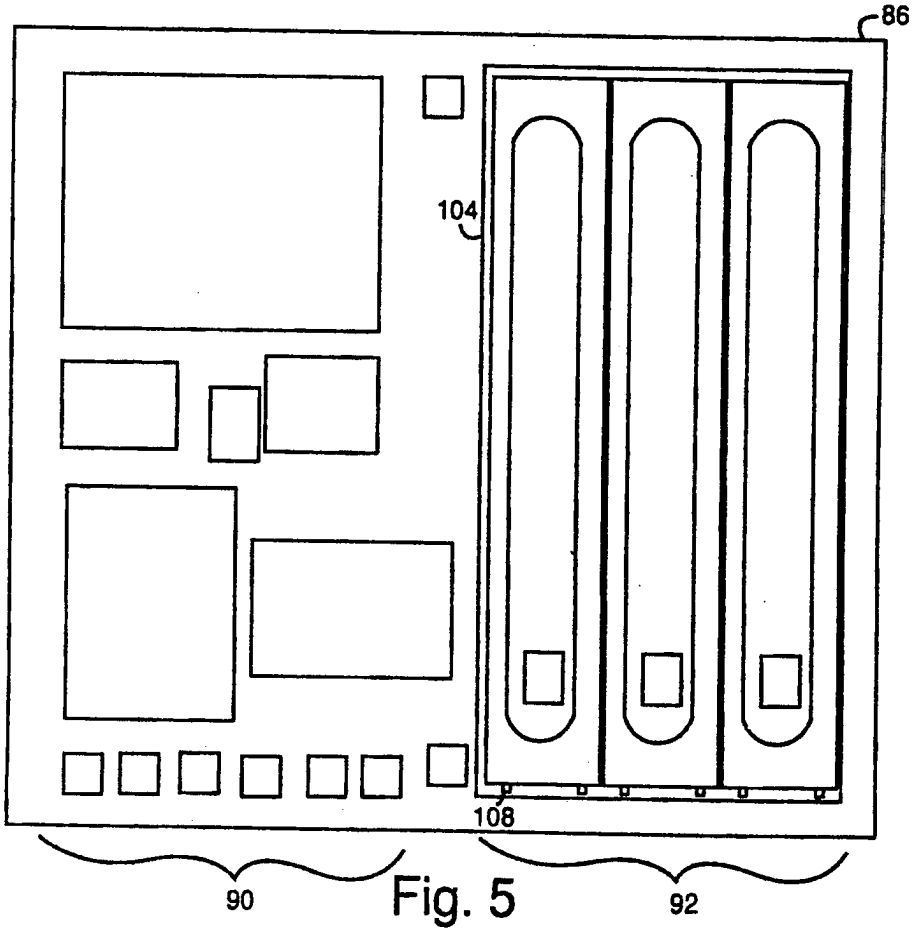
Fig. 3


86
104
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90
92

Fig. 5

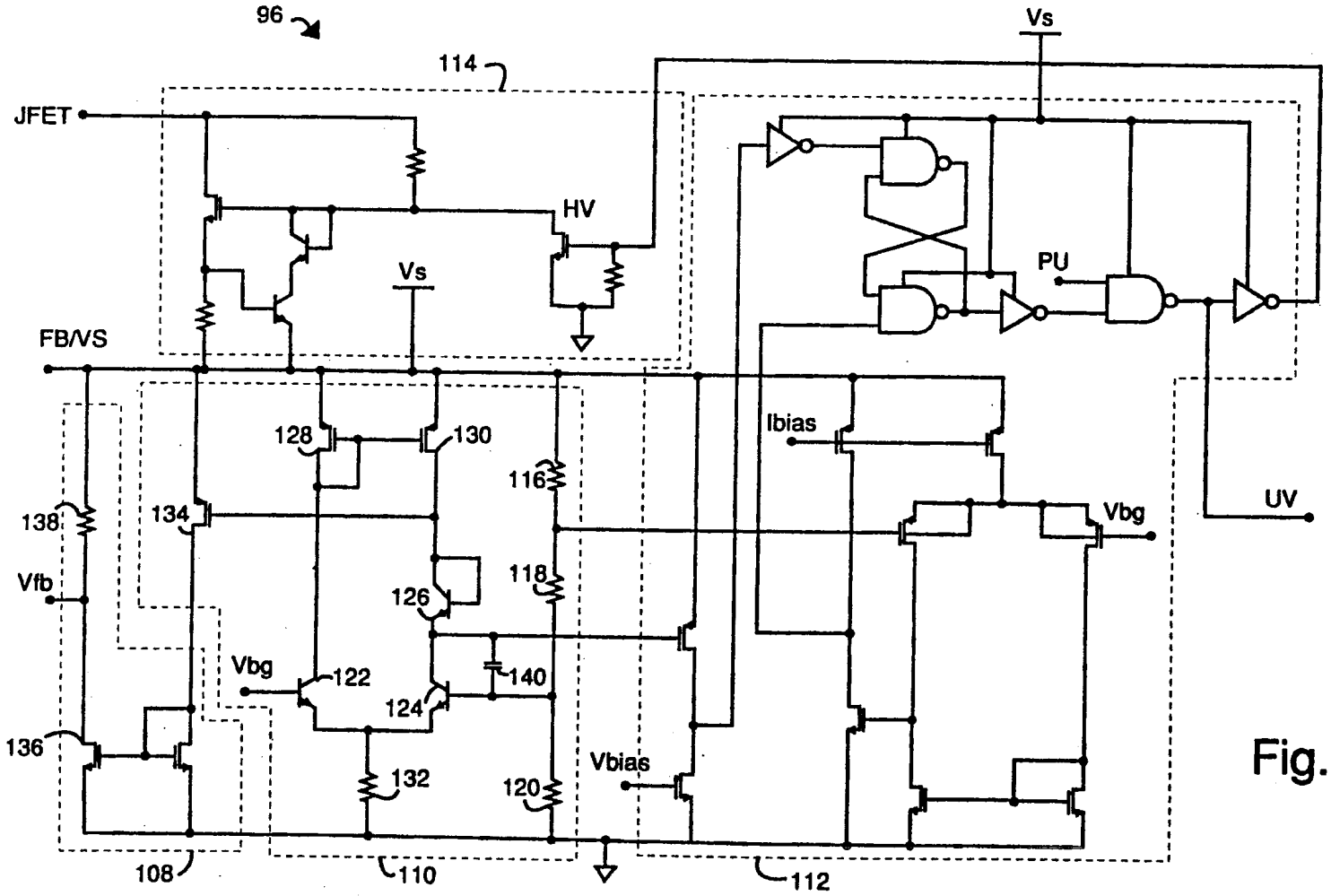

96
114
Vs
JFET
HV
Vs
PU
FB/VS
128
130
116
Ibias
UV
138
134
Vbg
Vfb
126
118
Vbg
122
140
124
136
132
120
Vbias
108
110
112

Fig. 4

THREE-TERMINAL SWITCHED MODE POWER SUPPLY INTEGRATED CIRCUIT

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to semiconductor integrated circuits and specifically to the integrated circuit devices used in switching power supplies with minimum numbers of pinouts.

2. Description of the Prior Art

The cost to manufacture a power supply is a principal concern in selecting between power supply types to be used in particular applications and the components selected to construct them. Switching power supplies have become cost competitive with much simpler linear power supplies because integrated circuit (IC) technology has advanced such that a majority of the complex switch mode circuits can be integrated on a single chip. As a rule of thumb, the fewer necessary pins on an IC package the lower will be the cost. A goal in switching power supply IC cost reduction has been the three-terminal package. One pin for power switching, one pin for ground and one pin for feedback. Conventional power supply ICs typically require as many as eight pins, thus limiting packaging options to the more expensive types.

FIG. 1 illustrates a prior art power supply 10 that includes a full-wave bridge rectifier 12, a filter capacitor 14, a transformer 16 with a primary winding 18 and a pair of secondary windings 20 and 22, a diode 24 and a capacitor 26 that provide DC output, a diode 28 and a capacitor 30 that provide a voltage Vbias, a compensated error amplifier 32, an opto-isolator 34, a four-pin switched mode power supply chip 36 and a Vbias smoothing capacitor 38 located near chip 36. Vbias provides power to operate chip 36. However, at power start-up, chip 36 will be without power because primary winding 18 will be open and no voltage will be induced into secondary winding 22 because chip 36 is not switching. To initiate such switching, a high voltage is tapped from the junction of a high voltage MOSFET 40 and the end of primary winding 18. This tap can supply enough current to start chip 36. A voltage regulator internal to chip 36 includes a high voltage preregulator transistor 42, a pass transistor 44 and an undervoltage comparator 46. During initial power-up when the voltage (Vs) across capacitor 38 is zero or near zero, a resistor 48 biases transistor 42 on and will pass current to charge up capacitor 38. When voltage Vs exceeds a predetermined threshold, comparator 46 will switch on transistor 44 and switch off transistor 42. Comparator 46 includes hysteresis, transistors 42 and 44 will not switch back unless the voltage Vs falls below a second threshold voltage that is lower than the first threshold voltage. With voltage Vs and transistor 44 on, power is supplied to a pulse width modulator (PWM) 50. This allows normal switching operation to begin and transistor 40 chops the current flowing through primary winding 18. Transformer 16 therefore begins operating and a voltage (V_{bias}) develops from secondary winding 22, diode 28 and capacitor 30. With V_{bias} being supplied across capacitor 38, comparator 46 operates to keep transistor 42 off and no further high voltage power is required. A feedback signal, proportional to the DC output, is returned by way of amplifier 32 and opto-isolator 34 to PWM 50. Chip 36 therefore requires a minimum of four pins, e.g., OUT, FB, VS and GND.

In the prior art, the need for a minimum of four terminals prevents the use of low cost three-terminal packages such as industry standards TO-220, DPAK, TO-5, and equivalents. A three-terminal switched mode power supply chip is therefore needed by the industry.

SUMMARY OF THE PRESENT INVENTION

It is therefore an object of the present invention to provide a three-terminal switched mode power supply chip.

Briefly, an embodiment of the present invention is a three-terminal switched mode power supply chip with a signal terminal for accepting a combination of a feedback control signal and bias supply voltage to operate the chip. A feedback extraction circuit provides for separating the feedback signal from the power supply voltage within the chip by sensing the excess current flow through a shunt regulator.

An advantage of the present invention is that an integrated circuit is provided that allows for a simple fully integrated power supply chip with very few pins and external components.

A further advantage of the present invention is that an integrated circuit is provided that is economical.

An advantage of the present invention is that an integrated circuit is provided that eliminates a high voltage pin and a high voltage transistor area conventionally necessary for an on chip preregulator.

An advantage of the present invention is that an integrated circuit is provided that allows for a fully integrated switching power supply with only one high-voltage pin, a low-voltage pin and ground.

These and other objects and advantages of the present invention will no doubt become obvious to those of ordinary skill in the art after having read the following detailed description of the preferred embodiment which is illustrated in the various drawing figures.

IN THE DRAWINGS

FIG. 1 is a schematic diagram of a prior art power supply;

FIG. 2 is a schematic diagram of a switched mode power supply of the present invention and includes a three-terminal switched mode power supply chip;

FIG. 3 is a block diagram of the switched mode power supply chip included in FIG. 2;

FIG. 4 is a schematic diagram of a feedback extractor, a Vs regulator and switching-noise filter, an undervoltage detector, and high voltage start-up regulator that are a part of the switched mode power supply chip included in FIG. 2; and

FIG. 5 is a chip map diagram of the switched mode power supply chip included in FIG. 2 showing the relative size of the high voltage MOSFET.

DETAILED DESCRIPTION OF THE EMBODIMENTS

FIG. 2 illustrates a power supply embodiment of the present invention, referred to by the general reference numeral 60. The power supply 60 comprises a full-wave bridge rectifier 62, a filter capacitor 64, a transformer 66 with a primary winding 68 and a pair of secondary windings 70 and 72, a diode 74 and a capacitor 76 that provide DC output, a diode 78 and a capacitor 80 that provides a voltage Vbias, a compensated error amplifier 82, an opto-isolator 84, a three-pin switched mode

power supply chip **86** and a vbias smoothing capacitor **88** located near chip **86**. V_{bias} is feed through opto-isolator **84** to provide combined DC output feedback and operational power (FB/VS) to a controller **90**. At power start-up, Vbias will be zero and chip **86** will be without power because primary winding **68** will be open and no voltage will be induced into secondary winding **72** because chip **86** is not switching. To initiate such switching, a low voltage is tapped from an internal junction within a high voltage MOSFET **92**. High voltage is present at the switched end of primary winding **68** when MOSFET **92** is off. Chip **86** therefore needs only three pins, OUT, GND and FB/VS, and may be mounted in an inexpensive plastic TO-220 industry standard type package.

MOSFET **92** is preferably similar to that described in U.S. Pat. No. 4,811,075, issued Mar. 7, 1989, to Klas H. Eklund. An insulated-gate, field-effect transistor and a double-sided, junction-gate field-effect transistor are connected in series on the same semiconductor chip to form a high-voltage MOS transistor. An extended drain region is formed on top of a substrate of opposite conductivity material. A top layer of material, similar to the substrate, is formed by ion implantation through the same mask window as the extended drain region. The top layer covers only a middle part of the extended drain which has ends that meet with a silicon dioxide layer above. Current flow through the extended drain is controlled by the substrate and top layer which pinch-off the extended drain between them in a familiar field-effect fashion. The drift region of the main power MOSFET **92** is used to drop the high line voltage to low voltage for biasing chip **86**.

Chip **86** accepts a combined feedback signal (Ifb) and internal low voltage supply current (Is) on a single pin. The supply current is approximately one milliams for CMOS versions of chip **86**. The supply current also serves as a bias current for the output of opto-isolator **84**. Opto-isolator **84** typically requires a bias current of 0.5–2.0 milliamps to operate optimally. In prior art power supplies, the opto-isolator bias current is in addition to current required by the switched mode power supply chip. The feedback signal secondary winding **70** modulates the current through the output transistor of opto-isolator **84**. The feedback modulation is extracted from the DC supply current by controller **90**.

FIG. **3** illustrates that three-terminal regulator chip **86** comprises MOSFET **92**, a bandgap and thermal shutdown **94**, a functional block **96**, an oscillator (OSC). **98**, a comparator (COMP) **100** and a pulse width modulator (PWM) **102**. An extracted feedback signal (Vfb) is output from block **96** and applied to COMP **100**. MOSFET **92** comprises the equivalent of a high voltage JFET **104** with a grounded gate and a low voltage MOSFET **106**. A tap **108** provides power from the junction of JFET **104** and MOSFET **106**.

As illustrated in FIG. **4**, functional block **96** comprises a feedback extractor **108**, a vs regulator and switching-noise filter **110**, an undervoltage detector **112**, and high voltage start-up regulator **114**. Regulator and filter **110** regulates the Vs voltage by comparing a bandgap reference voltage (Vbg) to a fraction of voltage Vs, as determined by the ratio of a group of resistors **116**, **118** and **120**. An error amplifier comprising a set of three transistors **122**, **124** and **126**, a pair of transistors **128** and **130**, and a resistor **132**. The output of the error amp drives a shunt transistor **134**. As long as there is sufficient supply current being input to FB/VS, the voltage Vs will be in regulation and any excess current will be shunted to ground through transistor **134**. This excess current is mirrored and converted into an extracted feedback voltage (Vfb) by a transistor **136** and a resistor **138**. During a power-up, the high voltage startup regulator **114** and capacitor **88** (FIG. **2**) provide the operating current and the voltage to start chip **86**. Once the power supply **60** is in operation, the secondary winding **72** and Vbias voltages begin to rise. When the DC output voltage (FIG. **2**) reaches a predetermined regulation level, error amplifier **82** turns on a LED in opto-isolator **84**. This, in turn, drives the output of opto-isolator **84** which starts conducting supply current to chip **86**. The current continues to increase until an excess current through transistor **134** is sufficient to bring Vfb into the active range of the sawtooth waveform (1–2 volts) from OSC **98** (Cosc, FIG. **3**), which is applied to the inverting input of COMP **100**. This sequence initiates voltage regulation in power supply **60**. When Vfb is above the normal active range, a maximum-on pulse width is sent to the output switch MOSFET **92**, resulting in maximum power output during start up. When Vfb is at or below the active range, the pulse width sent to MOSFET **92** will be minimum or zero. The feedback loop automatically adjusts the pulse width to remain in the active range to provide regulation of the output voltage at secondary winding **70**.

Stray switching currents in the Vs node from OSC **98**, Pwm **102** and power MOSFET **92** must be prevented from contaminating Vfb output. A low pass filter is included in regulator and filter **110** using a miller capacitor **140** coupled to transistor **124**. The cutoff frequency is approximately five KHz, which is low enough to effectively filter the high frequency switching noise (e.g., 100 KHz to 500 KHz) from modulating the gate of transistor **134**. However, this cutoff is high enough compared to the dominant pole of the regulator loop (e.g., 0.1 Hz to 100 Hz) so as to not affect the closed loop servo control stability.

Power supply current frequency components in the feedback signal frequency range (e.g., one KHz to ten KHz) can cause instability in the power supply loop. For example, if the supply current consumption of chip **86** varies with the pulse width applied to MOSFET **92**, an in-band signal would appear at Vfb and could result in an internal positive or negative feedback. The supply current should be independent of pulse width because nodes, such as the gate of MOSFET **92**, are charged and discharged once every cycle, regardless of pulse width. The net DC current is zero. Near zero pulse width, there may be an exception because the gate may not fully charge before the next discharge. This could cause some jitter at near zero load, which can be dealt with in several ways. For example, a resistor connected to input of a gate driver stage will consume current in the off state of MOSFET **92** that increases when the pulse width decreases, thus negating the problem.

FIG. **5** illustrates the large amount of chip area that is required by high voltage MOSFET **92**. JFET **104** consumes the greatest share of space.

Although the present invention has been described in terms of the presently preferred embodiments, it is to be understood that the disclosure is not to be interpreted as limiting. Various alterations and modifications will no doubt become apparent to those skilled in the art after having read the above disclosure. Accordingly, it is intended that the appended claims be interpreted as

covering all alterations and modifications as fall within the true spirit and scope of the invention.

What is claimed is:

1. A switched-mode power supply chip having exactly three electrical connections, comprising:

a first electrical connection terminal providing for a connection to a first end of a primary winding of a transformer with a second end of said primary winding connected to a source of direct current (DC) power;

a second electrical connection terminal providing for a ground reference for said source of DC power;

a third electrical connection terminal providing for a connection to a source of feedback current derived from a secondary winding of said transformer with a second end of said secondary winding connected to said ground reference for said source of DC power, wherein a combined feedback signal (Ifb) and internal low voltage supply current (Is) may be accepted on a single pin of said chip, such that said low voltage supply current may provide the operating power necessary for voltage regulation after a startup phase and during an operation phase of said chip;

a junction-type field effect transistor (JFET) having a drain electrode connected to the first electrical connection terminal, a gate electrode connected to the second electrical connection terminal, and a source electrode for providing a bias voltage that is reduced substantially from a voltage appearing at the first electrical connection terminal;

a metal oxide semiconductor field effect transistor (MOSFET) having a drain electrode connected to said source electrode of the JFET and thereby placing the MOSFET and JFET in series connection, a gate electrode for controlling a switching current through both the JFET and MOSFET in series, and a source electrode connected to the second electrical connection terminal;

voltage regulation means having an input connected to the third electrical connection terminal and an output connected to said gate of the MOSFET and having a bias voltage power supply connection to said source electrode of the JFET for switching the MOSFET and JFET on and off according to a feedback current received at the third electrical connection terminal, wherein a voltage output by said transformer is thereby regulated; and

input means connected to the third electrical connection terminal for accepting a combined feedback signal (Ifb) and internal low voltage supply current (Is) on a single pin, wherein said low voltage supply current provides operating power for the voltage regulation means after said startup and during said operation of said chip.

2. A semiconductor chip having as few as three external electrical connections, comprising:

a first electrical connection terminal providing for a pulse-width modulated output relative to an internal ground reference;

a second electrical connection terminal providing for connection of said internal ground reference to an external ground reference;

a third electrical connection terminal providing for a connection to a combined source of bias supply power and a feedback current that is controlled in part by said pulse-width modulated output;

voltage regulation means having an input connected to the third electrical connection terminal and an output connected to control the on and off duty cycle of an output transistor connected between the first and second electrical connection terminals according to said feedback current received at the third electrical connection terminal, wherein an output of a circuit including said chip is thereby regulated; and

input means connected to the third electrical connection terminal for accepting a combined feedback signal (Ifb) and internal low voltage supply current (Is) on a single pin for providing operating power with said low voltage supply current to the voltage regulation means after a startup and during operation of said chip.

3. The chip of claim 2, further comprising:

a first transistor having a drain electrode connected to the first electrical connection terminal, a gate electrode connected to the second electrical connection terminal, and a source electrode for providing a bias voltage that is reduced substantially from a voltage appearing at the first electrical connection terminal; and

a second transistor having a drain electrode connected to said source electrode of the first transistor and thereby placing the second transistor and first transistor in series connection, a gate electrode for controlling a switching current through both the first transistor and second transistor in series, and a source electrode connected to the second electrical connection terminal.

4. A switched-mode power supply chip having as few as three electrical connections, comprising:

a first electrical connection terminal providing for a connection to a first end of a primary winding of a transformer with a second end of said primary winding connected to receive a source of direct current (DC) power;

a second electrical connection terminal providing for a ground reference for said source of DC power;

a third electrical connection terminal providing for a connection to a sourced of feedback current derived from a secondary winding of said transformer with a second end of said secondary winding connected to said ground reference for said source of DC power;

voltage regulation means having an input connected to the third electrical connection terminal and an output connected to control an output transistor connected between the first and second electrical connection terminals on and off according to a feedback current received a the third electrical connection terminal, wherein a voltage output by said transformer is thereby regulated and the voltage regulation means is provided with a bias voltage power supply current during operation of said chip; and

input means connected to the third electrical connection terminal for accepting a combined feedback signal (Ifb) and internal low voltage supply current (Is) on a single pin, wherein said low voltage supply current provides operating power for the voltage regulation means after said startup and during said operation of said chip.

5. The chip of claim 4, further comprising:

a first transistor having a drain electrode connected to the first electrical connection terminal, a gate

electrode connected to the second electrical connection terminal, and a source electrode for providing a bias voltage to the voltage regulation means that is reduced substantially from a voltage appearing at the first electrical connection terminal; and

a second transistor having a drain electrode connected to said source electrode of the first transistor and thereby placing the second transistor and first transistor in series connection, a gate electrode for controlling a switching current through both the first transistor and second transistor in series, and a source electrode connected to the second electrical connection terminal.

6. The chip of claim 5, wherein:

the first transistor is a junction-type field effect transistor (JFET);

the second transistor is a metal oxide semiconductor field effect transistor (MOSFET); and

the voltage regulation means comprises a pulse width modulator.

7. The chip of claim 4, wherein:

the voltage regulation means further comprises a feedback extractor for separating said feedback signal (Ifb) from said internal low voltage supply current (Is), a Vs regulator and switching-noise filter for separating said feedback signal (Ifb) from said internal low voltage supply current (Is) and then stabilizing it for use by the voltage regulation means.

8. The chip of claim 7, wherein:

the voltage regulation means further includes a high-voltage startup regulator connected to the first electrical connection terminal for providing for a controlled voltage power supply source to the remaining parts of the voltage regulation means during said startup of said chip.

9. The chip of claim 7, wherein:

the voltage regulation means and said feedback extractor include means for monitoring whether there is a sufficient supply current being input to the third electrical connection terminal such that said voltage Vs may be in regulation and that provides for a shunting of an excess current to ground and a mirroring and a converting said shunted excess current to produce an extracted feedback voltage (Vfb).

10. A power supply, comprising:

a three-terminal switched-mode power supply chip, including:

a first electrical connection terminal providing for a connection to a first end of a primary winding of a transformer with a second end of said primary winding connected to receive a source of direct current (DC) power;

a second electrical connection terminal providing for a ground reference for said source of DC power;

a third electrical connection terminal providing for a connection to a source of feedback current derived from a secondary winding of said transformer with a second end of said secondary winding connected to said ground reference for said source of DC power;

voltage regulation means having an input connected to the third electrical connection terminal and an output connected to control an output transistor connected between the first and second electrical connection terminals on and off according to a feedback current received at the third electrical connection terminal for regulating a voltage output by said transformer and for providing the voltage regulation means with a bias voltage power supply current during operation of said chip; and

input means connected to the third electrical connection terminal for accepting a combined feedback signal (Ifb) and internal low voltage supply current (Is) on a single pin, wherein said low voltage supply current provides operating power for the voltage regulation means after said startup and during said operation of said chip;

a transformer, including a primary winding and a secondary winding, connected at a first end of said primary winding to said first electrical connection terminal of the switched-mode power supply chip, and connected at a second end of said primary winding to receive a source of direct current (DC) power;

DC output means for converting an output of a said secondary winding of the transformer to a regulated DC output voltage; and

bias means for converting a voltage induced in said secondary winding of the transformer to a bias supply and connected to said third electrical connection terminal to power the switched-mode power supply chip.

11. The power supply of claim 10, wherein:

the power supply chip further includes:

a first transistor having a drain electrode connected to the first electrical connection terminal, a gate electrode connected to the second electrical connection terminal, and a source electrode for providing a bias voltage that is reduced substantially from a voltage appearing at the first electrical connection terminal; and

a second transistor having a drain electrode connected to said source electrode of the first transistor and thereby placing the second transistor and first transistor in series connection, a gate electrode for controlling a switching current through both the first transistor and second transistor in series, and a source electrode connected to the second electrical connection terminal.

* * * * *

IN THE UNITED STATES DISTRICT COURT
FOR THE DISTRICT OF DELAWARE

POWER INTEGRATIONS, INC., a Delaware corporation, Plaintiff, v. BCD SEMICONDUCTOR CORPORATION, a California corporation, SHANGHAI SIM-BCD SEMICONDUCTOR MANUFACTURING, CO., LTD, a China corporation, Defendants.	Civil Action No. _____

NOTICE OF RELATED CASE
UNDER DELAWARE LOCAL RULE 3.1

I. RELATED CASES

Power Integrations, Inc., v. Motorola, Inc., Civil Action No. 98-490 JJF (D. Del.)

Power Integrations, Inc. v. Fairchild Semiconductor International, Inc. and Fairchild Semiconductor Corporation, Civil Action No. 04-1371 JJF (D. Del.)

Fairchild Semiconductor Corporation, Intersil Americas Inc., and Intersil Corporation v. Power Integrations, Inc., Civil Action No. 07-187-JJF (D. Del.)

Power Integrations, Inc. v. BCD Semiconductor Corporation and Shanghai SIM-BCD Semiconductor Manufacturing, Co., Ltd., Civil Action No. C 07-03137 WHA (N.D. Cal.)

II. DISCUSSION

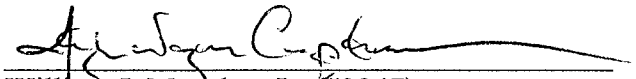
Delaware Civil Local Rule 3.1(b) provides that "[c]ounsel for a plaintiff in a civil action shall indicate on the civil cover sheet of such action and one or more other civil actions or proceedings previously decided or currently filed in this District or any other court . . . . (2) involve the same or substantially the same parties . . . [or] (3) involve the same patent or the

same trademark." Pursuant to this Rule, Plaintiff Power Integrations, Inc. submits the following statement.

This case is an action for infringement of United States Patent Nos. 6,107,851 ("the '851 patent"); 6,249,876 ("the '876 patent"); and 5,313,381 ("the '381 patent"), all of which are owned by Power Integrations. At present, Power Integrations has two pending cases before Judge Farnan, one of which involves both the '876 patent and the '851 patent, and Judge Farnan also presided over an earlier Power Integrations case that involved the '381 patent. During the course of these cases, Judge Farnan has construed the claims of all three of the patents-in-suit in this matter, and Judge Farnan has also presided over jury trials on all three patents. In both cases involving the patents-in-suit, Delaware juries found that the patents were valid and infringed, including during a recent jury trial in September 2007, which affirmed the validity of the '876 and '851 patents.

Power Integrations initially filed a substantially identical complaint in the U.S. District Court for the Northern District of California, but no substantive proceedings have occurred in that matter, and Power Integrations is voluntarily dismissing that complaint pursuant to Federal Rule of Civil Procedure 41(a) in favor of the present action.

Dated: October 15, 2007 FISH & RICHARDSON P.C.

By: 

William J. Marsden, Jr. (#2247)
Kyle Wagner Compton (#4693)
919 N. Market Street, Suite 1100
P.O. Box 1114
Wilmington, DE 19801
Telephone: (302) 652-5070
Facsimile: (302) 652-0607

Frank E. Scherkenbach
225 Franklin Street
Boston, MA 02110-2804
Telephone: (617) 542-5070
Facsimile: (617) 542-8906

Howard G. Pollack
Michael R. Headley
500 Arguello Street, Suite 500
Redwood City, CA 94063
Telephone: (650) 839-5070
Facsimile: (650) 839-5071

ATTORNEYS FOR PLAINTIFF
POWER INTEGRATIONS, INC.

CIVIL COVER SHEET

The JS-44 civil cover sheet and the information contained herein neither replace nor supplement the filing and service of pleadings or other papers as required by law, except as provided by local rules of court. This form, approved by the Judicial Conference of the United States in September 1974, is required for the use of the Clerk of Court for the purpose of initiating the civil docket sheet. (SEE INSTRUCTIONS ON THE REVERSE OF THE FORM.)

I. (a) PLAINTIFFS
Power Integrations, Inc., a California Corporation
(b) County of Residence of First Listed Plaintiff
(EXCEPT IN U.S. PLAINTIFF CASES)

DEFENDANTS
BCD Semiconductor Corporation, a California corporation, Shanghai Sim-BD Semiconductor Manufacturing, Co., Ltd. a China corporation
County of Residence of First Listed Defendant
(IN U.S. PLAINTIFF CASES ONLY)
NOTE: IN LAND CONDEMNATION CASES, USE THE LOCATION OF THE LAND INVOLVED

(c) Attorneys (Firm Name, Address, and Telephone Number)
William J. Marsden, Jr. (#2247)
Kyle Wagner Compton (#4693)
Fish & Richardson P.C.
919 N. Market Street, Suite 1100
Wilmington, Delaware 19899-1114
(302) 652-5070

Attorneys (If Known)

II. BASIS OF JURISDICTION (Place an "X" in One Box Only)

- ☐ 1. U.S. Government Plaintiff
- ☒ 3. Federal Question (U.S. Government Not a Party)
- ☐ 2. U.S. Government Defendant
- ☐ 4. Diversity (Indicate Citizenship of Parties in Item III)

III. CITIZENSHIP OF PRINCIPAL PARTIES (Place an "X" in One Box for Plaintiff and One Box for Defendant)
(For Diversity Cases Only)

	PTF	DEF		PTF	DEF
Citizen of This State	☐ 1	☐ 1	Incorporated *or* Principal Place of Business In this State	☐ 4	☐ 4
Citizen of Another State	☐ 2	☐ 2	Incorporated *and* Principal Place of Business In Another State	☐ 5	☐ 5
Citizen or Subject of a Foreign Country	☐ 3	☐ 3	Foreign Nation	☐ 6	☐ 6

IV. NATURE OF SUIT (Place an "X" in One Box Only)

CONTRACT
- ☐ 110 Insurance
- ☐ 120 Marine
- ☐ 130 Miller Act
- ☐ 140 Negotiable Instrument
- ☐ 150 Recovery of Overpayment & Enforcement of Judgment
- ☐ 151 Medicare Act
- ☐ 152 Recovery of Defaulted Student Loans (Excl. Veterans)
- ☐ 153 Recovery of Overpayment of Veteran's Benefits
- ☐ 160 Stockholders' Suits
- ☐ 190 Other Contract
- ☐ 195 Contract Product Liability
- ☐ 196 Franchise

TORTS
PERSONAL INJURY
- ☐ 310 Airplane
- ☐ 315 Airplane Product Liability
- ☐ 320 Assault, Libel & Slander
- ☐ 330 Federal Employers' Liability
- ☐ 340 Marine
- ☐ 345 Marine Product Liability
- ☐ 350 Motor Vehicle
- ☐ 355 Motor Vehicle Product Liability
- ☐ 360 Other Personal Injury

PERSONAL INJURY
- ☐ 362 Personal Injury- - - Med. Malpractice
- ☐ 365 Personal Injury Product Liability
- ☐ 368 Asbestos Personal Injury Product Liability

PERSONAL PROPERTY
- ☐ 370 Other Fraud
- ☐ 371 Truth In Lending
- ☐ 380 Other Personal Property Damage
- ☐ 385 Property Damage Product Liability

FORFEITURE/PENALTY
- ☐ 610 Agriculture
- ☐ 620 Other Food & Drug
- ☐ 625 Drug Related Seizure of Property 21 USC 881
- ☐ 630 Liquor Laws
- ☐ 640 R.R. & Truck
- ☐ 650 Airline Regs.
- ☐ 660 Occupational Safety/Health
- ☐ 690 Other

BANKRUPTCY
- ☐ 422 Appeal 28 USC 158
- ☐ 423 Withdrawal 28 USC 157

PROPERTY RIGHTS
- ☐ 820 Copyrights
- ☒ 830 Patent
- ☐ 840 Trademark

OTHER STATUTES
- ☐ 400 State Reapportionment
- ☐ 410 Antitrust
- ☐ 430 Banks and Banking
- ☐ 450 Commerce
- ☐ 460 Deportation
- ☐ 470 Racketeer Influenced and Corrupt Organizations
- ☐ 480 Consumer Credit
- ☐ 490 Cable/Sat TV
- ☐ 810 Selective Service
- ☐ 850 Securities/ Commodities/ Exchange
- ☐ 875 Customer Challenge 12 USC 3410
- ☐ 891 Agricultural Acts
- ☐ 892 Economic Stabilization Act
- ☐ 893 Environmental Matters
- ☐ 894 Energy Allocation Act
- ☐ 895 Freedom of Information Act
- ☐ 900 Appeal of Fee Determination Under Equal Access to Justice
- ☐ 950 Constitutionality of State Statutes
- ☐ 890 Other Statutory Actions

REAL PROPERTY
- ☐ 210 Land Condemnation
- ☐ 220 Foreclosure
- ☐ 230 Rent Lease & Ejectment
- ☐ 240 Torts to Land
- ☐ 245 Tort Product Liability
- ☐ 290 All Other Real Property

CIVIL RIGHTS
- ☐ 441 Voting
- ☐ 442 Employment
- ☐ 443 Housing/ Accommodations
- ☐ 444 Welfare
- ☐ 440 Other Civil Rights

PRISONER PETITIONS
- ☐ 510 Motions to Vacate Sentence
Habeas Corpus:
- ☐ 530 General
- ☐ 535 Death Penalty
- ☐ 540 Mandamus & Other
- ☐ 550 Civil Rights
- ☐ 555 Prison Condition

LABOR
- ☐ 710 Fair Labor Standards Act
- ☐ 720 Labor/Mgmt. Relations
- ☐ 730 Labor/Mgmt. Reporting & Disclosure Act
- ☐ 740 Railway Labor Act
- ☐ 790 Other Labor Litigation
- ☐ 791 Empl. Ret. Inc. Security Act

SOCIAL SECURITY
- ☐ 861 HIA (1395ff)
- ☐ 862 Black Lung (923)
- ☐ 863 DIWC/DIWW (405(g))
- ☐ 864 SSID Title XVI
- ☐ 865 RSI (405(g))

FEDERAL TAX SUITS
- ☐ 870 Taxes (U.S. Plaintiff or Defendant)
- ☐ 871 IRS – Third Party 26 USC 7609

V. ORIGIN (PLACE "X" IN ONE BOX ONLY)
☒ 1 Original Proceeding ☐ 2 Removed from State Court ☐ 3 Remanded from Appellate Court ☐ 4 Reinstated or Reopened ☐ 5 Transferred from another district (specify) ☐ 6 Multidistrict Litigation ☐ 7 Appeal to District Judge from Magistrate Judgment

VI. CAUSE OF ACTION (Cite the U.S. Civil Statute under which you are filing. **(Do not cite jurisdictional statutes unless diversity.)**
Brief description of cause: Patent infringement action under 28 U.S.C. Section 1338(a), 1391(b), 1391(c), and 1440, and 35 U.S.C. Section 1 et seq.

VII. REQUESTED IN COMPLAINT: ☐ CHECK IF THIS IS A CLASS ACTION UNDER F.R.C.P. 23 **Demand: $** CHECK YES only if demanded in Complaint
JURY DEMAND ☒ Yes ☐ No

VIII. RELATED CASE(S) IF ANY (See Instructions) JUDGE s Judge Farnan; *see* Notice of Related Case filed contemporaneously herewith DOCKET NUMBER 98-490, 04-1371, 07-187

DATE 10/15/07 SIGNATURE OF ATTORNEY OF RECORD TYPE NAME OF ATTORNEY Kyle Wagner Compton

FOR OFFICE USE ONLY
RECEIPT # _____ AMOUNT _____ APPLYING IFP _____ JUDGE _____ MAG. JUDGE _____

AO FORM 85 RECEIPT (REV. 9/04)

United States District Court for the District of Delaware

Civil Action No. 07-633

ACKNOWLEDGMENT OF RECEIPT FOR AO FORM 85

NOTICE OF AVAILABILITY OF A UNITED STATES MAGISTRATE JUDGE TO EXERCISE JURISDICTION

I HEREBY ACKNOWLEDGE RECEIPT OF 3 COPIES OF AO FORM 85.

10-15-07
(Date forms issued)

(Signature of Party or their Representative)

(Printed name of Party or their Representative)

Note: Completed receipt will be filed in the Civil Action