EXHIBIT A

IN THE UNITED STATES DISTRICT COURT
FOR THE DISTRICT OF DELAWARE

U.S. PHILIPS CORPORATION, Plaintiff, v. EASTMAN KODAK COMPANY, Defendant.	)	Civil Action No. 06-00251-GMS

EXPERT REPORT OF CHARLES J. NEUHAUSER, PH.D. ON BEHALF OF DEFENDANT EASTMAN KODAK COMPANY

Expert Report of Charles J. Neuhauser, Ph.D.

Introduction

My name is Charles J. Neuhauser. I am the owner and principal consultant of Neuhauser Associates, Inc. located at 525 West Remington Drive, Suite 126, Sunnyvale, California. I have been retained in this matter by DLA Piper US LLP on behalf of the Eastman Kodak Company to provide engineering opinions about the operation of the Widcom VTC-56 Coder Board (the "Coder Board").

Summary of Opinions

- I have developed a Verilog simulation based directly on the schematics of the Coder Board and the data values and logic contained in programmable devices in that schematic.
- The simulator correctly represents the functional operation of a section of the Coder Board.
- When provided with input data values, the Coder Board simulation produces outputs that include two distinct run length encoding techniques.
- The simulator output correctly represents what the actual Coder Board would produce if presented with these inputs.

Personal Background

I am an electrical engineer by training with specific education and experience in the operation of logic circuits and systems built from those circuits. My current *curriculum vita*, attached as Exhibit A to this report, outlines my general qualifications as an engineer. Below I will describe my specific qualifications and experience with respect to this matter.

This particular matter relates to the operation of the Widcom VTC-56 Coder Board. This board makes use of design techniques and circuit technology from the early to mid 1980s (I will explain this technology in detail below). From approximately 1970 to 1990 I worked actively in the field of logic and system design. My responsibilities covered the specification, selection of technology, design, simulation, debugging and validation of systems similar in structure and design to the Coder Board. During this period I participated directly in the design activities described and I also supervised other engineers undertaking similar activities. My experience with designs includes processors, communications interfaces, printer controllers and similar systems.

In particular I have designed a number of systems based on the logic families used in the Widcom Coder Board. The techniques used in the Coder Board design were widely known in the early 1980s because the particular logic families and components used were standards within the semiconductor industry.

In evaluating the Coder Board operation I have made use of certain simulation techniques (that I shall explain in detail below). Many of the systems I designed and worked with during the 1980s required extensive use of simulation systems similar to the system used in this project. Therefore, I am very familiar with the strengths and limitations of these systems.

Materials Considered

- Mentor Graphics, ModelSim 6.1c Simulation System.
- "A Verilog HDL Primer"; Second Edition; J. Bhasker; Star Galaxy Publishing; 1999.
- Various data sheets (Exhibit J)
- CD titled "Widcom Technical Documentation for Neuhauser" (3/17/06). The contents of the CD are listed in Exhibit B.
- "VTC-56B Coder Theory of Operation; Widcom Inc.; Draft 11-1-86 (WID0100264-314) from the CD mentioned above. (Exhibit C).
- "VTC-56B Theory of Operation: A System Overview: Widcom, Inc.; Draft 11-1-86 (WID0100475-490) from the CD mentioned above. (Exhibit D)
- Schematics titled "VTC-56 Coder" (WID 01002144-149) from the CD mentioned above (Exhibit R).
- CD labeled CLI351725 containing inspection photographs of the VTC-56. The contents of this CD are listed in Exhibit E.
- "Widcom VTC-56 Video Coder/Decoder Data Extraction Report"; Chipworks Inc.; July 16, 2004 from the Widcom Technical Documentation CD mentioned above (Exhibit F).
- Data files associated with the Chipworks report cited above from the CD titled "Widcom Technical Documentation" (3/17/06). (Exhibit K)
- Example DCT files. (Exhibit G)

Technical Background

The Widcom System and Coder Board

The Widcom VTC-56 is a complete teleconferencing system, that is, it provides an end to end system for the transmission of video information. The core of the system is a card rack containing electronic circuitry that processes video images for transmission and receives highly compressed video images and processes them for presentation on a monitor. CLI351725.006.jpg (Exhibit H) is a photograph of a portion of the electronics rack. The rack contains a number of circuit boards, which are electronic assemblies that plug into the rack. The circuit boards in the rack perform different functions. By communicating with each other through electrical conductors at the rear of the rack, the circuit boards, as an assembly, perform the overall teleconferencing function of the VTC-56. The Coder board, which is the subject of this report, is located in the fourth slot from the top in the photograph.

The Coder Board is a component of the Widcom VTC-56 system. My understanding based on the documents I have reviewed is that the VTC-56 is a videoconferencing terminal designed to enable the transmission of video signals over telephone lines. Because video signals contain more information content than can be passed over the telephone line to the remote video conferencing terminal it is necessary to reduce the amount of information content using certain computational techniques. This is referred to technically as *compression*. The VTC-56 uses several compression techniques in series. The Coder Board represents the last step in the chain of video information content compression. The Coder Board actually performs two main functions. About half the circuitry on the board is dedicated to encoding data and the other half is associated with serializing and buffering the data for transmission. Encoding is a process by which a representation of data is transformed into a different (possibly more compact) representation. My discussion and investigation is concerned only with the circuitry related to encoding. I will not be concerned with this serialization and buffering circuitry because no encoding takes place in that circuitry. Thus, the opinions expressed here are only related to the encoding circuitry of the Coder Board.

Design of an electronic system, such as the Coder Board, begins with a conceptual design. Engineers then refine the conceptual design into a detailed design that embodies all the critical elements related to the functioning of the circuitry. In the time frame when the VTC-56 was designed, engineers typically carried out the detailed design step by drafting electrical schematics of the required circuitry. Schematics are diagrams that describe precisely the circuit components required and how they will be interconnected to produce a system that will carry out the desired function, which in the case of the Coder Board includes data encoding. Typically, the schematics and certain other engineering documents provide all the information necessary to construct and produce the circuit board. Therefore, the schematics precisely embody the function of the product. Thus, a skilled engineer using the schematics (and certain additional information that I will describe below) can determine precisely how the device behaves (including the resulting output for a given input).

Technology

The encoding section of the Coder Board is a digital logic design, that is, the circuitry works in a digital or discrete fashion rather than in an analog or continuous manner. Physically, the Coder Board is composed of circuit components that are mounted on a large printed circuit board. The printed circuit board provides electrical pathways between circuit component packages. This general structure can be seen in the photo CLI351725.143.jpg in Exhibit I, to cite one example.

Circuit components in the Coder Board perform well-defined logic functions, such as storage, counting, addition and so forth. Thus, the components are many times referred to a "logic components" and the board and its components are referred to as "logic circuitry". The logic components of the Coder Board were selected from the well-known TTL (for Transistor Transistor Logic) family, an extensive series of logic components widely available at the time the VTC-56 was designed. The Coder Board design makes use of several types of logic components from the TTL family. These include SSI (Small Scale Integration) devices, FPLA (Field Programmable Logic Arrays), PROMs (Programmable Read Only Memories) and PALs (Programmable Array Logic).

SSI devices are fixed purpose devices, that is, they perform a well defined logic function that cannot be altered. Some devices, for example, perform the function of addition in a strictly fixed manner. Thus, if the device identifier is known (either from the schematic or from physical observation) the function of the device can also be determined. This is done by consulting "datasheets" which are standardized documentation provided publicly by device manufacturers. Specifically, the purpose of this documentation is to provide engineers with all the information about a device that they need to make use of it in a design or to determine the function of a design that includes that device. In order to understand the function of logic circuitry on the Coder Board I made use of datasheets for the SSI and other components. These datasheets are attached as Exhibit J. The datasheets I have provided are for specific manufacturers. Because logic devices have a standardized identification scheme (based on a part number such as the '74LS08,' which is an integrated circuit with quad 2-input AND gates) that is related to their function, the data sheet used to determine the function of a particular device on the Coder Board does not need to be from the manufacturer of that device, but may be from any manufacturer.

Programmable Devices

In addition to the fixed function SSI devices, the Coder Board contains a number of "programmable devices", such as, FPLAs, PROMs and PALs. These devices are manufactured with a generic internal function that can be made specific through a programming process that is carried out after device manufacture but before the device is placed on the circuit board. Because of this programmability feature, devices of the same type may be used in different ways in different parts of the design. For example, one PROM might be programmed to encode data and an identical PROM might be programmed to control logic sequencing. PALs and FPLAs may be used in a similar manner.

Generally, a schematic diagram does not include information about the specific programming of such programmable devices. Instead, this information is kept in another form, such as a set of equations or an array of data that is used to program the particular device. Although the Coder Board documentation I reviewed included a complete set of schematics it did not include the programming

information for the programmable devices used in the design. For this I made use of a different source of information derived from readouts of the actual programmable devices.

My understanding is that a complete operating VTC-56 system, S/N 212, which includes a working Coder Board, was obtained. For the particular programmable devices used in the Coder Board it is possible to "read out" of the device the programming that gives the device its particular logic personality. This is done by using well-known engineering techniques and equipment. I have performed such readouts on many occasions with many different types of devices, including devices like those used in the Coder Board design. It is a straight forward process.

I was provided with readouts for all FPLAs, PALs, and PROMs on the Coder Board. My understanding is that the readouts were performed by Chipworks (3685 Richmond Road, Suite 500, Ottawa, ON K2H 5B7 Canada), a well-known reverse engineering company that specializes in semiconductor analysis. Exhibit K contains the files provided to me with the data for the programmable devices. Each type of programmable device has a different internal organization and therefore the files are handled in a different manner. I will discuss this in more detail below under methodology. Chipworks also provided a report that details how they performed their analysis. This is attached as Exhibit F.

Methodology

My primary objective is to determine the precise operation of the encoding section of the Coder Board. To do this I employed a well-known engineering technique called *simulation*. To my knowledge, simulation has been used to evaluate the function of logic circuitry since at least the 1970s. It continues to be widely used today as the primary method of evaluating the operation of logic circuitry before a design is committed to manufacturing.

Simulations of logic circuit operation can be carried out at a number of levels. One level is functional, that is, the function of the logic is simulated without regard to physical issues such as timing. Many physical issues (such as loading, wire length, voltage and temperature) can influence the speed with which an actual implementation of a certain logic circuit runs when realized physically. Therefore a logic design that works functionally may not work (or may not work at full speed) when actually implemented. To assess this issue engineers make use of another level of logic simulation referred to as "timing" simulation. This type of simulation attempts to include all the timing constraints due to physical factors into the operation of the simulator.

In simulating the encoder logic circuitry of the Coder Board I used only a functional simulation. My reason for doing this was that the VTC-56 is known to be a functioning product, that is, the physical realization of the logic circuitry is

known to work properly. Therefore a timing simulation would not provide any additional information beyond what a functional simulation would.

To perform simulation I made use of the Mentor Graphics ModelSim Designer 6.1c running on a Windows XP platform. This particular simulator is very widely used by design engineers for precisely the purpose I am using it for. I wrote my simulation of the Coder Board encoder logic circuitry in Verilog, a well-known high level simulation language, using MultiEdit 9.0, a text editor, which includes some support for formatting Verilog. I wrote the Verilog code directly in MultiEdit rather than using the graphical interface provided by ModelSim. All simulations were run from the ModelSim command line.

My Verilog simulation was developed directly from the Widcom VTC-56 schematics. In particular, I made use of the following schematic pages (Exhibit R, WID01002144 – 147), which I refer to in the Verilog code as pages 1 through 4, respectively. To develop the simulation I carried out the following steps:

- Step 1: Develop and test device level logic circuitry
- Step 2: Build board level simulation by interconnecting device models
- Step 3: Test and debug the board level model
- Step 4: Develop a driver and formatter for the board level simulation
- Step 5: Run board level simulation on sample data

Step 1: Modeling Device Level Logic Circuitry

There are four general types of logic devices found in the VTC-56:

- SSI devices
- PROMs
- FPLAs
- PALs

Each type of device required different modeling approaches.

Modeling SSI Devices

I developed functional simulation models for each of the following SSI devices:

- 74LS02 – Quad NOR Gate
- 74LS04 – Hex Inverter
- 74LS32 – Quad OR Gate
- 74LS161 – 4-Bit Binary Counter
- 74LS163 – 4-Bit Binary Counter
- 74LS174 – Hex D-Type Flip/Flop
- 74LS244 – Octal Buffer with 3-State Output
- 74LS273 – Octal Register with Clear

declaration should I be presented with new materials or facts relevant to the opinions presented here.

I declare under penalty of perjury under the laws of the State of California that the foregoing is true and correct.

Executed this 13 day of December, 2007, at Sunnyvale, California.

Charles J. Neuhauser

Charles J. Neuhauser, Ph.D.

EXHIBIT B

UNITED STATES DISTRICT COURT

FOR THE DISTRICT OF DELAWARE

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U.S. PHILIPS CORPORATION, :

Plaintiff, :

vs. : Case No. 06-251-GMS

EASTMAN KODAK COMPANY, :

Defendant. :

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Palo Alto, California

Wednesday, January 30, 2008

Videotaped Deposition of CHARLES NEUHAUSER, Ph.D., held at the offices of Finnegan, Henderson, Farabow, Garrett & Dunner, 3300 Hill View Avenue, Palo Alto, California, commencing at 9:03 a.m., before Sharon Lancaster, a Certified Shorthand Reporter of the State of California.

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ALAN DIAZ, Videographer

C O N T E N T S

THE WITNESS:
CHARLES NEUHAUSER PAGE
By Mr. Campbell 5

E X H I B I T S

NEUHAUSER EXHIBIT NO. PAGE
1 Expert Report of Charles Neuhauser; 21 pages 47
2 Directory of CD "Widcom Technical Documentation for Neuhauser" (03/17/06); 4 pages 54
3 Directory of CD "CL1351725 re 5_20 CLI VTC-56 San Diego Inspection for Neuhauser (06/21/06); 8 pages 58
4 Widcom VTC-56B Video Coder/Decoder Data Extraction Report; 191 pages, double-sided 59
5 Dick James article, January 19, 2006; 4 pages, in color 77

week. That's just the writing part, you understand.

Q. What else went into the preparation of the report?

A. Well, of course, the testing and the development of the Verilog code and understanding of the system and all of those things went into -- It formed the foundation for the report.

Q. And so you're not offering any opinions on anticipation; is that correct?

MR. MULLOY: Objection. Seeks a legal conclusion.

You can answer.

THE WITNESS: I'm not sure I understand your question completely.

BY MR. CAMPBELL:

Q. Well, are you offering any opinion that the prior use or sale of the Widcom device invalidates the Philips patent?

A. I don't believe I'm offering an opinion about that. I'm just offering an opinion about how this device operates.

Q. And so you're also not offering an opinion on

never mentioned that you actually tested the physical device; is that correct?

A. Tested -- What device? You mean the actual board?

Q. The device -- Yes, there's a board shown in the photos. You never actually tested that, did you?

A. No, I did not.

Q. And why not?

A. I wasn't asked to.

Q. But do you know if Chipworks does that kind of test?

MR. MULLOY: Objection. Calls for speculation.

THE WITNESS: I don't know. I can tell you that a competent engineer could do such a test. Chipworks has competent engineers; therefore, they probably could do such a test if they were asked to.

BY MR. CAMPBELL:

Q. So it's physically possible to do such a test?

A. Well, let me put it this way: I believe that it's possible. But I'm giving you my best judgment as

to -- I guess it was the phone line, or likewise receive an image off the phone line, decode that for a TV monitor? Is that what you mean?

A. Well, in general, that's what -- you would have to have two of them, really. You would have to have one on the other end to really do a complete test.

Q. Do you know how Barry determined it was an operating system?

A. No, I don't.

Q. So you just took his word for it?

A. I did.

Q. And, likewise, what do you mean by a "working Coder Board"?

A. Where is that?

Q. Same sentence.

A. The same -- the same issue, that this board had functioned at one time --

Q. And again you --

A. -- and probably still did. And that -- it's just on his representation.

Q. So then in the next paragraph, the second

sentence -- I'll read both of them so it makes more sense. First and second.

"I was provided with readouts for all FPLAs, PALs and PROMS on the Coder Board. My understanding is that the readouts were performed by Chipworks" -- and it lists their address -- "a well-known reverse engineering company that specializes in semiconductor analysis."

So, again, what do you base this understanding on?

A. I've had contacts with Chipworks in the past or had investigated using them in projects. They are a well-known company.

Q. So how do you know they performed the readouts here?

A. Their report. It had their logo on it.

Q. How do you know they didn't make any mistakes?

A. Well, two reasons: One is, is that it's a relatively straightforward engineering task. Okay? And the second thing is, is that the results that were read out, they worked fine in the simulation. So if

there was a mistake, it would have to be something that didn't affect the simulation in any way.

Q. Well -- now, what do you mean by "they worked fine in the simulation"?

A. The simulation functioned over the input data that I gave it.

Q. So it didn't cause any -- Well, you put input in; you got output out?

A. I put input in. I got output that I expected to get out based on my knowledge of the circuitry and the technical documentation I had from Widcom. I didn't get any anomalies in the simulation that -- that, you know, indicated to me that something was wrong in any of programmable devices.

And then I also looked at each programmable device to see whether the information that was in there -- Remember, I tested these devices after I built up a model, I put I the programming, I tested them. It's not always possible to test them completely. But in the process of doing that, I analyzed what their function was. And their function seemed sensible against the function in the

schematic -- that was being suggested by the schematic and by the technical documentation and by the fact the system would run with those -- with those particular programmable devices.

Q. You took the data from Chipworks, put it into your system, and then determined that it was what you thought it was going to be; is that right?

A. I'm not sure that's what I -- I'm not sure that's a very good summary of what I just said.

Q. Well, what's wrong with it?

A. It's so vague, I can't -- I mean -- I basically did engineering validation, you know, that I would do on any project to make sure that everything looked consistent. It's an engineering type of process, right, to look at the programming, to look at the intended function of the device, to look at the schematics and to see if all of that seems to be reasonably consistent.

Q. All right. So further on this page in that section, is that starts -- well, it's the Methodology section. You state, "My primary objective is to determine the precise operation of the encoding

THIS DOCUMENT

WAS FILED

UNDER SEAL

THIS DOCUMENT

WAS FILED

UNDER SEAL

CERTIFICATE OF SERVICE

I, Francis DiGiovanni, hereby certify that on February 25, 2008, I caused to be electronically filed a true and correct copy of the foregoing document with the Clerk of the Court using CM/ECF, which will send notification that such filing is available for viewing and downloading to registered counsel of record via e-mail.

I hereby further certify that on February 25, 2008, I caused a copy of the foregoing document to be served on the following counsel of record by the manner so indicated:

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/s/ Francis DiGiovanni
Francis DiGiovanni (#3189)

IN THE UNITED STATES DISTRICT COURT
FOR THE DISTRICT OF DELAWARE

U.S. PHILIPS CORPORATION, Plaintiff, v. EASTMAN KODAK COMPANY, Defendant.	Case No. 06-0251 GMS

DECLARATION OF NICOLE WYLL IN SUPPORT OF DEFENDANT EASTMAN KODAK COMPANY'S OPPOSITION TO PHILIPS' MOTION *IN LIMINE* NO. 2: TO PRECLUDE KODAK FROM PRESENTING HEARSAY TESTIMONY BY EXPERT WITNESSES
[EXHIBITS C & D FILED UNDER SEAL]

I, Nicole Wyll, declare as follows:

1. I am an associate with the law firm DLA Piper US LLP, attorneys of record for defendant Eastman Kodak Company ("Kodak") in the above matter. Unless the context indicates otherwise, I make this declaration based upon my own personal knowledge.

2. Attached hereto as Exhibit A is a true and correct copy of the cover page and pages 1-6 and 20 of the Expert Report of Charles J. Neuhauser on Behalf of Defendant Eastman Kodak Company.

3. Attached hereto as Exhibit B is a true and correct copy of pages 1-3, 9, 74 and 90-93 of the deposition transcript of Charles Neuhauser.

4. Attached hereto as Exhibit C is a true and correct copy of the cover page and pages 1-2, 6-8, 11-13, 22, 28 and 31 of Mark Peterson's Expert Report on Damages, on behalf of U.S. Philips Corporation.

5. Attached hereto as Exhibit D is a true and correct copy of the cover page, the table of contents, pages 1-2 and 65, and Appendix A to Robert Wallace's Expert Report on Damages, on behalf of Eastman Kodak Company.

I declare under penalty of perjury that the forgoing is true and correct to the best of my knowledge.

Dated this 25th day of February, 2008, in San Diego, California.

Nicole Wyll