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APPLICANTS

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CONTINUING DATA********
VERIFIED

None (BK)

FOREIGN/PCT APPLICATIONS********
VERIFIED

	FED REP GERMANY	P 3631252.5	09/13/86
	FED REP GERMANY	P3638127.6	11/08/86
BK	FED REP GERMANY	P 3717399.5	05/23/87

Foreign priority claimed / 35 USC 119 conditions met / Verified and Acknowledged	Examiner's Initials	AS FILED	STATE OR COUNTRY	SHEETS DRWGS.	TOTAL CLAIMS	INDEP. CLAIMS	FILING FEE RECEIVED	ATTORNEY'S DOCKET NO.
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~~METHOD OF AND CIRCUIT ARRANGEMENT FOR BITRATE REDUCTION~~
method and apparatus for Bit Rate Reduction

U.S. DEPT. of COMM.-Pat. & TM Office — PTO-436L (rev. 10-76)

PARTS OF APPLICATION FILED SEPARATELY

NOTICE OF ALLOWANCE MAILED	PREPARED FOR ISSUE 8-30-89	CLAIMS ALLOWED
8-28-89	Assistant Examiner: William M. Young; Docket Clerk: C Robinson	Total Claims: 13; Print Claim: 1
ISSUE FEE: Amount Due: $620.00; Date Paid: 11/27/89	WILLIAM M. SHOOP, JR. SUPERVISORY PRIMARY EXAMINER ART UNIT 217 — Primary Examiner	DRAWING: Sheets Drwg.: 5; Figs. Drwg.: 6; Print Fig.: 6
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PATENT APPLICATION SERIAL NO.

U.S. DEPARTMENT OF COMMERCE
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FEE RECORD SHEET

N 10220 09/18/87 096177 21-0450 010 101 340.00CH

PTO-1556
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Case Docket No. PHD 86,327
Date: September 11, 1987

096177

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401-00

Enclosed for filing is the patent application of
Inventor(s): PETER VOGEL

301

For: METHOD OF AND CIRCUIT ARRANGEMENT FOR BITRATE REDUCTION

ENCLOSED ARE

[X] 5 sheets of [X] informal [ ] formal drawing.
[ ] An assignment of the invention to
[ ] A fully executed declaration.
[ ] An unsigned declaration.
[ ] A certified copy of application
Serial No.
[X] Associate power of attorney.
[X] Preliminary Amendment.

FEE COMPUTATION

CLAIMS AS FILED				
FOR	Number Filed	Number Extra	Rate	Basic Fee - $340.00
Total Claims	10 - 20 =	0	x $12 =	
Independent Claims	1 - 3 =	0	x $34 =	
Multiple Dependent Claims, if any			$110 =	

TOTAL FILING FEE $340.00
ASSIGNMENT RECORDING FEE ...$

Please charge Deposit Account No. 21-0450 in the amount of $340.00. The Commissioner is hereby authorized to charge any additional fees which may be required, except the issue fee, or credit any overpayment to Account No. 21-0450.

[ ] Amend the specification by inserting before the first line the sentence: - This is a continuation-in-part of application Serial No. , filed

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CERTIFICATE OF MAILING

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Send correspondence and papers to: Thomas A. Briody, U.S. Philips Corporation, 580 White Plains Road, Tarrytown, New York 10591.

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PHD 86.327 C 1 09.03.1987

Method of and circuit arrangement for bitrate reduction.

The invention relates to a method of and a circuit arrangement for bit rate reduction. Bit rate reduction is carried out when coding a signal, which comprises a series of digital signal values and has a signal value A, occurring most frequently in runs.

An Article by Wen-Hsiung Chen and William K. Pratt (Chen, When-Hsiung and Pratt, William K.: Scene Adaptive Coder IEEE Transactions on Communications, vol. Com-32, No. 3, March 1984, pages 225-232) describes a coding process of video signals for the purpose of transmitting video pictures of satisfactory quality at a minimum possible bit rate. Coding is effected in several steps. First, equally large video picture sections which are represented by blocks of pixels are subjected to a Discrete Cosine Transform. In this transform process a special two-dimensional Fourier transform is used. By the transform a new block of values (coefficients) is obtained from the original block. This coefficient block has the property that a large number of its elements - thus a large part of the coefficients - are approximately 0 or exactly 0. A subsequent quantisation of the coefficients always renders the greater part of the elements 0 so that a subsequent Huffman coding would therefore already involve a considerable bit rate reduction. The authors of the above-mentioned Article achieve a further bit rate reduction in that the frequent occurrence of zero runs in the intermediate signal in which the coefficients are serially arranged is utilized by means of a Huffman coding.

It is known that in a Huffman coding in which the codewords have different lengths, statistic properties of the signal to be coded are utilized. In the present case this particularly implies that the frequency with which zero runs having lengths 1, 2, 3, etc. occur in the above-mentioned intermediate signal is investigated. The shortest Huffman codeword is then assigned to the run that occurs most frequently. The next larger codeword is assigned to the run that occurs less frequently, and so forth.

For coding the intermediate signal two Huffman code

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tables are required according to the above-mentioned Article. A first table shows how the quantised coefficients different from 0 are to be coded. Only the coefficient values are coded because equally large coefficients also occur at the same frequency. The signs are transmitted in a separate bit. A second table shows how the run length is to be coded. In order that the codewords of one table can be distinguished from those of the other table during decoding, a separate codeword, the so-called run length prefix, is used for the identification of the coded run length.

It is an object of the invention to provide a coding method for a signal of the kind mentioned in the opening paragraph and comprising in a special case, an intermediate signal resulting from a picture coding operation, leading to a bit rate reduction which is larger than that hitherto known.

This object is achieved by assigning a Huffman codeword to each run of having length 0, 1, 2 etc., together with the signal value subsequent to the run or together with the signal value preceding the run.

Advantageous embodiments of the invention, particularly for exeptional cases of the signal characterized in the opening paragraph as well as a circuit arrangement for carrying out the method according to the invention, can be derived from the sub-claims.

The invention will now be described in greater detail by way of examples with reference to the accompanying drawings in which

Figure 1 is a table stating the occurrence of events,

Figure 2 is a further table elucidating the split-up of the events,

Figure 3 to Figure 5 show a coding table, and

Figure 6 shows the circuit diagram of arrangements for coding video signals according to the invention.

~~In the following embodiments explaining the invention the signal mentioned in the opening paragraph and occurring after coding blocks of video pictures elements. The signal values mentioned in the opening paragraph thus are the coefficients or the elements of the coefficients block, whilst the signal value is the value 0 because it occurs most frequently in runs in the intermediate signal.~~

~~It is evident from the invention, the occurrence of a zero~~

~~run and the coefficients subsequent to this run is considered as an event to be encoded. It is important that also when a coefficient different from 0 is not preceded by one or more 0 coefficients - thus~~ the occurrence of a run length 0 - is treated as an event to be coded.

~~Each of these events occurs in the video signal with a characteristic frequency. As has been proved by, for example, measurements, small-value coefficients occur more frequently than those having a high value as the preceding coefficients run with the value 0 becomes longer.~~

Figure 1 shows the frequency distribution of the above-mentioned events in the case of a cosine-transformed and subsequently ~~quantised~~ quantized video signal. Each field of the table represents an event characterized by the zero run length L and by the value B of the subsequent ~~(quantised)~~ quantized coefficient. The values B proceed through the natural numbers without the zero and the length L proceeds through the natural numbers with the zero. In order that the table does not become arbitrarily large, all events with B larger than or equal to 9 are combined to an overall event. The same applies to L when larger than or equal to 9.

The numbers in the different fields indicate how often the associated event occurs in a ~~quantised~~ quantized video signal with approximately 15000 signal values. The assignment of Huffman codewords is shown in the table: the series L=0, B=1 acquires the shortest codeword; this is followed by the series L=1, B=1 with the next longer codeword, and so forth.

If the assigned codewords instead of the ~~frequencies~~ frequencies are introduced in the event fields of the table, a two-dimensional coding table is obtained. It is not shown for the events according to Figure 1 because such coding tables can generally be set up by those skilled in the art. For the sake of completeness it is to be noted that a maximum number of 11 bits follows for the events in which L is larger than or equal to 9 or in which B is larger than or equal to 9 after the assigned Huffman codeword, which bits give the receiver accurate information about the value of L and the value of B, respectively.

An additional, ~~but~~ bit rate reduction of 12% is obtained when coding video signals in accordance with the above-mentioned two dimensional coding table as compared with the coding method described in

the opening paragraph.

This additional bit rate reduction is possible because, for example ~~the probability of the event in which three successive zeros with subsequent coefficient of the value 2 occur is different from the product of probability with which three successive zeros occur and the probability with which a coefficient of the value 2 occurs anyway~~.

The limitation of Figure 1 will now be considered in greater detail. As is evident from the above-mentioned embodiments the number of the events to be coded in accordance with Figure 1 is kept within efficient limits because all zero runs with an equally large subsequent value of a coefficient are considered as an event if the run length L is larger than eight.

Similarly, all zero runs of equal length are considered as an event if the subsequent value B of a coefficient is larger than eight.

As is shown in Figure 1, relatively rarely occurring events are concerned, and therefore they are coded with relatively long Huffman codewords. Since the receiver for decoding should know the exact zero run length or the exact value of a coefficient without any loss of information, an additional codeword is added to the Huffman codeword - as already indicated above - from which the exact length or the exact value or both can be derived.

A clearly defined state is encoded by the Huffman codeword and the additional information. Since the number of bits of such combinations is also dependent on the statistic properties of the signal, such combinations should also be present at the receiver and the decoder in order that the state which is based on these combinations can unambiguously be recognized at the receiver end.

The Huffman codewords defined in this sense may be up to 30 bits long. Since the processing of codewords which are at most 16 bits long does not require any special arrangements, but is possible, for example with a 16-bit microprocessor, given events are split up into sub-events - to improve the method described so far - such that codewords whose length is at most 16 bits are sufficient for coding all events and sub-events. This split-up will now be described in greater detail.

Firstly, an event to be coded consisting of an L = Lm zero run with subsequent coefficient of the value B = Bm is designated by

(Lm, Bm). In contrast to the foregoing, Bm = 0 is now also explicitly admitted. It is true that the two-dimensional diversity of events (Lm, Bm) occurring in practice is finite, because arbitrarily large values of coefficients do not occur, but it is very large. Consequently, the Huffman codewords to be used are correspondingly large as regards number and length. To reduce the overall number of the events to be coded the starting point is that, for example a run of 19 zeros with subsequent coefficient of the value 7 can be split up into sections, the first of which represents a run of 16 zeros, the second of which represents a run of 3 zeros and the third of which is a run without a zero and subsequent coefficient of the value 7. Each of these sections is now considered as a sub-event which is coded by a Huffman codeword. The length of each section is below a given value which can be predetermined and which will be further dealt with below.

This split-up is illustrated in Figure 2. In the horizontal direction all occurring values B - including the value 0 - of the coefficients are shown. In the vertical direction the length - also starting at 0 - of coefficient runs of the value 0 is shown. The "events Fields" shown symbolize the event (Lm, Bm) i.e. Lm zeros followed by a coefficient of the value Bm. The event (0, 3) for example means that a coefficient of the value 3 is preceded by a run length 0 which means that there is no coefficient of the value 0 preceding. Isolated zeros in the signal are symbolized by the event (0, 0). The reference (3,Bm) refers inter alia to the event in which a coefficient of the value Bm is succeeded by three successive zeros. Since the value of zero is also admitted for Bm, the event (3, 0) means that there are four successive zeros.

Figure 2 shows a polygonal curve in a solid line dividing the series fields into two ranges. The left-hand range comprises the events which are referred to as being codable and the right-hand range shows the events which are referred to as non-codable. The maximum length for a section of signal values - corresponding to a codable event - is 16; the events (0, 15), (1, 15) and (2, 15) are involved. All other codable events correspond to signal sections which are shorter. The division into codable and non-codable events is not completely arbitrary; the most frequently occurring event should be associated with the codable ones. The crossed non-codable event (8, 7) is split up, for

example into the events (0, 7) and (7, 0). There are various possibilities for the split-up; the simplest is the indicated "projection on the event axes".

The numbers in the event fields which are associated with the codable events signify the length - hence the number of bits - of the Huffman codewords with which the events are coded. The codewords also comprise the signs of the coefficients and possibly data about the magnitude of the value B; none of them is longer than 16 bits. In setting up the Huffman codewords it was assumed that coefficients having values of more than 136 do not occur.

Figures 3 to 5 show the exact structure of the Huffman codewords used. The first codeword 11 represents the coded signal value for characterizing a block end; at the transmission it succeeds the last codeword which is associated with a coefficient block. The first column of these figures states consecutive numbers, the second column states the values B of the coefficients and the third states the lengths L of the zero runs. The two latter data combined result in the "coordinates" of a codable event according to Figure 2. In the fourth column of Figs. 3 -5 the code words are shown bitwise. The bit s denotes the sign bit, the positions indicated by "-" are meaningless, and the positions indicated by "+" comprise the coded values of the coefficients in so far as they are larger than eight. The last column once more states the ~~lenght~~ of the Huffman codewords.

A possibility of further reducing the ~~bitrate~~ bit rate results from the fact that - as in the present embodiment - the signal to be coded is structured in accordance with blocks. As already indicated, the coefficients of a coefficient block are separated from those of the next block by an "end - of - block" signal. Also this "end - of - block" signal is converted into a codeword (compare Figure 3) whilst the sequence of m (codable) events of the type

(L1, B1)
(L2, B2) (1)
...
(Lm, Bm)

and into a sequence of assigned codewords. The number m of the events is dependent on the special values of the coefficients. If the overall coefficient block comprises, for example 63 zeros with subsequent

coefficients of the value 0, it is split up into only one event, namely (63, 1) or into several codable events according to Figure 2. As it is not known in advance into how many codable events a coefficient block is split up, the separate blocks must for this reason already be separated from one another by means of an "end - of - block" signal. At the receiver end the transmitted Huffman codewords are retransformed into events and these events are again converted into a sequence of coefficients. The receiver knows that, for example, 64 coefficients are associated with a coefficient block.

For further explanation and for the sake of simplicity, it is assumed that 4 x 4 blocks are concerned, so that one block comprises a total of 16 coefficients. All data associated with a block are separated from the data of the subsequent block by an "end of block" sign. This sign and the corresponding codeword is excepted from the split-up of the signal to be coded in accordance with the events. If, for example the sequence of coefficients of a block in a decimal representation has the form of

XX 4005000050000001 XX, (2)

The block is split up according to scheme (1) into the following events.

(0, 4)
(2, 5)(4, 5)
(6, 1) (3)

In order that the coefficient sequence of a block can at any rate be split up into events in accordance with scheme (1) or (3) above, the coefficients are temporarily stored before they are further processed. The temporal sequence of the coefficients in scheme (2) and that of the events in schemes (1) and (3) corresponds to the sequence of their written registration (European writing direction assumed). The symbols XX in the embodiment according to scheme (2) symbolize the "end-of-block" signs of the previous block and the represented block.

The coefficients in scheme (2) which are different from 0 are all positive and are represented as integral multiples of the smallest unit, namely 1. As can be seen from scheme (3), the last event

is the event (6, 1). The Huffman codewords assigned to the events are not indicated.

Firstly, the weight of reception of the last event, namely (6, 1) of the block according to (2) is checked for the receiver. In the coding of pictures general experience has proved that the transmission of events with a run of more than five zeros become less worthwhile as the value of the subsequent coefficient is smaller. If in accordance with the rule based on experience, checked events for which L = 5 and B = 1 are not transmitted, the transmission of the last event does not take place. In that case the preceding series (4, 5) is checked in accordance with the same criterion. In the example according to (2) the check for this block is ended because the event (4, 5) and the assigned Huffman codeword must be transmitted.

After decoding the Huffman codewords at the receiver end all coefficients of the block according to scheme (2) can be recovered, but for those which are associated with non-transmitted events. However, since these are associated with the last coefficients of the block, the decoded coefficients at the receiver end are augmented with coefficients of the value 0 until the overall number of coefficients is 16.

Figure 6 shows a circuit arrangement realising a simple split-up of the sequence of coefficients in accordance with codable events. The supply of clock pulses and details of the logic operation of binary values are not shown because they are known to those skilled in the art. In the circuit arrangement according to Figure 6 events are coded which consist of a run of coefficients of the value zero and a subsequent coefficient. If the run length L in the signal to be coded exceeds a predetermined length Lmax, the associated event cannot be encoded and is split up into codable events. Due to the predetermined maximum length Lmax which is independent of the subsequent coefficient, no delays or intermediate storages of the coefficients are required.

The coefficients are serially applied from an input E via a multiple lead e to the address inputs of an addressable memory PROM and to a first input E1 of a comparator circuit K. The multiple lead e comprises as many wires as bits are required for the binary representation of a coefficient. A coding table is filed in the memory PROM.

The position of a counter Z is applied to a second input

E2 of the comparator K - via a multiple lead f. The multiple lead f is simultaneously connected to further address inputs of the memory PROM.

It is assumed that a coefficient which is different from zero is present at the input E1. In this case the comparator circuit K supplies a pulse from an output A2, which pulse is applied via a lead a to the reset input R of the counter Z and to the clock input C2 of a flipflop circuit FF. The counter is reset to the zero position with this pulse and the codeword which is present at the output of the memory PROM is bit-parallel taken over in the flipflop circuit FF. The codeword can be derived from the output A of the circuit arrangement according to Figure 6. The codewords present at output A are not the ultimate Huffman codewords because all of them have the same length. To convert codewords of the same length into codewords of unequal length, and conversely - the latter conversion is required at the receiver end - reference is made to patent applications DE 35 10 902, DE 35 10 901 and DE 36 32 682.

If a zero is present at the input E1, the comparator circuit K supplies a counting pulse from a further output A1 and applies it to the clock input C1 of the counter Z which increases it count by one unit. The comparator circuit K continuously compares the actual counting with the value Lmax which is stored in one of its memories not shown. If the count reaches the value Lmax, the supply of a further counting pulse does not take place; ~~instead~~ the reset or transfer pulse is supplied from the output A2.

The complete coefficients - thus also their signs - are processed in the circuit arrangement according to Figure 6. In a modification the signs of the coefficients are applied ~~via~~ a separate ~~wire~~ to the output A of the circuit arrangement and to ~~except~~ them from a comparison by the comparator circuit K and from determining the codewords by the programmable memory PROM.

Cm What is claimed is:

1. A method of ~~bitrate~~ bit rate reduction when coding a signal ~~consisting of~~ comprising a sequence of digitally represented values and comprising a signal value A occurring most frequently in runs, characterized in that a Huffman codeword is assigned to each run length 0, 1, 2 etc. of signal values A together with the signal value subsequent to the run or together with the signal value preceding the run.

2. A method as claimed in Claim 1, characterized in that the same Huffman codeword is assigned to each run of signal values A together with the signal value subsequent to the run or together with the signal value preceding the run, if the run exceeds a predetermined ~~lenght and/or~~ length or if the subsequent or preceding signal value exceeds a predetermined value.

3. A method as claimed in ~~Claim 1 or 2~~, characterized in that if a run of signal values A together with the preceding or subsequent signal value exceeds a predetermined length, said overall run is split ~~up~~ into sections in such a manner that the length of each section is below a predetermined value and in that a Huffman codeword is assignad to each section.

4. A method as claimed in ~~Claim 1, 2 or 3, characterized in that~~ the signal comprises a sequence of coefficients which results after blockwise transform of pixels of a video signal with subsequent ~~quantization~~ quantization and in that the signal value A is the zero value.

5. A method as claimed in ~~Claim 4~~, characterized in that the advantages and drawbacks of non-transmission of the last Huffman codeword of a block are checked in a signal having the structure of equally long blocks, and in that the case of the advantages prevailing the Huffman codeword is not transmitted and subsequently the same check with the preceding Huffman codeword as last Huffman codeword is repeated.

6. A method as claimed in Claim 5, characterized in that a ~~checked~~ Huffman codeword is not transmitted if the length of the associated run of signal values A exceeds a barrier which is dependent on the magnitude of the subsequent ~~signal value~~.

A method as claimed in Claim 6, characterized in that the signal comprises a sequence of coefficients which results after a blockwise transform of pixels of a video signal with subsequent quantisation ~~and in that the signal value A is the zero value~~, and in that a checked Huffman codeword is not transmitted if the length of the associated zero run is larger than five and if the magnitude of the subsequent ~~signal value~~ non-zero-coefficient has the smallest possible value different from zero.

~~8.~~ A method as claimed ~~in Claim 4 or 7~~, characterized in that the Hufmann codeword is independent of the sign of that coefficient which succeeds or precedes the zero run and in that the sign is coded by a separate bit.

9. A circuit arrangement for performing the method as claimed in ~~any one of Claims 1 to 8~~ Claim 1, characterized in that the binary coded coefficients are applied with predetermined delays to the address inputs of a memory (PROM) and to a first input (E1) of a comparator circuit (K), in that a counter (Z) is provided whose count is applied to further address inputs of the memory (PROM) and to a second input (E2) of the comparator circuit (K), in that the comparator circuit (K) supplies a counting pulse to the counter (Z) from a first output (A1) if a zero value coefficient is present at the first input (E1) and if the count has not exceeded a value stored in a memory of the comparator circuit (K) supplies a pulse from a second output (A2) if the conditions for the supply of a counting pulse are not fulfilled, and in that the counter (Z) is reset by means of the pulse at the second output (A2) of the comparator circuit (K), and in that the codeword present at the outputs of the memory (PROM) is transferred to an intermediate memory (FF).

~~10.~~ A circuit arrangement as claimed in ~~Claim 9~~, characterized in that only the values of the coefficients are applied to the address inputs of the memory (PROM) and the comparator circuit (K) and in that the sign bits of the coefficients are supplied through a separate wire to the output (A) of the circuit arrangement.

Abstract:

Method of and circuit arrangement for bitrate reduction.

The method described for bitrate reduction is particularly intended for video signals in which so-called coefficients blocks occur. The coefficients have the property that a large part of them assumes the value 0. For this reason a zero run together with the subsequent coefficient is considered as an event, provided that the zero run length remains below a maximum value. If the maximum value is reached, this maximum zero run with its subsequent coefficient is considered as a event, and the coefficient then following are considered as a further event. A Huffman codeword is assigned to each event for the purpose of transmission.


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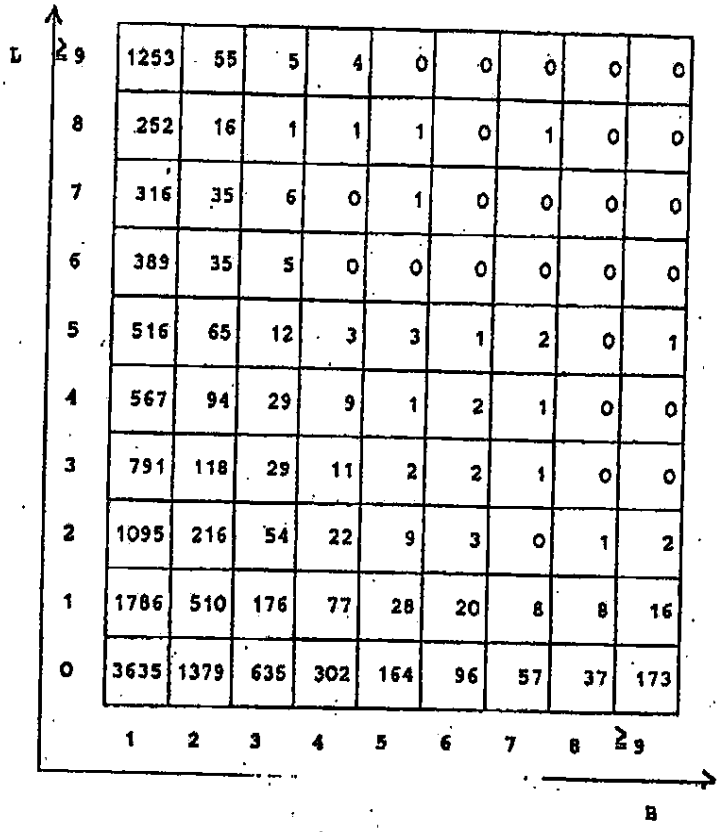

FIG. 1

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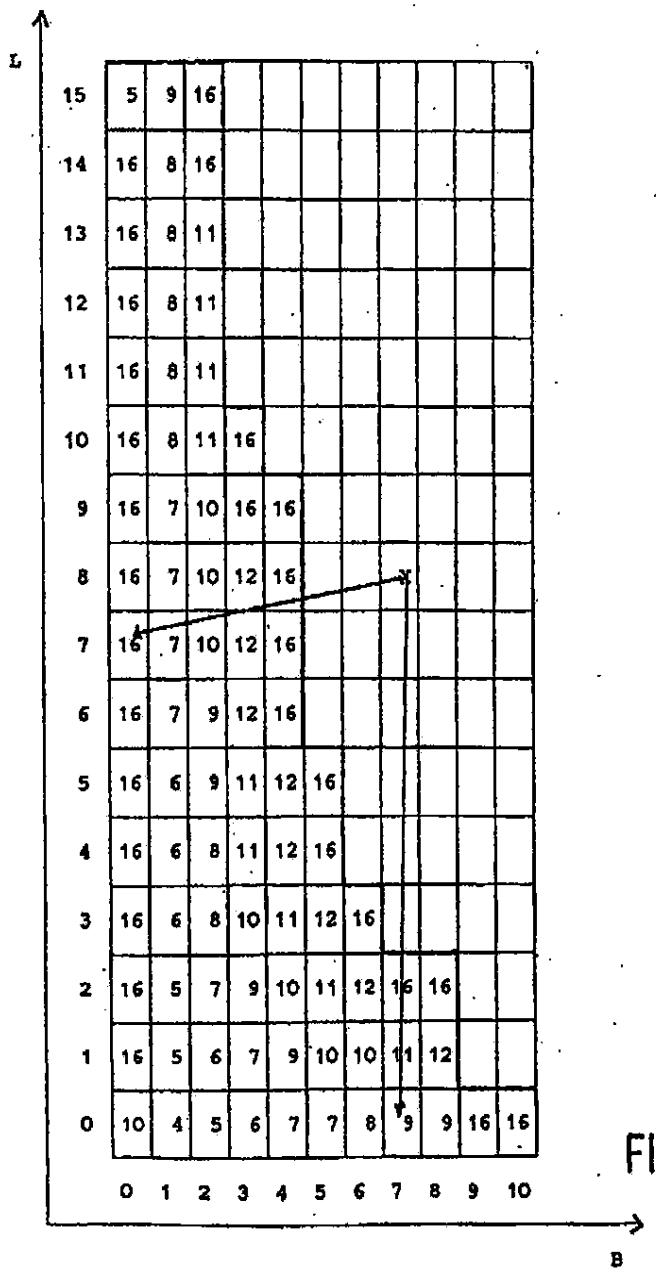

FIG. 2

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Nr.	B	L	code word		length
1	-	-	11	(end of block)	2
2	1	0	010s		4
3	1	1	1000s		5
4	1	2	1001s		5
5	2	0	1010s		5
6	0	15	10110		5
7	1	3	10111s		6
8	1	4	01100s		6
9	1	5	01101s		6
10	2	1	01110s		6
11	3	0	01111s		6
12	1	6	001000s		7
13	1	7	001001s		7
14	1	8	001010s		7
15	1	9	001011s		7
16	2	2	001100s		7
17	3	1	001101s		7
18	4	0	001110s		7
19	5	0	001111s		7
20	1	10	0001000s		8
21	1	11	0001001s		8
22	1	12	0001010s		8
23	1	13	0001011s		8
24	1	14	0001100s		8
25	2	3	0001101s		8
26	2	4	0001110s		8
27	6	0	0001111s		8
28	1	15	00001000s		9
29	2	5	00001001s		9
30	3	2	00001010s		9
31	4	1	00001011s		9
32	7	0	00001100s		9
33	8	0	00001101s		9

FIG. 3

3-V-PHD 86-327 C


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Nr.	B	L	code word	length
34	2	6	00001110s	9
35	2	7	000001000s	10
36	2	8	000001001s	10
37	2	9	000001010s	10
38	3	3	000001011s	10
39	4	2	000001100s	10
40	5	1	000001101s	10
41	6	1	000001110s	10
42	0	0	0000011111	10
43	2	10	0000011110s	11
44	3	4	0000001000s	11
45	3	5	0000001001s	11
46	4	3	0000001010s	11
47	5	2	0000001011s	11
48	7	1	0000001100s	11
49	2	11	0000001101s	11
50	2	12	0000001110s	11
51	2	13	0000001111s	11
52	3	6	00000001000s	12
53	3	7	00000001001s	12
54	3	8	00000001010s	12
55	4	4	00000001011s	12
56	4	5	00000001100s	12
57	5	3	00000001101s	12
58	6	2	00000001110s	12
59	8	1	00000001111s	12
60	9	0	00001111s+++++++	16
61	0	1	00000000100000--	16
62	0	2	00000000100001--	16
63	0	3	00000000100010--	16
64	0	4	00000000100011--	16
65	0	5	00000000100100--	16

FIG. 4

4-V-PHD 86-327C

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Nr.	B	L	code word	length
66	0	6	00000000100101--	16
67	0	7	00000000100110--	16
68	0	8	00000000100111--	16
69	0	9	00000000101000--	16
70	0	10	00000000101001--	16
71	0	11	00000000101010--	16
72	0	12	00000000101011--	16
73	0	13	00000000101100--	16
74	0	14	00000000101101--	16
75	2	14	00000000101110s-	16
76	2	15	00000000101111s-	16
77	3	9	00000000110000s-	16
78	3	10	00000000110001s-	16
79	4	6	00000000110010s-	16
80	4	7	00000000110011s-	16
81	4	8	00000000110100s-	16
82	4	9	00000000110101s-	16
83	5	4	00000000110110s-	16
84	5	5	00000000110111s-	16
85	6	3	00000000111000s-	16
86	7	2	00000000111001s-	16
87	8	2	00000000111010s-	16

FIG. 5

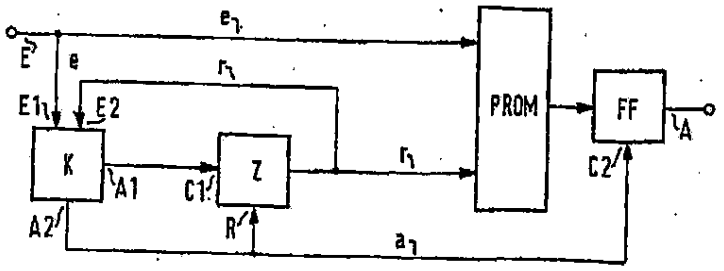

FIG.6

5-V-PHD 86-327C

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L \ B	1	2	3	4	5	6	7	8	≥9
≥9	1253	55	5	4	0	0	0	0	0
8	252	16	1	1	1	0	1	0	0
7	316	35	6	0	1	0	0	0	0
6	389	35	5	0	0	0	0	0	0
5	516	65	12	3	3	1	2	0	1
4	567	94	29	9	1	2	1	0	0
3	791	118	29	11	2	2	1	0	0
2	1095	216	54	22	9	3	0	1	2
1	1786	510	176	77	28	20	8	8	16
0	3635	1379	635	302	164	96	57	37	173

FIG. 1

1-V-PHD 86-327 C

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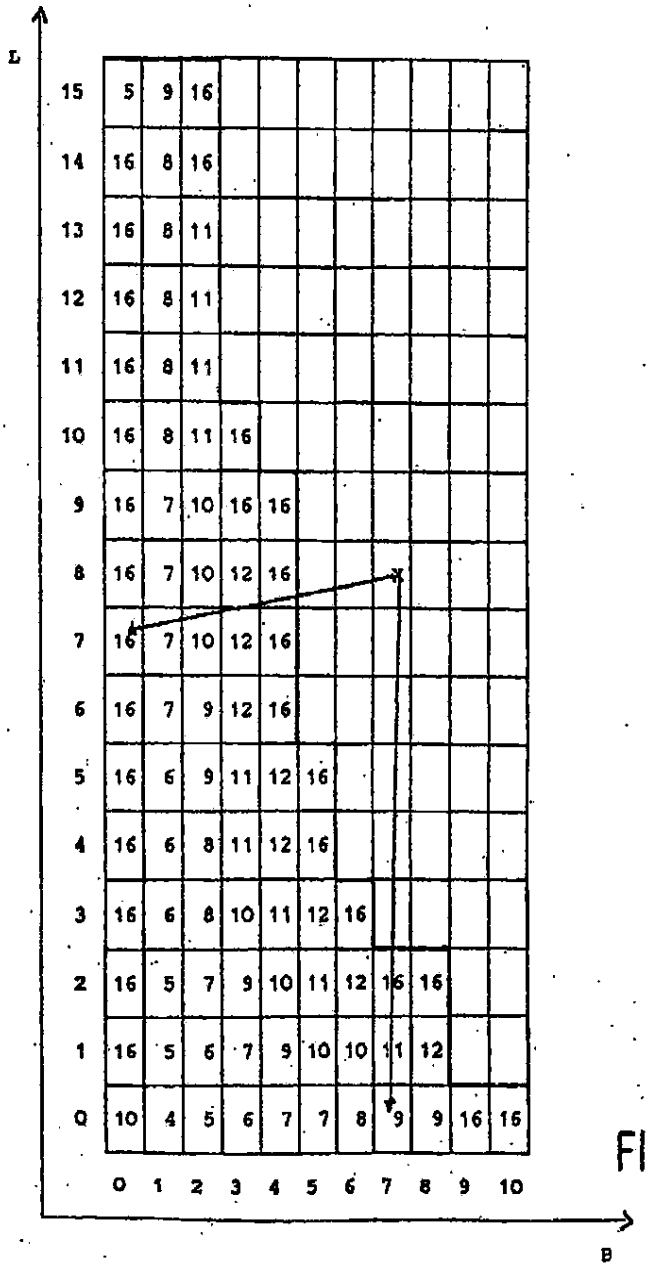

FIG. 2

2-V-PHO 86-327C

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Nr.	B	L	code word	length
1	-	-	11 (end of block)	2
2	1	0	010s	4
3	1	1	1000s	5
4	1	2	1001s	5
5	2	0	1010s	5
6	0	15	10110	5
7	1	3	10111s	6
8	1	4	01100s	6
9	1	5	01101s	6
10	2	1	01110s	6
11	3	0	01111s	6
12	1	6	001000s	7
13	1	7	001001s	7
14	1	8	001010s	7
15	1	9	001011s	7
16	2	2	001100s	7
17	3	1	001101s	7
18	4	0	001110s	7
19	5	0	001111s	7
20	1	10	0001000s	8
21	1	11	0001001s	8
22	1	12	0001010s	8
23	1	13	0001011s	8
24	1	14	0001100s	8
25	2	3	0001101s	8
26	2	4	0001110s	8
27	6	0	0001111s	8
28	1	15	00001000s	9
29	2	5	00001001s	9
30	3	2	00001010s	9
31	4	1	00001011s	9
32	7	0	00001100s	9
33	8	0	00001101s	9

FIG. 3

3-V-PHD 86-327 C

KODAK_000041

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As Original Filed

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4/5

Nr.	B	L	code word	length
34	2	6	00001110s	9
35	2	7	000001000s	10
36	2	8	000001001s	10
37	2	9	000001010s	10
38	3	3	000001011s	10
39	4	2	000001100s	10
40	5	1	000001101s	10
41	6	1	000001110s	10
42	0	0	0000011111	10
43	2	10	0000011110s	11
44	3	4	0000001000s	11
45	3	5	0000001001s	11
46	4	3	0000001010s	11
47	5	2	0000001011s	11
48	7	1	0000001100s	11
49	2	11	0000001101s	11
50	2	12	0000001110s	11
51	2	13	0000001111s	11
52	3	6	00000001000s	12
53	3	7	00000001001s	12
54	3	8	00000001010s	12
55	4	4	00000001011s	12
56	4	5	00000001100s	12
57	5	3	00000001101s	12
58	6	2	00000001110s	12
59	8	1	00000001111s	12
60	9	0	00001111s+++++++	16
61	0	1	000000000100000--	16
62	0	2	000000000100001--	16
63	0	3	000000000100010--	16
64	0	4	000000000100011--	16
65	0	5	000000000100100--	16

FIG. 4

4-V-PHD 86-327C

KODAK_000042

Print Of Drawing
As Original Filed

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Nr.	B	L	code word	length
66	0	6	00000000100101--	16
67	0	7	00000000100110--	16
68	0	8	00000000100111--	16
69	0	9	00000000101000--	16
70	0	10	00000000101001--	16
71	0	11	00000000101010--	16
72	0	12	00000000101011--	16
73	0	13	00000000101100--	16
74	0	14	00000000101101--	16
75	2	14	00000000101110s-	16
76	2	15	00000000101111s-	16
77	3	9	00000000110000s-	16
78	3	10	00000000110001s-	16
79	4	6	00000000110010s-	16
80	4	7	00000000110011s-	16
81	4	8	00000000110100s-	16
82	4	9	00000000110101s-	16
83	5	4	00000000110110s-	16
84	5	5	00000000110111s-	16
85	6	3	00000000111000s-	16
86	7	2	00000000111001s-	16
87	8	2	00000000111010s-	16

FIG. 5

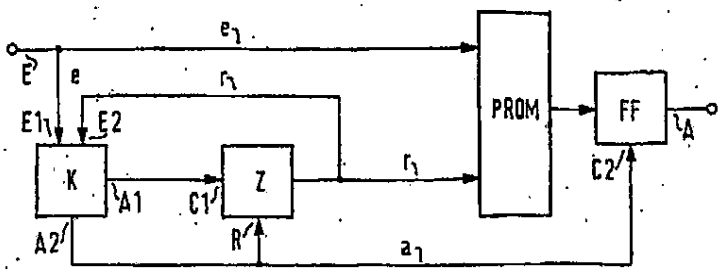

FIG.6

5-V-PHD 86-327

KODAK_000043

UNITED STATES DEPARTMENT OF COMMERCE
Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231

SERIAL NUMBER	FILING DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO.
07/096,177	09/11/87	VOGEL	PHD 86,327 P

PHD 86,327
#2

THOMAS A. BRIODY
U.S. PHILIPS CORPORATION
580 WHITE PLAINS ROAD
TARRYTOWN, NEW YORK 10591

000

DATE MAILED: 10/13/87

NOTICE TO FILE MISSING PARTS OF APPLICATION— FILING DATE GRANTED

A filing date has been granted to this application. However, the following parts are missing.

If all missing parts are filed within the period set below, the total amount owed by applicant as a ☒ large entity, ☐ small entity (verified statement filed), is $ 110.00

1. ☐ The statutory basic filing fee is: ☐ missing. ☐ insufficient. Applicant as a ☐ large entity, ☐ small entity, must submit $ _____ to complete the basic filing fee and MUST ALSO SUBMIT THE SURCHARGE AS INDICATED BELOW.
2. ☐ Additional claim fees of $ _____ as a ☐ large entity, ☐ small entity, including any required multiple dependent claim fee, are required. Applicant must submit the additional claim fees or cancel the additional claims for which fees are due. NO SURCHARGE IS REQUIRED FOR THIS ITEM.
3. ☒ The oath or declaration:
   ☒ is missing.
   ☐ does not cover items omitted at the time of execution.

   An oath or declaration in compliance with 37 CFR 1.63, identifying the application by the above Serial Number and Filing Date is required. A SURCHARGE MUST ALSO BE SUBMITTED AS INDICATED BELOW.
4. ☐ The oath or declaration does not identify the application to which it applies. An oath or declaration in compliance with 37 CFR 1.63 identifying the application by the above Serial Number and Filing Date is required. A SURCHARGE MUST ALSO BE SUBMITTED AS INDICATED BELOW.
5. ☐ The signature to the oath or declaration is: ☐ missing; ☐ a reproduction; ☐ by a person other than the inventor or a person qualified under 37 CFR 1.42, 1.43, or 1.47. A properly signed oath or declaration in compliance with 37 CFR 1.63, identifying the application by the above Serial Number and Filing Date is required. A SURCHARGE MUST ALSO BE SUBMITTED AS INDICATED BELOW.
6. ☐ The signature of the following joint inventor(s) is missing from the oath or declaration: _____ Applicant(s) should provide, if possible an oath or declaration signed by the omitted inventor(s), identifying this application by the above Serial Number and Filing Date. A SURCHARGE MUST ALSO BE SUBMITTED AS INDICATED BELOW.
7. ☐ The application was filed in a language other than English. Applicant must file a verified English translation of the application and a fee of $26.00 under 37 CFR 1.17(k), unless this fee has already been paid NO SURCHARGE UNDER 37 CFR 1.16(e) IS REQUIRED FOR THIS ITEM.
8. ☐ A $20.00 processing fee is required for returned checks. (37 CFR 1.21(m)).
9. ☐ Your filing receipt was mailed in error because check was returned.
10. ☒ Other: Surcharge of $110.00 required

A Serial Number and Filing Date have been assigned to this application. However, to avoid abandonment under 37 CFR 1.53(d), the missing parts and fees identified above in items 1 and 3-6 must be timely provided ALONG WITH THE PAYMENT OF A SURCHARGE OF $110.00 for large entities or $55.00 for small entities who have filed a verified statement claiming such status. The surcharge is set forth in 37 CFR 1.16(e). Applicant is given ONE MONTH FROM THE DATE OF THIS LETTER, OR TWO MONTHS FROM THE FILING DATE of this application, WHICHEVER IS LATER, within which to file all missing parts and pay any fees. Extensions of time may be obtained by filing a petition accompanied by the extension fee under the provisions of 37 CFR 1.136(a).

Direct the response to, and any questions about, this notice to the undersigned, Attention: Application Branch.

A copy of this notice MUST be returned with response.

Brenda A. Chea
For: Manager, Application Branch
(703) 557-3254

For Office Use Only	
☐ 102	☐ 202
☐ 103	☐ 203
☐ 104	☐ 204
☒ 105	☐ 205

FORM PTO-1533 (REV. 7-87) OFFICE COPY

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UNITED STATES DEPARTMENT OF COMMERCE
Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231

#3

SERIAL NUMBER	FILING DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO.
07/096,177	09/11/87	VOGEL	PHD 86,327

PHD 86,327

P

THOMAS A. BRIODY
U.S. PHILIPS CORPORATION
580 WHITE PLAINS ROAD
TARRYTOWN, NEW YORK 10591

000

DATE MAILED: 10/13/87

NOTICE TO FILE MISSING PARTS OF APPLICATION FILING DATE GRANTED

A filing date has been granted to this application. However, the following parts are missing.

If all missing parts are filed within the period set below, the total amount owed by applicant as a ☒ large entity, ☐ small entity (verified statement filed), is $ 110.00

1. ☐ The statutory basic filing fee is: ☐ missing. ☐ insufficient. Applicant as a ☐ large entity, ☐ small entity, must submit $ _____ to complete the basic filing fee and MUST ALSO SUBMIT THE SURCHARGE AS INDICATED BELOW.
2. ☐ Additional claim fees of $ _____ as a ☐ large entity, ☐ small entity, including any required multiple dependent claim fee, are required. Applicant must submit the additional claim fees or cancel the additional claims for which fees are due. NO SURCHARGE IS REQUIRED FOR THIS ITEM.
3. ☒ The oath or declaration:
   ☒ is missing.
   ☐ does not cover items omitted at the time of execution.

   An oath or declaration in compliance with 37 CFR 1.63, identifying the application by the above Serial Number and Filing Date is required. A SURCHARGE MUST ALSO BE SUBMITTED AS INDICATED BELOW.
4. ☐ The oath or declaration does not identify the application to which it applies. An oath or declaration in compliance with 37 CFR 1.63 identifying the application by the above Serial Number and Filing Date is required. A SURCHARGE MUST ALSO BE SUBMITTED AS INDICATED BELOW.
5. ☒ The signature to the oath or declaration is: ☐ missing; ☐ a reproduction; ☐ by a person other than the inventor or a person qualified under 37 CFR 1.42, 1.43, or 1.47. A properly signed oath or declaration in compliance with 37 CFR 1.63, identifying the application by the above Serial Number and Filing Date is required. A SURCHARGE MUST ALSO BE SUBMITTED AS INDICATED BELOW.
6. ☐ The signature of the following joint inventor(s) is missing from the oath or declaration: _____ Applicant(s) should provide, if possible an oath or declaration signed by the omitted inventor(s), identifying this application by the above Serial Number and Filing Date. A SURCHARGE MUST ALSO BE SUBMITTED AS INDICATED BELOW.
7. ☐ The application was filed in a language other than English. Applicant must file a verified English translation of the application and a fee of $26.00 under 37 CFR 1.17(k), unless this fee has already been paid NO SURCHARGE UNDER 37 CFR 1.16(s) IS REQUIRED FOR THIS ITEM.
8. ☐ A $20.00 processing fee is required for returned checks. (37 CFR 1.21(m)).
9. ☐ Your filing receipt was mailed in error because check was returned.
10. ☐ Other: Surcharge of $110.00 required

A Serial Number and Filing Date have been assigned to this application. However, to avoid abandonment under 37 CFR 1.53(d), the missing parts and fees identified above in items 1 and 3-6 must be timely provided ALONG WITH THE PAYMENT OF A SURCHARGE OF $110.00 for large entities or $55.00 for small entities who have filed a verified statement claiming such status. The surcharge is set forth in 37 CFR 1.16(e). Applicant is given ONE MONTH FROM THE DATE OF THIS LETTER, OR TWO MONTHS FROM THE FILING DATE of this application, WHICHEVER IS LATER, within which to file all missing parts and pay any fees. Extensions of time may be obtained by filing a petition accompanied by the extension fee under the provisions of 37 CFR 1.136(a).

Direct the response to, and any questions about, this notice to the undersigned, Attention: Application Branch.

S 20114 12/18/87 096177 21-0450 020 105 110.00CH

A copy of this notice MUST be returned with response.

Brenda A. Chea
For: Manager, Application Branch
(703) 557-3254

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☐ 103	☐ 203
☐ 104	☐ 204
☒ 105	☐ 205

FORM PTO-1533 (REV. 7-87)

COPY TO BE RETURNED WITH RESPONSE

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1987
PAT. & TRADE M

#3

Sole/Joint

DECLARATION AND POWER OF ATTORNEY

Attorney's Docket No.
PHD.86-327C

As a below named inventor, I hereby declare that:
My residence, post office address and citizenship are as stated below next to my name.
I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled

"Method of and circuit arrangement for bitrate reduction."

the specification of which (check one)

☐ is attached hereto.

☒ was filed on September 11, 1987 as Application Serial No. 096,177 and was amended on _____ (if applicable).

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.
I acknowledge the duty to disclose information which is material to the examination of this application in accordance with Title 37, Code of Federal Regulations, §1.56 (a).
I hereby claim foreign priority benefits under Title 35, United States Code, §119 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

PRIOR FOREIGN APPLICATION(S)

COUNTRY	APPLICATION NUMBER	DATE OF FILING (day, month, year)	PRIORITY Claimed Under 35 U.S.C. 119
West-Germany	P 3631252.5	13-9-1986	YES X NO ___
West-Germany	P 3638127.6	8-11-1986	YES X NO ___
~~West-Germany~~	~~P 3717399.5~~	~~23-5-1987~~	~~X~~

I hereby claim the benefit under Title 35, United States Code, §120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35 United States Code, §112, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, §1.56(a) which occurred between the filing date of the prior application and the national or PCT international filing date of this application:

PRIOR UNITED STATES APPLICATION(S)

APPLICATION SERIAL NUMBER	FILING DATE	STATUS (PATENTED, PENDING, ABANDONED)

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

POWER OF ATTORNEY: As a named inventor, I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and transact all business in the Patent and Trademark Office connected therewith. (list name and registration number)

Thomas A. Briody, Reg. No. 19,160
Jack Oisher, Reg. No. 17,317

SEND CORRESPONDENCE TO:	DIRECT TELEPHONE CALLS TO (name and telephone No.)
Corporate Patent Counsel U.S. Philips Corporation 580 White Plains Road Tarrytown, New York 10591	(914) 332-0222

Dated: October 19, 1987		Inventor's Signature: Peter Vogel		
FULL NAME OF INVENTOR	Last Name: VOGEL	First Name: Peter	Middle Name:	
RESIDENCE & CITIZENSHIP	City: DIEPERSDORF	State or Foreign Country: West-Germany	Country of Citizenship: West-Germany	
POST OFFICE ADDRESS	Street & No.: Wöhrletstr. 7a	City: 8566 DIEPERSDORF	State or Country: West-Germany	Zip Code:
Dated:		Inventor's Signature:		
FULL NAME OF INVENTOR	Last Name	First Name	Middle Name	
RESIDENCE & CITIZENSHIP	City	State or Foreign Country	Country of Citizenship	
POST OFFICE ADDRESS	Street & No.	City	State or Country	Zip Code

096,177
#35



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of
PETER VOGEL

Atty. Docket
PHD 86-327

Serial No.

Group Art Unit

Filed: Concurrently

Examiner

Title: METHOD OF AND CIRCUIT ARRANGEMENT FOR BITRATE REDUCTION

Honorable Commissioner of Patents and Trademarks
Washington, D.C. 20231

APPOINTMENT OF ASSOCIATES

Sir:

The undersigned Attorney of Record hereby revokes all prior appointments (if any) of Associate Attorney(s) or Agent(s) in the above-captioned case and appoints:

William J. Streeter (Registration No. 24,447)

Gregory P. Gadson (Registration No. 31,254) and

(Registration No.)

c/o U.S. PHILIPS CORPORATION, Intellectual Property Department, 580 White Plains Road, Tarrytown, New York 10591, his Associate Attorney(s)/Agent(s) with all the usual powers to prosecute the above-identified application and any division or continuation thereof, to make alterations and amendments therein, and to transact all business in the Patent and Trademark Office connected therewith.

ALL CORRESPONDENCE CONCERNING THIS APPLICATION AND THE LETTERS PATENT WHEN GRANTED SHOULD BE ADDRESSED TO THE UNDERSIGNED ATTORNEY OF RECORD.

Respectfully,

Thomas A. Briody

Thomas A. Briody, Reg. 19,160
Attorney of Record

Dated at Tarrytown, New York
this 9th day of September, 1987.

Appasoc.frm

MAIL ROOM SEP 11 1987 PAT. & TRADEMARK OFF.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of Atty. Docket

PHD 86-327

PETER VOGEL

Filed: Concurrently

METHOD OF AND CIRCUIT ARRANGEMENT FOR BITRATE REDUCTION

Honorable Commissioner of Patents and Trademarks
Washington, D.C. 20231

PRELIMINARY AMENDMENT

Sir:

Prior to examination, please amend the above-identified application as follows:

IN THE TITLE

Page 1, above line 1, delete in its entirety and insert

--METHOD AND APPARATUS FOR BIT RATE REDUCTION--;

IN THE SPECIFICATION

Page 1, above line 1, insert as a centered heading

--Background of the Invention--;

line 2, change "bitrate" to --bit rate--; change "Bitrate" to --Bit rate--;

line 10, change "bitrate" to --bit rate--; after "First" insert --,-- (comma);

line 12, after "process" insert --,-- (comma);

line 13, after "transform" insert --,-- (comma);

line 16, change "o" to --0--;

LDCI10050 -1-

Page 1, line 17, change "quantisation" to --quantization--;
line 19, change "bitrate" to --bit rate--;
line 20, change "bitrate" to --bit rate--;
line 25, change "lenghts" to --lengths--;
line 26, after "case" insert --,-- (comma);
line 27, change "lenghts" to --lengths--;

Page 2, between lines 9 and 10, insert as a centered heading
--Summary of the Invention--;
line 12, after "case" insert --,-- (comma);
line 22, after "invention" insert --,-- (comma);
between lines 22 and 23, insert as a centered heading
--Brief Description of the Drawing--;
line 28, change "Figure" to --Figures--; after "table" insert --,-- (comma);
between lines 30 and 31, insert as a centered heading
--Detailed Description of the Invention--;
line 35, change "whilst" to --while--;
line 37, after "invention" insert --,-- (comma);

Page 3, line 6, after "example" insert --,-- (comma);
line 12, change "quantised" to --quantized--;
line 15, change "lenght" to --length--;
line 21, change "quantised" to --quantized--;
line 26, change "frequenties" to --frequencies--;
line 35, change "bitrate" to --bit rate--;

Page 4, line 2, change "bitrate" to --bit rate--;
line 13, after "Similarly" insert --,-- (comma);
line 15, after "1" insert --,-- (comma);
line 16, after "concerned" insert --,-- (comma);

Page 4, line 31, delete "up";
line 36, after "Firstly" insert --,-- (comma);
Page 5, line 1, after "foregoing" insert --,-- (comma);
line 4, after "Consequently" insert --,-- (comma);
line 8, after "sections" insert --,-- (comma);
line 12, change "lenght" to --length--;
line 20, after "example" insert --,-- (comma);
line 21, change "lenght" to --length--;
line 24, change "inter alia" to --inter alia,--;
line 37, change "split-up" to --split--;
Page 6, line 1, after "example" insert --,-- (comma);
line 20, after "meaningless" insert --,-- (comma);
line 23, change "lenght" to --length--;
line 24, change "bitrate" to --bit rate--;
line 29, change "whilst" to --while--;
Page 7, line 4, delete "up";
line 8, after "example" insert --,-- (comma);
line 10, after "simplicity" insert --,-- (comma);
line 28, delete "up";
line 33, change "symbolise" to --symbolize--;
Page 8, line 3, after "Firstly" insert --,-- (comma);
line 28, change "split-up" to --split--;
Page 9, line 22, change ", instead" to --. Instead,--;
line 26, change "eia" to --via--;
line 27, change "wise" to --wire--; change "except" to --accept--;

IN THE ABSTRACT

Page 12, above line 1, delete in its entirety and insert as a centered heading --Abstract of the Disclosure--;

line 1, change "bitrate" to --bit rate--;

line 8, after "event" insert --,-- (comma); change "coefficient" to --coefficients--;

IN THE CLAIMS

Please amend the claims as follows:

Page 10, above Claim 1, insert --What is claimed is:--;

Claim 1, line 1, change "bitrate" to --bit rate--;

line 2, change "consisting of" to --comprising--;

Claim 2, line 5, change "lenght and/or" to --length or--;

Claim 3, line 1, delete "or 2";

line 4, delete "up";

line 5, after "value" insert --,-- (comma);

Claim 4, line 1, delete "2 or 3,";

line 4, change "quantisation" to --quantization,--;

Claim 7, line 6, change "it" to --if--; after "magnitude" insert --of--;

Claim 8, line 1, delete "or 7";

Claim 9, line 2, change "any one of Claims 1 to 8" to --Claim 1--;

Claim 10, line 5, change "wise" to --wire--;

REMARKS

This amendment is being submitted in order to place the application in proper U.S. form. An early allowance is requested.

Respectfully submitted,

PETER VOGEL

By Gregory P. Gadson
Gregory P. Gadson, Reg. 31,254
Assoc. Attorney for Applicant
(914) 332-0222, Ext. 232
September 11, 1987


SEP
11
1987

UNITED STATES DEPARTMENT OF COMMERCE
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SERIAL NUMBER	FILING DATE	FIRST NAMED APPLICANT	ATTORNEY DOCKET NO.
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EXAMINER	
YOUNG, B	
ART UNIT	PAPER NUMBER
217	5

DATE MAILED: 09/20/88

This is a communication from the examiner in charge of your application.
COMMISSIONER OF PATENTS AND TRADEMARKS

☑ This application has been examined ☐ Responsive to communication filed on _____ ☐ This action is made final.

A shortened statutory period for response to this action is set to expire 3 month(s), _____ days from the date of this letter. Failure to respond within the period for response will cause the application to become abandoned. 35 U.S.C. 133

Part I THE FOLLOWING ATTACHMENT(S) ARE PART OF THIS ACTION:
1. ☑ Notice of References Cited by Examiner, PTO-892.
2. ☑ Notice re Patent Drawing, PTO-948.
3. ☐ Notice of Art Cited by Applicant, PTO-1449
4. ☐ Notice of Informal Patent Application, Form PTO-152
5. ☐ Information on How to Effect Drawing Changes, PTO-1474
6. ☐ _____

Part II SUMMARY OF ACTION

1. ☑ Claims 1-10 are pending in the application.
   Of the above, claims _____ are withdrawn from consideration.
2. ☐ Claims _____ have been cancelled.
3. ☐ Claims _____ are allowed.
4. ☑ Claims 1-10 are rejected.
5. ☐ Claims _____ are objected to.
6. ☐ Claims _____ are subject to restriction or election requirement.
7. ☐ This application has been filed with informal drawings which are acceptable for examination purposes until such time as allowable subject matter is indicated.
8. ☐ Allowable subject matter having been indicated, formal drawings are required in response to this Office action.
9. ☐ The corrected or substitute drawings have been received on _____. These drawings are ☐ acceptable; ☐ not acceptable (see explanation).
10. ☐ The ☐ proposed drawing correction and/or the ☐ proposed additional or substitute sheet(s) of drawings, filed on _____ has (have) been ☐ approved by the examiner. ☐ disapproved by the examiner (see explanation).
11. ☐ The proposed drawing correction, filed _____, has been ☐ approved. ☐ disapproved (see explanation). However, the Patent and Trademark Office no longer makes drawing changes. It is now applicant's responsibility to ensure that the drawings are corrected. Corrections MUST be effected in accordance with the instructions set forth on the attached letter "INFORMATION ON HOW TO EFFECT DRAWING CHANGES", PTO-1474.
12. ☑ Acknowledgment is made of the claim for priority under 35 U.S.C. 119. The certified copy has ☐ been received ☑ not been received ☐ been filed in parent application, serial no. _____; filed on _____.
13. ☐ Since this application appears to be in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under Ex parte Quayle, 1935 C.D. 11; 453 O.G. 213.
14. ☐ Other

EXAMINER'S ACTION

PTOL-326 (Rev. 7-82)

KODAK_000054

Applicant is reminded of the proper language and format of an Abstract of the Disclosure.

The abstract should be in narrative form and generally limited to a single paragraph on a separate sheet within the range of 50 to 250 words. It is important that the abstract not exceed 250 words in length since the space provided for the abstract on the computer tape used by the printer is limited. The form and legal phraseology often used in patent claims, such as "means" and "said", should be avoided. The abstract should describe the disclosure sufficiently to assist readers in deciding whether there is a need for consulting the full patent text for details.

The language should be clear and concise and should not repeat information given in the title. It should avoid using phrases which can be implied, such as, "The disclosure concerns," "The disclosure defined by this invention," "The disclosure describes," etc.

The present abstract is not worded in a clear and concise manner. Examples of vagueness include; "so-called coefficients blocks occur", "a large part of them assumes", "a zero run together with", and "a further event".

Claims 1-10 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 1 recites a "method of .... coding a signal", however, the method steps have been completely omitted from the claim and its dependent claims 2-10. If a method is claimed, the steps of the method must be recited.

Claim 1 recites "a signal value A occurring most frequently in runs", however, what "A" represents is never recited in the claims. Further, "most frequently" is very vague.

Claim 1 recites "a Huffman codeword is assigned", however, again no steps to perform this are disclosed.

Claim 1 recites "run length 0, 1, 2, etc. of signal values", which, is very vague. What do "0, 1, 2, etc." represent?

Claim 1 recites "subsequent to the run or .... preceding the run", which, is very vague and ambiguous.

Claims 1-10 are narrative in form and replete with indefinite and vaguely worded language.

Claims 9 and 10 are rejected under 35 U.S.C. 112, fourth paragraph, as being of improper dependent form for failing to further limit the subject matter of a previous claim. The claims introduce a "circuit arrangement for performing the method" and fail to further limit the subject matter of the method claims.

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless-
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claim 1 is rejected under 35 U.S.C. 102(b) as being anticipated by Widergreen et al.

Claim 1 recites "a method for bit rate reduction" utilizing "Huffman" coding. Widergreen et al. disclose a method for bit rate reduction characterized in that a Huffman code is assigned to a "run length" (such as a run of zeros) (col. 15, lns. 40-49), and, that signals corresponding to the beginning of the "run" and the ending of the "run" are generated (col. 16, lns. 3-6).

Any inquiry concerning this communication should be directed to Brian K. Young at telephone number 703-557-8694.

Young/vsh
(703) 557-8694
09-10-88

WILLIAM M. SHOOP, JR.
SUPERVISORY PRIMARY EXAMINER
ART UNIT 217

PTO - 948
(Rev. 8-82)

U.S. DEPARTMENT OF COMMERCE
PATENT AND TRADEMARK OFFICE

ATTACHMENT TO PAPER NUMBER 5

S.N. 096,177

GROUP 210

NOTICE OF PATENT DRAWINGS OBJECTION

Drawing Corrections and/or new drawings may only be submitted in the manner set forth in the attached letter, "Information on How to Effect Drawing Changes" PTO-1474.

A. ☑ The drawings, filed on 9-11-87, are objected to as informal for reason(s) checked below:

1. ☐ Lines Pale.
2. ☐ Paper Poor.
3. ☑ Numerals Poor.
4. ☑ Lines Rough ~~and Blurred.~~
5. ☐ Shade Lines Required.
6. ☐ Figures Must be Numbered.
7. ☐ Heading Space Required.
8. ☐ Figures Must Not be Connected.
9. ☐ Criss-Cross Hatching Objectionable.
10. ☐ Double-Line Hatching Objectionable.
11. ☐ Parts in Section Must Be Hatched.
12. ☐ Solid Black Objectionable.
13. ☐ Figure Legends Placed Incorrectly.
14. ☐ Mounted Photographs.
15. ☑ Extraneous Matter Objectionable. [37 CFR 1.84 (1)] AT BOTTOM OF SHEET
16. ☐ Paper Undersized: either 8½" x 14", or 21.0 cm. x 29.7 cm. required.
17. ☐ Proper A4 Margins Required:
    ☐ TOP 2.5 cm. ☐ RIGHT 1.5 cm.
    ☐ LEFT 2.5 cm. ☐ BOTTOM 1.0 cm.
18. ☐ Other:

B. ☑ The drawings, submitted on 9-11-87, are so informal they cannot be corrected. New drawings are required. Submission of the new drawings MUST be made in accordance with the attached letter.

TO SEPARATE, ...D TOP AND BOTTOM EDGES, SNAP--APART AI ...ISCARD CARBON

FORM PTO-892 (REV. 3-78) U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE	SERIAL NO.	GROUP ART UNIT	ATTACHMENT TO PAPER NUMBER
NOTICE OF REFERENCES CITED	096177	217	5
	APPLICANT(S) P. Vogel		

U.S. PATENT DOCUMENTS

*		DOCUMENT NO.	DATE	NAME	CLASS	SUB-CLASS	FILING DATE IF APPROPRIATE
	A	4394774	7/83	Widergren et al.	340	347DD	
	B						
	C						
	D						
	E						
	F						
	G						
	H						
	I						
	J						
	K						

FOREIGN PATENT DOCUMENTS

*		DOCUMENT NO.	DATE	COUNTRY	NAME	CLASS	SUB-CLASS	PERTINENT SHTS. DWG	PERTINENT PP. SPEC.
	L								
	M								
	N								
	O								
	P								
	Q								

OTHER REFERENCES (Including Author, Title, Date, Pertinent Pages, Etc.)

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EXAMINER	DATE	
B. K. Young	9/3/88	

* A copy of this reference is not being furnished with this office action.
(See Manual of Patent Examining Procedure, section 707.05 (a).)

340-347 DD AU 217 CA
7/19/83 XR 4,394,774

United States Patent [19]
Widergren et al.

[11] 4,394,774
[45] * Jul. 19, 1983

[54] **DIGITAL VIDEO COMPRESSION SYSTEM AND METHODS UTILIZING SCENE ADAPTIVE CODING WITH RATE BUFFER FEEDBACK**

[75] Inventors: Robert D. Widergren, Saratoga; Wen-Hsiung Chen, Sunnyvale; Stanley C. Fralick, Saratoga; Andrew G. Tescher, Claremont, all of Calif.

[73] Assignee: Compression Labs, Inc., San Jose, Calif.

[*] Notice: The portion of the term of this patent subsequent to Nov. 24, 1998, has been disclaimed.

[21] Appl. No.: 277,981

[22] Filed: Jun. 26, 1981

Related U.S. Application Data

[63] Continuation of Ser. No. 969,991, Dec. 15, 1978, Pat. No. 4,302,775.

[51] Int. Cl.³ G06K 9/36; H04N 9/32; H04N 7/12; H04B 3/46

[52] U.S. Cl. ..... 382/56; 358/13; 358/136; 364/514; 364/582; 340/347 DD; 375/31

[58] Field of Search ..... 358/12, 13, 133, 136, 358/138; 364/514, 515, 576, 582; 340/347 DD; 382/56; 375/31; 179/15.55 R

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Primary Examiner—Aristotelis M. Psitos
Attorney, Agent, or Firm—David B. Harrison

[57] **ABSTRACT**

A digital video compression and expansion system and its methods for compressing and expanding digitalized video signals in real time at rates up to NTSC color broadcast rates are disclosed. The system compressor receives digitalized video frames divided into subframes, performs in a single pass a spatial domain to transform domain transformation in two dimensions of the picture elements of each subframe, normalizes the resultant coefficients by a normalization factor having a predetermined compression ratio component and an adaptive rate buffer capacity control feedback component, to provide compression, encodes the coefficients with a minimum redundancy coding scheme and stores them in a first rate buffer memory asynchronously at a high data transfer rate from which they are put out at a slower, synchronous rate. The compressor adaptively determines the rate buffer capacity control feedback component in relation to instantaneous data content of the rate buffer memory in relation to its capacity, and it controls the absolute quantity of data resulting from the normalization step so that the buffer memory is never completely emptied and never completely filled. In expansion, the system essentially mirrors in reverse the steps performed during compression. An efficient, high speed decoder forms an important aspect of the present invention. The compression system forms an important element of a disclosed color broadcast compression system.

11 Claims, 30 Drawing Figures

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DIGITAL VIDEO COMPRESSION SYSTEM AND METHODS UTILIZING SCENE ADAPTIVE CODING WITH RATE BUFFER FEEDBACK

This is a continuation of application Ser. No. 969,991, filed Dec. 15, 1978, now U.S. Pat. No. 4,302,775.

BACKGROUND OF THE INVENTION

The present invention relates to methods and apparatus for compression, transfer through a limited bandwidth medium, and expansion of digitalized television picture signals at real time rates up to standard broadcast frame rates. More particularly, the present invention relates to methods and apparatus for television picture single pass scene adaptive compression, transfer and expansion with two dimensional transformation in conjunction with compression coding schemes wherein rate buffer feedback is effectively utilized to provide optimalized compression normalization factoring in real time without undue degradation of restored picture imagery and with minimized hardware implementation requirements.

Digital coding techniques are increasingly employed in processing television signals for transfer over noisy transmission channels. Digital data streams may be made essentially free of noise degradation, and this advantage in the transmission of digitized information has been advantageously utilized over long, noisy transmission paths. Thus, it is an increasingly common practice today to digitalize broadcast television signals for transmission and relay through otherwise noisy long distance paths, such as stationary earth satellites many thousands of miles away from the earth.

To digitize a television signal, a significant number of bits, 4, 5, 6 or even more, may be required to provide for the proper range of gray scale of each of the hundreds of thousands of separate picture elements (pixels). Consequently, data rates for digitalized television signals are far in excess of the highest frequency components of analog television signals. It is not unusual to find in a digitalized television communications link, a required video bandwidth of 40 megabits per second. While digitalized television transmission formats advantageously overcome the signal to noise problem inherent in analog transmission over similar path lengths, the substantial bandwidths for such digitalized signals often occupy the entire bandwidth capability of the communications link. If the communications link is an earth satellite in stationary orbit above the earth, the video signal typically occupies the entire transpouder bandwidth of the satellite, with very few channels, if any, left over for other uses. Thus, need has arisen for a practical yet effective way to reduce the bandwidth of digitalized television signals to provide for more channels within a communications path such as an earth satellite.

BRIEF DESCRIPTION OF PERTINENT PRIOR ART

It is known and discussed in the prior art relating to television image bandwidth compression that two-dimensional cosine transform techniques have yielded reproduced pictures of superior quality at the same and even higher picture data compression ratios than were obtainable with other transforms or techniques. Heretofore, television picture compression techniques have been directed to simple implementations with substantial throughput speeds in real time with concomitant

significant degradation of restored picture resolution and the introduction of unwanted compression process artifacts into the restored picture. Such techniques have included two-dimensional digital pulse code modulation schemes with block adaptive coding or with rate buffering; hybrid cosine transformation and digital pulse code modulation schemes; and, unidimensional, bidimensional and hybrid Haar-Hadamard transformations. Run length coding has also been employed.

Two basic techniques for coding transform domain coefficients were known in the prior art, namely zonal coding and adaptive coding. Zonal coding essentially eliminated all high frequency picture transform coefficients regardless of energy content with a resultant loss of picture detail upon reconstitution of the picture. On the other hand, adaptive coding schemes, including threshold sampling techniques, were used to identify and preserve large amplitude high frequency coefficients, and those schemes provided reconstituted pictures having less distortion from the compression process at significantly higher degrees of compression. In threshold sampling when a coefficient exceeded a preset amplitude, it was sent with full precision (normaly 6 to 8 bits), and many times a coefficient was transmitted with 8 bits when one or two bits would have accurately characterized the coefficient.

Adaptive coding techniques followed two basic approaches: multiple class energy bit map coding and recursive coding with rate buffer feedback. In the multiple class bit map approach, transform sub-frames of the picture were sorted into categories related to the level of image activity present in each sub-frame. Within each activity level, AC energy coding bits were allocated to individual transform elements in classes according to a variance matrix of the transform data with the variance matrix being computed for each of the classes and different bit allocation matrices being created with more bits being assigned to areas of high image activity and fewer bits to those areas of lower activity. Such classifications were carried out either with a two-pass statistical gathering and mapping scheme or with a fixed pregenerated statistical model created upon assumptions made for the particular system application.

In the two-pass approach, the first pass of processing generated statistics for sub-block classification maps, set up bit assignment matrices and calculated normalization factors for compression. The second pass was for multiplying the normalization factor to quantize transform coefficients, for encoding the resultant data, and for adding overhead information. The drawback of the two pass approach is the substantial times required for two pass processing within existing equipment which unduly limited the size of pictures to be compressed and the number of sub-frame activity classifications that could be utilized. Also, the hardware requirements for real time implementation were prohibitively complex, and hence the two pass approach is presently impractical, particularly at picture broadcast rates.

The pregenerated statistics modeling approach sufferened from the fact that no pregenerated statistics ever exactly matched those of a real time picture being compressed. Additionally, several sets of pregenerated statistics were often needed to accommodate multiple applications which required multiple passes to preselect the most nearly appropriate statistical set to be utilized for the particular picture.

In the recursive coding with rate buffer feedback scheme, the sub-frame activity was determined by the

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estimated variances of the transform coefficients, the variances being derived by a simple linear predicter. One significant drawback in the recursive coding approach was the elimination of high frequency AC coefficients, including those having significant amplitudes. Once the linear predicter produced a variance which needed a zero bit assignment, the encoding of that particular picture subframe was terminated, and all subsequent AC terms, including those with significant values, were lost. Such losses unduly degraded high activity regions in the reconstituted pictures following inverse expansion and reconstruction of the compressed picture signal. Another drawback of the recursive coding scheme was that heretofore there has been no theoretical analysis which justifies the assumed optimality of a linear predicter. One feature of recursive coding which has been advantageously incorporated into and significantly expanded in the present invention is that of the rate buffer technique.

A major problem with image data compression has been the non-stationarity of image statistics. Early coding schemes such as a single map zonal coder attempted to ignore the problem by assuming image statistics as a stationary process. The Markov model used by investigators was an example of the stationary statistical characterization of image data. Adaptive coding procedures have been proposed to take care of the non-stationary nature of the image processes and to improve the image quality. A well designed adaptive coder generally needs a priori non-stationary statistical information. This a priori information can either be estimated or computed on line, or predetermined a priorily. Neither case is desirable since it causes complications in hardware implementation on the former and causes statistical mismatches on the latter. The undesirable feature can be eliminated by introducing the rate buffer concept for the channel rate equalization in accordance with the present invention.

SOME OBJECTS OF THE PRESENT INVENTION

A general object of the present invention is to provide a digital video compression system which effectively combines scene adaptive coding with rate buffer feedback in methods and apparatus which overcome limitations and drawbacks of the prior art.

Another object of the present invention is to provide a digital video compression system which operates effectively at real time picture frame rates as high as those of the NTSC color broadcast standards.

Another object of the present invention is to combine novel circuits and subsystems into a digital video compressor and expander which effectively compresses the bandwidth of a television picture in accordance with novel methods and techniques.

Another object of the present invention is to provide a digital video compression system which effectively implements a two dimensional discrete cosine transform of blocks of the picture.

Another object of the present invention is to provide a digital video compression system which effectively implements a two-dimensional transform in which the DC term of each transformed picture block may always be transmitted in a fixed number of bits.

Another object of the present invention is to provide a digital video compression system which effectively implements a two-dimensional transform of blocks of the picture in which uniformly quantized AC coefficients of each block fall into a single minimum redundancy, e.g. Huffman codeable statistical set.

Another object of the present invention is to provide a digital video compression system which effectively implements a two dimensional tranform of blocks of the picture in which low order uniformly quantized AC coefficients can be efficiently Huffman coded by compressor and decoded by the expander in accordance with a predetermined Huffman code table, without transmitting the Huffman table or generating a new table for each block.

Another object of the present invention is to provide a digital video compression system which implements a two-dimensional transform of blocks of the picture in which long strings of zero value high order AC coefficients may be effectively run length encoded and in which high amplitude high order AC coefficients will be preseved.

Another object of the present invention is to provide a digital video compression system which implements a two-dimensional transformer of blocks of the picture in which variance calculations, bit allocation matrix calculations, and nonlinear block quantization are eliminated and not required in the compression process.

Another object of the present invention is to provide a single pass digital video compression system which implements a two-dimensional transform of blocks of the picture which eliminates the requirement of preliminary statistical matching or preprocessing to determine applicable statistics needed by prior two-pass picture compression techniques.

Another object of the present invention is to provide a digital video compression system which effectively utilizes rate buffer feedback control to provide global adaptivity of the system to the picture in real time.

Another object of the present invention is to provide a digital video compression system which requires only one two-dimensional block of a fraction of the picture for input buffering, but which in practice will buffer at input an image strip of blocks of the same number of lines as defines the block size and will further provide some preformatting of the data.

Yet another object of the present invention is to provide a digital video compression system in which the output of the compression process yields a white noise error image with no apparent structure.

A further object of the present invention is to provide a digital video compression and expansion system in which the expander includes an instantaneous decoder which operates on each bit as it is received.

SUMMARY OF THE INVENTION

An NTSC color broadcast compression and expansion system incorporating the principles of the present invention divides the color picture into luminance (monochrome) and I and Q chrominance components. The luminance signal is compressed and expanded with the scene adaptive coding with rate buffer feedback techniques of the present invention. The I and Q chrominance components are given simple spatial low pass filtering followed by spatial subsampling with two-dimensional interpolation at the system receiver. The audio is filtered and sampled at a predetermined rate, with each sample quantized to a predetermined bit resolution. The digitalized and compressed luminace (including picture synchronization pulses), chrominance and audio components are multiplexed together with bit

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screen synchronization codes and transmitted as a single composite bit stream.

The scene adaptive coding with rate buffer feedback compression system of the present invention receives each digitalized video luminance frame divided into a predetermined matrix of subframes or blocks. The compressor performs a spatial domain to transform domain transformation in both horizontal and vertical dimensions of the picture elements of each subframe to provide transform coefficients corresponding to each subframe. The compression normalizes the coefficients by a normalization factor having a predetermined compression ratio component and an adaptive rate buffer capacity control feedback component to provide compression to the transform coefficients and to provide normalized transform coefficients compatible with a predetermined data coding scheme. The coefficients are encoded in accordance with a predetermined minimum redundancy coding scheme, e.g., Huffman a.c. amplitude coefficient codes and zero coefficient run length codes, and then stored in a first rate buffer memory asynchronously at a high data transfer rate from which they are put out at a slower, synchronous bit stream rate capable of passing through a limited bandwidth medium. The compressor adaptively determines the rate buffer capacity control feedback component in relation to the instantaneous data content of the rate buffer memory in relation to its capacity to control at normalization the absolute quantity of data resulting from that process so that the buffer memory is never completely emptied and never completely filled.

In expansion, the system stores the coded coefficients in a second, decoder rate buffer memory at the slow synchronous data transfer rate through the limited medium. The coefficients are then put out from the second memory asynchronously at a high data transfer rate. The coefficients are decoded in accordance with an inverse of the predetermined coding scheme, and then the decoded coefficients are inversely normalized by operation of an inverse normalization factor with a predetermined expansion ratio coefficient and an adaptive decorder rate buffer capacity control feed forward component to provide expansion of the transform coefficients.

The scene adaptive coded picture expansion system adaptively determines the rate buffer capacity control feed forward component in relation to the instantaneous data content of its rate buffer memory in further relation to its capacity. This is done to control at an inverse normalization step the absolute quantity of data resulting therefrom and thus the rate at which the coded coefficients are put out asynchronously from the expander's rate buffer memory so that it, too, is never completely emptied and never completely filled. A high speed decoder decodes the minimum redundancy in real time in accordance with a "tree" state functional scheme which progressively decides upon a new state on the basis of the old state and the next bit received. The scene adaptive expansion system then performs the inverse of the predetermined transformation of the expanded transform coefficients to provide reconstituted luminance picture elements of the subframes.

The subframes are then assembled into the predetermined matrix to reconstruct the digitalized luminance picture frame which closely approximates the corresponding original frame. The scene adaptive compression/expansion process is repeated frame by frame in real time and the compression ratios achieved are significant, on the order of 40 to 1.

The color broadcast signal is recovered by demultiplexing the decoded luminance, chrominance and audio signals at the system receiver, and these signals are then provided as output.

Other objects, advantages and features of the present invention will become apparent from the following detailed description of a preferred embodiment, presented with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

In the drawings:

FIG. 1 is a block diagram of an NTSC color broadcast compression and expansion system in accordance with the principles of the present invention.

FIG. 2 is a functional block diagram of the scene adaptive coding and decoding method with rate buffer feedback in accordance with the principles of the present invention.

FIG. 3 is a detailed block diagram of the scene adaptive luminance coder and scene adaptive luminance decoder of the system of FIG. 1.

FIG. 4 is a trellis diagram for the discrete cosine transform in one dimension which is implemented in both of the horizontal and vertical consine transformers of the luminance coder of FIG. 4.

FIG. 5 is a block diagram of the discrete cosine transformer used for the horizontal and vertical cosine transformer of the luminance coder of FIG. 3.

FIG. 6 is a block diagram of a shuffle and add module of the discrete cosine transformer of FIG. 5.

FIG. 7 is a block diagram of a shuffle, multiply and add module of the discrete cosine transformer of FIG. 5.

FIG. 8 is a block diagram of the strip memory in the luminance coder and decoder of FIG. 3.

FIG. 9 is a block diagram of the diagonal access memory in the luminance coder of FIG. 3.

FIG. 10 is a functional graph of the operation of the diagonal access memory of FIG. 9.

FIG. 11 is a block diagram of the encoder in the luminance coder of FIG. 3.

FIG. 12 is a timing diagram for a read coefficient code cycle of the encoder of FIG. 11.

FIG. 13 is a block diagram of the encoder controller in the luminance order of FIG. 3.

FIG. 14 is a state diagram for the encoder controller of FIG. 13.

FIG. 15 is a timing diagram of the encoder controller of FIG. 13.

FIG. 16 is a state table for the encoder controller of FIG. 13.

FIG. 17 is a block diagram of the rate buffer memory in the luminance coder of FIG. 3.

FIG. 18 is a block diagram of the buffer memory controller in the luminance coder of FIG. 3.

FIG. 19 is a timing diagram for control sequences of the buffer memory controller of FIG. 17.

FIG. 20 is a block diagram of the rate normalization processor in the luminance coder of FIG. 3.

FIG. 21 is a flow diagram of calculations performed by the rate normalization processor of FIG. 20.

FIG. 22 is a block diagram of the receive buffer memory in the luminance decoder of FIG. 3.

FIG. 23 is a timing diagram for operational sequences of the receive buffer memory of FIG. 22.

FIG. 24 is a block diagram of the receive buffer memory controller in the luminance decoder of FIG. 3.

FIG. 25 is a block diagram of the Huffman decoder in the luminance decoder of FIG. 3.

FIG. 26 is a state diagram of the Huffman decoder of FIG. 25.

FIG. 27 is a timing diagram of terminal state sequence of the Huffman decoder of FIG. 25.

FIG. 28 is a timing diagram of the zero insertion sequence of the Huffman decoder of FIG. 25.

FIG. 29 is a block diagram of the chrominance encoder and chrominance decoder of the system of FIG. 1.

FIG. 30 is a block diagram of the multiplexer and demultiplexer of the system of FIG. 1.

DETAILED DESCRIPTION OF A PREFERRED EMBODIMENT

Compressor 10 and Expander 12

A functional block diagram of an NTSC color broadcast compression/expansion system is provided by FIG. 1. The system includes a composite signal compressor 10. A composite signal expander 12 is connected to the compressor 10 via a limited bandwidth transmission medium 14.

The compressor 10 includes a standard video interface and sync separator 16 which accepts a composite color video input, extracts vertical and horizontal synchronization signals from the video, and demultiplexes luminance (Y) and chrominance (I,Q) components thereof. The separated luminance or monochrome video component along with composite color synchronization information is provided to a horizontal and vertical dimension cosine transformer 18 and a scene adaptive coder 20 which transform and compress the composite luminance video in accordance with principles of this invention. The transformer 18 and coder 20 are described later in connection with FIGS. 2–28.

Separated chrominance components (I,Q) are provided to a chrominance encoder 22 which is described in connection with FIG. 29. Audio is passed through an audio interface 24 which includes an anti-aliasing filter, and then a standard audio PCM encoder 26 which samples the audio at, e.g., 31.25 KHz/sec. and quantizes the samples to, e.g., 256 levels (8 bits). This generates an, e.g., 250 kilobit/sec. data rate. The exemplary sampling rate provides a standard broadcast quality 15 KHz bandwidth audio channel, and the quantization achieves a 55 dB signal to noise ratio.

Coded luminance from the scene adaptive coder 20, coded chrominance from the chrominance encoder 22, and coded audio from the PCM encoder 26 are combined in a multiplexer 28 in a time division format in which the serial bit stream is divided into frames of, e.g. 32 bits. Each frame begins with a sync bit followed by an audio bit, then 10 bits of chrominance and 20 bits of luminance. Preferably, the frame sync bits are alternated in a repetitive pattern which aids in sync acquisition. One entire multiplex frame is reserved for an, e.g., 20 bit "end of block" code which is inserted in a fixed place in the frame to avoid loss of synchronization and catastrophic picture failure in the event of propagation of a bit error. Bit errors can cause incorrect decoding in a way in which code-sync is entirely lost. Use of an end of block code assures restoration of sync without catastrophic picture failure.

In the event that greater security is required against bit error transmission and loss of sync, a convolutional coder, such as a rate one half coder 29 and Viterbi decoder 30 may be used. The coder 29 and decoder 30 are available commercially, and a Linkabit LV 7017A works well.

The expander 12 includes a demultiplexer 32 connected to the Viterbi decoder 20. The demultiplexer 32 separates audio, chrominance and luminance. The luminance is sent to a scene adaptive decoder 34 and two dimensional inverse cosine transformer 36 which restores the original analog picture field/frame format to the luminance (Y) channel. The chrominance is passed through a two dimensional chrominance interpolator 38, described later in connection with FIG. 29, which inputs out the chroma I and Q subcarriers. The chrominance and luminance components are recombined, along with recovered picture sync in a video interface and combiner 40 which puts out a composite color signal.

Audio from the demultiplexer 32 is first passed through a PCM digital to analog converter and filter 42 and then an audio output interface 44 which is the symmetrical inverse of the input interface 24.

Principles of Scene Adaptive Coding with Rate Buffer Feedback

In accordance with one aspect of the present invention, the normalization factor with rate buffer feedback enables a desired variable coding rate for incoming data to be achieved while approaching at all times convergence of an overall desired rate. The normalization process can best be described by mathematical equations written for a 16 pixel (picture element) by 16 pixel block (subframe).

In the adaptive coder 20 of the preferred embodiment, the quantizer is scaled appropriately according to local image statistics and gives rise to a variable rate coding scheme. An appropriate buffering associated with variable rate transform coding on the input and fixed rate channel on the output, then, adapts the coder 20 to local statistical characteristics of the data. The rate buffer will force the adaptive coder 20 to adjust to the local coding variations while ensuring global performance at the desired level.

The rate buffer with feedback normalization factor is designed to permit the desired variable coding rate for incoming data while attempting at all times to converge to the overall rate. The operation can best be described by mathematical formulation: Let

$\bar{R}$=desired channel operating rate

R(i)=required rate for the ith block

$\hat{R}$(i)=accumulated rate at the end of the ith block

n(i)=number of bits into the rate buffer for the ith block

D(i)=feedback normalization factor for the ith block

$\hat{D}$(i)=accumulated normalization factor for the ith block

$$\alpha(i) = \frac{\Delta D(i)}{\Delta R(i)} = \text{slope of the } D \text{ vs. } R \text{ curve at the time of the } i\text{th block}$$

S(i)=normalized buffer status at the end of the ith block

N=size of the rate buffer in bit

$F_i(u,v)$=cosine transform coefficients of the ith block

$\phi(k)$=damping factor at the end of the ith block.

Without loss of generality, assume that the rate buffer is initially half full. The buffer status of this half full posi-

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tion is defined as S(0)=0. The buffer status is normalized and can swing without ±0.5. For a given channel code rate R, buffer size N, initial conditions are set to

$D(1)=D>0$

$\alpha(1)=\alpha<\theta$

The number of bits into the buffer for the first block which is a function of the Huffman code can be represented by

$$n(1)=\sum_{u=0}^{15}\sum_{\substack{v=0\\(u,v)\neq(0,0)}}^{15} H\,F_1\{(u,v)/D(1)\}+F_1(0,0) \quad (1)$$

the first term on the right is the number of Huffman code bits into the buffer for the ac coefficients in the first block while the second term accounts for the number of code bits for the dc term. The buffer status at the end of the first block can be written as,

$$S(1)=\frac{1}{N}[n(1)-256\bar{R}] \quad (2)$$

and gives the normalized deviation of the buffer from its normal half-full status. It is assumed that the block size is 16 by 16=256 coefficients, so that $256\bar{R}$ is the number of bits out of the buffer at the end of the first block. The normalization factor D(1) during the first block operation is assumed to be the initial condition set D(1)=D.

The accumulated rate is then simply given by,

$$\hat{R}(1)=\frac{n(1)}{256} \quad (3)$$

The average feedback normalization factor at this time is identical to the initial condition, i.e.,

$$\hat{D}(1)=D(1)=D \quad (4)$$

Now due to the buffer change the required rate for the second block has to be modified in order to force the buffer to stay as close to the normal half full position as possible. This modification can be described by

$$R(2)=\bar{R}[1.0-S(1)] \quad (5)$$

The deviation btween the required rate for the second block and the accumulated rate at the end of the first block forces the feedback normalization factor to change to

$$D(2)=\alpha(d)\,[R(2)-\hat{R}(1)]+\hat{D}(1) \quad (6)$$

The process carries on block by block basis until the last block of the image is completed.

The generalized equations for K^{th} block can be written as:

$$n(k)=\sum_{u=0}^{15}\sum_{\substack{v=0\\(u,v)\,(0,0)}}^{15} H\,\{F_K(u,v)/D(K)\}+F_K(0,0) \quad (7)$$

$$S(K)=\frac{1}{N}\left[\sum_{i=1}^{K} n(i)-256\,K\,\bar{R}\right] \quad (8)$$

$$\hat{R}(K)=\frac{\sum_{i=1}^{K} n(i)}{256K} \quad (9)$$

-continued

$$\hat{D}(K)=\frac{1}{K}\sum_{i=1}^{K} D(i) \quad (10)$$

$$R(K+1)=\bar{R}\,[1.0-S(K)] \quad (11)$$

$$D(K+1)=[\Phi(K)]^m\,\alpha(K)[R(K+1)-\hat{R}(K)]+\hat{D}(K) \quad (12)$$

A damping factor Φ (K) is introduced in Equation (12) to keep the data inside the rate buffer rapidly converging towards the normal half full position. The introduction of the damping factor not only keeps the data inside the buffer in rapid convergence but also allows one to use a small size buffer for a practical application. The damping factor is strictly dependent upon buffer status and is given by:

$$(K)=1+\theta S(K) \quad (13)$$

where θ is a positive constant.

The slope (K) in Equation (12) is estimated from R(K) and D(K) regardless of the input images, as:

$$|\alpha(K)|=\left|\frac{D(K)}{R(K)}\right| \quad (14)$$

This image independent relationship can be derived by modelling the rate and feedback normalization curve as:

$$RD=C \quad (15)$$

where C is a constant. It can easily be shown that for this model

$$dD/dR\cdot R/D=-1$$

or

$$\alpha=dD/dR=-(D/R) \quad (16)$$

Equations (7) through (12) can be combined to obtain

$$D(K+1)=-[\Phi(K)]^m\alpha(K)\left[\left(\frac{R}{N}-\frac{1}{256K}\right)\left\{\sum_{i=1}^{K}\sum_{u=0}^{15}\sum_{\substack{v=0\\(u,v)\neq(0,0)}}^{15} H\{F_i(u,v)/D(i)\}+F_i(0,0)\right\}-\bar{R}\left(1+\frac{256K}{N}\right)\right]+\frac{1}{K}\sum_{i=1}^{K} D(i) \quad (17)$$

The solution of this difference equation essentially gives the feedback normalization constant D(K) for the required rate R(K) for the Kth block.

The desired operating conditions for the rate buffer algorithm are:

(a) The feedback normalization factor must be as stable as possible.

(b) the buffer status must be able to converge rapidly and stay as close to the half full position as possible.

The condition (a) is key to the performance of the adaptive coder system while the condition (b) is key to the stability of the rate buffer algorithm.

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These two conditions generally work against each other. However with a proper compromise between them a stable system can be achieved with little loss in image quality. By providing enough dynamic range for the feedback normalization factor D(K) the problem of both the underflow and overflow can be successfully prevented, thereby satisfying the desired operating condition (b) above with a minimum buffer size and a moderate damping factor.

Scene Adaptive Coding/Decoding System

The scene adaptive coding and decoding components of the compressor 10 and expander 12 are functionally depicted in the block diagram of FIG. 2, and are shown architecturally in the structural block diagram of FIG. 3.

In the cosine transformer 18, the original image undergoes a two-dimensional cosine transform in 16×16 pixel (picture element) blocks. In the scene adaptive coder 20, the resultant transform coefficients are first normalized at a normalization step 46 by a feedback parameter from a rate buffer. The normalized coefficients are then quantized at a quantization step 48, Huffman coded and run length coded at a coding step 50, and are then rate buffered in a buffering step 52. The rate buffering process 52 is characterized by a variable data rate input and a constant data output with differentials buffer status fed back to control data quantity at the normalization step 46.

In the decoder 34 the received fixed rate data are converted to a variable rate in a rate buffering step 54. Then the data are Huffman decoded and run length decoded in a decoding step 56. The decoded data are the inverse normalized at a normalization step 58 by a feedback parameter developed at the buffering step 54. An inverse two dimensional discrete cosine transform is then performed by the transformer 36 to reconstruct the spatial picture data. The expander rate buffering process 54 keeps track of data flow in the same way as is done by the compressor rate buffering step 52. Thus, no overhead is required anywhere throughout the coding and decoding processes.

Luminance Coder: Cosine Transformer 18 and Scene Adaptive Coder 20

As shown in FIG. 3, the video compressor 10 includes in the cosine transformer 18, a horizontal dimension cosine transformer 60, a corner turning strip memory 62, a vertical dimension cosine transformer 64, a diagonal access memory 66, and a transform timing and control element 68. The scene adaptive coder 20 includes a normalization multiplier 70, a rate normalization processor 72, an encoer 74, an encoder controller 76, a buffer memory 78, and a buffer controller 80, shown diagrammatically with interconnecting data and control signal paths in FIG. 3. Data exits the luminance coder and passes either directly through the communications channel 14 or after multiplexing with chrominance, audio and sync, as shown for the compressor 10 in FIG. 1.

Luminance Decoder: Scene Adaptive Decoder 34 and Cosine Transformer 36

Referring to FIG. 3, transmitted data is received into a luminance decoder comprising the scene adaptive decoder 34 and inverse cosine transformer 36. The decoder includes an input buffer memory 82, a buffer controller 84, a Huffman/run length decoder 86, a normalization multiplier 88, and a rate normalization processor 90. The inverse two dimensional cosine transformer 36 includes a diagonal read in memory 92, a vertical dimension inverse cosine transformer 94, a corner turning strip memory 96, a horizontal dimension inverse cosine transformer 98, and a transform timing and control element 100, as shown in FIG. 3 along with interconnecting data and control signal lines.

Two-Dimensional Cosine Transformers 18, 36

Processors capable of implementing the fast discrete cosine transform are known in general theory to those skilled in the art. The transform processors 60, 66, 94 and 98 are the most critical elements of the entire system by virtue of the sheet magnitude of the calculations and speeds requiring to produce the required transform coefficients at NTSC rates. The processors 60, 64, 94 and 98 are substantially identical to one another and only the horizontal dimension cosine transform processor 60 will be described, it being understood that the other three processors 64, 94 and 98 are substantial duplications of the processor 60.

Cosine Processor 60

The cosine transform processor 60 is a modified implementation of a discrete cosine transform algorithm suggested by the coinventors Chen and Fralick and by C. H. Smith in a paper entitled "A Fast Computational Algorithm for the Discrete Cosine Tranform," published in *IEEE Transactions on Communications*, September 1977. It is the fastest algorithm known, in the sense that it requires the fewest multiply cycles. Furthermore, it is particularly well-suited to a modular pipelined processor. A trellis diagram for this algorithm is shown in FIG. 4. Computations are grouped into five sets of 16 operations. These five stages are:

Stage 1: Sixteen pairs of input data (F_{1x}) points are added or subtracted to result in sixteen intermediate (f_{2x}) results. This is called a shuffle and add operation.

Stage 2: This is a second shuffle and add operation with a different shuffling rule operating on f_{2x} to result in f_{3x}.

Stage 3: In this stage, the sixteen intermediate results (f_{3x}) are shffled, multiplied by constants (in some cases ± 1) and, pairwise, added to result in sixteen more intermediate results (f_{4x}).

Stage 4: This is another shuffle and add operating on f_{4x} with a new shuffling rule to result in f_{5x}.

Stage 5: This is a second shuffle, multiply and add stage with a new shuffling rule and a new set of multiplier constants. The result is F_O, the cosine transform.

Thus, the one-dimensional cosine transform processor 60 may be implemented from a series of shuffle and add stages and shuffle, multiply and add stages. This pipelined concept is shown diagrammatically in FIG. 5. In FIG. 5, data is passed through a first shuffle and add circuit 102, shown diagrammatically in FIG. 6, and configured to perform the arithmetic operations required at stage 1 of the trellis diagram (FIG. 4). A second shuffle and add circuit 104 (FIG. 6) performs the operations required at stage 2 (FIG. 4). A shuffle, multiply and add circuit 106 shown in FIG. 7, performs the operations required at stage 3 (FIG. 4), and a third shuffle and add circuit 108 performs the operations required at stage 4 (FIG. 4). A second shuffle, multiply

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and add circuit 110 performs the calculations required at stage 5 (FIG. 4).

In the implementation shown in FIG. 5, the entire processor 60 is synchronously clocked at the input data rate. During each clock cycle, each stage is provided with a set of control signals which control the stage operation. A four bit counter 12 and a control PROM 114 are provided to control each stage.

To better understand processor operation, consider FIG. 6 which shows shuffle and add modules 102, 104, 108. Data are loaded into one of the two 16-word dual-port RAM's 116, 118, such as the AMD29705. The other RAM is used for the shuffle and add operation. The roles of the RAM's 116 and 118 are interchanged every 16 clock cycles. These RAM's 116, 118 have two output ports, each of which may be independently connected to an addressable memory cell. Thus, to add f_{li} to f_{lj} port A is addressed with an "i" and port B is addressed with a "j". Within one memory-access time, f_{li} and f_{lj} will appear on the two output ports. It is necessary to latch the output of each RAM 116, 118 in a corresponding pipeline register 120, 122 at this point in order to achieve a cycle time short enough to handle data at the 8M bit/sec. data rate. An arithmetic logic unit (ALU) 124 is set to "ADD", so that the resultant sum of the ALU 124 will be $f_{li}+f_{lj}$ although sometimes it is set to "SUBTRACT" to produce a difference $f_{li}-f_{lj}$. The next stage must store this resultant, since it will only remain stable until the next clock cycle. 23 lines from the PROM 114 are required to contro this stage. Eleven lines go to each RAM 116, 118. These include four "A" port address lines, four "B" port address lines, a write-enable and an output-enable for each port. The twenty-third line determines whether the operation of the ALU 124 is "ADD" or "SUBTRACT". Whenever one of the ports is not enabled, its outputs are held low so that a "0" can be added. This allows transfer of data through the ALU 124 with no operation. It is required twice during each stage but the last; e.g., f_{10} and f_{115} are transferred directly to f_{20} and f_{21}.

FIG. 7 shows a shuffle, multiply and add module. It is very similar to the shuffle and add modules 102, 104, 108. the shuffle multiply and add modules 106, 110 include two dual RAM's 126, 128 and pipeline registers 130, 132. A pair of multipliers 134, 136 has been included in series between each register 130, 132 and its input port to an ALU 138. Each multiplier (which must work faster than the maximum operating speed of single chip multipliers such as the AMD 25LS2516) includes two output latched PROMs 140, 142 and an n-bit adder 144.

The inclusion of the multipliers 134, 136 enables each data element to be multiplied by a coefficient prior to adding two products. Because of increased time required to accomplish a multiply operation, the PROMs 140, 142 are provided with pipeline registers in the form of the output latches therein.

In order to operate sequentially, the multiply operation must be accomplished once each cycle. Since NTSC signals must be sampled at 8.269 Mbit/sec., each cycle is 120.9 ns.

This configuration shown in FIG. 7 works because the data to be multiplied are never more than 10 bits wide, and they are always multiplied by a constant which can be selected by 3 bits (i.e., there are never more than 8 distinct constants per stage). The multiplicand is split into the 5 most significant bits and the 5 least significant bits. Each half is used to address a look-up table storedin the PROMs 140, 142. Stored in the look-up table are the partial-products of the 5-bit nibble and every possible coefficient (multiplier). The control PROM 114 generates a 3 bit address corresponding to the coefficient. The partial-products are added in the adder 138. The shuffe, multiply and add modules 106, 110 require 6 more control lines than the shuffle and add modules 102, 104, 108 in order to specify each of the multipliers.

The transform control PROM 114 is shown in FIG. 5. The PROM 114 generates each of the control bits during each cycle and the counter 112 addresses the PROM. The control cycle repeats every 32 clocks, and there are 127 lines to be controlled. Hence, the PROM 114 must be at least 32×128 bits. The speed of the PROM 114 is critical, since it is in series with all pipeline operations. A bipolar PROM with 25 ns access time has been chosen.

Corner Turning Strip Memory 62, 96

The memory 62 in the transformer 18 (and memory 96 in the tranformer 36) serves as a temporary buffer between the horizontal transform processor 60 and the vertical transform processor 64. Sixteen horizontal transforms are performed before the first vertical transform. As shown in FIG. 8, the memory 62, 96 comprises four RAMs 140, 142, 144, 146 configured as a double buffer, each buffer being large enough to store a full 16×16 block of coefficients. These fur RAMs 140, 142, 144, 146 are flip-flopped so that, while one pair 140, 142 is being loaded from the horizontal transform processor 60, the other pair 44, 146 is providing the data to the vertical transform processor 64 (FIG. 3). When a full block has been loaded from the horizontal transform processor 60 and the previous block has been read to the vertical transform processor 64, the function of the pairs is flipped so that the horizontal transform data just loaded into the RAMs 140, 142 will be read to the vertical transform processor 64 while the RAMs 144, 146 just emptied to the vertical transform processor 64 will be loaded from the horizontal transform processor 60. Each pair 140, 142 and 144, 146 is organized as a 4K by 16 bit matrix in order to carry 16 bits precision for the coefficient data, with 256 coefficients per block. A write address counter 148 which counts horizontally through the memory 62 is multiplexed by a write multiplexer 150 between the two pairs 140, 142 and 144, 146. Similarly, a read address counter 152 is connected through a read multiplexer 154 to count vertically through the two memory pairs. Control logic 156 enables the read address counter 152 to count vertically. An inverter 158 is provided in the "write select" line to control the read multiplexer 154.

Diagonal Acces Memory 66; Diagonal Read In Memory 62

The diagonal access memory 66 shown in the cosine transfrmer 18 of the luminance coder of FIG. 3 (and the equivalent diagonal read in memory 92 of the luminance decoder of FIG. 3) is shown in the detailed block diagram of FIG. 9. This memory 66 stores a 16 by 16 block of transformed coefficients in rectangular coordinate format (i.e., one 16-point column at a time). Each RAM bank 160, 162 must be read out in a nonrectangular format, such as illustrated by the diagonal tracing shown in FIG. 10. In order to accomplish diagonal (or more appropriately "non-rectangular" access) the mem-

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ory includes a rectangular write-address counter 164 connected to the bank 160, 162 through a latched multiplexer 166. A read address counter 168 addresses a PROM 170 in which a non-rectangular address map is stored. The address values stored in the PROM 170 are passed through a read multiplexer 172 to read the bank 160, 162 non-rectangularly or diagonally as shown in FIG. 10 (the ideal theoretical case). In practice, the actual read out will define a random pattern, as the coefficients resulting from (or supplied to) the vertical transform processor 64 (94) are in the order shown in the trellis diagram of FIG. 4. One of the RAM banks 160, 162 is loaded with a new pixel on every clock pulse. The loading address is generated by the write counter 164, incremented with each clock pulse. The other bank is read once each clock cycle from the address put out by the PROM as it is addressed sequentially each clock cycle by the read counter 168. The memory 66 is under the control of the transformer timing and control module 68 (FIG. 3).

Transform Control Module 68, (100)

The transform control module 68, (100) shown in FIG. 3 generates all of the required control and clock signals for the transform processors 60, 64, (94), (98), strip memory 62, (96) and diagonal access memory 66 (diagonal read-in memory 92) of the transformer 18, (36). The module 68 accepts the pixel clock and the sync signals which identify the start of each field and line. It trims the field to 512 by 256 pixels per line, by counting six pixels before it starts the transform process, and by stopping the process 512 pixels later. It also ignores the first three lines in every field and stops the process after 256 lines. This module generates clocks and control signals for all other modules of the compressor system 10 (expander system 12).

Encoder 74

The encoder 74 is shown in the detailed block and logic diagram of FIG. 11. It accepts the normalized coefficients frm the normalization multiplier 70 (described later in connection with FIG. 19) and encodes them in accordance with a variable length minimum redundancy code, such as a Huffman code and other known and statistically efficient variations thereof such as a truncted Huffman code. If the coefficients are zero, the encoder 74 counts the run length of zeros and encodes this number as a Huffman code.

The encoder 74 includes a coefficient FIFO memory 174 to buffer the speed variations between the COS transformer 18 and the encoder 74. Two 256-word PROMs 176, 178, respectively, store the Huffman codes corresponding to the coefficients and the run lengths of zero coefficient strings. Each PROM 176, 178 also stores a 5-bit word which is the length of the code word. To speed up the encoding process, each PROM 176, 178 is connected to a corresponding pipeline register 180, 182 which accepts up to 21 bits in parallel and shifts these out serially. A typical read sequence is shown in FIG. 12. The coefficient code PROM 176 accepts the 8 magnitude bits of the cosine coefficient as an address and outputs up to 21 bits of code plus 5 bits of length to a coefficient length register 184. The run-length PROM 178 accepts the run length as an address and outputs a similar code and length word to a zero coefficient length register 186. The run-length PROM 178 is addressed by a zero counter 188 which counts the run length of zero bit strings and selects a code corresponding to that length.

Three sets of tri-state registers 190, 192, 194 and associated buffers 196, 198, 200 are used to generate the end of block (EOB) run length start (RLS) frame sync (FS) codes. The cosine coefficient sign-bit is stored in a flip flop 202 and output through a tri-state buffer 204.

The encoder controller 76 generates a set of control signals which provide all clocks and enable gating signals to pop a new word out of the FIFO 174, advance the run length counter 18, latch the codes in the shift registers 180, 182 and so on. The encoder FIDO 174 output feeds an OR gate 206 and a flip flop 208 which generate a control flag F_c which is input to the encoder controller 76.

The Encoder Controller 76

The encoder controller 76, a sequential state machine, is described structurally in FIG. 13. It implements the state diagram shown in FIG. 14. It includes a pipeline register 210 to hold the state, and a high speed Schottky state table logic element 212 to generate the next state and three flags F_c, $F_B$and F_s in accordance with and as shown in the state table of FIG. 16. The controller 76 further comprises a frame counter 214 to count picture frames, a block counter 216 to count blocks, a bit counter 218 to provide a bit count, and a length counter 220 to count length of end of bit, run length start and frame sync. A two phase clock 222, a shift clock 224, AND gates 226, 228, 230, 232, an OR gate 234, and two flip-flops 236, 238 are also part of the controller 76 and are interconnected as shown in FIG. 13. These logical elements provide the control signals required for the encoder 74.

The timing sequence for the controller 76 is shown in FIG. 15. Assume that the state held in the pipeline register 210 has just stabilized. Then, after a few nanoseconds of delay, both the next state and the control variables should have stabilized and are ready for use. The first phase of the two-phase clock 222 is used with the control variables to generate a set of pulses which advance counters, shift data, and so on in the encoder 74.

If a given state of the controller 76 requires that a code be read (e.g., "Read Coeff Code"), an appropriate pulse is put out to load the correct code into the encoder P/S register 180, and to jam the "Length" word into the preset length counter 220. The "length" word is 2^5 (length in bits of code). The state machine 76 is temporarily halted by disabling its clock 222, and the code is shifted from the parallel to serial register 180. As it is shifted, the shift pulses are counted in the 5-bit length counter 220. When the counter 220 overflows, shifting is stopped, and the controller clock 224 is enabled.

A few nanoseconds after the control variables have been pulsed, the control action will be completed, and the flags will be stable. The second phase of the clock 224 latches the combination of next-state variables and flags which become the new input to the state table logic 212.

Rate Buffer Memory 78

The rate buffer memory 78 is shown in block diagram of FIG. 17. The rate buffer memory 78 comprises an input register 240 which functions to convert the serial data from the encoder 74 into an eight-parallel-bit format which is supplied as a data input to a 32 bit by 8 bit FIFO 242. The FIFO 242 is supplied with two input control signals: load input FIFO and shift FIFO; and

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supplies two output flags: FIFO Full and Data Ready. The FIFO 242 supplies eight bit words stored therein to a 4K by 8 rate buffer memory array 244. The array 244 is a random access read/write memory and is supplied with a twelve bit address word, a negative chip select control signal (CS) and a negative write enable (read/-write) control signal. The output from the RAM 244, which is a parallel eight bit word, is supplied to an eight bit parallel to serial register 246 which functions to return the data to a serial format which is provided at a Q output as serial data. The serial to parallel register 240 is supplied with a clocking signal Φ_S from the encoder controller 76 while the output parallel to serial register 246 is supplied with a different clocking signal Φ_D also from the encoder controller 76. It is to be understood that the clocking signal Φ_S supplied to the input register 240 is a different asynchronus clocking signal from the clocking signal Φ_D supplied to the output parallel to serial register 246. Because the input data arriving at the serial to parallel register 240 may arrive at any time in the encoder output cycle, and the output data must be loaded into the output register 246 synchronously once every eight bits, the input data must occasionally wait to be written into the memory 244; for this reason the 32 by 8 bit FIFO 242 is supplied to compensate for such timing variations.

In the event that the luminance coder and decoder subsystem shown in FIG. 3 is used as a stand-alone compression system, error control will have to be provided by the scene adaptive coder 34. To provide such error control at the scene adaptive decoder 34, an eight bit sync word may be inserted between every 512 output bits of serial data from the eight bit parallel serial register 246 of the buffer memory 78. This word consists of alternating "sync" bit which is utilized to synchronize the decoder 34. Six bits of the word are a binary count to the first bit of the next Huffman Code and a parity calculated over the seven bits. Since the location of the first bit of the Huffman Code is available only at the encoder 74, the six "distance" bits must be counted as the data is input to the memory 244. Then the eight bit sync word must be stored until the proper time for insertion into the output serial data stream. This function is accomplished by the following elements shown in FIG. 17: an eight bit synchronous counter 248, a six bit counter 250, a parity coder 252, an error control 32 by 8 FIFO 254, and a second eight bit parallel to serial output shift register 256 which has its output connected parallel with the output from the output shift register 246 in a tri-state bus configuration. The interleaving of the sync word with the serial data stream is timed and controlled by the memory controller 80 which will be described hereinafter. Additional logic elements are required for the proper functioning of the error control circuit and these include three D type flip flops 258, 260, 262 and AND gates 264, 266, 268, and 270, all configured as shown in FIG. 16.

Buffer Memory Controller 80

The buffer memory controller 80 is shown in the detailed block diagram of FIG. 18. The buffer controller 80 interfaces to the encoder controller 76 to assure that the encoder 74 does not try to shift data to the buffer memory 78 when it is busy. The controller 80 als interfaces to the multiplexer 28 (FIG. 1) accepting timing signals, so that the luminance data stream may be properly interleaved with the chrominance, sound and sync data. The controller 80 functions to generate the required control signals and clocks operate the buffer memory by accomplishing four sequences to be described below and shown in FIG. 19. These four sequences are output read cycle, sync insertion sequence, load input FIFI sequence, and input write cycle.

The buffer controller 80 provides a controller for the buffer memory FIFO 242 which includes a programmable counter 272, a flip flop 274, a four bit counter 276, an AND gate 278, and an OR gate 280 to provide the load input FIFO control signals to the FIFO 242 and generate a wait state when it is full.

Other elements of the buffer controller 80 include a two phase data rate clock 282, a four bit counter 284, a read flip flop 286, a write flip flop 288, a five bit counter 290, an insert sync flip flop 292, a read address counter of twelve bits 294, and a write address counter of twelve bits 296, to provide read/write addresses to the memory 78. Other control signal producing logic elements of the controller 80 include AND gates 298, 300, 302, 304, 306, and 308. An OR gate 310 and an inverter 312 make up the balance of logic elements for the controller 40. These elements 298–312 are configured as shown in FIG. 17 to produce the control signals desired.

As shown in FIG. 19, the output read cycle control sequence must be accomplished synchronously with the output data once every eight bits, and so it may be regarded as a master cycle taking precedence over the other cycles. As the buffer memory output register 246 (FIG. 17) is shifted, the shift pulses are counted by the four bit counter 284. When the eighth bit occurs, the counter 284 overflows and sets the read flip flop 286 which together with the two phase clock 282 generate the chip select (CS) and load shift register pulses. These pulses enable the buffer memory 244 to be read and to load the output shift register 246.

In the case of the stand-alone scene adaptive coder sync insertion sequences are provided once every 512 bits (64 bytes). At such occurrence the sync word is interleaved into the data stream by operation of the sync word register 256. The output read cycle is inhibited for eight bits while the interleaving of the sync word is accomplished. The five bit counter 290 counts the output bytes and generates the required control signals when it overflows and sets the sync flip flop 292.

The load input FIFO sequence occurs when the buffer memory input shift register 240 fills which occurs once every eight bits. At this point, it is loaded into the FIFO 242. The four bit counter 276 counts the input bits and halts the encoding process long enough to load the FIFO 242 when the eighth bit occurs. If the FIFO fills, the encoding process is stopped by a wait state generated through the OR gate 280 until the word is loaded from the FIFO 242 into the memory 244.

The input write cycle occurs whenever the FIFO 242 has data ready to load into the memory 244 and it is not then being read. This cycle is initiated by the FIFO "data ready" signal supplied to the AND gate 300, passed through the flip flop 288 and returned to the memory 244 as a write enable (WE) signal from the gate 306. Also the inverting input of gate 248 is connected to the input of gate 254. The input read cycle is inhibited during the output write cycle.

The read address counter 294 contains the address of the next data output byte while the write address counter 296 points to the next input byte. The read address counter 294 is enabled and clocked whenever

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the output is read. The write address counter 296 is enabled and clocked whenever input data is written.

Rate Normalization Multiplier 70 and Processor 72

The buffer feedback controlled state normalization multiplier 70 and processor 72 are shown in FIG. 20. Their function is to calculate the normalization factor $1/D_K$ for each block of the input transform coefficient in real time. The computation is based on the last value of D and the number of bits loaded into the rate buffer memory 78 during the last block or subframe. A simplified flowchart for the calculations made by the rate normalization processor 72 is set forth in FIG. 21. The calculations which must be made are based on the recursive relations

$$D(K+1) = \Phi(k)^m D(k) \frac{S(k) - S(k-1)}{1.5 - S(k-1)} + D(k) \quad (18)$$

$$\Phi(k) = k + S(K) \text{ sign } (S(k) - S(k-1)) \quad (19)$$

$$S(K) = S(k-1) + \Delta(k) - R_o/R_I \quad (20)$$

where

(k)=Number of coded bits in block k

R_o=desired synchronous output bit rate

R_I=desired synchronous input bit rate

The calculations set forth in the flow diagram of FIG. 21 require the use of eight of sixteen bit registers for storage of intermediate results and recursive constants. The calculations require the following arithmetic operations on two sixteen bit numbers: five additions, three multiplies and two divides.

The rate normalization processor 72 comprises four bipolar bit-slice MPUs 314, 316, 318 and 320, such as the AMD 2903, as shown in FIG. 20. These four bit-slice processors 314, 316, 318, 320 are connected with lookahead carry and are used in a pipeline control architecture for maximum speed. A microprogram controller 322 (AMD type 2910) and a 256 by 40 bit microprogram memory 324 are provided to control the operation of the processors 314, 316, 318 and 320. The rate normalization processor 72 also includes a 32 by 8 bit interrupt vector map 326, a pipeline register 328, a constant PROM 330, a decoder 332, a status and shift control 334 (AMD type 2904), a look ahead carry 336 (AMD 2902), and four latches 338, 340, 342 and 344, all configured as shown in FIG. 20.

The processor 70 operates with four external interrupts: a power up restart, a change rate, a bit count ready, and block transform done, all supplied to the vector interrupt map 326. Each of these interrupts vector the program stored in the memory 324 to the appropriate subroutine shown in FIG. 21. The power up restart starts the initialization process which loads the initial values of the constants R_o/R_I, D_o, $D_I(1.5\text{-}S^{-1})$ and $(S_o S_{-1})$ into appropriate registers, and outputs $1/D_o$.

The "change rate" interrupt causes the processor 72 to read an external i/o port which contains the desired value of R_o/F_I, and then initializes all other constants. The change rate interrupt enables an operator to vary the input and output rates.

The bit count ready interrupt causes the processor 72 to input a new value of bit count (Δ), and calculates a new value of 1/D. This value is then stored awaiting the end of the block transform interrupt. This latter interrupt transfers the new value of 1/D to the output latch 344.

Scene Adaptive Decoder 34

Decoder Buffer Memory 82

The decoder buffer memory 82 is shown in the block diagram of FIG. 22 which reads from right to left. The expander buffer memory 82 functions to buffer the input serial data received from the communications channel 14 to accommodate the operation of the Huffman decoder 86, normalization multiplier 88 and processor 90, and inverse transformer 36 (FIG. 3). The buffer 82 converts the input serial data into a parallel format, stores the data and then reconverts the data back into a serial format. Thus, it includes a serial to parallel register 346, an eight bit latch 348, a rate buffer memory array 350, a 32 by 8 bit FIFO 352, and a parallel to serial register 354. Because of the speed of the data and the access time of the memory 350, the eight bit latch 348 is provided as a buffer between the serial to parallel register 346 and the rate buffer memory array 350. This latch 348 functions to pipeline input data into the memory 350. Furthermore, to put out data asynchronously as rapidly as needed and so as not to interfere with the input write cycle, the 32 word FIFO 352 is provided between the rate buffer memory 350 and the output parallel to serial register 354.

The control sequence is to write data into the memory 350, read data from the memory 350 and load the output shift register 354 as shown in the sequences timing chart in FIG. 23. The timing shown in FIG. 23 writes one eight bit byte and then reads none, one or two eight bit bytes while the input shift register 346 is accepting eight bits. Then the eight bit latch 348 latches the input data. The state of the output FIFO 352 determines how many bytes are read. When the output FIFO 352 is full, no more bytes will be read. Until the FIFO 352 is full, two bytes will be read as shown in FIG. 23. The FIFO 352 is emptied as rapidly as the Huffman decoder 86 can decode the data received from the register 354 and generate coefficients which will then be inversely transformed in the decoder transformer 36.

Decoder Buffer Controller 84

The decoder buffer controller 84 is shown in FIG. 24. The controller 84 generates all of the timing signals necessary to control the decoder buffer memory 82.

The controller 84 includes a two phase clock 356 synchronized to the data clock and the logic elements required to generate the control signals shown in FIG. 22. Thus, the controller 84 includes a four bit counter 358, a write flip flop 360, and an AND gate 362 which provide the latch control signal. Two flip flops 364 and 366 along with an OR gate 368 are configured to provide a write enable ($\overline{WE}$) control signal. A write address counter 370 and a read address counter 372 provide the necessary addressing for the memory array 350 (FIG. 22).

The load FIFO signal is provided by the combination of AND gate 374, 376, and 378 along with two flip flops 380 and 382. The operation of the read address counter is enabled by an AND gate 384. The load shift register signal is provided by a counter 386 to which a flip flop 388 is connected to provide the shift FIFO control signal.

Synchronizer

A synchronizer, not shown, would be connected to the memory 82 and controller 84 to decode error control sync generated by the scene adaptive coder in a stand-alone system. It would monitor the input data stream to obtain sync from the error control byte inserted by the coder 20 as described above. The synchronizer would also read the six bit portion of the sync word which contains the count to the start of the next Huffman code. The synchronizer would generate a signal which resets the Huffman decoder 86 to a "start" state thus assuring periodically that it is and remains in sync with the incoming data. Preferably, the synchronizer is implemented as a high speed hardware processor.

Huffman Decoder 86

The Huffman decoder 86 is shown in the detailed block and logic diagram of FIG. 25. A decoder state diagram for a typical Huffman code is shown in FIG. 26. As will be appreciated by reference to FIGS. 25 and 26, the decoder 86 has been implemented as a finite state machine which functions instantaneously to decode each bit as it is received. This approach is required because the data arriving at the decoder 86 from the buffer memory 82 (and synchronizer) is in a serial data stream format of a sequence of Huffman codes which must be decoded very rapidly. The Huffman code results in coefficient words at variable length. The length is not known to the decoder 86 until the word has been decoded.

With reference to FIG. 25, the decoder is seen to include a decoder PROM 390 which receives the input data in serial format, a ten bit latch 392 which functions to address the decoder PROM 390, a FIFO 394 which receives decoded coefficients from the decoder PROM and stores them, a two bit decoder 396 which functions to decode the end of bit signal (EOB) and frame sync signal (FS), an output selector 398 which receives eight parallel bits from the FIFO 394 or eight zero bits and selects between them in accordance with the nature of the output coefficient. The encoder 86 further includes an eight bit counter 400 to which a dual D flip flop 402 and two AND gates 404 and 406 are connected, a logic element 408 which implements the following logic equations:

$$D_1=(\overline{Q}_1\cap Q_2\cup Q_1\cap\overline{Q}_2\cap ZC) \quad (21)$$

$$D_2=(\overline{Q}_1\cap Q_2\ (\cup)\ Q_1\cap Q_2\cap\overline{OF}), \quad (22)$$

and a three input AND gate 410 which is connected to the shift out input of the FIFO 394.

Additional circuitry of the decoder includes three AND gates 412, 414 and 416, an operator selector control circuit 418, and a serial to parallel register 420 which provides outputs for compression, frame rate and resolution control.

The decoder 86 sequentially decodes the input serial bit stream, one bit at a time with the 2 K by 12 PROM 390 which implements the state diagram of FIG. 26. From the state diagram, it is clear that a decision of the new state can be made knowing old state and the next bit. The output of the decoder 86 is captured in the latch 392 and is used with the next bit to address the PROM 390 which implements the state diagram of FIG. 26. The new state has been preprogrammed into the PROM 390 and it is then put out as the old state for the next bit. The latch 392 must be strobed once per bit, if the bit is to be decoded, and so it is connected to the sync clock input. The decoder 86 must decode two Huffman codes, each with 256 words. It can be shown that a "tree" diagram, such as that shown in FIG. 26, requires less than 512 states to decode a 256 word code, hence a total of 1 K states are required, no more. The states are numbered so that the least-significant eight bits of the ten bits determining the state for the terminal states are either the coefficient of the coded cosine coefficient, or they are the run length of the run length, depending on the code word. When a terminal state is reached, as shown in the timing diagram of FIG. 27, the eight least significant bits and two control bits are loaded into the FIFO. The next data bit is also loaded into the FIFO 394.

The two control bits are used to designate the nature of the code word: frame sync, end of block, coefficient, or run length. These are programmed into the PROM 390 as part of the state diagram implementation shown in FIG. 26.

The FIFO 394 acts to separate the operation of the decoder 86 which must operate asynchronously from the inverse cosine transformer 36 which operates synchronously with the video output.

When a word reaches the end of the FIFO 394, the control bits are decoded by the two bit decoder 396 to generate the end of bit and frame sync signals. If a run length has been decoded, the appropriate number of zero value coefficients are generated by operation of the eight bit counter 400, dual D flip flops 402 and logic 408. These coefficients are inserted into the coefficient stream by operation of the two to one output selector 398. The timing sequence for zero insertion is shown in FIG. 28.

Chrominance Encoder 22, Decoder 38

The chrominance encoder 22 and chrominance decoder 38 are shown in FIG. 29. The encoder 22 operates on the separated I and Q analog signals to produce an encoded digital bit stream at an average rate of 0.375 bits per pixel. This is accomplished by sampling I and Q chrominance components at the full bandwidth pixel rate with eight quantization levels per pixel. The digitized chrominance is then filtered and down-sampled along the scan line to achieve a 4 to 1 bit rate reduction. Filtering in the vertical dimension is achieved by averaging pairs of lines, and temporal filtering is realized by recoding only I data for, e.g., odd-line fields and only Q data for even-line fields. The chrominance signals are sampled at full bandwidth rates and all filtering operations are performed digitally using finite impulse response techniques capable of perfect phase linearity.

In the chrominance encoder 22, the I and Q chrominance signals are first applied to a 2 to 1 multiplexer 424 which selects the I signal for odd line fields and the Q signal for even line fields. This selection is followed by a buffer amplifier 426 which provides a low source impedance signal to an analog to digital converter 428. A high speed parallel or flash 3 bit converter 428 is used which eliminates any need for a sample and hold circuit. Standard modules such as the Datel MX808 multiplexer, AM-102A buffer amplifier and HU38MC A/D are used for the multiplexer 424, amplifier 426 and converter 428.

The digitized data are averaged along the scan line in blocks of 4 pixels and vertically over two lines by an

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ALU 430 formed, for example, of two 74LS181 integrated circuits and associated control logic. On the first scan, i.e., one to be averaged within a field, 4 pixels are added to form a 5-bit sum which is stored in a line buffer 432 after passing through a multiplexer 434. The process is repeated for all 464 pixels to be processed in a line, on the next scan in the field, the 4 pixel sums are formed as before and added to the corresponding sum from the line buffer 432 to form a 6-bit sum of 8 pixels. The three most significant bits of this 8 pixel sum are then loaded from the ALU 430 to an output FIFO buffer 436 via the multiplexer 434. A controller 438 for the ALU 430 and an output parallel to serial shift register 440 are also required for the encoder 22, as shown in FIG. 29.

The chrominance decoder 38 shown in FIG. 29 performs the inverse function of the encoder 22. Since the I chrominance component is encoded and transmitted for, e.g., the odd-line fields and the Q component for the evenline fields, it is necessary to store in a field buffer memory 442 the previous field of chrominance data (in compressed form) to provide the I and Q data for each reconstructed pixel. Every other line in the regenerated field is interpolated from its adjacent lines. This interpolation is accomplished with a single ALU chip 444 which is connected to the field buffer 442 through a latching demultiplexer 446. The reconstructed line chrominance data (still compressed 4 to 1 horizontally) is fed to an output FIFO buffer 448 for sequential I, Q pairs. These data are then retrieved from the FIFO 448, demultiplexed into separate I and Q channels, expanded horizontally and converted to the analog domain in a digital to analog converter 450. A controller 452 and an input serial to parallel shift register, buffer 454 are also required for the decoder 38 in the configuration shown in FIG. 29.

Multiplexer 28, Demultiplexer 32

As shown in FIG. 30, the multiplexer 28 (FIG. 1) accepts the three coded signals: luminance, chrominance and sound, into three FIFO buffer memories 456, 458, 460. The outputs of these memories 456, 458, 460 are combined with a sync word from a sync generator 462 into a single composite data stream by a selector 464. Video sync is carried within luminance data. (If the scene adaptive coder 20 and decoder 34 are configured as a stand-alone system, the sync word would be provided by the buffer memory 78 and a synchronizer in the decoder 34, as already mentioned.) A five bit frame counter 466 and a selector control PROM 468 are provided to control the selector 464.

The demultiplexer 32 accepts the data stream, and it separates out the sync word with a synchronizer 470 which synchronizes operation of the entire expander 12 to the incoming data stream. The incoming data is provided to selector 472 which separates luminance, chrominance and audio data and loads the data into three elastic buffers 474, 476, 478. These buffers are emptied at a constant rate by the scene adaptive decoder 34, the chrominance decoder 38 and the audio decoder 42 (FIG. 1) already described. The selector 472 requires a five bit frame counter 480 and a selector mapping PROM 482, for locating sync words and directing data to the FIFOs 474, 476, 478.

To those skilled in the art to which this invention relates, many changes in construction and widely differing embodiments and applications of the invention will suggest themselves without departing from the spirit and scope of the invention. The disclosures and the description herein are purely illustrative and are not intended to be in any sense limiting.

We claim:

1. A data compression method for adaptive coding, transferring, and decoding a stream of data coefficients in which some of said coefficients are of zero magnitude, said method comprising compression steps prior to transfer through a limited bandwidth medium and expansion steps following such transfer, said compression steps comprising:

multiplying said data coefficients by a normalization factor which includes an automatically variable feedback control component and a predetermined compression component and putting out the product resulting therefrom as normalized data coefficients;

minimum redundancy coding of the amplitude of said normalized coefficients and including run length coding of zero magnitude coefficients between coefficients greater than zero;

writing said minimum redundancy and run length coded coefficients into a compressor buffer memory at a high asynchronous rate, deriving said feedback control component which is a function of the instantaneous quantity of data in said memory in relation to the capacity thereof, and reading out to said limited bandwidth medium said coded coefficients at a predetermined low synchronous transmission rate,

said expansion steps comprising:

receiving said coder coefficients from said limited bandwidth medium at said low synchronous transmission rate;

writing said coded coefficients rate into an expander rate buffer memory, reading out of said memory said written coefficients at a high asynchronous rate and supplying an automatically variable feed forward control component which is a function of the instantaneous quantity of data in said expander buffer memory in relation to the capacity thereof;

decoding said minimum redundancy and run length coded coefficients;

multiplying said decoded coefficients by a predetermined inverse normalization factor which includes said automatically variable feed forward control component and an inverse of said predetermined compression component, and putting out the product resulting therefrom as a stream of reconstituted data coefficients.

2. The method set forth in claim 1 wherein said step of deriving said feedback control component in said compression steps includes the further step of generating said rate buffer feedback control component nonlinearly in accordance with a predetermined capacity control damping factor so that said compressor buffer memory may be of less storage capacity than otherwise and not be subject to data overflow in accordance with said predetermined damping factor.

3. A data compression system for coding, transferring and decoding a stream of data coefficients in which some of said coefficients are of zero magnitude, said system comprising a compressor and an expander connected to the compressor through a communications path,

said compressor including:

normalization multiplier means for multiplying said data coefficients by a normalization factor which

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includes an automatically variable rate buffer capacity control feedback component and a predetermined compression component and for putting out the product resulting therefrom;

encoder means connected to said normalization multiplier means including coding means for providing variable length, substantially derived, minimum redundancy coding of amplitude coefficients and run length coding of zero amplitude coefficients for further compression and transfer through said communications path to said expander,

compressor rate buffer memory means connected to said encoder means and having a feedback connection to said normalization mulitplier means, for writing said coded coefficients from said encoder means at a high asynchronous rate, for supplying said normalization multiplier means with said rate buffer capcity control feedback component which is a function of the instantaneous quantity of data in said memory in relation to the capacity thereof, and for reading out to said communications path said cooled coefficients at a predetermined low synchronous transmission rate, said rate buffer memory means further including means for generating said rate buffer capacity control feedback component nonlinearly in accordance with a predetermined capacity control damping factor so that said rate buffer memory means may be of less capacity than otherwise and not be subjected to data overflow in accordance with said predetermined damping factor,

said expander including:

expander rate buffer memory means having an input connected to said communications path, for writing said synchronously sent coded coefficients at said predetermined rate, for reading out said written coefficients at a high asynchronous rate and for supplying an automatically variable feed forward control component which is a function of the instantaneous quantity of data in said memory in relation to the capacity thereof;

decoder means connected to said expander rate buffer memory means for decoding said minimum redundance and zero run length coded coefficients in accordance with an inverse of said predetermined data coding scheme;

inverse normalization multiplier means connected to said decoder means and to said expander rate buffer memory means for multiplying said decoded coefficients by a predetermined inverse normalization factor which includes said automatically variable feed forward control component and an inverse of said predetermined compression component, and for putting out the product resulting therefrom as a stream of reconstituted data coefficients.

4. A data compression system for coding, transferring through a limited bandwidth communications path and decoding color television broadcast signal in real time, including a compressor, and an expander, wherein said processor comprises:

audio encoding and compression means for compressing an audio component of said broadcast signals and for providing a compressed digital data stream thereof,

video separator means for separating a video component of said broadcast signals into chrominance and luminance portions,

chrominance encoder means connected to said separator means for encoding said chrominance portion to provide a digital data stream theoref;

transformer means connected to said separator means for performing predetermined transformations to the picture elements of said luminance portion to provide transform coefficients thereof,

normalization multiplier means connected to said transformer means for multiplying said transform coefficients by a normalization factor having a predetermined compression component and an adaptive rate buffer capacity control feedback component to provide compression and to provide normalized transform coefficients compatible with a predetermined data coding scheme,

encoder means for encoding said normalized transform coefficients in accordance with said predetermined data coding scheme, including coding means for providing a variable length, statistically derived, minimum redundancy coding of amplitude coefficients and run length coding of zero amplitude coefficients for further compression thereof,

rate buffer memory means connected to said encoder means for storing said coded coefficients asynchronously at a high data transfer rate, for putting out said coded coefficients at a slow data transfer rate capable of passing through said limited bandwith medium, and for adaptively determining said rate buffer capacity control feedback component in relation to the instantaneous data content of said rate buffer memory means in further relation to its capacity, to control at said normalization multiplier the absolute quantity of data resulting from the operation thereof so that said rate buffer memory means is never completely emptied and is never completely filled,

multiplexer means connected to said audio encoding means, said chrominance encoder means, and said rate buffer memory means, for multiplexing said digital data streams of audio, chrominance portion, and compressed luminance portion into a single composite data stream for transmission through said limited bandwidth medium,

and wherein said expander comprises:

demultiplexer means for demultiplexing said composite data stream into said compressed luminance and chrominance portions and said audio component,

chrominance decoder means connected to said demultiplexer means for decoding said chrominance portion into a chrominance signal,

second rate buffer means connected to said demultiplexer means for receiving said coded coefficients at said slow data transfer rate, for putting out said coded coefficients at an asynchronous high data transfer rate, and for determining a rate buffer capacity control feed forward component in relation to said instantaneous data content of said second rate buffer memory means in further relation to its capacity so as to control the absolute quantity of data contained therein,

decoder means connected to said second rate buffer memory means for decoding said coded coefficients in accordance with an inverse of said predetermined data coding scheme;

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inverse normalization multiplexer means for inversely normalizing said coded transform coefficients by operation of an inverse normalization factor having a predetermined expansion ratio component, and said second rate buffer capacity control feed forward component to provide expansion of said transform coefficients in relation to the instantaneous absolute quantity of data contained in said second rate buffer memory means,

inverse transformer means connected to said inverse normalization multiplier means for performing inverses of said predetermined transformations of said expanded transform coefficients, to provide reconstituted said luminance portion,

video combiner means connected to said inverse transformer means and to said chrominance decoder means for combining and putting out said expanded and decoded luminance portion and chrominance portion as a single composite color video signal, and

audio expander and decoder means connected to said demultiplexer means for expanding, decoding and putting out said audio component as an audio signal.

5. A data compression method for adaptive coding a stream of data coefficients in which some of said coefficients are of zero magnitude, and transferring said adaptively coded coefficients through a limited bandwidth medium, comprising the steps of:

multiplying said data coefficients by a normalization factor which includes an automatically variable feedback control component and a predetermined compression component and putting out the product resulting therefrom as normalized data coefficients;

encoding said normalized transform coefficients in accordance with said predetermined data coding scheme including variable length, statistically derived, minimum redundancy coding of amplitude coefficients and including run length coding of zero amplitude coefficients for further compression and transfer through said limited bandwidth medium

writing said minimum redundancy and run length coded coefficients into a compressor buffer memory at a high asynchronous rate and deriving said feedback control component as a function of the instantaneous quantity of data in said memory in relation to the capacity thereof; and,

reading out to said limited bandwidth medium said coded coefficients at a predetermined low synchronous transmission rate.

6. A method for one pass compression and transfer at a slow synchronous rate through a limited bandwidth medium of digitalized television images in real time, including the steps of:

performing predetermined transformations of the picture elements of said images to provide transform coefficients thereof,

multiplying said transform coefficients by a normalization factor having a predetermined compression component and an adaptive rate buffer capacity control feedback component to provide compression and to provide normalized transform coefficients compatible with a predetermined data coding scheme,

encoding said normalized transform coefficients in accordance with said predetermined data coding scheme including variable length, statistically derived, minimum redundancy coding of amplitude coefficients and including run length coding of zero amplitude coefficients for further compression and transfer through said limited bandwidth medium,

storing said coded coefficients in a rate buffer memory asynchronously at a high data transfer rate and adaptively determining said rate buffer capacity control feedback component in relation to the instantaneous data content of said rate buffer memory in further relation to its data storage capacity, thereby for controlling at said normalization step the absolute quantity of data resulting therefrom so that said rate buffer memory is never completely emptied and is never completely filled, and

putting out to said limited bandwidth medium said coded coefficients at a slow data transfer rate capable of passing through said medium.

7. A data expansion method for adaptive decoding of a stream of data coefficients which have been compressed in accordance with a predetermined compression component which includes minimum redundancy coding of amplitude coefficients and run length coding of zero amplitude coefficients and which have been received from a limited bandwidth medium at a low synchronous transmission rate, comprising the steps of:

writing said compressed data coefficients into an expander rate buffer memory and generating an automatically variable feed forward control component which is a function of the instantaneous quantity of data in said expander rate buffer memory in relation to the capacity thereof;

reading out of said memory said written coefficients at a high asynchronous data rate;

decoding said minimum redundancy and run length coded coefficients;

multiplying said decoded coefficients by a predetermined expansion normalization factor which includes said feed forward control component and an inverse of said predetermined compression component, and putting out the product resulting therefrom as a stream of reconstituted data coefficients.

8. A data compression system for coding a stream of dat coefficients in which some of said coefficients are of zero magnitude and transferring said coded coefficients through a communications path, said compression system including:

normalization multiplier means for multiplying said data coefficients by a normalization factor which includes an automatically variable feedback control component and a predetermined compression component and for putting out the product resulting therefrom;

encoder means connected to said normalization multiplier means for encoding said normalized coefficients including coding means for providing variable length, statistically derived, minimum redundancy coding of amplitude coefficients and run length coding of said zero amplitude coefficients for further compression and transfer through said communications path,

compressor rate buffer memory means connected to said encoder means and having a feedback connection to said normalization multiplier meand, for writing said coded coefficients from said encoder means at a high asynchronous rate, for generating and supplying said normalization multiplier means

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with said feedback control component as a function of the instantaneous quantity of data in said memory in relation to the capacity thereof, and for reading out to said communications path said coded coefficients at a predetermined low synchronous transmission rate.

9. A system for one pass expansion of digitalized video images in which picture elements have been transformed pursuant to a predetermined transformation and then compressed to data coefficients in accordance with a predetermined data coding scheme which includes variable length, statistically derived minimum redundancy coding of amplitude coefficients and run length coding of zero amplitude coefficients, said transformed and compressed data coefficients being received from a limited bandwidth medium, said system comprising:

expansion rate buffer memory means connected to said limited bandwidth medium to receive said data coefficients at a slow synchronous transfer rate, for putting out said data coefficients at an asynchronous high data transfer rate, and for generating a rate buffer capacity control feed forward component in relation to said instantaneous data content of said expansion rate buffer memory means in further relation to its data storage capacity so as to control the absolute quantity of data contained therein,

decoder means connected to said expansion rate buffer memory means for decoding said data coefficients in accordance with an inverse of said predetermined data coding scheme,

inverse normalization multiplier means for inversely normalizing said decoded data coefficients by operation of an inverse normalization factor having a predetermined expansion ratio component and said expansion rate buffer capacity control feed forward component to provide expansion of said transform coefficients in relation to the instantaneous absolute quantity of data contained in said expansion rate buffer memory means;

inverse transformer means connected to said inverse normalization multiplier means for performing inverses of said predetermined transformations of said expanded transform coefficients, to provide reconstituted picture elements of digitalized video images.

10. In a one pass digitalized video compression system enabling digitalized video to be passed through a limited bandwidth communications path, a compressor comprising:

a compressor input connected to receive digitalized data in line scan format and at a synchronous rate related to the video sync, said data corresponding to subframes of each frame of a television picture;

first discrete cosine transformer means for computing the discrete cosine transform in one dimension of each said subframe;

first buffer memory means connected to said first transformer means for writing discrete cosine transform coefficients of each said subframe in a predetermined writing pattern and for reading said written coefficients in a second predetermined pattern which differs from said first predetermined writing pattern;

second discrete transformer means connected to receive said read coefficients from said buffer memory means, for computing the discrete cosine transform of each said subframe in a second dimension relative to the dimension followed by said first cosine transformer means;

first diagonalization memory means connected to said second transformer means for writing descrete cosine transform coefficients put out by said second transformer means in a third predetermined pattern and for reading said written coefficients in a fourth predetermined pattern;

normalization multiplier means connected to said diagonalization memory means for multiplying the coefficients read in said fourth pattern therefrom by a normalization factor which includes an automatically variable feedback control component and a predetermined compression component and for putting out the product resulting therefrom;

ecoder means connected to said normalization mulitplier means for encoding said normalized coefficients by providing a variable length, statistically derived minimum redundancy coding of amplitude coefficients and run length coding of zero amplitude coefficients between coefficients greater than zero;

compressor rate buffer memory means connected to said encoder means and having a feedback connection to said normalization multiplier means, for writing said coded coefficients from said encoder means at a high asynchronous rate, for supplying said normalization multiplier means with said feedback control component as a function of the instantaneous quantity of data in said rate buffer memory means in relation to the capacity thereof, and for reading out said coded coefficients at a predetermined lower synchronous rate than as asynchronously received from said encoder means and written therein; and,

an output connecting said rate buffer memory means to said limited bandwidth medium.

11. In a one pass digitalized video expansion system for data corresponding to subframes of video which has been subjected to discrete cosine transformation in two spatial dimensions and further subjected to predetermined data compression including a predetermined compression component and further including variable length, minimum redundancy coding of amplitude coefficients and run length coding of zero amplitude coefficients lying between said amplitude coefficients and which has then passed through a limited bandwidth medium, an expander comprising:

an expander input connected to said limited bandwidth medium for receiving said coefficients at a predetermined low synchronous data rate to said medium,

expander rate buffer memory means connected to said expander input for writing said synchronously received coded coefficients at said predetermined transmission rate, for reading out said written coefficients at a higher asynchronous rate and for supplying an automatically variable feed forward control component which is a function of the instantaneous quantity of data in said memory in relation to the data storage capacity thereof,

decoder means connected to said expander rate buffer memory means for decoding said minimum redundancy coded amplitude coefficients and said run length encoded zero amplitude coefficients,

inverse normalization multiplier means connected to said decoder means and to said expander rate buffer

KODAK_000076

memory means for multiplying said decoded coefficients by a predetermined normalization factor which includes said automatically variable feed forward control component and an inverse of said predetermined compression component, and for putting out the product resulting therefrom,

diagonalization memory means connected to said inverse normalization multiplier means for writing said coefficients received therefrom in a first predetermined pattern and for reading out said coefficients in a second predetermined pattern,

first inverse discrete cosine transformer means connected to said diagonalization memory means for

computing the inverse discrete cosine transform of said coefficients in a third pattern,

second buffer memory means connected to said first inverse discrete cosine transformer means for writing said inversely tranformed coefficients in a fourth pattern,

second inverse discrete cosine transformer means connected to said second buffer memory means for computing the inverse cosine transform for said coefficients read in a fifth pattern and for putting out reconstituted digitalized data of each subframe in line scan format.

* * * * *

340-347 DO AU 234 EX
CCC22 Exp XR 4,394,774

UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO. : 4,394,774
DATED : July 19, 1983
INVENTOR(S) : Widergren, et al.

It is certified that error appears in the above-identified patent and that said Letters Patent are hereby corrected as shown below:

In the drawings, sheet 21 of 22, Fig. 29, the titles of the two block diagrams reading "CHROM/NANCE ENCODER" should read --CHROMINANCE ENCODER--.

In the specification, in column 1 at line 42, "televsion" should read --television--. In column 2 at line 23, "normaly" should read --normally--; at lines 59 and 60, "sufferened" should read --suffered--. In column 4 at line 5, "tranform" should read --transform--; at line 18, "preseved" should read --preserved--. In column 5 at line 42, "decorder" should read --decoder--. In column 6 at line 26, "consine" should read --cosine--. In column 8 at line 6, "Viterbi decoder 20" should read --Viterbi decoder 30--; at line 14, "inputs" should read --puts--. In column 9 at line 40, "buffer change" should read --buffer status change--; in column 9 at line 46, "btween" should read --between--. In column 11 at line 35, "the" should read --then--; at line 54, "encoer" should read --encoder--. In column 12 at line 16, "sheet" should read --sheer--; at line 17, "requiring" should read --required--; at line 30, "Tranform" should read --Transform--; at line 46, "shffled" should read --shuffled--. In column 13 at line 7, "12" should read --112--; at line 30, "contro" should read --control--; at line 44, "the shuffle multiply" should read --The shuffle multiply--. In column 14 at line 2, "storedin" should read --stored in--; at line 7, "shuffe" should read --shuffle--; at line 23, "tranformer" should read --transformer--; at line 30, "fur" should read --four--; at line 33, "pair 44, 146" should read --pair 144, 146--; at line 56, "Acces" should read --Access--;

KODAK_000078

UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO. : 4,394,774

DATED : July 19, 1983

INVENTOR(S) : Widergren, et al.

It is certified that error appears in the above-identified patent and that said Letters Patent are hereby corrected as shown below:

at line 59, "transfrmer" should read --transformer--. In column 15 at line 17, "PROM" should read --PROM 170--; at line 38, "Encloder" should read --Encoder--; at line 42, "frm" should read --from--; at line 47, "truncted" should read --truncated--. In column 16 at line 11, "18" should read --188--; at line 13, "FIDO" should read --FIFO--; at line 24, "$F_B$and" should read --F_B, and--. In column 17 at line 64, "$a_B$ls" should read --also--. In column 18 at line 5, "FIFI" should read --FIFO--. In column 19 at line 29, "eight of sixteen" should read --eight to sixteen--; at line 49, "70" should read --72--.

In the claims, and specifically in claim 1 at line 28, "coder" should read --coded--. In claim 3 at line 16, "substantially" should read --statistically--; at line 28, "capcity" should read --capacity--; at line 32, "cooled" should read --coded--. In claim 4 at line 14, "theoref" should read --thereof--.

UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO. : 4,394,774

DATED : July 19, 1983

INVENTOR(S) : Widergren, et al.

It is certified that error appears in the above-identified patent and that said Letters Patent are hereby corrected as shown below:

In claim 6 at line 10, "capaicty" should read --capacity--. In claim 8 at line 2, "dat" should read --data--; at line 22, "meand" should read --means--. In claim 10 at line 20, "said buffer" should read --said first buffer--; at line 26, "descrete" should read --discrete--; at line 38, "ecoder" should read --encoder--. In claim 11 at line 14, "rate to" should read --rate adapted to--; at line 48, "tranformed" should read --transformed--.

Signed and Sealed this

Twenty-ninth Day of May 1984

[SEAL]

Attest:

GERALD J. MOSSINGHOFF

Attesting Officer

Commissioner of Patents and Trademarks

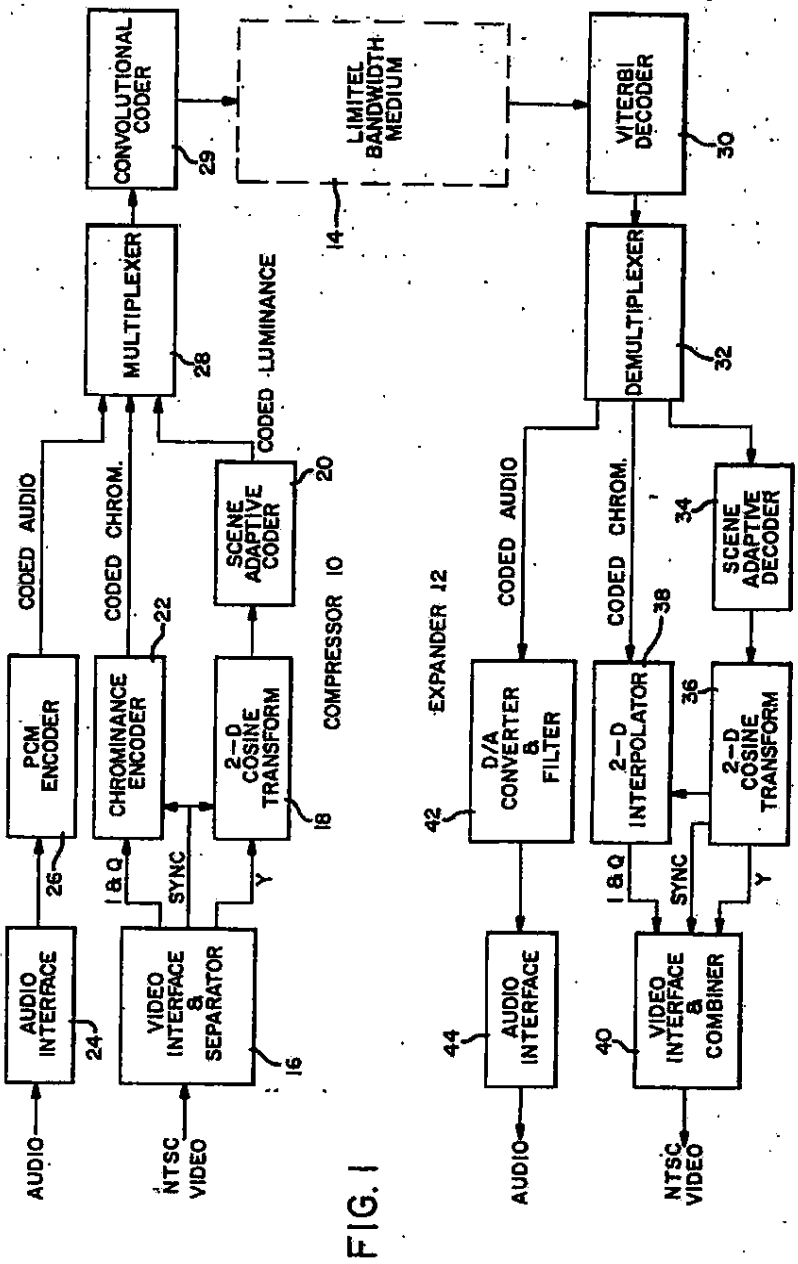

CONVOLUTIONAL CODER
29
LIMITED BANDWIDTH MEDIUM
14
VITERBI DECODER
30
MULTIPLEXER
28
DEMULTIPLEXER
32
CODED LUMINANCE
CODED AUDIO
CODED CHROM.
SCENE ADAPTIVE CODER
20
SCENE ADAPTIVE DECODER
34
COMPRESSOR 10
EXPANDER 12
PCM ENCODER
26
CHROMINANCE ENCODER
22
2-D COSINE TRANSFORM
18
D/A CONVERTER & FILTER
42
2-D INTERPOLATOR
38
2-D COSINE TRANSFORM
36
I & Q
SYNC
Y
AUDIO INTERFACE
24
VIDEO INTERFACE & SEPARATOR
16
AUDIO INTERFACE
44
VIDEO INTERFACE & COMBINER
40
AUDIO
NTSC VIDEO
AUDIO
NTSC VIDEO

FIG. 1

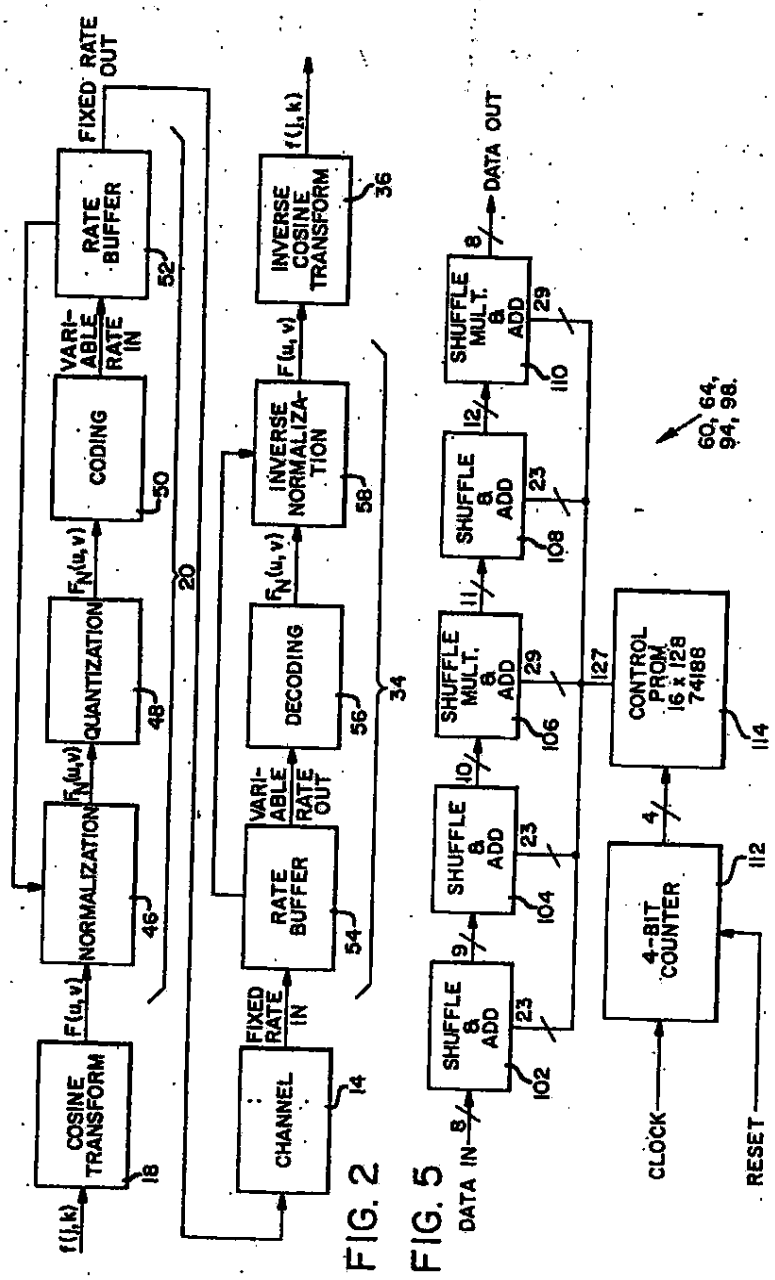

f(j,k)
COSINE TRANSFORM
18
F(u,v)
NORMALIZATION
46
F_N(u,v)
QUANTIZATION
48
F_N(u,v)
CODING
50
VARIABLE RATE IN
RATE BUFFER
52
FIXED RATE OUT
20
FIXED RATE IN
CHANNEL
14
VARIABLE RATE OUT
RATE BUFFER
54
F_N(u,v)
DECODING
56
F(u,v)
INVERSE NORMALIZATION
58
f(j,k)
INVERSE COSINE TRANSFORM
36
34

FIG. 2

DATA IN
8
SHUFFLE & ADD
102
23
9
SHUFFLE & ADD
104
23
10
SHUFFLE MULT. & ADD
106
29
11
SHUFFLE & ADD
108
23
12
SHUFFLE MULT. & ADD
110
29
8
DATA OUT
60, 64, 94, 98.
CONTROL PROM 16 x 128 74188
114
127
4
4-BIT COUNTER
112
CLOCK
RESET

FIG. 5

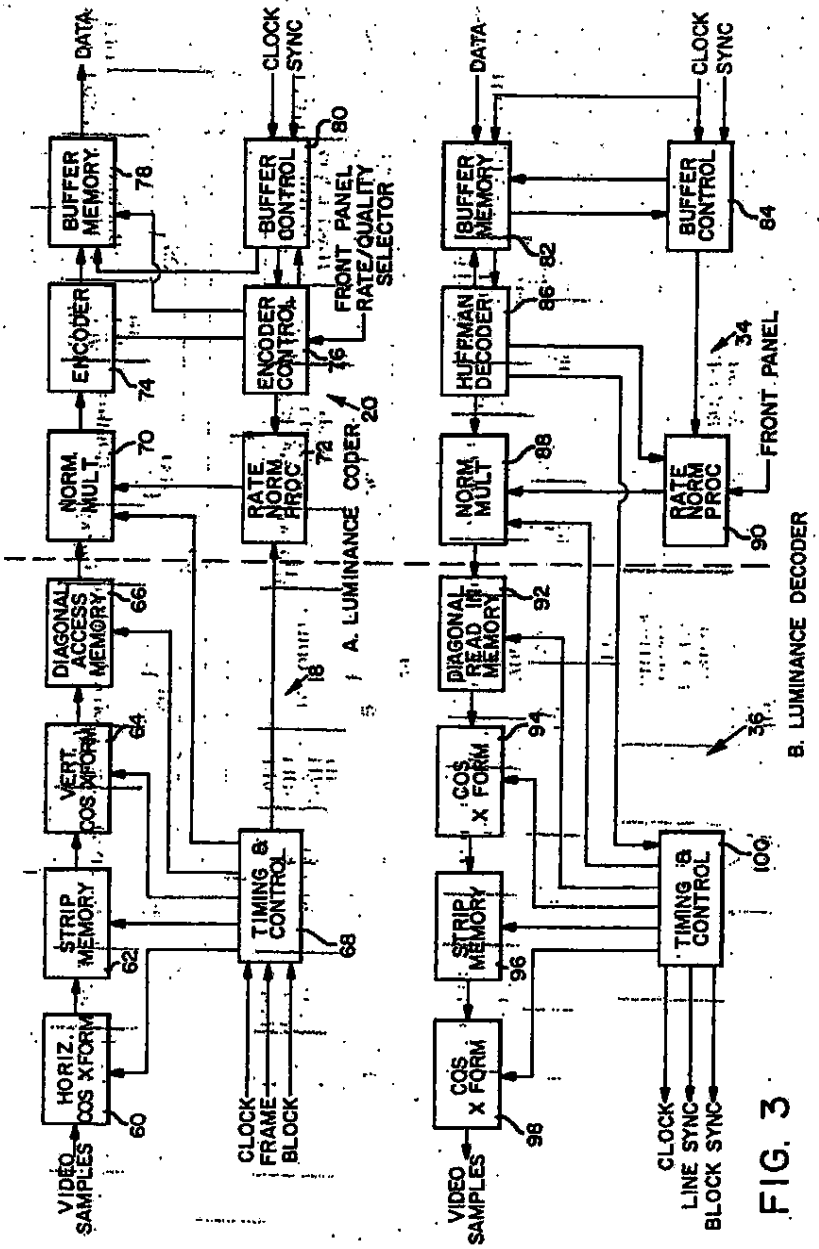

DATA
CLOCK
SYNC
BUFFER MEMORY
78
BUFFER CONTROL
80
ENCODER
74
ENCODER CONTROL
76
FRONT PANEL RATE/QUALITY SELECTOR
NORM. MULT.
70
RATE NORM PROC
72
CODER
20
A. LUMINANCE
DIAGONAL ACCESS MEMORY
66
18
VERT. COS XFORM
64
STRIP MEMORY
62
TIMING & CONTROL
68
HORIZ. COS XFORM
60
VIDEO SAMPLES
CLOCK
FRAME
BLOCK
DATA
CLOCK
SYNC
BUFFER MEMORY
82
BUFFER CONTROL
84
HUFFMAN DECODER
86
34
FRONT PANEL
NORM. MULT.
88
RATE NORM PROC
90
FRONT PANEL
B. LUMINANCE DECODER
DIAGONAL READ IN MEMORY
92
36
COS X FORM
94
STRIP MEMORY
96
TIMING & CONTROL
100
COS X FORM
98
VIDEO SAMPLES
CLOCK
LINE SYNC
BLOCK SYNC

FIG. 3

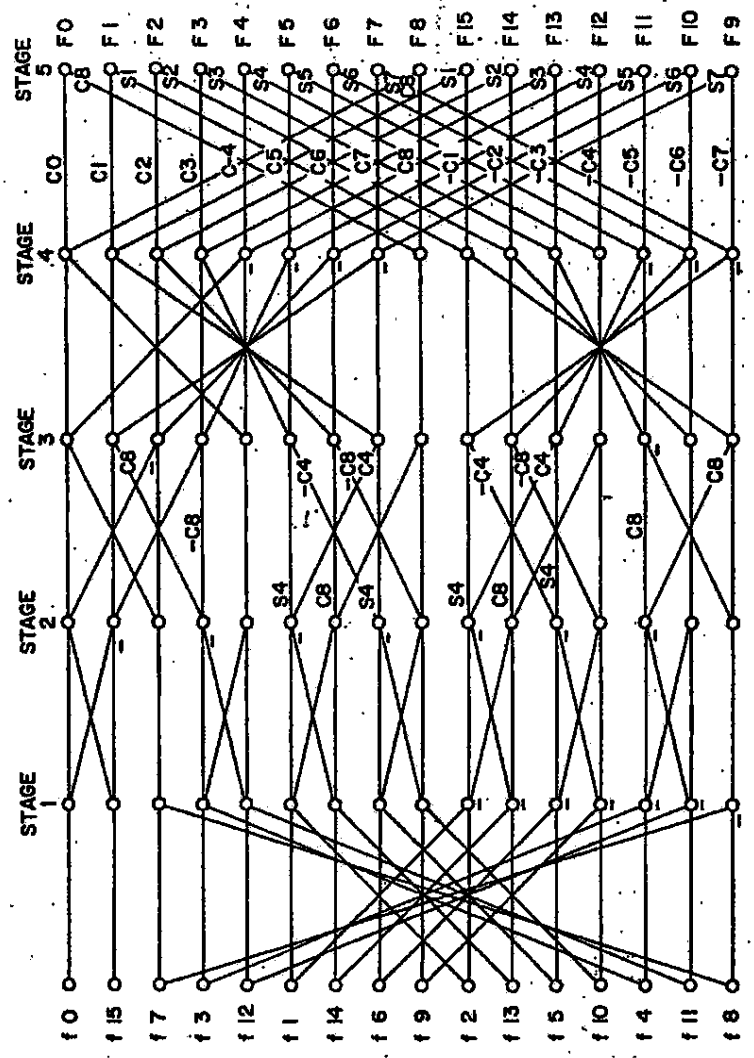

STAGE 5
STAGE 4
STAGE 3
STAGE 2
STAGE 1
F0 F1 F2 F3 F4 F5 F6 F7 F8 F15 F14 F13 F12 F11 F10 F9
C0 C1 C2 C3 C4 C5 C6 C7 C8
S1 S2 S3 S4 S5 S6 S7
f0 f15 f7 f3 f12 f1 f14 f6 f9 f2 f13 f5 f10 f4 f11 f8

FIG. 4

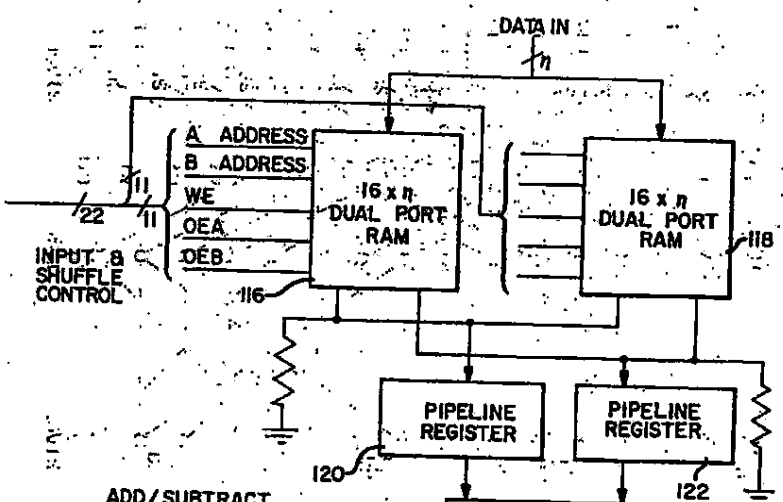

DATA IN
n
A ADDRESS
B ADDRESS
WE
OEA
OEB
11
11
22
INPUT & SHUFFLE CONTROL
116
16 x n DUAL PORT RAM
16 x n DUAL PORT RAM
118
PIPELINE REGISTER
PIPELINE REGISTER
120
122
ADD/SUBTRACT
ALU (n-BIT)
124
n+1
DATA OUT
102, 104, 108.

FIG. 6

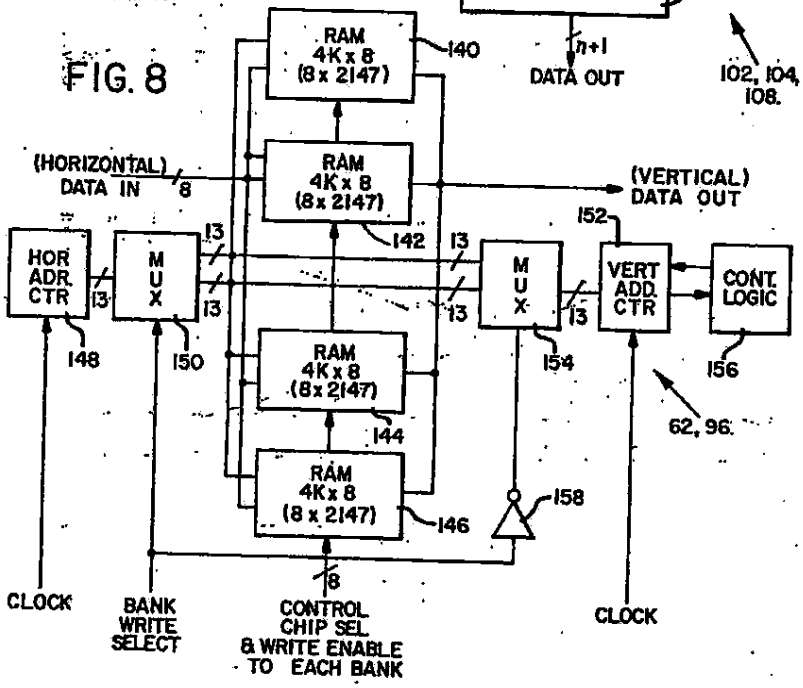

RAM 4K x 8 (8 x 2147)
140
(HORIZONTAL) DATA IN
8
RAM 4K x 8 (8 x 2147)
142
(VERTICAL) DATA OUT
152
HOR ADR CTR
13
MUX
13
13
13
MUX
13
VERT ADD CTR
CONT. LOGIC
148
150
154
156
RAM 4K x 8 (8 x 2147)
144
62, 96.
RAM 4K x 8 (8 x 2147)
146
158
8
CLOCK
BANK WRITE SELECT
CONTROL CHIP SEL & WRITE ENABLE TO EACH BANK
CLOCK

FIG. 8

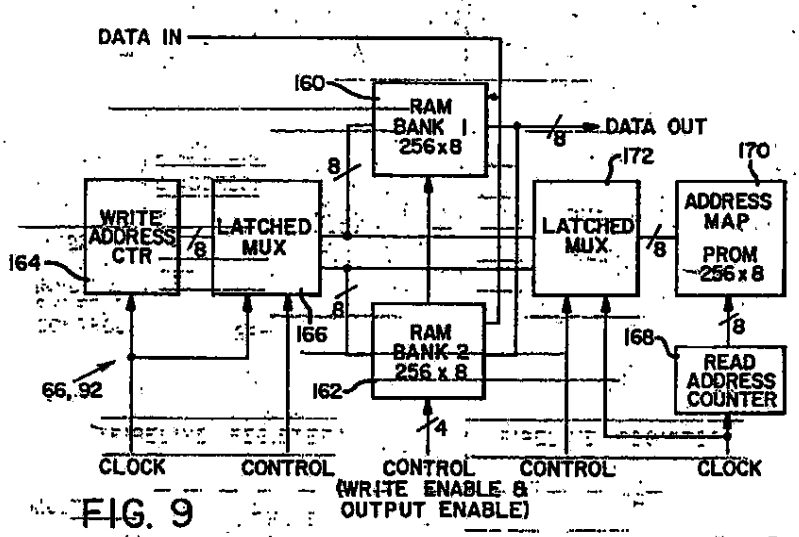
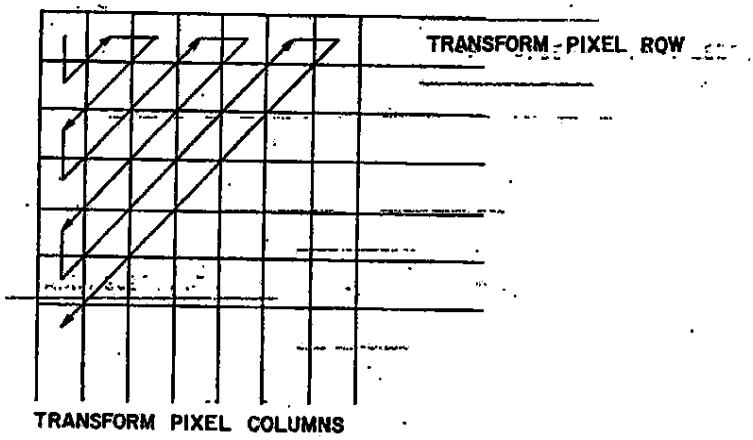

DATA IN
160
RAM BANK 1 256x8
DATA OUT
8
172
170
WRITE ADDRESS CTR
LATCHED MUX
LATCHED MUX
ADDRESS MAP PROM 256x8
164
166
RAM BANK 2 256 x 8
168
READ ADDRESS COUNTER
66, 92
162
4
CLOCK
CONTROL
CONTROL (WRITE ENABLE & OUTPUT ENABLE)
CONTROL
CLOCK

FIG. 9

FIG. 10


TRANSFORM PIXEL ROW
TRANSFORM PIXEL COLUMNS

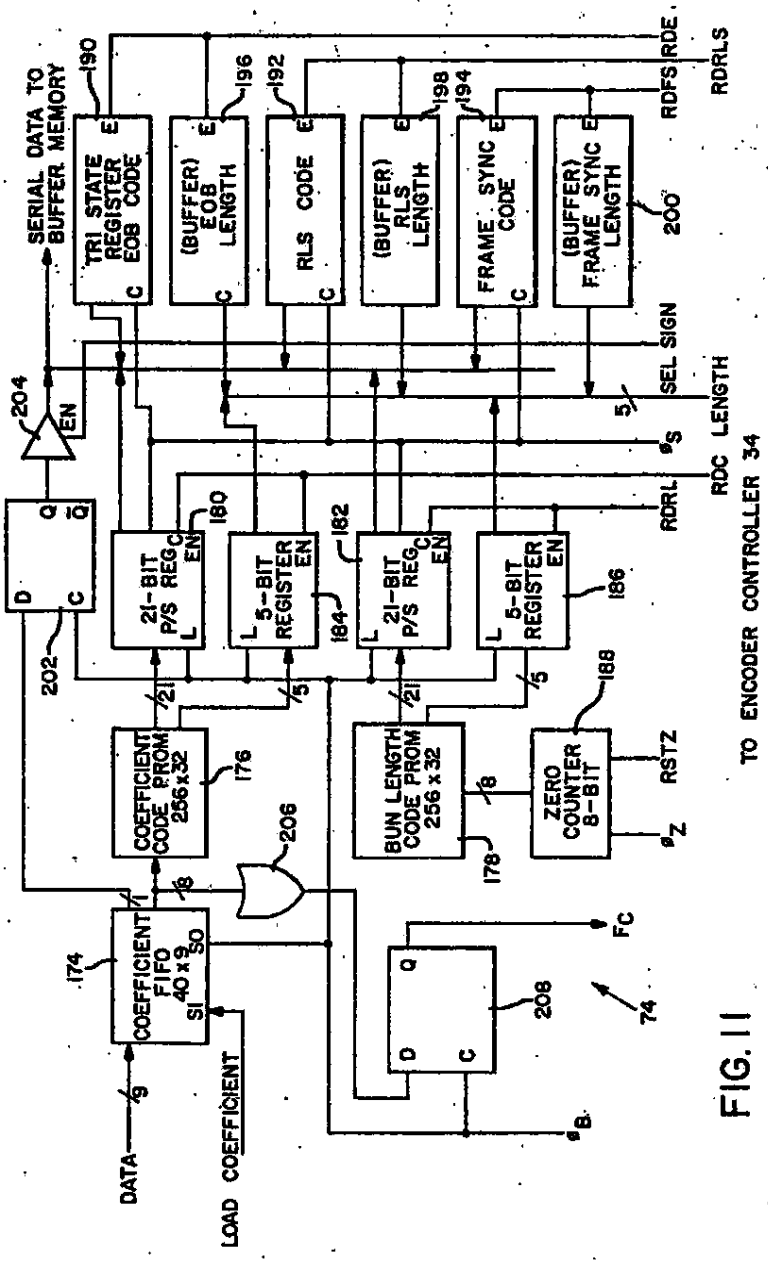

SERIAL DATA TO BUFFER MEMORY
TRI STATE REGISTER EOB CODE
(BUFFER) EOB LENGTH
RLS CODE
(BUFFER) RLS LENGTH
FRAME SYNC CODE
(BUFFER) FRAME SYNC LENGTH
RDE
RDFS
RDRLS
SEL SIGN
RDC LENGTH
RDRL
TO ENCODER CONTROLLER 34
21-BIT P/S REG
5-BIT REGISTER
COEFFICIENT CODE PROM 256x32
BUN LENGTH CODE PROM 256 x 32
ZERO COUNTER 8-BIT
RSTZ
COEFFICIENT FIFO 40 x 9
DATA
LOAD COEFFICIENT
Fc
EN
190
196
192
198
194
200
204
180
182
184
186
188
202
176
206
174
208
178
74

FIG. 11

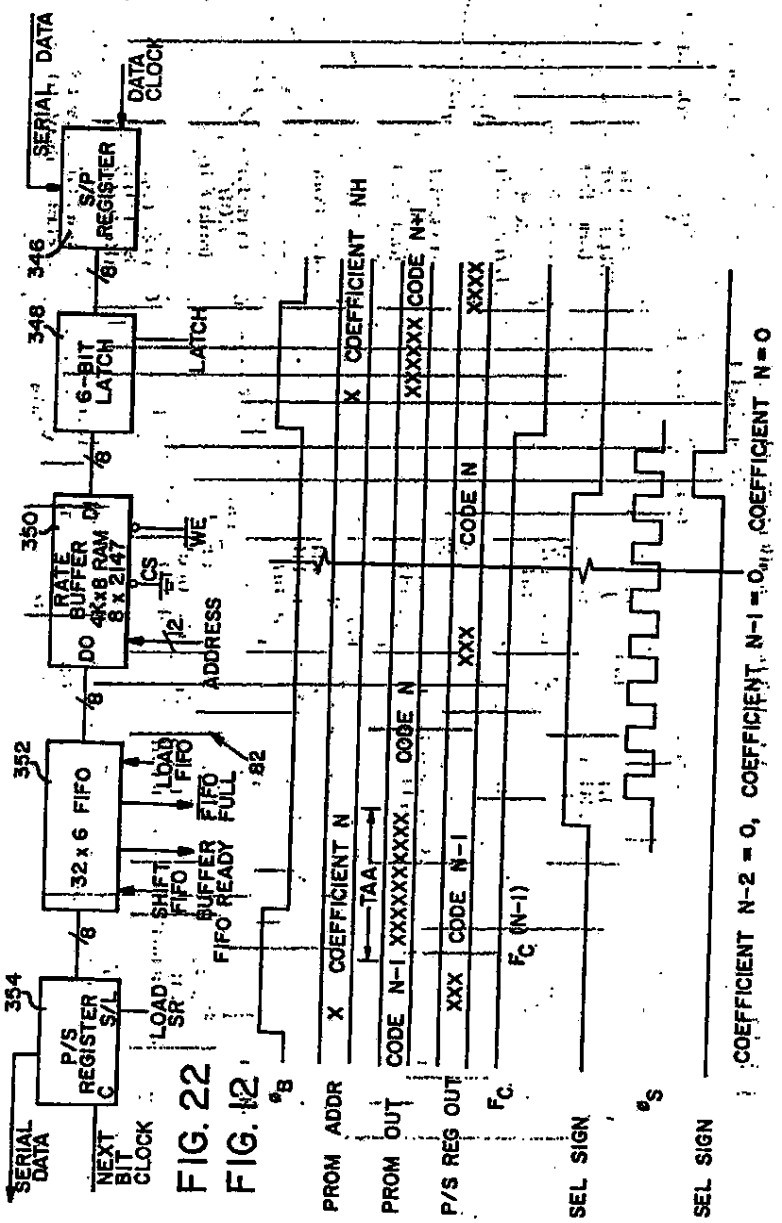

SERIAL DATA
DATA CLOCK
S/P REGISTER
346
348
6-BIT LATCH
LATCH
350
RATE BUFFER 4K x 8 RAM 8 x 2147
DO
CS
WE
ADDRESS
352
32 x 6 FIFO
LOAD FIFO
FIFO FULL
82
SHIFT FIFO
BUFFER READY
FIFO
354
P/S REGISTER S/L
LOAD SR
SERIAL DATA
NEXT BIT CLOCK
X COEFFICIENT NH
XXXXXX CODE N+1
XXXX
X COEFFICIENT N
CODE N
XXX
CODE N-1 XXXXXXXXXXXX CODE N
TAA
XXX CODE N-1
F_C (N-1)
F_C
PROM ADDR
PROM OUT
P/S REG OUT
SEL SIGN
SEL SIGN
COEFFICIENT N-2 = 0, COEFFICIENT N-1 = O_{off}, COEFFICIENT N = 0

FIG. 22

FIG. 12

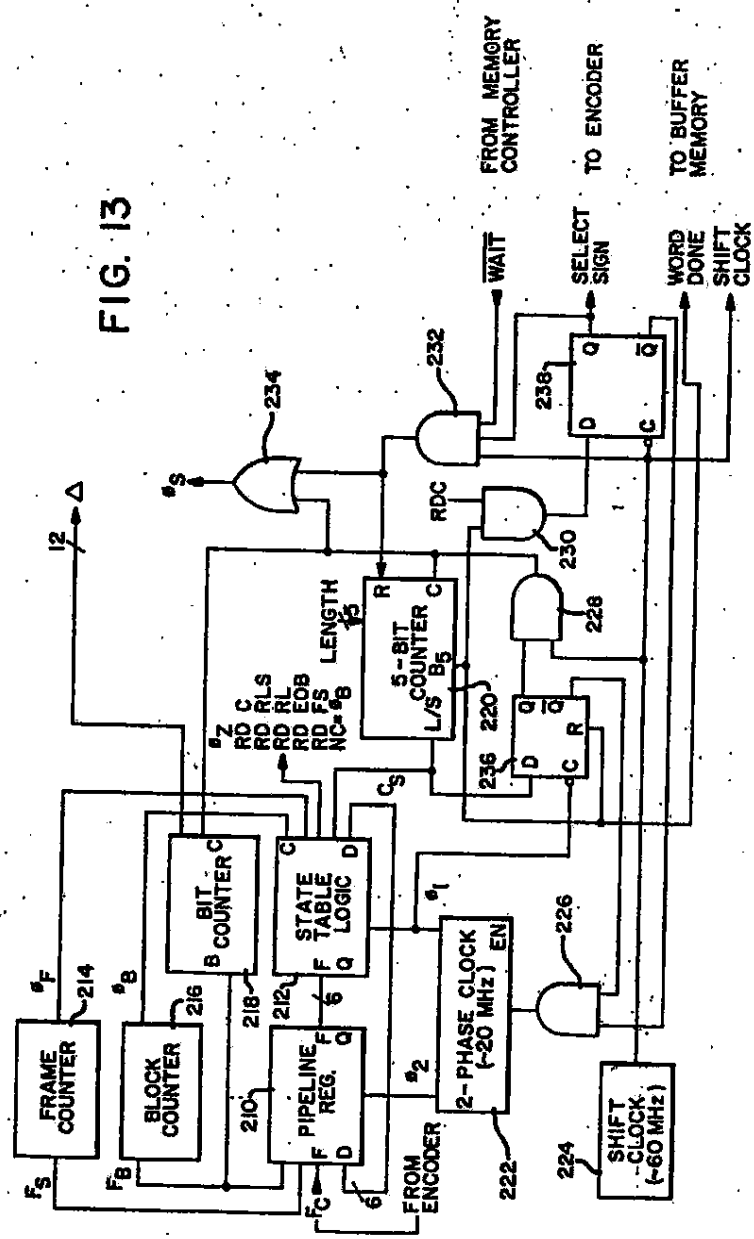

FROM MEMORY CONTROLLER
TO ENCODER
TO BUFFER MEMORY
WAIT
SELECT SIGN
WORD DONE
SHIFT CLOCK
FRAME COUNTER
BLOCK COUNTER
BIT COUNTER
STATE TABLE LOGIC
PIPELINE REG.
2-PHASE CLOCK (~20 MHz)
SHIFT CLOCK (~60 MHz)
5-BIT COUNTER
LENGTH
RDC
FROM ENCODER
RD C
RD RLS
RD RL
RD EOB
RD FS
NC=ØB
12
214
216
218
210
212
220
222
224
226
228
230
232
234
236
238

FIG. 13

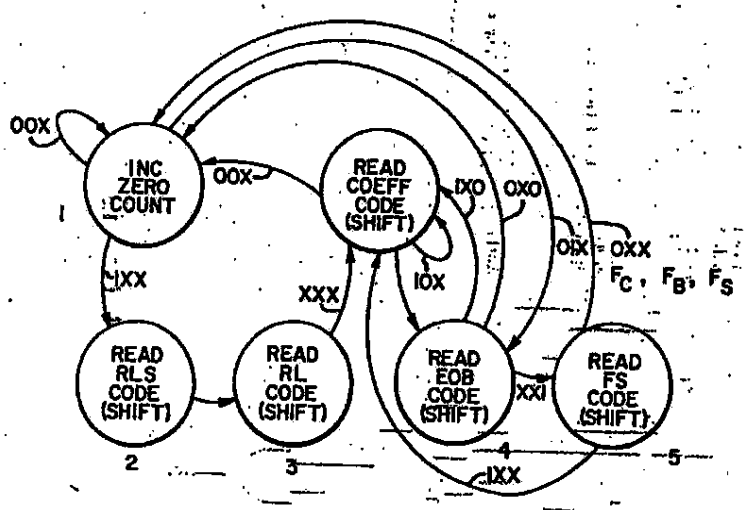
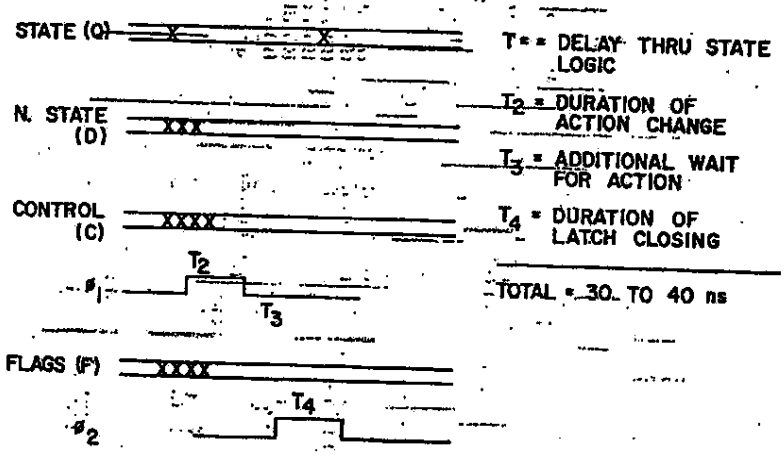

OOX
INC ZERO COUNT
1
OOX
READ COEFF CODE (SHIFT)
IXO
OXO
OIX
OXX
F_C, F_B, F_S
IXX
XXX
IOX
READ RLS CODE (SHIFT)
2
READ RL CODE (SHIFT)
3
READ EOB CODE (SHIFT)
XXI
4
READ FS CODE (SHIFT)
5
IXX

FIG. 14

FIG. 15


STATE (Q)
N. STATE (D)
XXX
CONTROL (C)
XXXX
T_2
ϕ_1
T_3
FLAGS (F)
XXXX
T_4
ϕ_2
T = DELAY THRU STATE LOGIC
T_2 = DURATION OF ACTION CHANGE
T_3 = ADDITIONAL WAIT FOR ACTION
T_4 = DURATION OF LATCH CLOSING
TOTAL = 30 TO 40 ns

STATE			FLAG			NEXT STATE			CONTROL					
Q_1	Q_2	Q_3	F_C	F_B	F_S	D_1	D_2	D_3	ϕ_F	ϕ_B	ϕ_Z	C_S	R_D	N_C
0	0	0	0	0	X	0	0	1	0	1	1	1	R_C	1
0	0	0	1	0	X	0	0	0	0	1	RST	1	R_C	1
0	0	0	X	1	X	1	0	0	0	0	0	1	R_C	0
0	0	1	0	0	X	0	0	1	0	1	1	0	0	1
0	0	1	0	1	X	1	0	0	0	0	RST	0	0	0
0	0	1	1	X	X	0	1	0	0	0	0	0	0	0
0	1	0	X	X	X	0	1	1	0	0	0	1	RLS	0
0	1	1	X	X	X	0	0	0	0	0	0	1	RL	0
1	0	0	1	X	0	0	0	0	1	RST	RST	1	R_E	1
1	0	0	0	X	0	0	0	1	0	1	1	1	R_E	1
1	0	0	X	X	1	1	0	1	0	0	0	1	R_E	0
1	0	1	1	X	X	0	0	0	RST	1	0	1	R_F	1
1	0	1	0	X	X	0	0	1	RST	1	1	1	R_F	1

FIG. 16

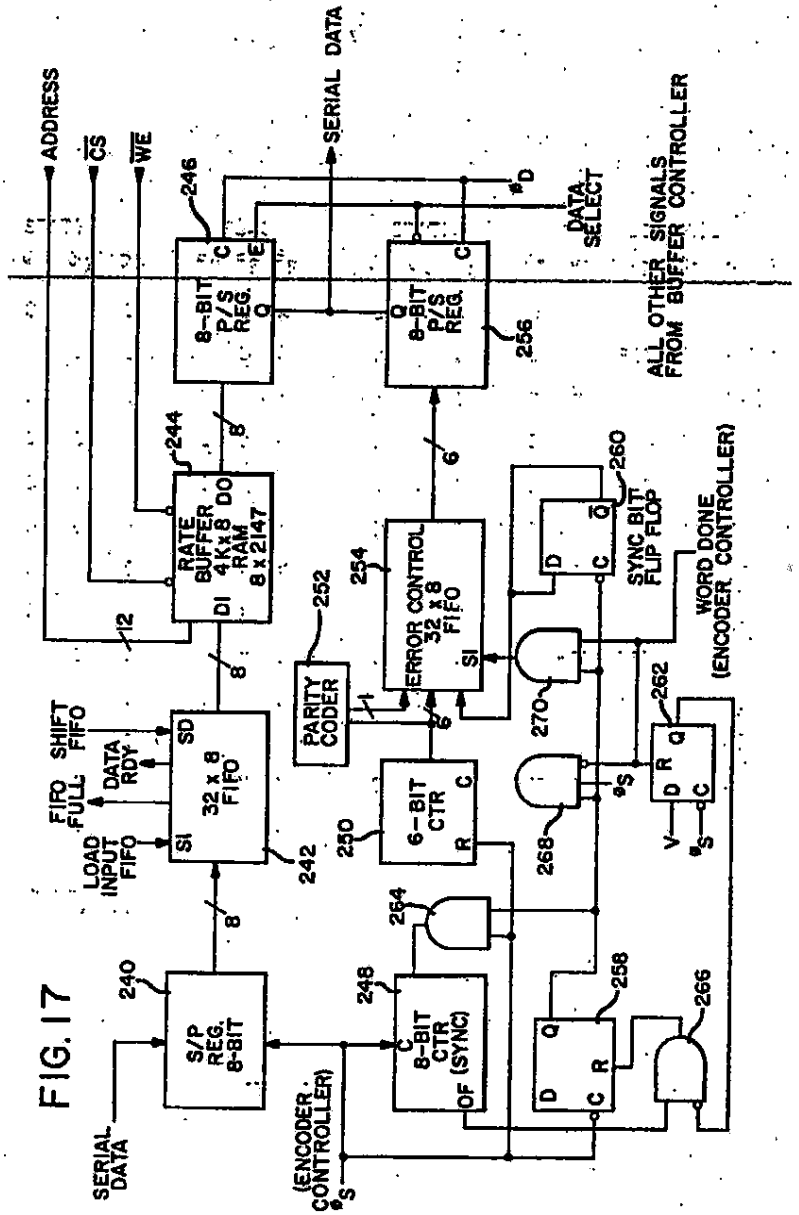

ADDRESS
CS
WE
SERIAL DATA
246
8-BIT P/S REG.
8-BIT P/S REG.
256
DATA SELECT
ALL OTHER SIGNALS FROM BUFFER CONTROLLER
244
RATE BUFFER 4K x 8 RAM 8 x 2147
DO
DI
12
8
6
260
SYNC BIT FLIP FLOP
WORD DONE (ENCODER CONTROLLER)
254
ERROR CONTROL 32 x 8 FIFO
SI
252
PARITY CODER
270
262
SHIFT FIFO
FIFO FULL
DATA RDY
LOAD INPUT FIFO
SD
32 x 8 FIFO
SI
242
6-BIT CTR
250
268
264
240
S/P REG. 8-BIT
248
8-BIT CTR (SYNC)
OF
258
266
SERIAL DATA
(ENCODER CONTROLLER)

FIG. 17

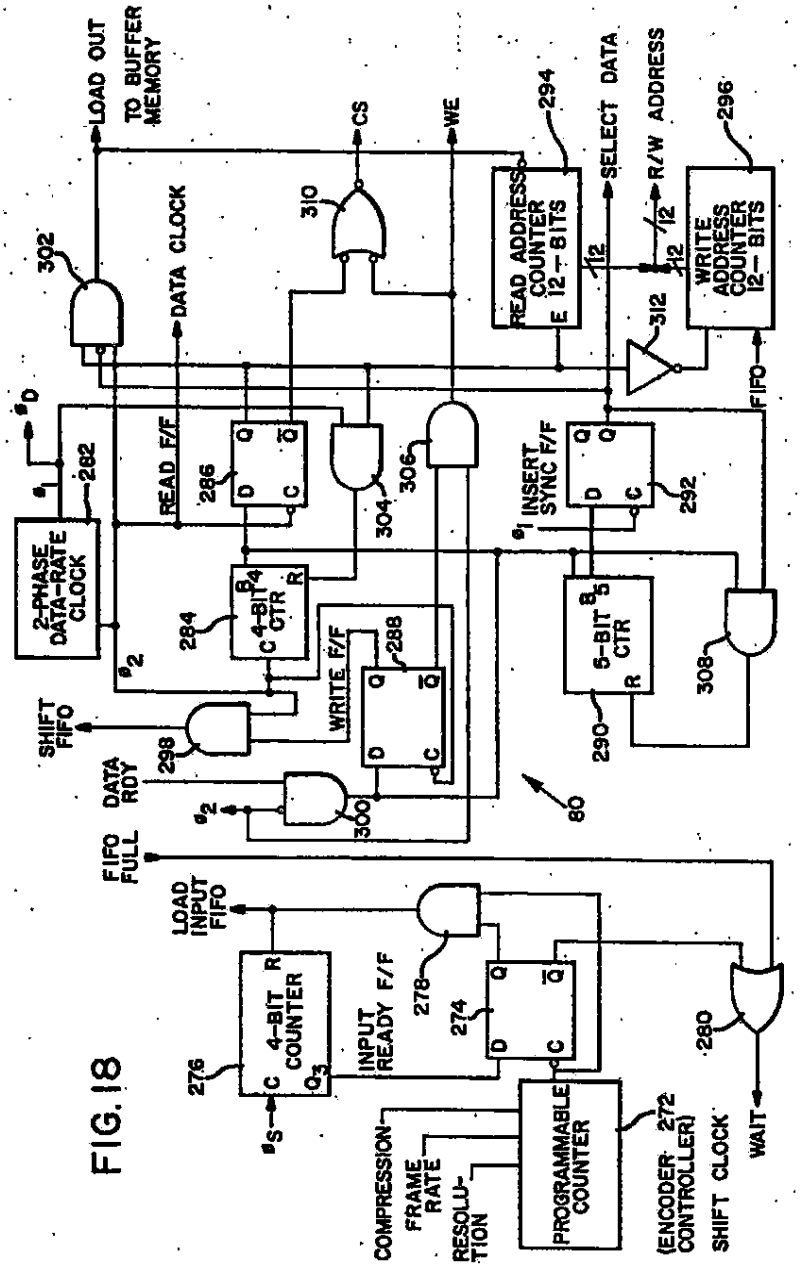
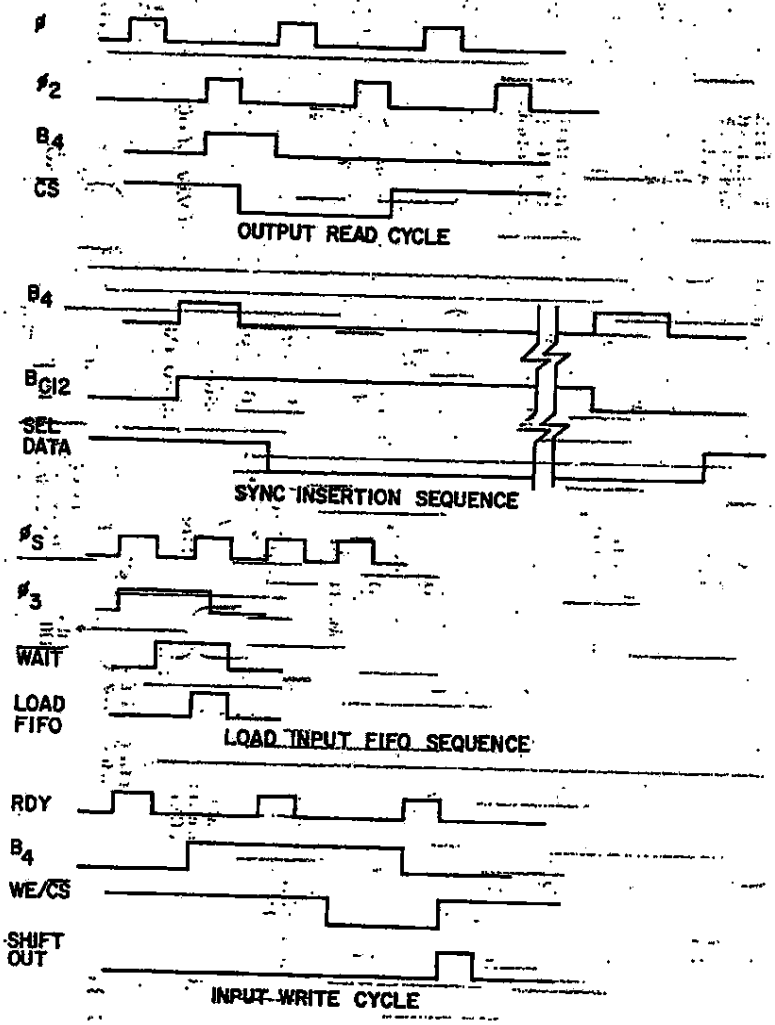

LOAD OUT TO BUFFER MEMORY
CS
WE
294
SELECT DATA
R/W ADDRESS
296
DATA CLOCK
310
302
READ ADDRESS COUNTER 12-BITS
WRITE ADDRESS COUNTER 12-BITS
312
FIFO
ϕ_0
ϕ_1
282
READ F/F
286
304
306
INSERT SYNC F/F
292
2-PHASE DATA-RATE CLOCK
284
4-BIT CTR
ϕ_2
WRITE F/F
288
5-BIT CTR
308
290
SHIFT FIFO
298
DATA RDY
300
80
FIFO FULL
LOAD INPUT FIFO
4-BIT COUNTER
276
INPUT READY F/F
278
274
280
WAIT
COMPRESSION
FRAME RATE
RESOLU-TION
PROGRAMMABLE COUNTER
272
(ENCODER CONTROLLER)
SHIFT CLOCK

FIG. 18

FIG. 19


ϕ
ϕ_2
B_4
$\overline{CS}$
OUTPUT READ CYCLE
B_4
B_{CI2}
SEL
DATA
SYNC INSERTION SEQUENCE
ϕ_S
ϕ_3
$\overline{WAIT}$
LOAD
FIFO
LOAD INPUT FIFO SEQUENCE
RDY
B_4
WE/CS
SHIFT
OUT
INPUT WRITE CYCLE