EXHIBIT C

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UNITED STATES DISTRICT COURT

NORTHERN DISTRICT OF CALIFORNIA

SAN JOSE DIVISION

APPLE INC.,

Plaintiff,

vs.

CHANG LIU, TANG YEW TAN, OPENAI FOUNDATION f/k/a OPENAI, INC., OPENAI GROUP PBC, and IO PRODUCTS, LLC F/K/A IO PRODUCTS, INC.,

Defendants.

Case No. 5:26-cv-07078-EJD

DECLARATION OF DR. AYMAN FAYED IN SUPPORT OF APPLE INC.'S SUPPLEMENTAL BRIEF IN SUPPORT OF ITS MOTION FOR EXPEDITED DISCOVERY

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I. INTRODUCTION

1. As explained in my August 3, 2026 declaration, I, Ayman Fayed, have been retained by Apple as an expert in this case.

2. I incorporate by reference into this declaration the Introduction, Technical Background, Apple's Trade Secrets, including the Additional Documents Reviewed subsection, Apple's Trade Secrets Are Valuable Due to Their Secrecy, and the Information in the Materials at Issue is not Generally Known and is not Readily Ascertainable sections of my August 3, 2026 declaration in support of Apple's Motion for a Preliminary Injunction ("PI Declaration").

3. Since I submitted my declaration on August 3, 2026, I understand that new forensic evidence has been uncovered indicating that Patel Ex. 24, the [redacted] file, was opened and used with a circuit simulation program called LTspice, after Mr. Chang Liu departed Apple, and that the file may also have been uploaded to or otherwise made available to an AI agent. (Roffman Decl. ¶¶ 15-22.)

4. I was asked to explain the LTspice software; how engineers use LTspice in hardware development; to further describe Patel Ex. 24, one of the Apple documents I previously discussed in my PI Declaration; explain the use and value of that file to a competitor in view of use of this file after Mr. Liu departed Apple; and explain why evidence of use of that file is at risk of loss and why prompt recovery of information is therefore necessary. If called on to testify, I would do so competently and truthfully regarding this matter, consistent with the opinions and conclusions I provide below.

5. In forming the opinions in this declaration, I have relied on my education, the areas of my research, my professional experience, the materials cited herein, and the materials I reviewed in connection with the PI Declaration. I reserve the right to supplement the opinions in this declaration should additional information be provided to me for consideration.

II. TECHNICAL BACKGROUND

A. Circuit Simulation in Hardware Development

6. SPICE (Simulation Program with Integrated Circuit Emphasis) is a standard class of circuit simulation tools that allows a user to design, test, and analyze an electronic circuit in software

without the need for physical hardware. More specifically, SPICE provides a user with the digital equivalent of building the circuit on a bench and probing it with laboratory instruments. They can use it to digitally assemble a circuit from various components, run it under any operating conditions of interest, and measure the behavior of any point within the circuit. They can then iterate freely by adjusting components and parameters, testing edge cases and failure conditions, and refining the design without the time and expense of fabricating a physical prototype for each iteration.

7. Circuit simulation is a critical component of hardware development. Physical prototyping takes time, incurs costs, and carries inherent structural risk—a prototype embodies one specific set of design choices, and discovering a flaw in it means waiting for, and paying for, another build. Simulation, by contrast, lets an engineer test many variations of a circuit design, see how it behaves, and diagnose and correct potential issues before investing in physical prototypes. (*See also* PI Decl. ¶¶ 24, 31, 44.)

8. For consumer electronics specifically, simulation is crucial. Consumer products are cost- and time-sensitive and are often built in large volumes once they reach mass production, so design errors that persist into fabrication or manufacturing are multiplied across every unit and can cause potential delays in shipping a finished product. (PI Decl. ¶¶ 31-32.) Circuit simulation is therefore an indispensable tool for validating circuit behavior, deciding on and further refining component values (the specific electrical sizes for each component in the design), and verifying tolerances and edge cases (confirming the design still works when real parts deviate slightly from their labeled values) before fabrication. That saves both time and money.

B. The LTspice Program

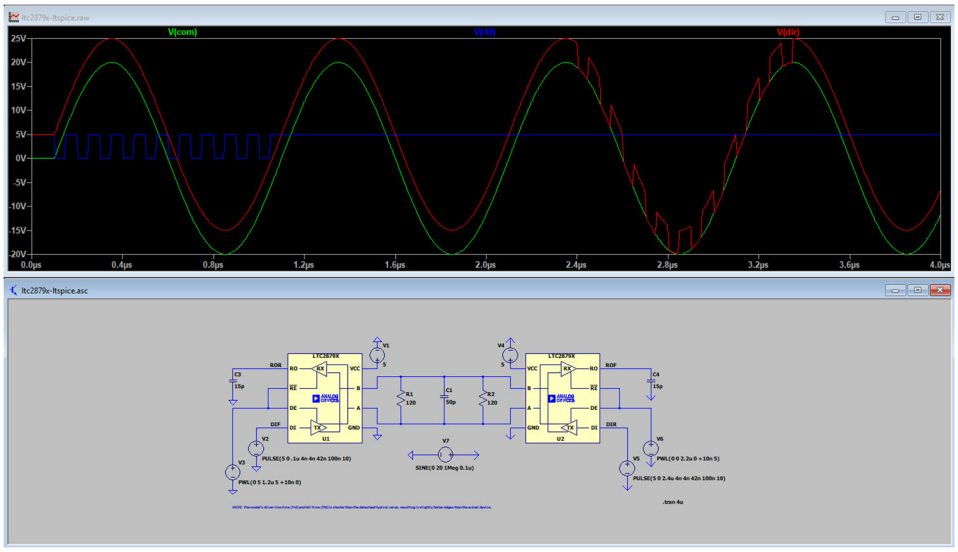
9. LTspice is a free, widely used SPICE-family circuit-simulation program distributed by Analog Devices, Inc. *See, e.g.*, LTspice, available at https://www.analog.com/en/resources/design-tools-and-calculators/ltspice-simulator.html (last visited Aug. 30, 2026). It allows an engineer to draw a circuit schematic on the screen, apply each component's operating parameters, define the operating conditions of interest (such as the battery voltage feeding the circuit), and then watch the circuit respond in real time as it operates. The results are shown as "waveforms," or plots showing

how each voltage and current within the circuit behaves over time, or versus frequency, or even versus other parameters in the circuit, thus allowing the circuit to be evaluated visually.

10. Although the program itself is free and commonly used in hardware development, the circuit designs and related information that engineers input into it, the simulations themselves and their setup, and the resulting outputs are often highly confidential and proprietary to the organizations who develop them. The value resides not in the tool but in the design, the data provided to and run through it, and the resulting outputs.

C. How the LTspice Program is Used

11. A LTspice simulation begins with a schematic file containing the components and parameters of the circuit. The circuit design itself is stored as an .asc file, which is a plain-text file listing every component in the circuit, its functional value (the resistance for a resistor, the inductance for an inductor, etc.), its placement, the wiring that connects the components, the simulation commands to be executed, and any annotations the designer has added for design or development context. Opening a compatible .asc file in LTspice displays the circuit schematic exactly as its author constructed it. When an engineer runs a simulation in LTspice, LTspice computes the circuit's behavior under the specified conditions and opens a waveform viewer displaying the results.



12. Within the waveform viewer and schematic window, the engineer can "probe" any node or component interactively by clicking or mousing over it. For example, when the cursor is placed over a wire or node, it becomes a voltage probe that plots the voltage at that point; when placed

over a component, it becomes a current clamp that plots the current flowing through that component. This interactivity is what makes the simulation a working design environment rather than a static calculation. The user can inspect any electrical quantity anywhere in the circuit while it is operating, change a component value, re-run the simulation, and immediately observe the effect.

13. LTspice generates specific companion file types alongside the .asc schematic once a simulation is run. These include:

i) ".raw" files: generated after a simulation runs and contain the actual numerical results of the simulation—the computed waveform data itself.

ii) ".net" files: text files defining the electrical connectivity of the schematic (the "netlist"), and which are small, temporary-type files that some users retain for further review.

iii) ".log" files: records of simulation statistics such as the elapsed time during the simulation, warning and error messages, and the step parameters used in stepped analyses.

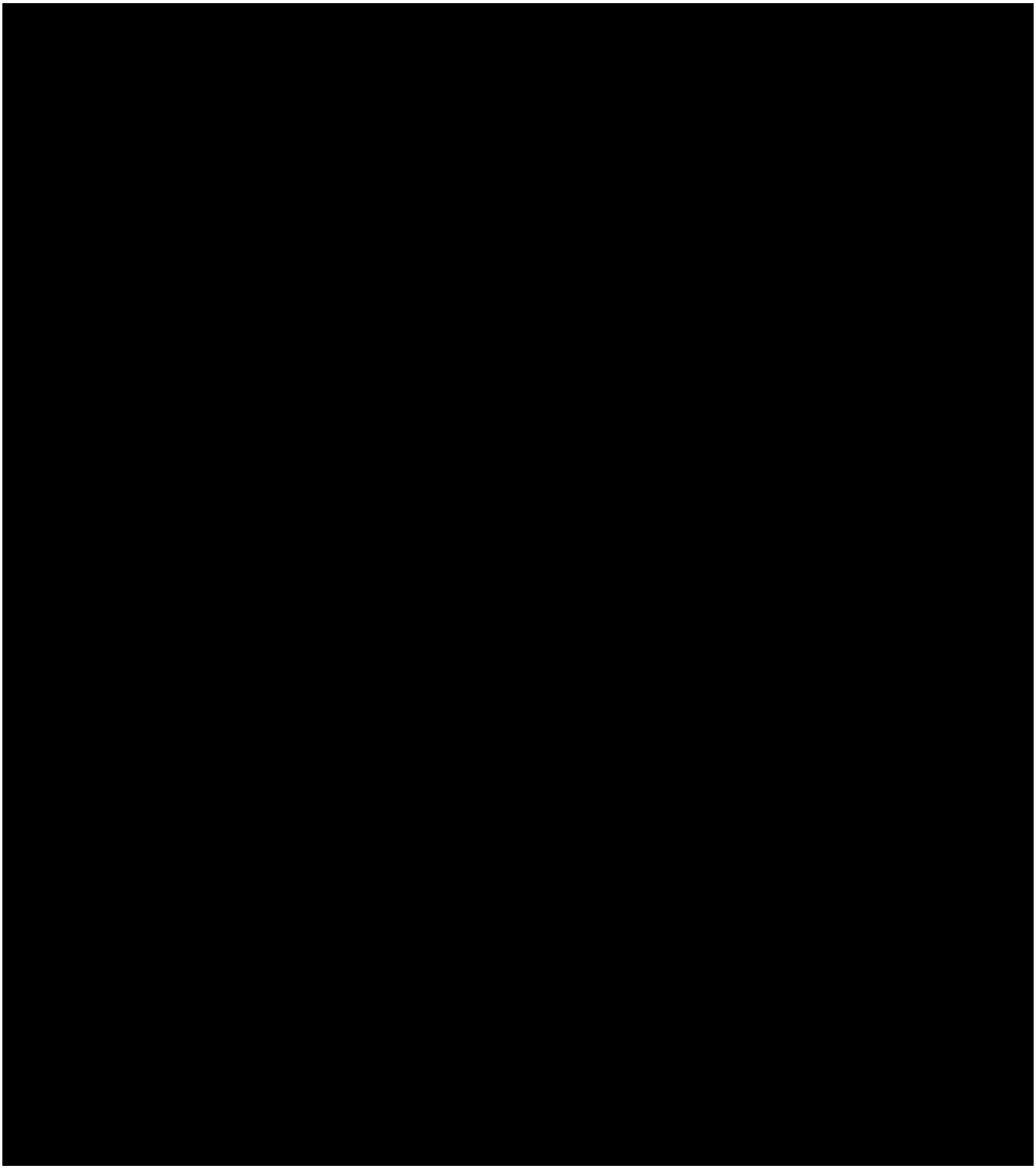
14. These are the .asc-related file types discussed in Mr. Roffman's declaration, which I have also reviewed. (*See, e.g.*, Roffman Decl. ¶ 15 [redacted].) The presence, contents, and timestamps of these companion files are the ordinary digital footprint of a specific .asc file having been used.

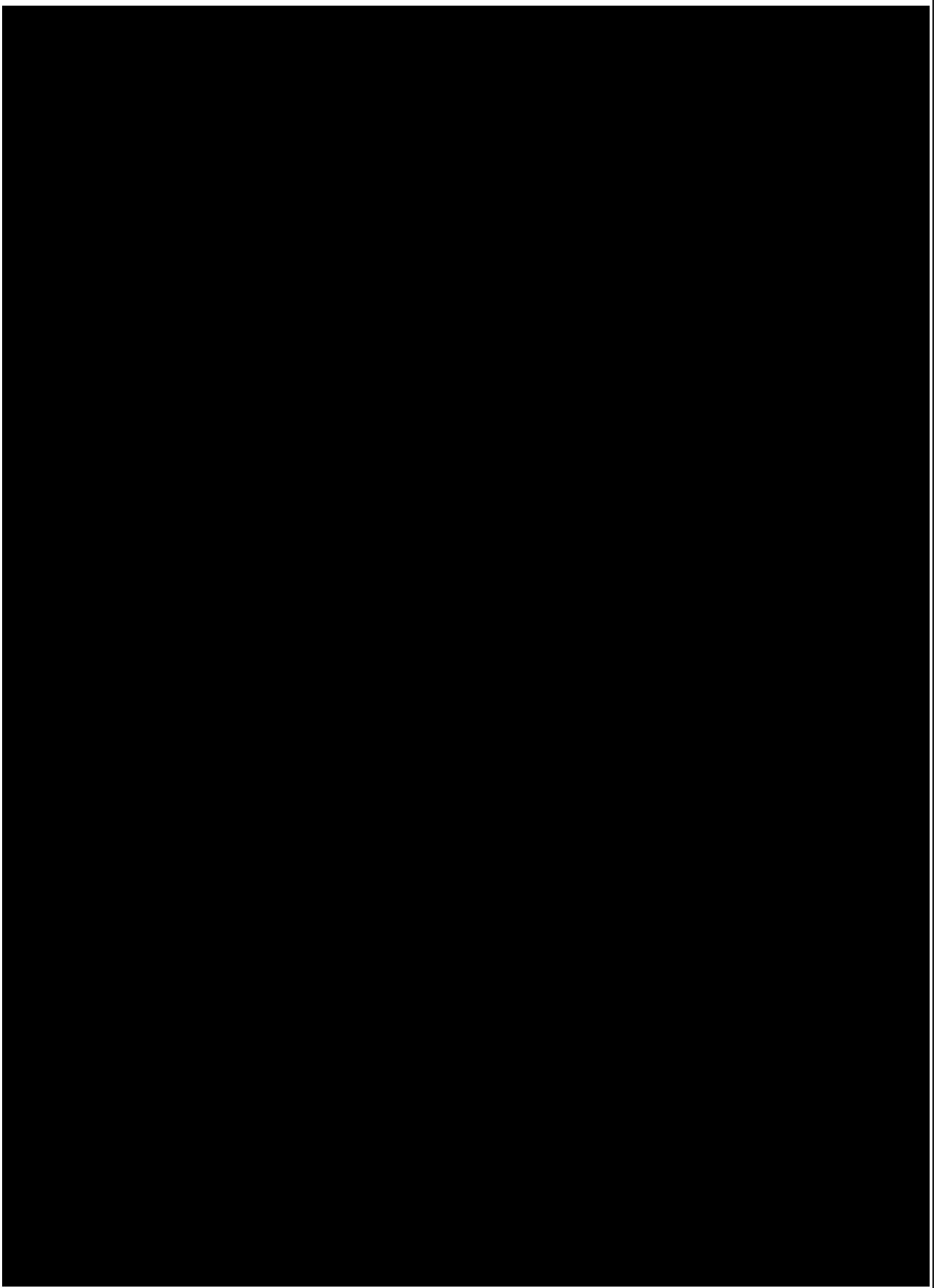
D. LTspice Simulation Analyses

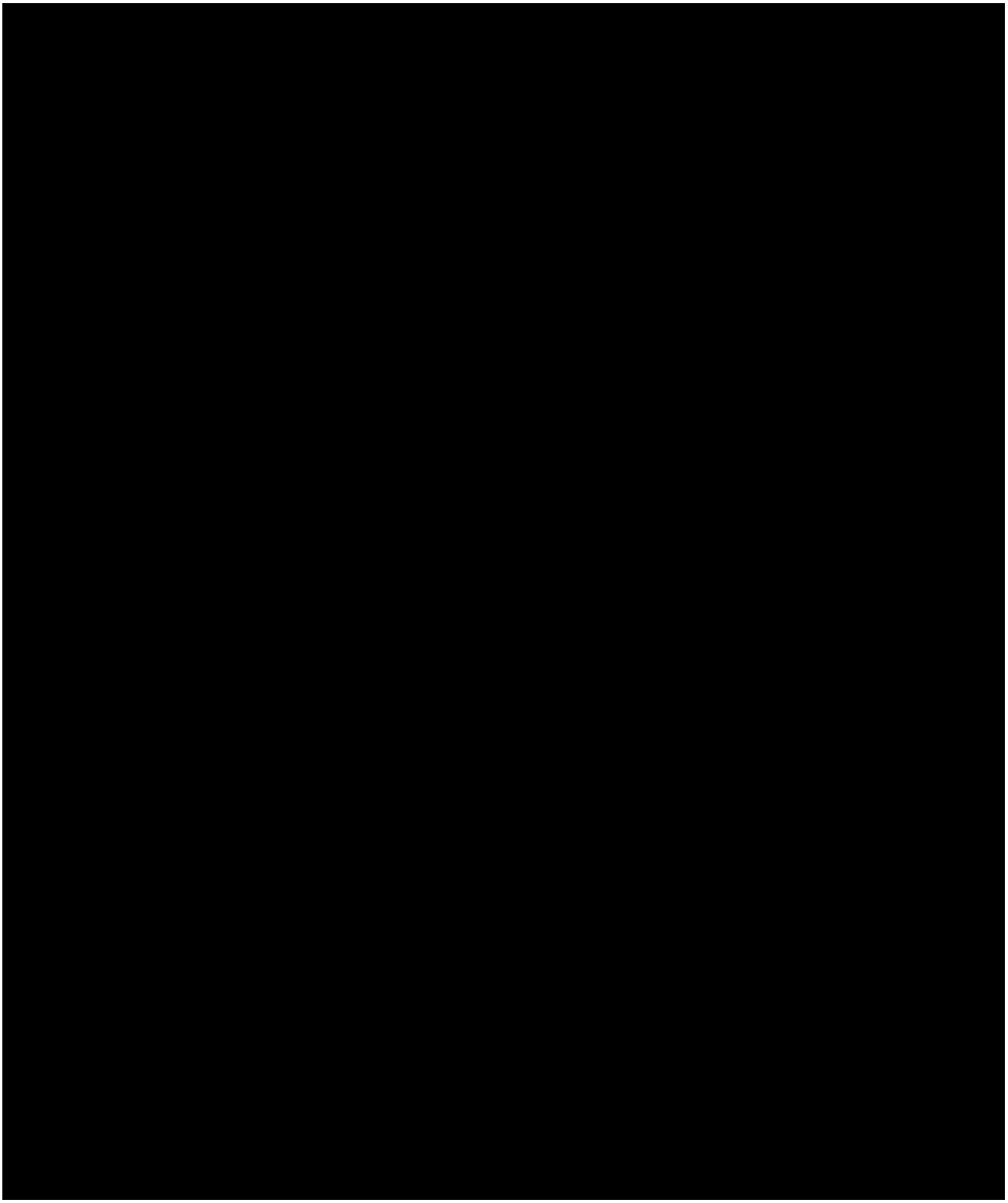
15. LTspice supports several types of simulation, each evaluating a different aspect of a circuit's behavior. For example, a transient analysis shows how voltages and currents within the circuit change over time. An AC analysis shows how the circuit responds across a range of frequencies (its "frequency response"). A DC operating point analysis calculates the circuit's steady-state DC voltages and currents while holding time-varying signals constant, establishing baseline conditions around which the other analyses operate. A power-converter design of the kind at issue here is evaluated using several of these analyses, such as AC analysis (for example, to check a converter's stability and predict its transient response), as well as transient analysis, and the [redacted] file contains a saved transient analysis command specifying the

simulation's duration and recording window, the initial operating conditions, and the load conditions to run the circuit against. In other words, it is essentially a ready-to-run simulation that, apart from supplying or disconnecting any external files the schematic references, requires nothing more than opening it in the LTspice application and clicking run.

III. APPLE'S PROPRIETARY CIRCUIT SIMULATION FILE







19. The circuit design and the parasitic modeling in Patel Ex. 24 are proprietary. The circuit design reveals the arrangement of components of an in-process design, which cannot be obtained from a shipped product. Additionally, which parasitics are modeled, at which locations, and with what values, reflects knowledge acquired through building and testing prior designs. This

information is not published. This information is also valuable because it tells a competitor what parasitics are worth investigating, and specific values that may be acceptable, feasible to achieve, or should be striven to be achieved. A circuit will have many parasitic effects but not all are meaningful or important, and brute force simulations of all parasitics tremendously slow down simulations. Therefore, determining what parasitics are most critical for the specific performance parameter of interest, what ranges are to be expected for these parasitics, and which are worth considering in simulations and which can be ignored, is a lengthy and iterative process that takes many years of accumulated experience. In other words, knowing what Apple has considered worth evaluating could potentially save significant development time. It also tells competitors what Apple has determined is achievable. [redacted] Knowing that Apple can drive that [redacted] is worth pursuing in its own design. Knowing that this solution exists is, by itself, an enormous savings of development time.

[redacted]

IV. THE VALUE OF APPLE'S CIRCUIT SIMULATION FILE

21. SPICE files are working engineering documents that are stored as plain text. Anyone can read one with a text editor and anyone with the requisite software can run it. A working .asc

schematic embodies the circuit design itself: the circuit topology, the component selection, the component parameters, the assumptions about real-world component imperfections, and the operating conditions against which the design was validated. Nor is a file like Patel Ex. 24 merely the record of a completed design. It is part of the design process itself, and a user can adopt it as a starting point and revise it toward its own designs. A competitor with the schematic does not need to reconstruct any of that. It can open the file in a free program like LTspice, run the design, modify it, and validate its own variations against Apple's baseline, all without incurring the original development effort that produced the design. It can then move directly to layout and prototyping. The measurement campaigns, dead ends, and tuning iterations that ordinarily separate a concept from a validated converter design are reduced or avoided. (PI Decl. ¶¶ 74–75, 81–82.) Individual elements of the file also carry value on their own. For example, the results of building circuitry against a measured load profile are useful. A competitor can test its own candidate designs and parasitic effects against a real, measured demand. And the parasitic values themselves give a competitor a benchmark for what is achievable in this type of power delivery network as it develops its own product.

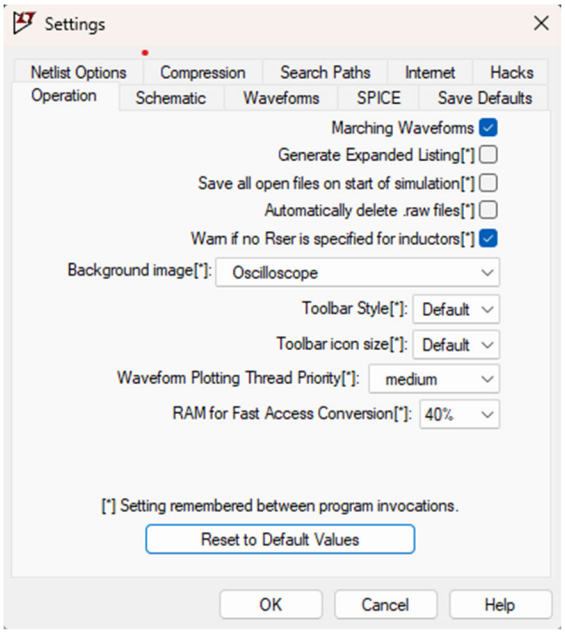
22. The file can become more useful when it is given to an AI agent. Because an .asc file is plain text, an AI system can ingest it directly and parse the complete design. Further, an AI agent can run simulations more quickly than an engineer clicking through the application, and can sweep parameters, explore design variations, and optimize the design without human intervention. This process can take an engineer days or weeks, but potentially only hours or less for an AI agent. The file is also the kind of validated, internally consistent engineering data used to train or fine-tune AI models for expert technical work. (PI Decl. ¶ 68.) A model trained on Apple's working design files can then assimilate Apple's proven design decisions into its permanent working knowledge with every subsequent engineering decision it makes, whether or not the original file is ever opened again.

V. NECESSITY FOR EXPEDITED INVESTIGATION

23. It is my opinion that there is a risk that information generated by LTspice indicating how and to what extent Apple's development files were used could be lost if this information is not obtained now. This information could be erased or otherwise permanently lost through even normal use of the LTspice software, and it may become difficult or impossible to connect any designs based

on Patel Ex. 24 back to the source file.

24. For example, when simulations are run in LTspice, previously run simulations are not always saved. As described in Section II.C above, running an .asc file produces companion .raw, .net, and .log files. LTspice, however, can be configured to automatically delete its companion files. *See* Operation, https://ltwiki.org/LTspiceHelp/LTspiceHelp/Operation.htm (last visited Aug. 30, 2026). The screenshot below was captured from the current version of LTspice as of August 30, 2026, which illustrates how one can automatically delete .raw files[*], within LTspice:



In other words, the files evidencing use of the schematics can be deleted during the ordinary operation of the software, with no affirmative act of deletion required.

25. Also, even where the companion files are not deleted, the software does not maintain a history of use. LTspice writes a schematic's companion files under the schematic's own name and regenerates them each time the simulation is run. Re-running a simulation therefore replaces the prior run's .raw, .net, and .log files with new versions. As a matter of the software's normal operation, the record of any earlier use of the schematic is overwritten. Additionally, simulations create temporary "scratch" files that may not be preserved long-term. LTspice uses a designated directory for temporary storage of such files, and remnants of prior simulation runs may be recoverable from that path. Temporary directories, however, are by design subject to routine deletion and overwriting, so the window for recovering this category of evidence closes on its own.

26. Also, delay makes it harder to trace where a design has gone. Circuit simulations are development documents, a precursor to hardware while a design is still being developed. A misappropriated circuit design does not remain static once it is in use. Engineers will modify component values, substitute parts based on who can supply that part, and adjust the architecture to fit a product's constraints for example. Each revision moves the design further from its source. A design that today matches Apple's file closely enough that the correspondence is unmistakable may, after successive rounds of revision, no longer resemble it closely enough to demonstrate the connection—even though it works because it began there. This is particularly true if the circuit design is integrated into an AI model. When a design is used to train or refine a model, it stops being a single file. It becomes part of the model and users may build on that file and iterate quickly, making it challenging to trace how the design has been used. So, while the benefit of the misappropriation persists, the evidence of it may not.

VI. CONCLUSION

27. For the reasons stated above, it is my opinion that evidence of use and extent of use of the [redacted] (Patel Ex. 24) should be saved now before this information is no longer recoverable.

I declare under penalty of perjury that, to the best of my knowledge, the foregoing is true and correct.

Executed in Columbus, Ohio, on August 31, 2026.

Dr. Ayman Fayed