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E-FILING ORIGINAL FILED
MAY 20 2004
Richard W. Wieking
Clerk, U.S. District Court
Northern District of California
San Jose

UNITED STATES DISTRICT COURT

NORTHERN DISTRICT OF CALIFORNIA

C04 02000 JL

MONOLITHIC POWER SYSTEMS, INC., a California corporation,

Plaintiff,

v.

O2 MICRO INTERNATIONAL LTD., a Cayman Islands corporation,

Defendant.

No.

COMPLAINT FOR DECLARATORY JUDGMENT

DEMAND FOR JURY TRIAL

Plaintiff Monolithic Power System, Inc., a California Corporation ("MPS"), for its Complaint, avers as follows:

1. **Jurisdiction.** This is an action for a declaratory judgment that MPS does not infringe any valid and enforceable claim of United States Patent No. 6,396,722 (a true and correct copy of which is attached hereto as Exhibit A) ("the '722 patent"). On information and belief, plaintiff O2 Micro International, Ltd. ("O2 Micro") is the assignee of the '722 patent. This action is filed pursuant to 28 U.S.C. §§ 2201 and 2202 for the purpose of resolving an actual and justiciable controversy between the parties hereto. This Court has subject matter

jurisdiction over this action pursuant to 28 U.S.C. §§ 1331 and 1338(a) because the action arises under the patent statutes of the United States.

2. **Venue.** Venue is proper in this district pursuant to 28 U.S.C. § 1391(d) because, *inter alia*, defendant O2 Micro International, Ltd. ("O2 Micro") is an alien corporation organized under the laws of the Cayman Islands.

3. **Intradistrict Assignment.** Pursuant to Civil Local Rule 3-2(c), this action for a declaratory judgment of non-infringement of a patent shall be assigned on a district-wide basis.

4. MPS is a corporation organized under the laws of the State of California with its principal place of business in Santa Clara, California.

5. Upon information and belief, O2 Micro is a corporation organized under the laws of the Cayman Islands. O2 Micro does business in this District and elsewhere in the State of California. Among other things, O2 Micro has a subsidiary, O2 Micro Inc., in Santa Clara, California, within this District, that designs, makes, uses, and/or sells products that O2 Micro contends practice the '722 patent.

6. In October 2001, O2 Micro brought an action against MPS in the Northern District of California for alleged infringement of United States Patent No. 6,259,615 ("the '615 patent"). That case, No. CV-01-3995 CW (consolidated with an earlier, related action, No. CV-00-4071 CW), is presently pending before The Honorable Claudia Wilken ("the prior California action"). The prior California action is in its later stages. Summary judgment motions have already been filed and ruled upon by the Court for the '615 patent (a true and correct copy of the Court's Order Granting Summary Judgment for MPS on the '615 patent is attached hereto as Exhibit B).

7. The '722 patent is a continuation of the '615 patent. The '722 patent (a) claims the benefit of the same filing date as the '615 patent application; (b) generally has the same specification as the '615 patent; and (c) has many claim limitations in common with the claims of the '615 patent.

8. By a complaint filed on or about January 6, 2003, in the United States District Court for the Eastern District of Texas ("the Texas action"), O2 Micro charged Sumida

Corporation ("Sumida Corp.") and Taiwan Sumida Electronics, Inc., ("Sumida Taiwan") (collectively, "Sumida") with infringement of the '615 patent and the '722 patent. The Texas Action is Case No. 03-CV-00007-TJW and is captioned, "O2 Micro Int'l. v. Sumida Corporation, et al." Sumida Corp. is a corporation organized under the laws of Japan, and Sumida Taiwan is a corporation organized under the laws of Taiwan. Sumida Corp. was voluntarily dismissed from the action, but Sumida Taiwan's motion to dismiss the Texas complaint on the grounds that the Texas Court lacked personal jurisdiction over Sumida Taiwan was denied on or about March 22, 2004.

9. The same claims for the '615 patent that will likely be at issue in the Texas action have already been construed and ruled upon by this Court in the prior California action. Similar claims will also be at issue for the '722 patent.

10. MPS is a manufacturer of inverter controllers for use in DC to AC converters. Sumida Taiwan is a customer of MPS, which purchases MPS's inverter controllers for use in Sumida Taiwan's inverter modules. The accused Sumida Taiwan inverter modules contain one or more of the MPS MP1010, MP1011, and/or MP1015 inverter controllers. O2 Micro has accused some or all of those same products of infringing the '615 patent in its California action against MPS. At Sumida Taiwan's request, MPS has agreed to indemnify Sumida Taiwan in the Texas action filed against it by O2 Micro. O2 Micro has engaged in a pattern of communicating to MPS's customers and MPS's customers' end users its belief that MPS is infringing O2 Micro patents related to DC to AC converters, including, but not limited to, the '615 and '722 patents.

11. As a result of O2 Micro's suit against Sumida Taiwan in Texas, and other acts listed above, MPS is under a reasonable apprehension of imminent legal action in a court of competent jurisdiction, so there exists an actual and justiciable controversy between the parties hereto.

12. MPS contends that it has not infringed, and is not infringing, any valid and enforceable claim of the '722 patent. MPS further contends that by reason of the proceedings in the United States Patent and Trademark Office during the prosecution of the applications that resulted in the '722 patent, and by reason of the admissions and representations therein made by

or on behalf of the applicant for the '722 patent, O2 Micro is estopped from construing the claims of the '722 patent, even if this were otherwise possible, to cover and include any acts by MPS. MPS is informed and believes, and on that basis avers, that O2 Micro denies some or all of the above contentions. Accordingly, a valid and justiciable controversy has arisen and exists between MPS and O2 Micro. MPS desires a judicial determination and declaration of the respective rights and duties of the parties in accordance with MPS's foregoing contentions.

13. By reason of the above acts, O2 Micro has caused, is causing, and unless enjoined and restrained by this Court, will continue to cause MPS great and irreparable injury to, among other things, the good will and business reputation of MPS and its business relations with its customers, all of which cannot be adequately compensated or measured in money. MPS has no adequate remedy at law. MPS is entitled to a preliminary and permanent injunction enjoining and restraining O2 Micro and its respective officers, partners, employees, agents, parents, subsidiaries or anyone in privity with them, and all persons acting in concert with them and each of them:

a. From making any claims to any person or entity that MPS's products infringe the '722 patent;

b. From interfering with, or threatening to interfere with the manufacture, sale, or use of MPS's products by MPS, its customers, distributors, predecessors, successors or assigns; and

c. From instituting or prosecuting any lawsuit or proceeding, placing in issue the right of MPS, its customers, distributors, predecessors, successors or assigns, to make, use or sell products which allegedly infringe the '722 patent.

WHEREFORE, MPS prays for a judgment as follows:

1. For a declaration that its products do not infringe any valid and enforceable claim of the '722 patent;

2. For a preliminary and permanent injunction enjoining and restraining O2 Micro and its respective officers, partners, employees, agents, parents, subsidiaries or anyone in privity with them, and all persons acting in concert with them and each of them:

a. from making any claims to any person or entity that MPS's products infringe the '722 patent;

b. from interfering with, or threatening to interfere with the manufacture, sale, or use of MPS's products by MPS, its customers, distributors, predecessors, successors or assigns; and

c. from instituting or prosecuting any lawsuit or proceeding, placing in issue the right of MPS, its customers, distributors, predecessors, successors or assigns, to make, use or sell products which allegedly infringe the '722 patent.

3. For MPS's reasonable attorneys' fees and costs of suit incurred herein; and

4. For such other and further relief as the Court may deem proper.

Dated: May 20, 2004

WILSON SONSINI GOODRICH & ROSATI
Professional Corporation

By: _____
Michael Barclay

Attorneys for Plaintiff
MONOLITHIC POWER SYSTEMS, INC.

DEMAND FOR JURY TRIAL

Pursuant to Rule 38(b) of the Federal Rules of Civil Procedure and Civil Local Rule 3-6(a), plaintiff demands a trial by jury of this action.

Dated: May 20, 2004

WILSON SONSINI GOODRICH & ROSATI
Professional Corporation

By: Michael Barclay
Michael Barclay

Attorneys for Plaintiff
MONOLITHIC POWER SYSTEMS, INC.

Exhibit A

US006396722B2

(12) **United States Patent**
Lin

(10) **Patent No.: US 6,396,722 B2**
(45) **Date of Patent: May 28, 2002**

(54) **HIGH-EFFICIENCY ADAPTIVE DC/AC CONVERTER**

(75) Inventor: **Yung-Lin Lin**, Palo Alto, CA (US)

(73) Assignee: **Micro International Limited** (KY)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **09/850,222**

(22) Filed: **May 7, 2001**

Related U.S. Application Data

(63) Continuation of application No. 09/437,081, filed on Nov. 9, 1999, now Pat. No. 6,259,615.
(60) Provisional application No. 60/145,118, filed on Jul. 22, 1999.

(51) **Int. Cl.**[7] **H02M 3/24**; H02M 3/335

(52) **U.S. Cl.** **363/98**; 363/17

(58) **Field of Search** 363/98, 132, 17, 363/89, 56, 37

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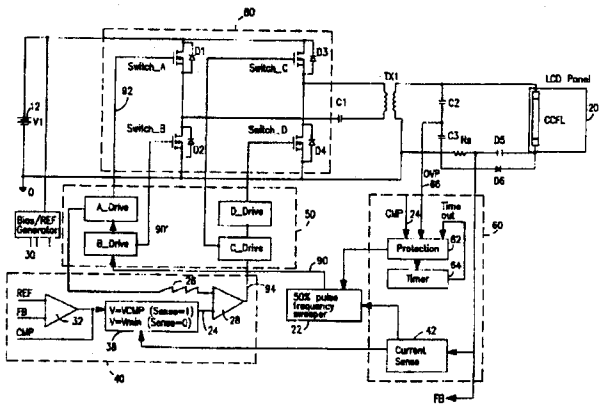
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Primary Examiner—Rajnikant B. Patel
(74) *Attorney, Agent, or Firm*—Grossman, Tucker, Perreault & Pfleger, PLLC

(57) **ABSTRACT**

A CCFL power converter circuit is provided using a high-efficiency zero-voltage-switching technique that eliminates switching losses associated with the power MOSFETs. An optimal sweeping-frequency technique is used in the CCFL ignition by accounting for the parasitic capacitance in the resonant tank circuit. Additionally, the circuit is self-learning and is adapted to determine the optimum operating frequency for the circuit with a given load. An over-voltage protection circuit can also be provided to ensure that the circuit components are protected in the case of open-lamp condition.

19 Claims, 11 Drawing Sheets



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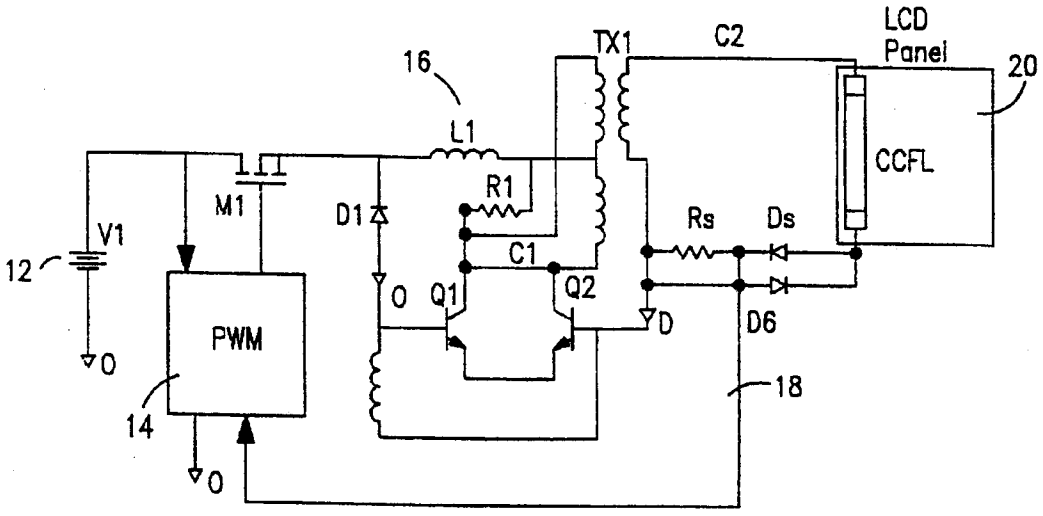


FIG. 1
PRIOR ART

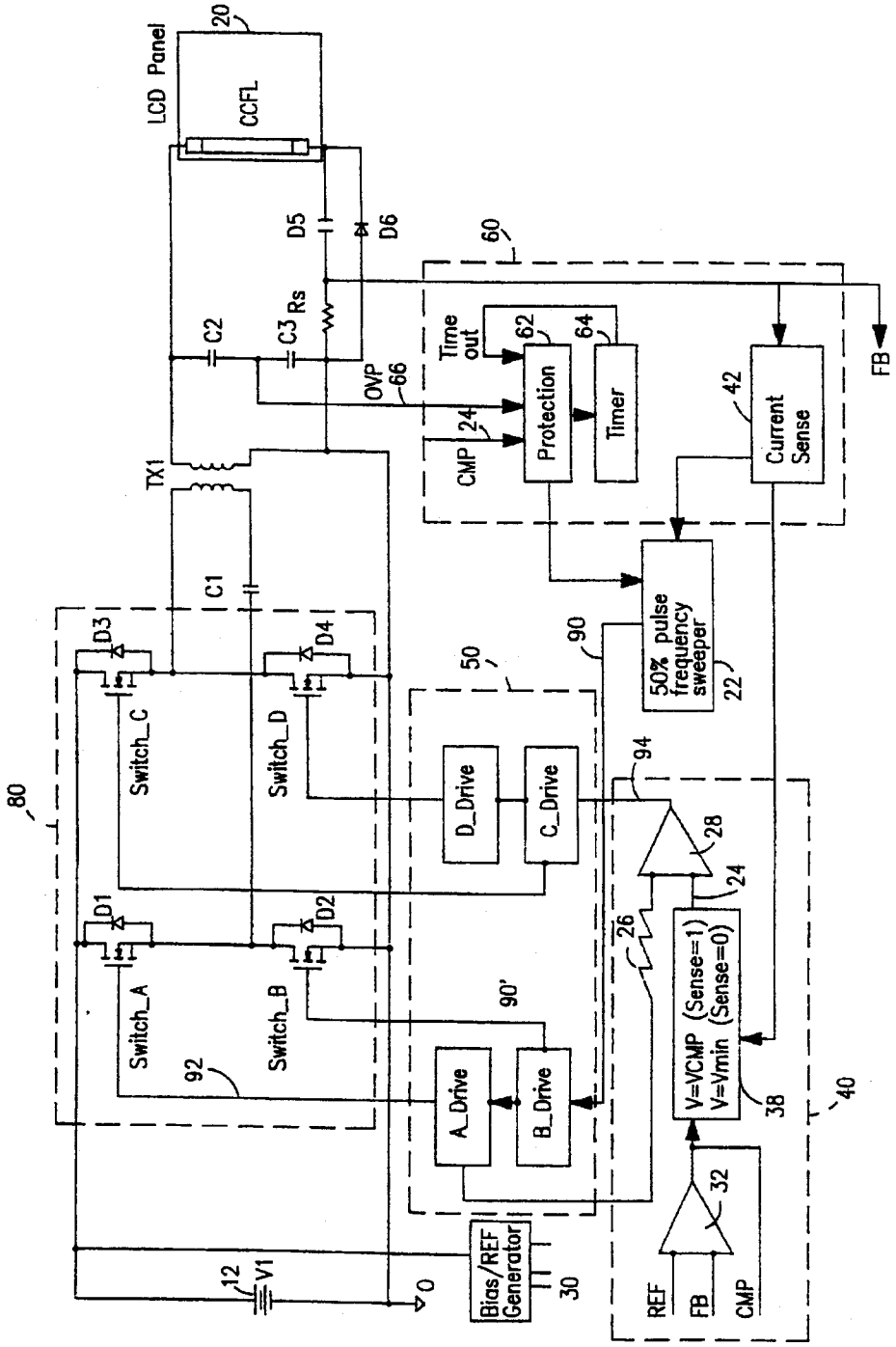

LCD Panel
20
CCFL
D5
D6
60
C2
C3
Rs
Time out
62
64
OVP
66
Protection
Timer
42
Current Sense
FB
CMP
24
TX1
C1
50% pulse frequency sweeper
22
90
D3
D4
50
Switch_C
Switch_D
D_Drive
C_Drive
94
80
28
24
D1
D2
26
Switch_A
Switch_B
90'
V=VCMP (Sense=1)
V=Vmin (Sense=0)
92
A_Drive
B_Drive
38
40
32
Bias/REF Generator
30
12
V1
0
REF
FB
CMP

FIG. 2

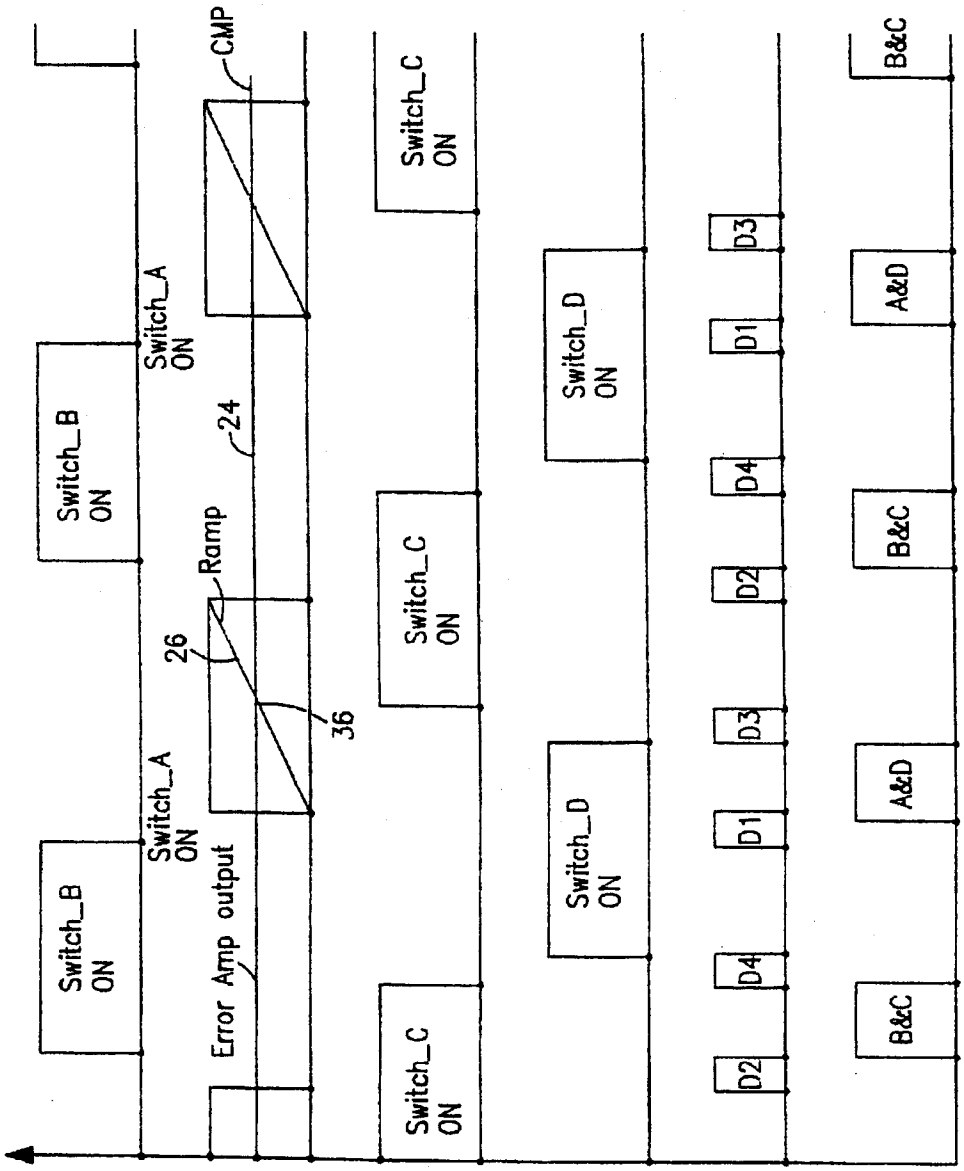


FIG. 2a

FIG. 2b

FIG. 2c

FIG. 2d

FIG. 2e

FIG. 2f

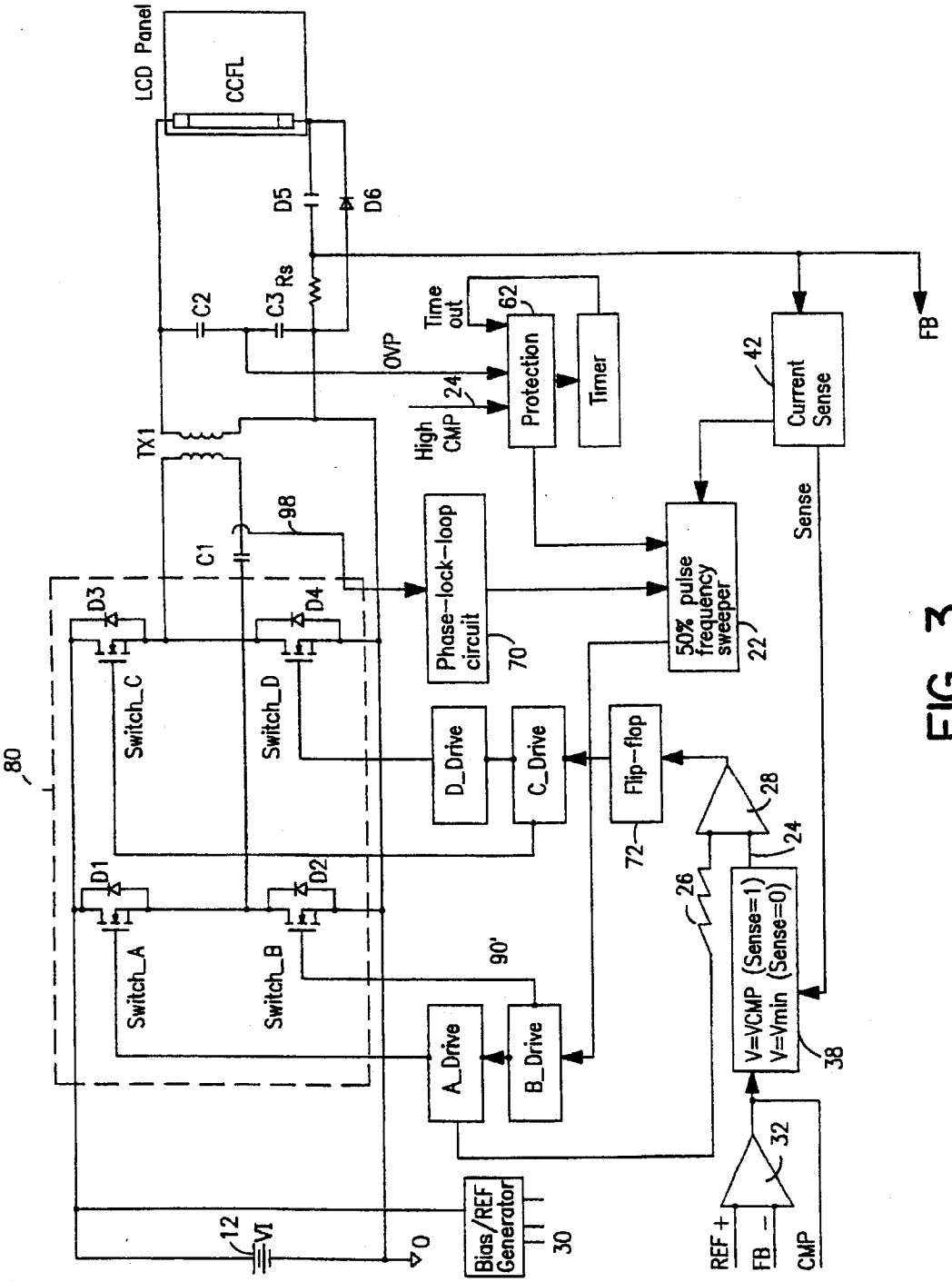

LCD Panel
CCFL
D5
D6
C2
C3
Rs
Time out
62
OVP
High CMP
24
Protection
Timer
42
Current Sense
FB
TX1
C1
98
Phase-lock-loop circuit
70
50% pulse frequency sweeper
22
Sense
D3
D4
Switch_C
Switch_D
D_Drive
C_Drive
Flip-flop
28
72
26
24
80
D1
D2
Switch_A
Switch_B
90'
A_Drive
B_Drive
V=VCMP (Sense=1)
V=Vmin (Sense=0)
38
32
12
VI
0
Bias/REF Generator
30
REF +
FB
CMP

FIG. 3

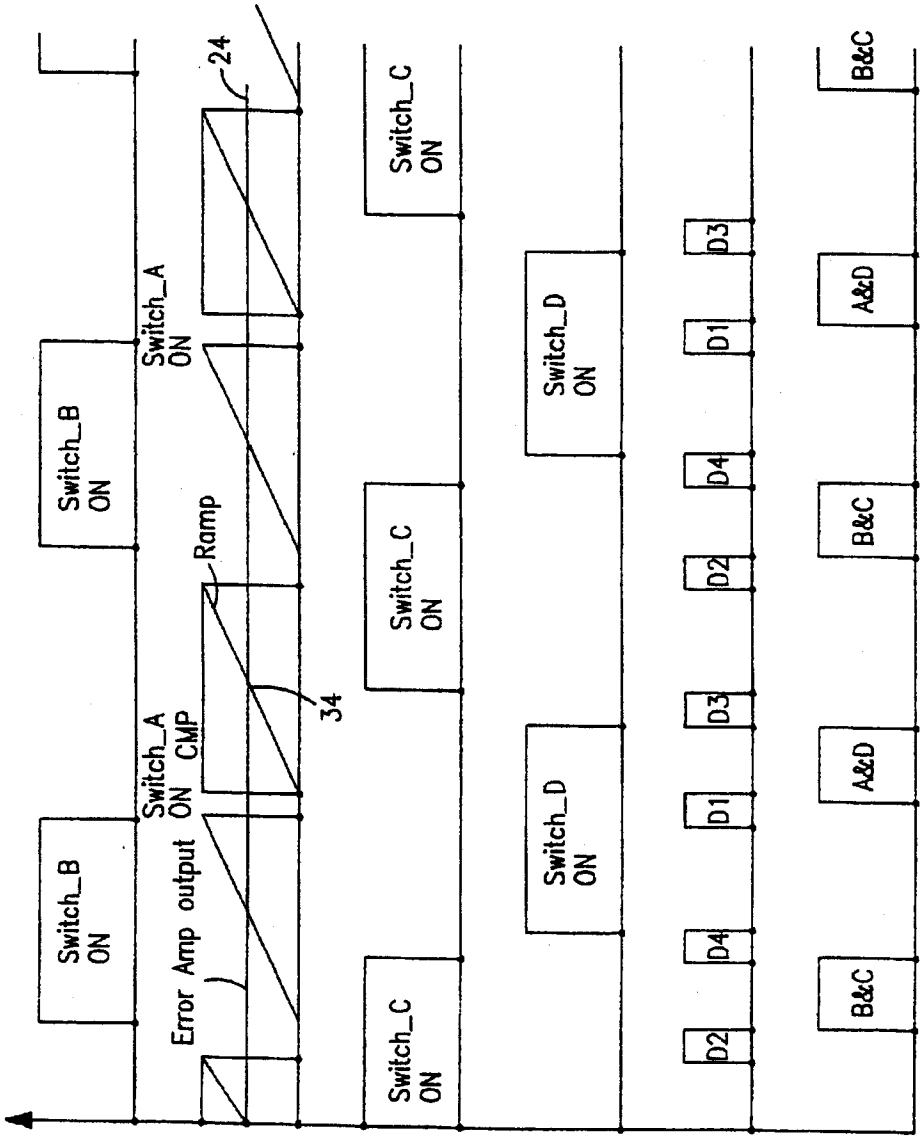


FIG. 3a

FIG. 3b

FIG. 3c

FIG. 3d

FIG. 3e

FIG. 3f

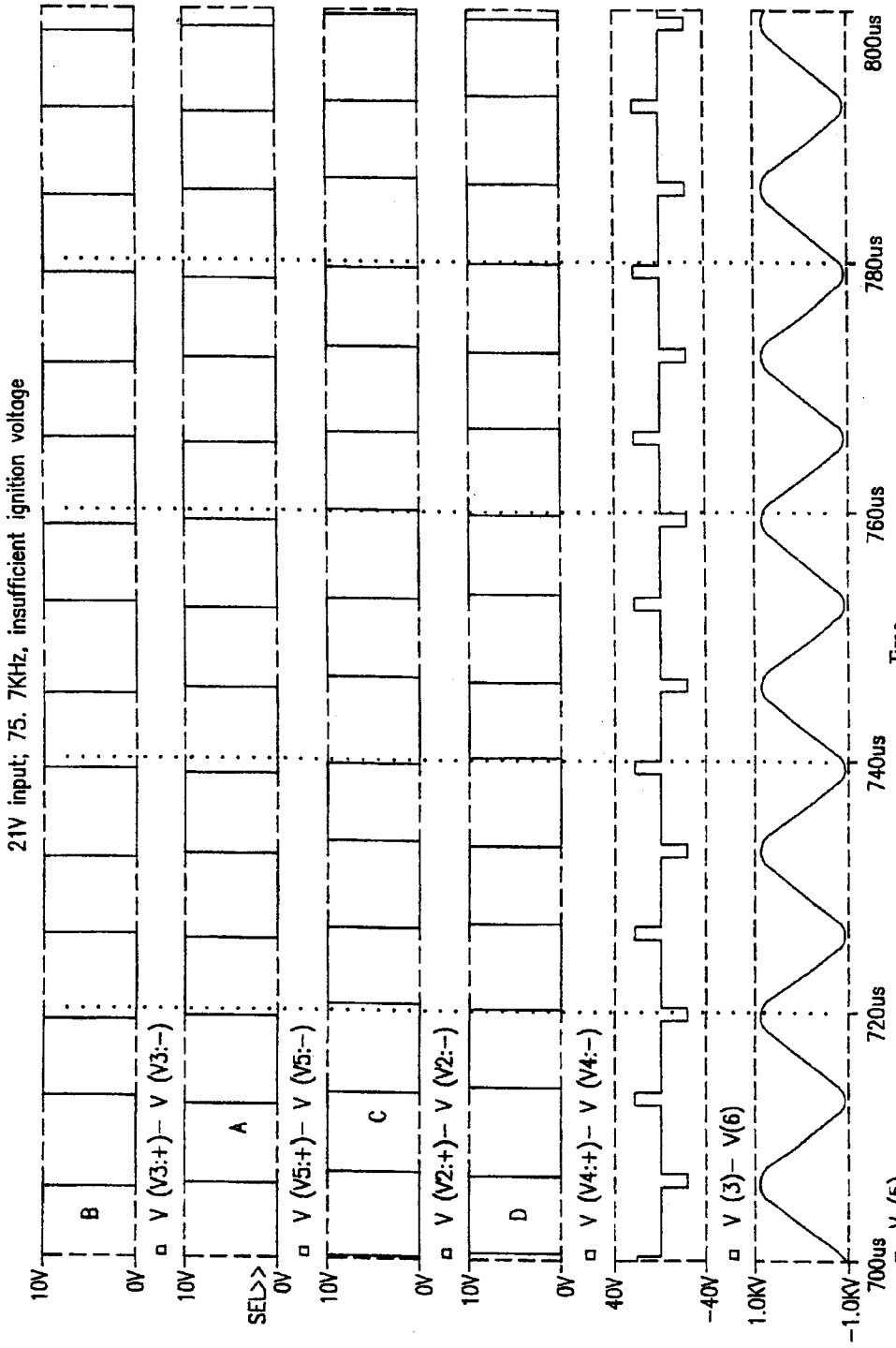

21V input; 75. 7KHz, insufficient ignition voltage
B
A
C
D
SEL>>
10V
0V
V (V3:+)– V (V3:–)
V (V5:+)– V (V5:–)
V (V2:+)– V (V2:–)
V (V4:+)– V (V4:–)
40V
–40V
V (3)– V(6)
1.0KV
–1.0KV
V (5)
700us
720us
740us
760us
780us
800us
Time

FIG. 4a

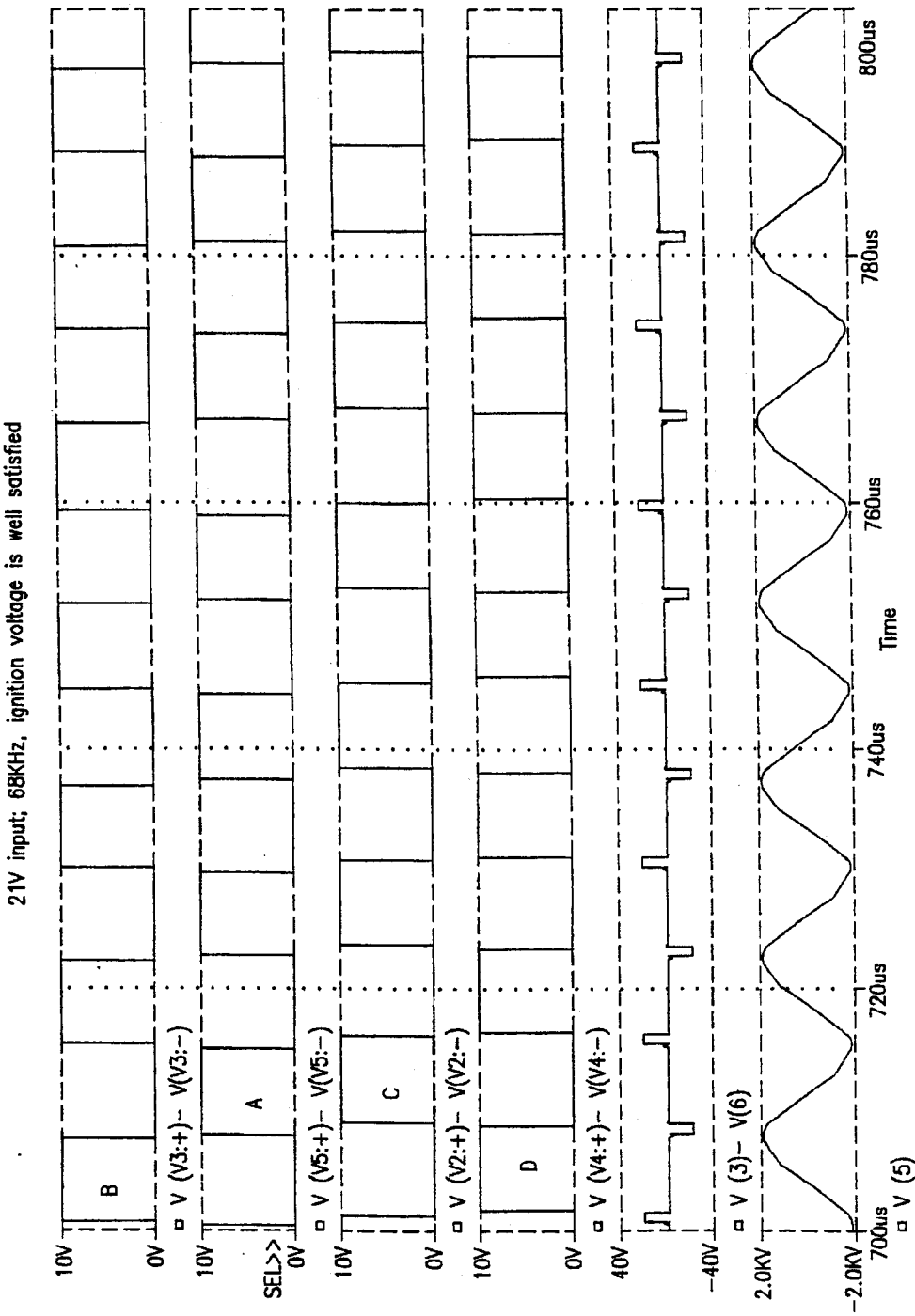

21V input; 68KHz, ignition voltage is well satisfied
B
A
C
D
SEL>>
10V
0V
40V
-40V
2.0KV
-2.0KV
V (V3:+)- V(V3:-)
V (V5:+)- V(V5:-)
V (V2:+)- V(V2:-)
V (V4:+)- V(V4:-)
V (3)- V(6)
V (5)
700us
720us
740us
760us
780us
800us
Time

FIG. 4b

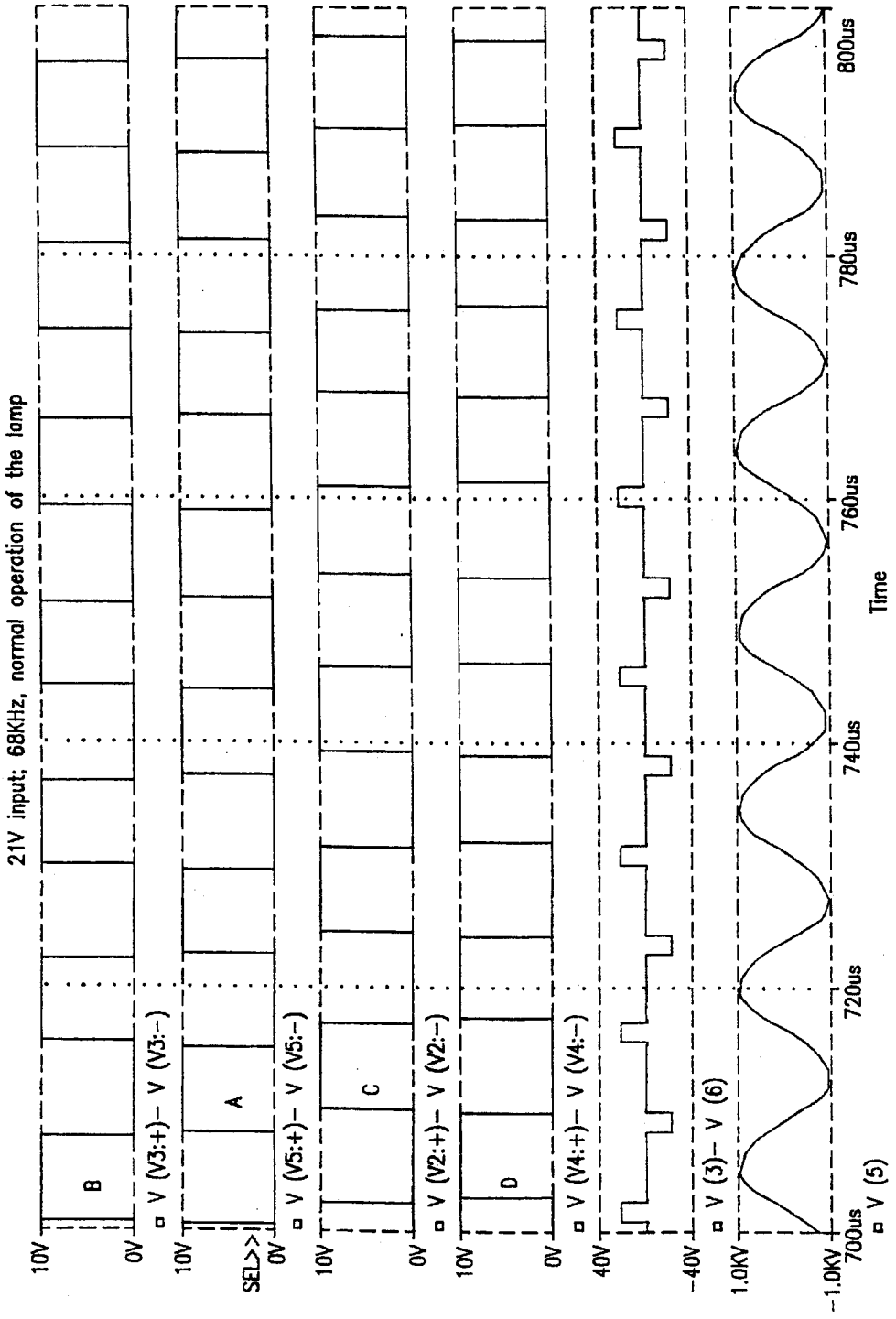

21V input; 68KHz, normal operation of the lamp
10V
0V
B
V (V3:+)– V (V3:–)
10V
SEL>>
0V
A
V (V5:+)– V (V5:–)
10V
0V
C
V (V2:+)– V (V2:–)
10V
0V
D
V (V4:+)– V (V4:–)
40V
–40V
V (3)– V (6)
1.0KV
–1.0KV
V (5)
700us
720us
740us
760us
780us
800us
Time

FIG. 4c

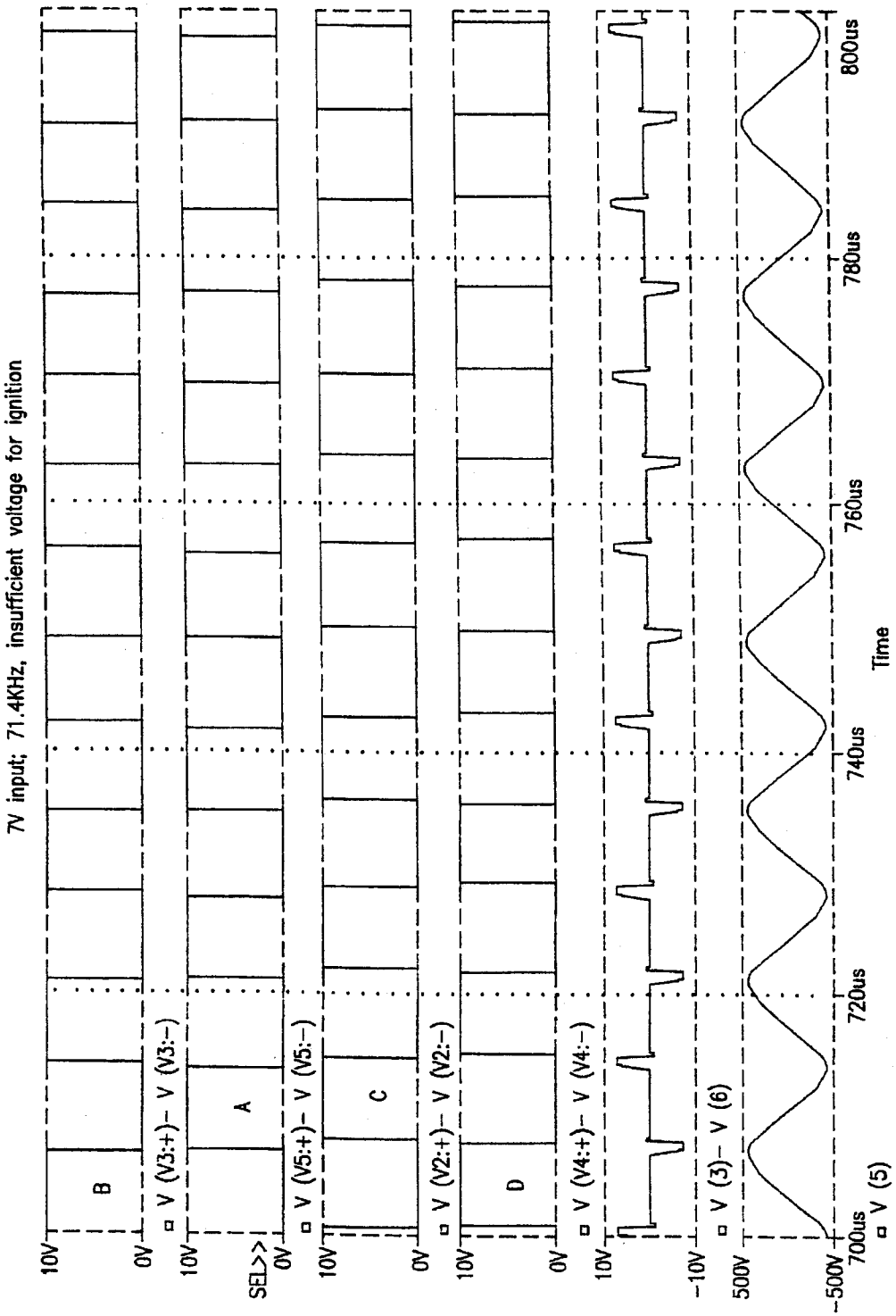

7V input; 71.4KHz, insufficient voltage for ignition
B
A
C
D
SEL>>
10V
0V
-10V
500V
-500V
V (V3:+)- V (V3:-)
V (V5:+)- V (V5:-)
V (V2:+)- V (V2:-)
V (V4:+)- V (V4:-)
V (3)- V (6)
V (5)
700us
720us
740us
760us
780us
800us
Time

FIG. 4d

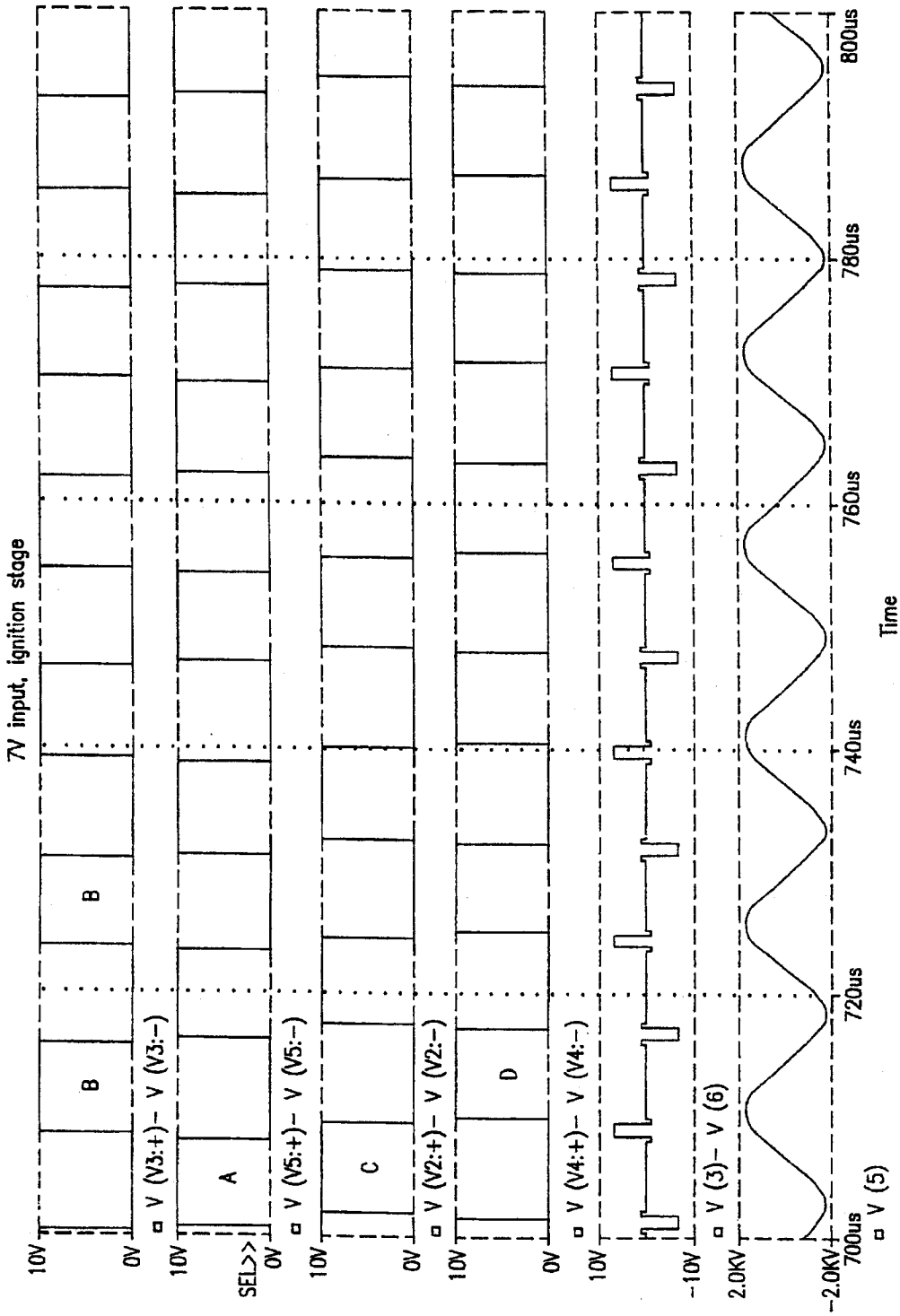

7V input, ignition stage
10V
0V
B
B
V (V3:+)- V (V3:-)
10V
SEL>>
0V
A
V (V5:+)- V (V5:-)
10V
0V
C
V (V2:+)- V (V2:-)
10V
0V
D
V (V4:+)- V (V4:-)
10V
-10V
V (3)- V (6)
2.0KV
-2.0KV
V (5)
700us
720us
740us
760us
780us
800us
Time

FIG. 4e

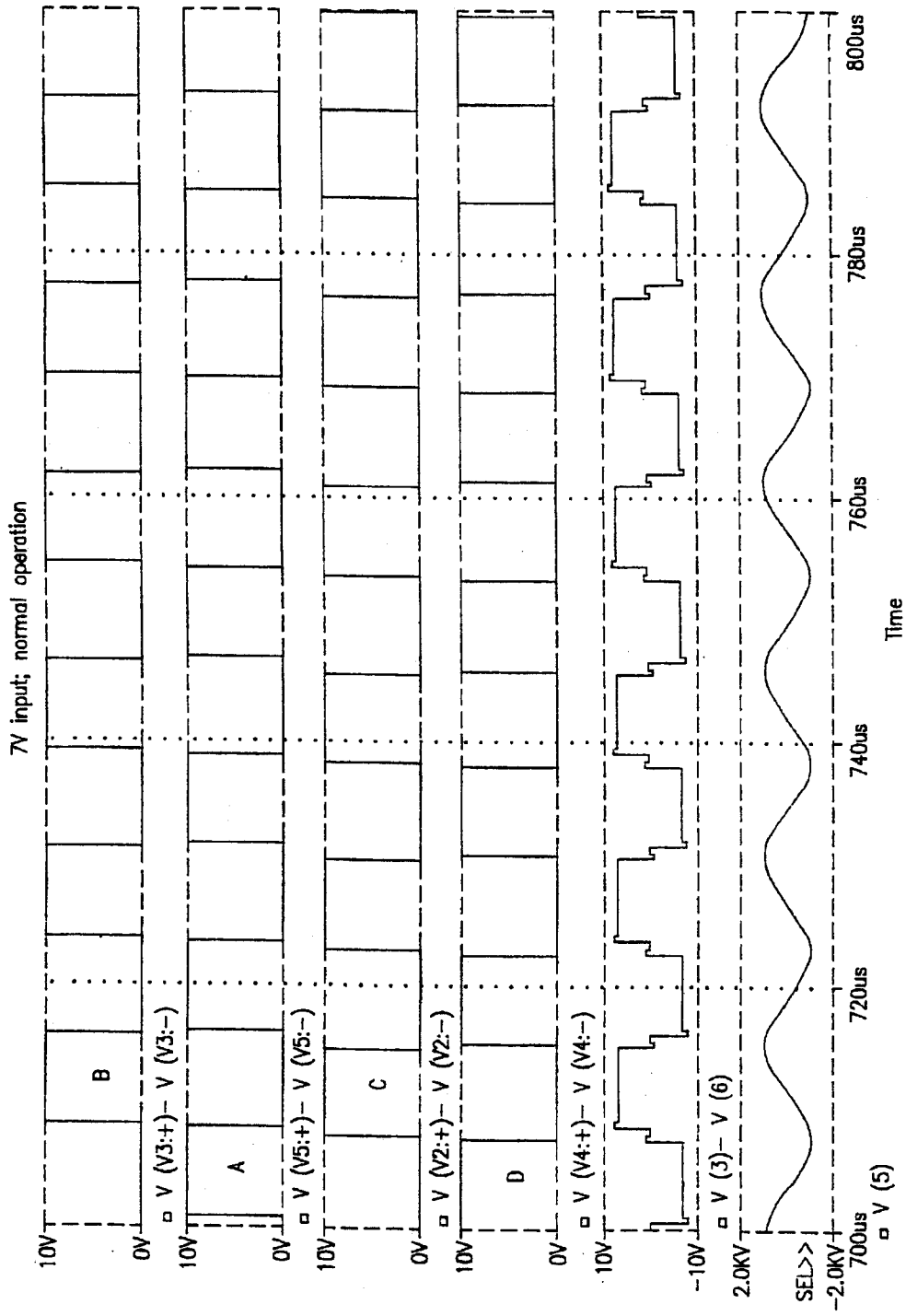

7V input; normal operation
B
A
C
D
10V
0V
-10V
V (V3:+)- V (V3:-)
V (V5:+)- V (V5:-)
V (V2:+)- V (V2:-)
V (V4:+)- V (V4:-)
V (3)- V (6)
V (5)
2.0KV
-2.0KV
SEL>>
700us
720us
740us
760us
780us
800us
Time

FIG. 4f

HIGH-EFFICIENCY ADAPTIVE DC/AC CONVERTER

CLAIM OF PROVISIONAL APPLICATION RIGHTS

This application is a continuation application under 37 C.F.R § 1.53(b) of application Ser. No. 09/437,081, filed Nov. 9, 1999, now U.S. Pat. No. 6,259,615, and claims the benefit of U.S. Provisional Application No. 60/145,118 filed on Jul. 22, 1999.

FIELD OF THE INVENTION

The present invention is directed to a DC to AC power converter circuit. More particularly, the present invention provides a high efficiency controller circuit that regulates power delivered to a load using a zero-voltage-switching technique. General utility for the present invention is found as a circuit for driving one or more Cold Cathode Fluorescent Lamps (CCFLs), however, those skilled in the art will recognize that the present invention can be utilized with any load where high efficiency and precise power control is required.

DESCRIPTION OF RELATED ART

FIG. **1** depicts a convention CCFL power supply system **10**. The system broadly includes a power supply **12**, a CCFL driving circuit **16**, a controller **14**, a feedback loop **18**, and one or more lamps CCFL associated with an LCD panel **20**. Power supply **12** supplies a DC voltage to circuit **16**, and is controlled by controller **14**, through transistor Q3. Circuit **16** is a self-resonating circuit, known as a Royer circuit. Essentially, circuit **16** is a self-oscillating dc to ac converter, whose resonant frequency is set by L1 and C1, and N1–N4 designate transformer windings and number of turns of the windings. In operation, transistors Q1 and Q2 alternately conduct and switch the input voltage across windings N1 and N2, respectively. If Q1 is conducting, the input voltage is placed across winding N1. Voltages with corresponding polarity will be placed across the other windings. The induced voltage in N4 makes the base of Q2 positive, and Q1 conducts with very little voltage drop between the collector and emitter. The induced voltage at N4 also holds Q2 at cutoff. Q1 conducts until the flux in the core of TX1 reaches saturation.

Upon saturation, the collector of Q1 rises rapidly (to a value determined by the base circuit), and the induced voltages in the transformer decrease rapidly. Q1 is pulled further out of saturation, and V_{CE} rises, causing the voltage across N1 to further decrease. The loss in base drive causes Q1 to turn off, which in turn causes the flux in the core to fall back slightly and induces a current in N4 to turn on Q2. The induced voltage in N4 keeps Q1 conducting in saturation until the core saturates in the opposite direction, and a similar reversed operation takes place to complete the switching cycle.

Although the inverter circuit **16** is composed of relatively few components, its proper operation depends on complex interactions of nonlinearities of the transistors and the transformer. In addition, variations in C1, Q1 and Q2 (typically, 35% tolerance) do not permit the circuit **16** to be adapted for parallel transformer arrangements, since any duplication of the circuit **16** will produce additional, undesirable operating frequencies, which may resonate at certain harmonics. When applied to a CCFL load, this circuit produces a "beat" effect in the CCFLs, which is both noticeable and undesirable.

Even if the tolerances are closely matched, because circuit **16** operates in self-resonant mode, the beat effects cannot be removed, as any duplication of the circuit will have its own unique operating frequency.

Some other driving systems can be found in U.S. Pat. Nos. 5,430,641; 5,619,402; 5,615,093; 5,818,172. Each of these references suffers from low efficiency, two-stage power conversion, variable-frequency operation, and/or load dependence. Additionally, when the load includes CCFL(s) and assemblies, parasitic capacitances are introduced, which affects the impedance of the CCFL itself. In order to effectively design a circuit for proper operation, the circuit must be designed to include consideration of the parasitic impedances for driving the CCFL load. Such efforts are not only time-consuming and expensive, but it is also difficult to yield an optimal converter design when dealing with various loads. Therefore, there is a need to overcome these drawbacks and provide a circuit solution that features high efficiency, reliable ignition of CCFLs, load-independent power regulation and single frequency power conversion.

SUMMARY OF THE INVENTION

Accordingly, the present invention provides an optimized system for driving a load, obtains an optimal operation for various LCD panel loads, thereby improving the reliability of the system.

Broadly defined, the present invention provides A DC/AC converter circuit for controllably delivering power to a load, comprising an input voltage source; a first plurality of overlapping switches and a second plurality of overlapping switches being selectively coupled to said voltage source, the first plurality of overlapping switches defining a first conduction path, the second plurality of overlapping switches defining a second conduction path. A pulse generator is provided to generate a pulse signal. Drive circuitry receives the pulse signal and controls the conduction state of the first and second plurality of switches. A transformer is provided having a primary side and a secondary side, the primary side is selectively coupled to the voltage source in an alternating fashion through the first conduction path and, alternately, through the second conduction path. A load is coupled to the secondary side of the transformer. A feedback loop circuit is provided between the load and the drive circuitry that supplies a feedback signal indicative of power being supplied to the load. The drive circuitry alternates the conduction state of the first and second plurality of switches, and the overlap time of the switches in the first plurality of switches, and the overlap time of the switches in the second plurality of switches, to couple the voltage source to the primary side based at least in part on the feedback signal and the pulse signal.

The drive circuitry is constructed to generate a first complimentary pulse signal from the pulse signal, and a ramp signal from the pulse signal. The pulse signal is supplied to a first one of the first plurality of switches to control the conduction state thereof, and the ramp signal is compared with at least the feedback signal to generate a second pulse signal, where a controllable conduction overlap condition exists between the conduction state of the first and second switches of the first plurality of switches. The second pulse signal is supplied to a second one of the first plurality of switches and controlling the conduction state thereof. The drive circuitry further generates a second complimentary pulse signal based on the second pulse signal, wherein said first and second complimentary pulse signals control the conduction state of a first and second ones of the

second plurality of switches, respectively. Likewise, a controllable conduction overlap condition exists between the conduction state of the first and second switches of the second plurality of switches.

In method form, the present invention provides a method for controlling a zero-voltage switching circuit to deliver power to a load comprising the steps of supplying a DC voltage source; coupling a first and second transistor defining a first conduction path and a third and fourth transistor defining a second conduction path to the voltage source and a primary side of a transformer; generating a pulse signal to having a predetermined pulse width; coupling a load to a secondary side of said transformer; generating a feedback signal from the load; and controlling the feedback signal and the pulse signal to determine the conduction state of said first, second, third and fourth transistors.

In the first embodiment, the present invention provides a converter circuit for delivering power to a CCFL load, which includes a voltage source, a transformer having a primary side and a secondary side, a first pair of switches and a second pair of switches defining a first and second conduction path, respectively, between the voltage source and the primary side, a CCFL load circuit coupled to the secondary side,a pulse generator generating a pulse signal, a feedback circuit coupled to the load generating a feedback signal, and drive circuitry receiving the pulse signal and the feedback signal and coupling the first pair of switches or the second pair of switches to the voltage source and the primary side based on said pulse signal and said feedback signal to deliver power to the CCFL load.

Additionally, the first embodiment provides a pulse generator that generates a pulse signal having a predetermined frequency. The drive circuitry includes first, second, third and fourth drive circuits; and the first pair of switches includes first and second transistors, and the second pair of switches includes third and fourth transistors. The first, second, third and fourth drive circuits are connected to the control lines of the first, second, third and fourth transistors, respectively. The pulse signal is supplied to the first drive circuit so that the first transistor is switched in accordance with the pulse signal. The third drive circuit generates a first complimentary pulse signal and a ramp signal based on the pulse signal, and supplies the first complimentary pulse signal to the third transistor so that the third transistor is switched in accordance with the first complimentary pulse signal. The ramp signal and the feedback signal are compared to generate a second pulse signal. The second pulse signal is supplied to the second drive circuit so that the second transistor is switched in accordance with the second pulse signal. The forth driving circuit generates a second complementary pulse signal based on the second pulse signal and supplies the second complementary pulse signal to the fourth transistor so that the fourth transistor is switched in accordance with the second complimentary pulse signal. In the present invention, the simultaneous conduction of the first and second transistors, and the third and fourth transistors, respectively, controls the amount of power delivered to the load. The pulse signal and the second pulse signal are generated to overlap by a controlled amount, thus delivering power to the load along the first conduction path. Since the first and second complementary pulse signals are generated from the pulse signal and second pulse signal, respectively, the first and second complementary pulse signals are also generated to overlap by a controlled amount, power is delivered to the load along the second conduction path, in an alternating fashion between the first and second conduction paths.

Also, the pulse signal and first complementary pulse signal are generated to be approximately 180° out of phase, and the second pulse signal and the second complementary signal are generated to be approximately 180° out of phase, so that a short circuit condition between the first and second conduction paths is avoided

In addition to the converter circuit provided in the first embodiment, the second embodiment includes a flip-flop circuit coupled to the second pulse signal, which triggers the second pulse signal to the second drive signal only when the third transistor is switched into a conducting state. Additionally, the second embodiment includes, a phase-lock loop (PLL) circuit having a first input signal from the primary side and a second input signal using the feedback signal. The PLL circuit compares the phase difference between these two signals and supplies a control signal to the pulse generator to control the pulse width of the pulse signal based on the phase difference between the first and second inputs.

In both embodiments, the preferred circuit includes the feedback control loop having a first comparator for comparing a reference signal with the feedback signal and producing a first output signal. A second comparator is provided for comparing said first output signal with the ramp signal and producing said second pulse signal based on the intersection of the first output signal and the ramp signal. The feedback circuit also preferably includes a current sense circuit receiving the feedback signal and generating a trigger signal, and a switch circuit between the first and second comparator, the switch circuit receiving the trigger signal and generating either the first output signal or a predetermined minimum signal, based on the value of the trigger signal. The reference signal can include, for example, a signal that is manually generated to indicate a desires power to be delivered to the load. The predetermined minimum voltage signal can include a programmed minimum voltage supplied to the switches, so that an overvoltage condition does not appear across the load.

Likewise, in both embodiments described herein, an overcurrent protection circuit can be provided that receives the feedback signal and controls the pulse generator based on the value of said feedback signal. An overvoltage protection can be provided to receive a voltage signal from across the load and the first output signal and compare the voltage signal from across the load and the first output signal, to control the pulse generator based on the value of the voltage signal from across the load.

It will be appreciated by those skilled in the art that although the following Detailed Description will proceed with reference being made to preferred embodiments and methods of use, the present invention is not intended to be limited to these preferred embodiments and methods of use. Rather, the present invention is of broad scope and is intended to be limited as only set forth in the accompanying claims.

Other features and advantages of the present invention will become apparent as the following Detailed Description proceeds, and upon reference to the Drawings, wherein like numerals depict like parts, and wherein:

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a conventional DC/AC converter circuit;

FIG. 2 is one preferred embodiment of a DC/AC converter circuit of the present invention;

FIGS. 2*a*–2*f* is an exemplary timing diagram of the circuit of FIG. 2;

FIG. **3** is another preferred embodiment of a DC/AC converter circuit of the present invention;

FIGS. **3***a*–**3***f* is an exemplary timing diagram of the circuit of FIG. **3**; and

FIGS. **4***a*–**4***f* depict emulation diagrams for the circuits shown in FIGS. **2** and **3**.

DETAILED DESCRIPTION OF THE INVENTION

While not wishing to be bound by example, the following Detailed Description will proceed with reference to a CCFL panel as the load for the circuit of the present invention. However, it will be apparent that the present invention is not limited only to driving one or CCFLs, rather, the present invention should be broadly construed as a power converter circuit and methodology independent of the particular load for a particular application.

As an overview, the present invention provides circuitry to controllably deliver power to a load using feedback signals and pulse signals to adjust the ON time of two pairs of switches. When one pair of switches are controllably turned ON such that their ON times overlap, power is delivered to a load (via a transformer), along a conduction path defined by the pair of switches. Likewise, when the other pair of switches are controllably turned ON such that their ON times overlap, power is delivered to a load (via a transformer), along a conduction path defined by other pair of switches. Thus, by selectively turning ON switches and controlling the overlap between—switches, the present invention can precisely control power delivered to a given load. Additionally, the present invention includes over-current and over-voltage protection circuits, which discontinues power to the load in the event of a short circuit or open circuit condition. Moreover, the controlled switching topology described herein enables the circuit to operate irrespective of the load, and with a single operating frequency independent of the resonant effects of the transformer arrangement. These features are discussed below with reference to the drawings.

The circuit diagram shown in FIG. **2** illustrates one preferred embodiment of a phase-shift, full-bridge, zero-voltage-switching power converter of the present invention. Essentially, the circuit shown in FIG. **2** includes a power source **12**, a plurality of switches **80** arranged as diagonal pairs of switches defining alternating conduction paths, drive circuitry **50** for driving each of the switches, a frequency sweeper **22** which generates a square wave pulse to the drive circuitry **50**, a transformer TX1 (with an associated resonant tank circuit defined by the primary side of TX1 and C1) and a load. Advantageously, the present invention also includes an overlap feedback control loop **40** which controls the ON time of at least one of each pair of switches, thereby permitting controllable power to be delivered to the load.

A power source **12** is applied to the system. Initially, a bias/reference signal **30** is generated for the control circuitry (in control loop **40**) from the supply. Preferably, a frequency sweeper **22** generates a 50% duty-cycle pulse signal, starting with an upper frequency and sweeping downwards at a pre-determined rate and at pre-determined steps (i.e., square wave signal of variable pulse width). The frequency sweeper **22** preferably is a programmable frequency generator, as is known in the art. The pulse signal **90** (from the sweeper **22**) is delivered to B_Drive (which drives the Switch_B, i.e., controls the gate of Switch_B), and is delivered to A_Drive, which generates a complementary pulse signal **92** and a ramp signal **26**. The complementary pulse signal **92** is approximately 180° out of phase with pulse signal **90**, and the ramp signal **26** is approximately 90° out of phase with pulse signal, as will be described below. The ramp signal is preferably a sawtooth signal, as shown in the Figure. The ramp signal **26** is compared with the output signal **24** (referred to herein as CMP) of the error amplifier **32**, through comparator **28**, thus generating signal **94**. The output signal **94** of the comparator **28** is likewise a 50% duty pulse delivered to C_Drive to initiate the turning on of Switch_C which, in turn, determines the amount of overlap between the switches B and C, and switches A and D. Its complimentary signal (phased approximately 180°) is applied to Switch_D, via D_Drive. It will be understood by those skilled in the art that circuits Drive_A–Drive_D are connected to the control lines (e.g., gate) of Switch_A–Switch_D, respectively, which permits each of the switches to controllably conduct, as described herein. By adjusting the amount of overlap between switches B, C and A, D, lamp-current regulation is achieved. In other words, it is the amount of overlapping in the conduction state of the pairs of switches that determines the amount of power processed in the converter. Hence, switches B and C, and switches A and D, will be referred to herein as overlapping switches.

"While not wishing to be bound by example, in this embodiment, B_Drive is preferably formed of a totem pole circuit, generic low-impedance op-amp circuit, or emitter follower circuit. D_Drive is likewise constructed. Since both A-Drive and C_Drive are not directly connected to ground (i.e., floating), it is preferred that these drives are formed of a boot-strap circuit, or other high-side drive circuitry known in the art. Additionally, as stated above, A_Drive and D_Drive include an inverter to invert (i.e., phase) the signal flowing from B_Drive and C_Drive, respectively."

High-efficiency operation is achieved through a zero-voltage-switching technique. The four MOSFETs (Switch_A-Switch_D) **80** are turned on after their intrinsic diodes (D1—D4) conduct, which provides a current flowing path of energy in the transformer/capacitor (TX1/C1) arrangement, thereby ensuring that a zero voltage is across the switches when they are turned on. With this controlled operation, switching loss is minimized and high efficiency is maintained.

The preferred switching operation of the overlapping switches **80** is shown with reference to the timing diagrams of FIGS. **2***a*–**2***f*. Switch_C is turned off at certain period of the conduction of both switches B and C (FIG. **2***f*). The current flowing in the tank (refer to FIG. **2**) is now flowing through diode D4 (FIG. **2***e*) in Switch_D, the primary of transformer, C1, and Switch_B, after Switch_C is turned off, thereby resonating the voltage and current in capacitor C1 and the transformer as a result of the energy delivered when switches B and C were conducting (FIG. **2***f*). Note that this condition must occur, since an instantaneous change in current direction of the primary side of the transformer would violate Faraday's Law. Thus, current must flow through D4 when Switch_C turns off. Switch_D is turned on after D4 has conducted. Similarly, Switch_B is turned off (FIG. **2***a*), the current diverts to Diode D1 associated with Switch_A before Switch_A is turned on (FIG. **2***e*). Likewise, Switch_D is turned off (FIG. **2***d*), and the current is now flowing now from Switch_A, through C1, the transformer primary and Diode D3. Switch_C is turned on after D3 has conducted (FIG. **2***e*). Switch_B is turned on after Switch_A is turned off which allows the diode D2 to conduct first before it is turned on. Note that the overlap of

turn-on time of the diagonal switches B,C and A,D determines the energy delivered to the transformer, as shown in FIG. *2f*.

In this embodiment, FIG. *2b* shows that the ramp signal **26** is generated only when Switch_A is turned on. Accordingly, Drive_A, which generates the ramp signal **26**, preferably includes a constant current generator circuit (not shown) that includes a capacitor having an appropriate time constant to create the ramp signal. To this end, a reference current (not shown) is utilized to charge the capacitor, and the capacitor is grounded (via, for example a transistor switch) so that the discharge rate exceeds the charge rate, thus generating the sawtooth ramp signal **26**. Of course, as noted above, this can be accomplished by integrating the pulse signal **90**, and thus, the ramp signal **26** can be formed using an integrator circuit (e.g., op-amp and capacitor).

In the ignition period, a pre-determined minimum overlap between the two diagonal switches is generated (i.e., between switches A,D and B,C). This gives a minimum energy from the input to the tank circuit including C1, transformer, C2, C3 and the CCFL load. Note that the load can be resistive and/or capacitive. The drive frequency starts at a predetermined upper frequency until it approaches the resonant frequency of the tank circuit and equivalent circuit reflected by the secondary side of the transformer, a significant amount of energy is delivered to the load where the CCFL is connected. Due to its high-impedance characteristics before ignition, the CCFL is subjected to high voltage from the energy supplied to the primary side. This voltage is sufficient to ignite the CCFL. The CCFL impedance decreases to its normal operating value (e.g., about 100 Kohm to 130 Kohm), and the energy supplied to the primary side based on the minimum-overlap operation is no longer sufficient to sustain a steady state operation of the CCFL. The output of the error amplifier **26** starts its regulating function to increase the overlap. It is the level of the error amplifier output determines the amount of the overlap. For example:

20 Referring to FIGS. *2b* and *2c* and the feedback loop **40** of FIG. **2**, it is important to note that Switch_C is turned on when the ramp signal **26** (generated by Drive_A) is equal to the value of signal CMP **24** (generated by error amplifier **32**), determined in comparator **28**. This is indicated as the intersection point **36** in FIG. *2b*. To prevent a short circuit, switches A,B and C,D must never be ON simultaneously. By controlling the CMP level, the overlap time between switches A,D and B,C regulates the energy delivered to the transformer. To adjust the energy delivered to the transformer (and thereby adjust the energy delivered to the CCFL load), switches C and D are time-shifted with respect to switches A and B, by controlling the error amplifier output, CMP **24**. As can be understood by the timing diagrams, if the driving pulses from the output of comparator **28** into switches C and D are shifted to the right by increasing the level of CMP, an increase in the overlap between switches A,C and B,D is realized, thus increasing the energy delivered to the transformer. In practice, this corresponds to the higher-lamp current operation. Conversely, shifting the driving pulses of switches C and D to the left (by decreasing the CMP signal) decreases the energy delivered.

To this end, error amplifier **32** compares the feedback signal FB with a reference voltage REF. FB is a measure of the current value through the sense resistor Rs, which is indicative of the total current through the load **20**. REF is a signal indicative of the desired load conditions, e.g., the desired current to flow through the load. During normal operation, REF=FB. If, however, load conditions are intentionally offset, for example, from a dimmer switch associated with an LCD panel display, the value of REF will increase/decrease accordingly. The compared value generates CMP accordingly. The value of CMP is reflective of the load conditions and/or an intentional bias, and is realized as the difference between REF and FB (i.e., REF–FB).

To protect the load and circuit from an open circuit condition at the load (e.g., open CCFL lamp condition during normal operation). the FB signal is also preferably compared to a reference value (not shown and different from the REF signal described above) at the current sense comparator **42**, the output of which defines the condition of switch **28**, discussed below. This reference value can be programmable, and/or user-definable, and preferably reflects the minimum or maximum current permitted by the system (for example, as may be rated for the individual components, and, in particular, the CCFL load). If the value of the feedback FB signal and the reference signal is within a permitted range (normal operation), the output of the current sense comparator is 1 (or, HIGH). This permits CMP to flow through switch **38**, and the circuit operates as described herein to deliver power to the load. If, however, the value of the FB signal and the reference signal is outside a predetermined range (open circuit or short circuit condition), the output of the current sense comparator is 0 (or, LOW), prohibiting the CMP signal from flowing through the switch **38**. (Of course, the reverse can be true, in which the switch triggers on a LOW condition). Instead a minimal voltage Vmin is supplied by switch **38** (not shown) and applied to comparator **28** until the current sense comparator indicates permissible current flowing through Rs. Accordingly, switch **38** includes appropriate programmable voltage selection Vmin for when the sense current is 0. Turning again to FIG. *2b*, the effect of this operation is a lowering of the CMP DC value to a nominal, or minimum, value (i.e., CMP=Vmin) so that a high voltage condition is not appearing on the transformer **TX1**. Thus, the crossover point **36** is shifted to the left, thereby decreasing the amount of overlap between complementary switches (recall Switch_C is turned ON at the intersection point **36**). Likewise, current sense comparator **42** is connected to the frequency generator **22** to turn the generator **22** off when the sense value is 0 (or some other preset value indicative of an open-circuit condition). The CMP is fed into the protection circuit **62**. This is to shut off the frequency sweeper **22** if the CCFL is removed during operation (open-circuit condition).

To protect the circuit from an over-voltage condition, the present embodiment preferably includes protection circuit **60**, the operation of which is provided below (the description of the over current protection through the current sense comparator **42** is provided above). The circuit **60** includes a protection comparator **62** which compares signal CMP with a voltage signal **66** derived from the load **20**. Preferably, voltage signal is derived from the voltage divider C2 and C3 (i.e., in parallel with load **20**), as shown in FIG. **2**. In the open-lamp condition, the frequency sweeper continues sweeping until the OVP signal **66** reaches a threshold. The OVP signal **62** is taken at the output capacitor divider C2 and C3 to detect the voltage at the output of the transformer TX1. To simplify the analysis, these capacitors also represent the lump capacitor of the equivalent load capacitance. The threshold is a reference and circuit is being designed so that the voltage at the secondary side of the transformer is greater than the minimum striking voltage (e.g., as may be required by the LCD panel) while less than the rated voltage of the transformer. When OVP exceeds the threshold, the frequency sweeper stops the frequency sweeping. Meanwhile,

the current-sense **42** detects no signal across the sense resistor Rs. Therefore the signal at **24**, the output of a switch block **38**, is set to be at minimum value v_{min} so that minimum overlap between switches A,C and B,D is seen. Preferably, a timer **64** is initiated once the OVP exceeds the threshold, thereby initiating a time-out sequence. The duration of the time-out is preferably designed according to the requirement of the loads (e.g., CCFLs of an LCD panel), but could alternately be set at some programmable value. Drive pulses are disabled once the time-out is reached, thus providing safe-operation output of the converter circuit. That is, circuit **60** provides a sufficient voltage to ignite the lamp, but will shut off after a certain period if the lamp is not connected to the converter, so that erroneous high voltage is avoided at the output. This duration is necessary since a non-ignited lamp is similar to an open-lamp condition.

FIGS. **3** and **3***a*–**3***f* depict another preferred embodiment of the DC/AC circuit of the present invention. In this embodiment, the circuit operates in a similar manner as provided in FIG. **2** and FIGS. **2***a*–**2***f*, however this embodiment further includes a phase lock loop circuit (PLL) **70** for controlling the frequency sweeper **22**, and a flip-flop circuit **72** to time the input of a signal into C_Drive. As can be understood by the timing diagrams, if the 50% driving pulses of switches C and D are shifted to the right by increasing the level of CMP, an increase in the overlap between switches A,C and B,D is realized, thus increasing the energy delivered to the transformer. In practice, this corresponds to the higher-lamp current operation (as may be required, e.g., by a manual increase in the REF voltage, described above). Conversely, shifting the driving pulses of switches C and D to the left (by decreasing the CMP signal) decreases the energy delivered. The phase-lock-loop circuit **70** maintains the phase relationship between the feedback current (through Rs) and tank current (through TX1/C1) during normal operation, as shown in FIG. **3**. The PLL circuit **70** preferably includes input signals from the tank circuit (C1 and the primary of TX1) signal **98** and Rs (FB signal, described above). Once the CCFL is ignited, and the current in the CCFL is detected through Rs, the PLL **70** circuit is activated which locks the phase between the lamp current and the current in the primary resonant tank (C1 and transformer primary). That is, the PLL is provided to adjust the frequency of the frequency sweeper **22** for any parasitic variations such as temperature effect, mechanical arrangement like wiring between the converter and the LCD panel and distance between the lamp and metal chassis of LCD panel that affect the capacitance and inductance. Preferably, the system maintains a phase difference of 180 degrees between the resonant tank circuit and the current through Rs (load current). Thus, irrespective of the particular load conditions and/or the operating frequency of the resonant tank circuit, the system finds an optimal operation point.

The operation of the feedback loop of FIG. **3** is similar to the description above for FIG. **2**. However, as shown in FIG. **3***b*, this embodiment times the output of an initiating signal through C_Drive through flip-flop **72**. For instance, during normal operation, the output of the error amplifier **32** is fed through the controlled switch block **38** (described above), resulting in signal **24**. A certain amount of overlap between switches A,C and B,D is seen through comparator **28** and flip-flop **72** which drives switches C and D (recall D_Drive produces the complementary signal of C_Drive). This provides a steady-state operation for the CCFL (panel) load. Considering the removal of the CCFL (panel) during the normal operation, CMP rises to the rail of output of the error amplifier and triggers the protection circuit immediately. This function is inhibited during the ignition period.

Referring briefly to FIGS. **3***a*–**3***f*, the triggering of switches C and D, through C-Drive and D_Drive, is, in this embodiment, alternating as a result of the flip-flop circuit **72**. As is shown in FIG. **3***b*, the flip-flop triggers every other time, thereby initiating C_Drive (and, accordingly, D_Drive). The timing otherwise operates in the same way as discussed above with reference to FIG. **2***a*–**2***f*.

Referring now to FIGS. **4***a*–**4***f*, the output circuit of FIG. **2** or **3** is emulated. For example, FIG. **4***a* shows that at 21V input, when the frequency sweeper approaches 75.7 KHz (0.5 us overlapping), the output is reaching 1.67 KVp-p. This voltage is insufficient to turn on the CCFL if it requires 3300Vp-p to ignite. As the frequency decreases to say 68 KHz, the minimum overlap generates about 3.9 KVp-p at the output, which is sufficient to ignite the CCFL. This is illustrated in FIG. **4***b*. At this frequency, the overlap increases to 1.5 us gives output about 1.9 KVp-p to operate the 130 Kohm lamp impedance. This has been shown in FIG. **4***c*. As another example, FIG. **4***d* illustrates the operation while the input voltage is 7V. At 71.4 KHz, output is 750Vp-p before the lamp is striking. As the frequency decreases, the output voltage increases until the lamp ignites. FIG. **4***e* shows that at 65.8 KHz, the output reaches 3500Vp-p. The regulation of the CCFL current is achieved by adjusting the overlap to support 130 Kohm impedance after ignition. The voltage across the CCFL is now 1.9 KVp-p for a 660Vrms lamp. This is also illustrated in FIG. **4***f*. Although not shown, the emulation of the circuit of FIG. **3** behaves in a similar manner.

It should be noted that the difference between the first and second embodiments (i.e., by the addition of the flip flop and the PLL in FIG. **3**) will not effect the overall operational parameters set forth in FIG. **4***a*–**4***f*. However, the addition of the PLL has been determined to account for non-ideal impedances that develop in the circuit, and may be added as an alternative to the circuit shown in FIG. **2**. Also, the addition of the flip-flop permits the removal of the constant current circuit, described above.

Thus, it is evident that there has been provided a high efficiency adaptive DC/AC converter circuit that satisfies the aims and objectives stated herein. It will be apparent to those skilled in the art that modifications are possible. For example, although the present invention has described the use of MOSFETs for the switched, those skilled in the art will recognize that the entire circuit can be constructed using BJT transistors, or a mix of any type of transistors, including MOSFETs and BJTs. Other modifications are possible. For example, the drive circuitry associated with Drive_B and Drive_D may be comprised of common-collector type circuitry, since the associated transistors are coupled to ground and are thus not subject to floating conditions. The PLL circuit described herein is preferably a generic PLL circuit **70**, as is known in the art, appropriately modified to accept the input signal and generate the control signal, described above. The pulse generator **22** is preferably a pulse width modulation circuit (PWM) or frequency width modulation circuit (FWM), both of which are well known in the art. Likewise, the protection circuit **62** and timer are constructed out of known circuits and are appropriately modified to operate as described herein. Other circuitry will become readily apparent to those skilled in the art, and all such modifications are deemed within the spirit and scope of the present invention, only as limited by the appended claims.

What is claimed is:

1. A DC to AC inverter circuit, comprising:

an input voltage source;

a plurality of switches arranged in a full bridge configuration wherein opposite corners of said full bridge configuration being selectively coupled to said voltage source;

a transformer having a primary side and a secondary side, said primary side being selectively coupled to said voltage source in an alternating fashion through said full bridge switch configuration;

a load coupled to said secondary side of said transformer;

a pulse generator circuit generating a first pulse signal for driving one of the corner switches of said full bridge configuration;

a feedback control loop circuit receiving a feedback signal indicative of power being supplied to the load and adapted to generate a second pulse signal for controlling the conduction state of a switch on the opposite corner of said switch being controlled by said first pulse signal, said second pulse signal having a first state which overlaps said first pulse signal to deliver an amount of power to said load determined by said feedback signal, and a second state which overlaps the first signal with a predetermined minimum overlap to deliver a predetermined minimum power to the load.

2. An inverter circuit as claimed in claim 1, said feedback control loop circuit comprises an error amplifier comparing said feedback signal to a predetermined reference signal and generating an error signal indicative of the difference between said feedback signal and said predetermined reference signal; a flow-through switch coupled to said error amplifier and having a first conduction state wherein the output of said switch comprises a DC signal indicative of said first state of said second pulse signal, and a second conduction state wherein the output of said switch comprises a DC signal indicative of said second state of said second pulse signal.

3. An inverter circuit as claimed in claim 2, further comprising a ramp signal generator circuit receiving said first pulse signal and generating a ramp signal approximately 180 degrees out phase from said first pulse signal, said feedback control loop circuit further comprises a comparator comparing said ramp signal to said DC output signal of said switch and generating said second pulse signal.

4. An inverter circuit as claimed in claim 3, wherein the intersection of said DC output signal and said ramp signal determines the overlap between said first and second pulse signal.

5. An inverter circuit as claimed in claim 2, further comprising protection circuitry comprising a current sense comparator, said current sense comparator comparing said feedback signal to a second reference signal; wherein if the compared value of said feedback signal and said second reference signal is within a predetermined range said current sense comparator generates a first control signal to control the conduction state of said switch corresponding to said first conduction state; and wherein if the compared value of said feedback signal is outside a predetermined range said current sense comparator generates a second control signal to control the conduction state of said switch corresponding to said second conduction state.

6. An inverter circuit as claimed in claim 5, further comprising a sense resistor coupled between said load and said secondary side of said transformer, said sense resistor generating said feedback signal.

7. An inverter circuit as claimed in claim 5, said protection circuitry further comprising an overvoltage protection circuit comprising a voltage comparator comparing a predetermined voltage reference to a voltage signal indicative of load voltage conditions and generating a voltage control signal.

8. An inverter circuit as claimed in claim 7, further comprising a pulse generator generating said first pulse signal having a 50% duty cycle, pulse generator receiving said voltage control signal and/or said control signal generated by said current sense comparator, said pulse generator shutting off if said voltage control signal and/or said control signal generated by said current sense comparator is indicative of an open lamp or short circuit condition at the load during operation.

9. An inverter as claimed in claim 2, wherein said reference signal represents desired load conditions.

10. An inverter as claimed in claim 5, wherein said second reference signal represents the minimum or maximum current permitted by said switches and/or said load.

11. An inverter as claimed in claim 7, wherein said third reference signal represents the maximum voltage at said secondary side of said transformer.

12. An inverter circuit comprising:

an input voltage source;

a full bridge circuit comprising a first pair of switches arranged at opposite corners of a full bridge circuit, and a second pair of switches arranged at other opposite corners of said full bridge circuit, said first and second pair of switches being selectively coupled to said input voltage source such that said first pair of switches defines a first conduction path and said second pair of switches defines a second conduction path;

a transformer having a primary side and a secondary side, said primary side selectively coupled to said input voltage source in an alternating fashion through said first and second conduction paths;

a load coupled to said secondary side of said transformer;

a pulse generator generating a first pulse signal for controlling the conduction state of one of said first pair of switches;

a feedback control loop circuit receiving a feedback signal indicative of power being supplied to said load and adapted to generate a second pulse signal for controlling the conduction state of a different one of said first pair of switches, said second pulse signal having a phase overlap with said first pulse signal to deliver power to said load only if said feedback signal is above a predetermined threshold.

13. An inverter as claimed in claim 12, wherein the amount of overlap between said first and second pulse signals determines the amount of power delivered to said load.

14. An inverter as claimed in claim 12, wherein if said feedback signal is below said predetermined threshold, said feedback loop generating said second pulse signal to have a minimum phase overlap with said first pulse signal to reduce power delivered to said load to a predetermined minimum amount.

15. An inverter as claimed in claim 12, further comprising a first driver circuit receiving said first pulse signal and generating a first complimentary pulse signal 180 degrees out of phase from said first pulse signal, said first complimentary pulse signal controlling the conduction state of one of said second pair of said switches; and a second driver receiving said second pulse signal and generating a second

complimentary pulse signal 180 degrees out of phase from said second pulse signal, said second complimentary pulse signal controlling the conduction state of the other of said second pair of said switches.

16. An inverter as claimed in claim **12**, wherein said first pulse signal comprises a PWM signal having approximately 50% duty cycle.

17. An inverter as claimed in claim **12**, said second pulse signal having a first state which overlaps said first pulse signal to deliver an amount of power to said load determined by said feedback signal, and a second state which overlaps the first signal with a predetermined minimum overlap to deliver a predetermined minimum power to the load.

18. A DC to AC inverter circuit comprising:

a plurality of switches arranged in a full bridge configuration wherein switches on opposite corners of said full bridge being controlled in an alternating fashion;

a pulse generator circuit generating a first pulse signal for driving one of the corner switches of said full bridge configuration; and

a feedback control loop circuit receiving a feedback signal indicative of power being supplied by said switches to a load, said feedback loop adapted to generate a second pulse signal for controlling the conduction state of a switch on the opposite corner of said switch being controlled by said first pulse signal, said second pulse signal having a first state which overlaps said first pulse signal to deliver an amount of power to said load determined by said feedback signal, and a second state which overlaps the first signal with a predetermined mininum overlap to deliver a predetermined minimum power to the load.

19. An inverter circuit comprising:

a full bridge circuit comprising a first pair of switches arranged at opposite corners of a full bridge circuit, and a second pair of switches arranged at other opposite corners of said full bridge circuit, said first and second pair of switches being selectively coupled to said input voltage source such that said first pair of switches defines a first conduction path and said second pair of switches defines a second conduction path;

a pulse generator generating a first pulse signal for controlling the conduction state of one of said first pair of switches;

a feedback control loop circuit receiving a feedback signal indicative of power being supplied to a load coupled to said switches, and adapted to generate a second pulse signal for controlling the conduction state of a different one of said first pair of switches, said second pulse signal having a phase overlap with said first pulse signal to deliver power to said load only if said feedback signal is above a predetermined threshold.

* * * * *

Exhibit B

FILED
FEB 11 2004
RICHARD W. WIEKING
CLERK, U.S. DISTRICT COURT
NORTHERN DISTRICT OF CALIFORNIA
OAKLAND

IN THE UNITED STATES DISTRICT COURT

FOR THE NORTHERN DISTRICT OF CALIFORNIA

02 MICRO INTERNATIONAL LIMITED, a Cayman Islands corporation,

Plaintiff,

v.

MONOLITHIC POWER SYSTEMS, INC., a California Corporation, and DOES 1 to 10,

Defendant.

MONOLITHIC POWER SYSTEMS, INC., a California Corporation,

Counterclaimant,

v.

02 MICRO INTERNATIONAL LIMITED, a Cayman Islands corporation, and 02 MICRO, INC., a California corporation,

Counterdefendants.

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Nos. C 00-4071 CW (EDL) and C 01-3995 CW

ORDER RE CROSS-MOTIONS FOR SUMMARY JUDGMENT AND MPS' MOTION TO STRIKE CONTRADICTORY ASSERTION IN 02 MICRO'S SECOND AMENDED COMPLAINT, 02 MICRO'S MOTION TO STRIKE UNAUTHORIZED AFFIRMATIVE DEFENSES IN MPS' ANSWER TO SECOND AMENDED COMPLAINT AND COUNTERCLAIM, 02 MICRO'S MOTION TO AMEND COMPLAINT AND REOPEN DISCOVERY REGARDING TRADE SECRET CLAIMS

The current motions arise from C 01-3995, in which Plaintiffs and Counterdefendants 02 Micro International Limited and 02 Micro,

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cc: EDL

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Inc. (collectively, 02 Micro) sue Monolithic Power Systems, Inc. (MPS) alleging infringement of U.S. Patent No. 6,259,615 (the '615 patent) and misappropriation of its trade secrets. MPS counterclaims, alleging invalidity and/or non-infringement of the '615 patent.

Presently before the Court are four separate motions in C 01-3995. First, 02 Micro moves for summary judgment. MPS opposes this motion and cross-moves for summary judgment. Second, MPS moves to strike a contradictory assertion in 02 Micro's second amended complaint. Third, 02 Micro moves to strike unauthorized affirmative defenses in MPS' answer to the second amended complaint. Fourth, 02 Micro moves to amend its second amended complaint and to re-open discovery to add additional trade secret claims. A hearing was held on these motions on November 21, 2003.[1]

Having considered all of the papers filed by the parties and oral argument on these motions, the Court GRANTS MPS' cross-motion for summary adjudication of non-infringement of the '615 patent, DENIES as moot 02 Micro's motion for summary adjudication of infringement of the '615 patent, DENIES both parties' motions for summary adjudication of trade secret misappropriation, DENIES MPS' motion to strike a contradictory assertion in 02 Micro's second amended complaint, GRANTS in part and DENIES in part 02 Micro's motion to strike unauthorized affirmative defenses in MPS' answer to the second amended complaint and GRANTS 02 Micro's motion to

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[1]For a summary of the issues discussed at the November 21 2003 hearing, and the issues still pending, see Docket nos. 534 and 540 in C 01-3995.

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amend its complaint and to reopen discovery regarding trade secret claims.

BACKGROUND

02 Micro holds the '615 patent. The '615 patent involves technology used to light laptop computer screens. Laptops are powered by batteries, which provide a direct current (DC) power source. The lamps used to illuminate laptop screens require an alternating current (AC) power source. The '615 patent solves this problem with a system that turns switches on and off to convert DC to AC. A transformer sends the AC to the "load," the lamp which illuminates the screen. '615 patent, 2:19-20. The system claimed in the '615 patent includes two pairs of switches. When one pair of switches is turned on, the circuit delivers power to the load along a path defined by the pair of switches. When the other pair of switches is turned on, the circuit delivers power to the load along a path defined by the other pair of switches. '615 patent at 5:6-19. The on-time of the switches is determined by feedback signals and pulse signals. '615 patent at 5:7-10. 02 Micro believes that twelve MPS drivers and demo boards infringe claims 1 and 18 of the '615 patent.

02 Micro also manufactures power supply controllers used in circuits which convert DC to AC. One such controller is the OZ960. 02 Micro alleges that the OZ960, boards containing the OZ960, and data sheets describing the OZ960 contain trade secrets. Wells Dec. Ex. A. 02 Micro contends that, in 2000, it released the data sheet and samples of the product to potential costumers who signed non-disclosure agreements, maintaining its secrecy. Wells Dec. Ex. B.

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02 Micro further alleges that MPS misappropriated these trade secrets by obtaining a copy of the confidential OZ960 data sheet and incorporating 02 Micro's trade secrets into its products. Wells Dec. Ex. K.

LEGAL STANDARD

I. Summary Judgment

Summary judgment is properly granted when no genuine and disputed issues of material fact remain, and when, viewing the evidence most favorably to the non-moving party, the movant is clearly entitled to prevail as a matter of law. Fed. R. Civ. P. 56; Celotex Corp. v. Catrett, 477 U.S. 317, 322-23 (1986); Eisenberg v. Ins. Co. of N. Am., 815 F.2d 1285, 1288-89 (9th Cir. 1987).

The moving party bears the burden of showing that there is no material factual dispute. Therefore, the court must regard as true the opposing party's evidence, if supported by affidavits or other evidentiary material. Celotex, 477 U.S. at 324; Eisenberg, 815 F.2d at 1289. The court must draw all reasonable inferences in favor of the party against whom summary judgment is sought. Matsushita Elec. Indus. Co. v. Zenith Radio Corp., 475 U.S. 574, 587 (1936); Intel Corp. v. Hartford Accident & Indem. Co., 952 F.2d 1551, 1558 (9th Cir. 1991).

Material facts which would preclude entry of summary judgment are those which, under applicable substantive law, may affect the outcome of the case. The substantive law will identify which facts are material. Anderson v. Liberty Lobby, Inc., 477 U.S. 242, 248 (1986).

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Where the moving party does not bear the burden of proof on an issue at trial, the moving party may discharge its burden of showing that no genuine issue of material fact remains by demonstrating that "there is an absence of evidence to support the nonmoving party's case." Celotex, 477 U.S. at 325. The moving party is not required to produce evidence showing the absence of a material fact on such issues, nor must the moving party support its motion with evidence negating the non-moving party's claim. Id.; see also Lujan v. Nat'l Wildlife Fed'n, 497 U.S. 871, 885 (1990); Bhan v. NME Hosps., Inc., 929 F.2d 1404, 1409 (9th Cir. 1991), cert. denied, 502 U.S. 994 (1991). If the moving party shows an absence of evidence to support the non-moving party's case, the burden then shifts to the opposing party to produce "specific evidence, through affidavits or admissible discovery material, to show that the dispute exists." Bhan, 929 F.2d at 1409. A complete failure of proof concerning an essential element of the non-moving party's case necessarily renders all other facts immaterial. Celotex, 477 U.S. at 323.

Where the moving party bears the burden of proof on an issue at trial, it must, in order to discharge its burden of showing that no genuine issue of material fact remains, make a prima facie showing in support of its position on that issue. See UA Local 343 v. Nor-Cal Plumbing, Inc., 48 F.3d 1465, 1471 (9th Cir. 1994). That is, the moving party must present evidence that, if uncontroverted at trial, would entitle it to prevail on that issue. See id.; see also Int'l Shortstop, Inc. v. Rally's, Inc., 939 F.2d 1257, 1264-65 (5th Cir. 1991). Once it has done so, the non-moving

party must set forth specific facts controverting the moving party's prima facie case. See UA Local 343, 48 F.3d at 1471. The non-moving party's "burden of contradicting [the moving party's] evidence is not negligible." Id. This standard does not change merely because resolution of the relevant issue is "highly fact specific." See id.

II. Motion to Strike

Pursuant to Federal Rule of Civil Procedure 12(f), the Court may strike from a pleading "any redundant, immaterial, impertinent or scandalous matter." Fed. R. Civ. Proc. 12(f). Rule 12(f) also allows a court to "order stricken from any pleading any insufficient defense." Id. The purpose of a Rule 12(f) motion is to avoid spending time and money litigating spurious issues. Fantasy, Inc. v. Fogerty, 984 F.2d 1524, 1527 (9th Cir. 1993), reversed on other grounds, 510 U.S. 517 (1994). Matter is immaterial if it has no essential or important relationship to the claim for relief pleaded. Id. Matter is impertinent if it does not pertain and is not necessary to the issues in question in the case. Id.

III. Motion to Amend

Federal Rule of Civil Procedure 15(a) provides that leave of the court allowing a party to amend its pleading "shall be freely given when justice so requires." Leave to amend lies within the sound discretion of the trial court, which discretion "must be guided by the underlying purpose of Rule 15 -- to facilitate decisions on the merits rather than on the pleadings or technicalities." United States v. Webb, 655 F.2d 977, 979 (9th

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Cir. 1981) (citations omitted). Thus, the rule's policy of favoring amendments to pleadings should be applied with "extreme liberality." Id.; DCD Programs, Ltd. v. Leighton, 833 F.2d 183, 186 (9th Cir. 1987) (citations omitted).

The Supreme Court has identified four factors relevant to whether a motion for leave to amend should be denied: undue delay, bad faith or dilatory motive, futility of amendment, and prejudice to the opposing party. Foman v. Davis, 371 U.S. 178, 182 (1962). The Ninth Circuit holds that these factors are not of equal weight; specifically, delay alone is insufficient ground for denying leave to amend. Webb, 655 F.2d at 980.

Prejudice to the opposing party is the most important factor. Jackson v. Bank of Hawaii, 902 F.2d 1385, 1387 (9th Cir. 1990). Prejudice typically arises where the opposing party is surprised with new allegations which require more discovery or will otherwise delay resolution of the case. See, e.g., Acri v. International Ass'n of Machinists & Aerospace Workers, 781 F.2d 1393, 1398-99 (9th Cir.), cert. denied, 479 U.S. 816 (1986). The party opposing the motion bears the burden of showing prejudice. DCD Programs, 833 F.2d at 186.

DISCUSSION

I. Infringement of the '615 Patent

02 Micro accuses twelve MPS drivers and demo boards of infringing claims 1 and 18 of the '615 patent. The accused products are chip numbers MP1011A, MP1012, MP1013, MP1015, MP1016, MP1018, MP1022A, MP1023, MP1024, MP1025, MP1026, and MP1027. MPS counterclaims and seeks a finding of non-infringement and/or

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invalidity of the '615 patent. 02 Micro now moves for summary adjudication that MPS infringes the '615 patent and on MPS' invalidity contentions. MPS brings a cross-motion for summary adjudication on the same issues.

A. MPS' Cross-Motion for Summary Adjudication of Non-Infringement

Claim 1 of the '615 patent claims, in part, "a feedback control loop circuit receiving a feedback signal indicative of power being supplied to said load, and adapted to generate a second signal pulse signal for controlling the conduction state of said second plurality of switches only if said feedback signal is above a predetermined threshold." '615 patent at 10:67-11:5. Claim 18 has a similar limitation. Id. at 12:56-64. "Only if" modifies "controlling." '615 Claim Construction Order at 13. In its Final Infringement Contentions, 02 Micro alleges that MPS devices infringe the "only if" limitation. In order to determine whether a device infringes the "only if" limitation, one must compare the feedback signal to the threshold in the allegedly infringing devices. The present dispute emerges out of 02 Micro's various theories for measuring the feedback signal and threshold.

In its Final Infringement Contentions, 02 Micro compared the feedback signal to the threshold under an "I sense" theory, using units of current to discuss the signals. Barclay Dec. Ex. H at 5-6. MPS' expert opined that under the I sense theory, MPS products do not practice the "only if" limitation because the pulse signal controls the conduction state of the switches both when I sense is above and when I sense is below the Bright pin. Franklin Dec Ex. D at ¶ 15-21.

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However, at the deadline for disclosing expert reports, 02 Micro did not offer any evidence to refute MPS' expert on its own I sense theory. 02 Micro's expert, Dr. Erickson, did not opine on infringement on the I sense theory. Instead, Dr. Erickson opined only on a second and different theory, the "open lamp" theory, which compared the feedback signal to the threshold in voltage. Erickson Dec. Ex. C at 21-23. Now, after the close of discovery and the deadline for disclosure of expert reports, 02 Micro advances a third theory of infringement. 02 Micro's third theory, the "V sense" theory, compares the feedback signal to the threshold in measurements of voltage. However, 02 Micro has no evidence in the record supporting the V sense theory.

02 Micro opposes MPS' motion for summary judgment of non-infringement of the '615 patent on two grounds. First, 02 Micro offers supplemental expert testimony opining on the V sense theory. Erickson Dec. at ¶¶ 10-14; Lin Dec. at ¶¶ 5-7. 02 Micro argues that it should be permitted to supplement its expert report because MPS allegedly broke an oral agreement to allow 02 Micro to offer a supplemental report. However, 02 Micro's motion to amend its Final Invalidity Contentions in order to supplement its infringement theory has already been twice denied on these grounds. See Docket nos. 175 and 281. Second, 02 Micro argues that the V sense and I sense theories merely use different terms to describe MPS' alleged infringement. Even if the Court considers the supplemental expert testimony of Dr. Erickson and Dr. Lin, who opine that the V sense theory is identical to the I sense theory, 02 Micro still fails to meet its burden of providing evidence of infringement. The V sense

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theory and I sense theory express different ideas. One makes the "only if" comparison in units of current, and the other in units of voltage.

Because 02 Micro has failed to support its V sense theory with evidence, it has not met its burden of producing some evidence that MPS meets the "only if" limitations of claim 1 and 18 of the '615 patent. The Court GRANTS MPS' cross-motion for summary adjudication of non-infringement of the '615 patent.

B. 02 Micro's Motion for Summary Judgment of Infringement

Because the Court grants MPS' motion for summary adjudication of non-infringement, the Court need not address 02 Micro's motion for summary judgment of infringement of the '615 patent. It is DENIED as moot. In addition, MPS has agreed that if the Court granted its motion for summary adjudication of non-infringement of the '615 patent, it would withdraw its arguments that the '615 patent is invalid because of anticipation. Accordingly, the Court need not address those arguments either.

II. Cross Motions for Summary Judgment of 02 Micro's Trade Secret Claim

02 Micro claims that MPS misappropriated the trade secrets articulated in its preliminary data sheet on its OZ960 power supply controller. Wells Dec. Ex. A, (Docket no. 218). MPS asserts three arguments in response. First, MPS contends that 02 Micro has not identified the alleged trade secrets with adequate specificity to show that they actually exist. Second, MPS argues that 02 Micro did not make reasonable efforts to maintain the secrecy of any trade secrets. Third, MPS contends that 02 Micro cannot show that

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MPS made use of its alleged trade secrets. 02 Micro moves for summary judgment on its trade secret claim, and MPS cross-moves.

Misappropriation of a trade secret occurs when a defendant discloses or makes use of a plaintiff's trade secret without express or implied consent, and the defendant: (1) used improper means to acquire knowledge of the trade secret; or (2) at the time of the disclosure or use, knew or had reason to know that its knowledge of the trade secret was (a) derived from or through a person who had utilized improper means to acquire it; (b) acquired under circumstances giving rise to a duty to maintain its secrecy or limit its use; or (c) derived from or through a person who owed a duty to the owner to maintain its secrecy or limit its use. Cal. Civ. Code § 3426.1(b)(1).

A. Identity of the Information

The threshold issue is whether 02 Micro has demonstrated that it possesses trade secrets at all. A trade secret plaintiff cannot survive a defendant's motion for summary judgment if it fails to identify its alleged secrets with sufficient specificity so that the reviewing court can test whether the information is actually secret or is instead in the public domain. See Imax Corp. v. Cinema Tech., Inc., 152 F.3d 1161, 1164-67 (9th Cir. 1998). The parties agree that on October 31, 2003, subsequent to the briefing of MPS's cross-motion, 02 Micro submitted a statement identifying its trade secrets with more specificity. At the hearing on these motions, MPS conceded that 02 Micro's subsequent identification statement moots its argument that the trade secrets were not adequately identified.

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B. Secrecy of the Information

A trade secret plaintiff must make reasonable efforts to maintain secrecy. Cal. Civ. Code § 3426.1(d)(2). Communications disclosed to customers without non-disclosure agreements and/or placed in the stream of commerce are not trade secrets. VSL Corp. v. General Tech. Inc., 44 U.S.P.Q. 1301, 1303 (N.D. Cal. 1997); Futurecraft Corp. v. Clary Corp., 205 Cal. App. 2d 279, 282-83, 289 (1962). 02 Micro asserts that it made reasonable efforts to keep secret the allegedly misappropriated information. However, MPS contends that 02 Micro actually released to customers the data sheets containing the alleged trade secrets without acquiring non-disclosure agreements.

There is a genuine dispute of material fact as to the secrecy of the information. 02 Micro offers evidence that it exercised reasonable efforts to protect its trade secrets. It is undisputed that the documents in question were labeled "confidential" and "NOT FOR PUBLIC RELEASE." Wells Dec. Ex. F. at 119:13-120:5; Wells Rep. Dec. Ex. B at 263:12-264:14, 268:17-269:2. 02 Micro offers evidence that it required its customers and potential customers to sign non-disclosure agreements before releasing data sheets. Wells Rep. Dec. Exs. E-H. 02 Micro relies on testimony that its normal practice was to require every potential customer to sign a non-disclosure agreement before releasing any data sample, and that it refused to sell 02 Micro products to any customer who refused to sign a non-disclosure agreement. Wells Dec. Ex. H 126:3-9; 135:14-21.

MPS cites evidence which indicates a dispute whether 02 Micro

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made reasonable efforts to maintain secrecy. Many of 02 Micro's witnesses cannot recall whether or not they required customers to sign non-disclosure agreements. Graves Dec. Ex. 46. MPS points out that while twenty five companies likely received the datasheet advertising the OZ960, 02 Micro has produced non-disclosure agreements for no more than five of these companies. Wells Dec. Exs. E-G, I.

C. Use of the Information

MPS offers evidence that it did not use 02 Micro's alleged trade secrets in its technology or marketing efforts, Moyer Trade Secret Dec. at ¶¶ 6-15, and contends that there is no evidence that it did use 02 Micro's alleged trade secrets. 02 Micro offers evidence that MPS distributed a misappropriated 02 Micro data sheet to its product designers, who used information about 02 Micro's product to improve the transformer design in MPS products. Wells Opp. Dec. Ex. D; Ex. E at 334:5-340:8. This evidence demonstrates a dispute whether MPS used the alleged trade secrets.

Because there is a dispute of material fact as to both the secrecy and the use of the information, the Court DENIES 02 Micro's motion for summary judgment of trade secret misappropriation and DENIES MPS' cross-motion for summary judgment on 02 Micro's trade secret claim.

III. MPS' Motion to Strike Contradictory Assertion in the Second Amended Complaint in C 01-3995

02 Micro was previously granted leave to amend its complaint in C 01-3995 to add additional trade secrets to its trade secret misappropriation claim. In its First Amended Complaint (FAC), 02

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Micro asserted, "Before the issuance of the '615 patent, 02 Micro's trade secrets were not generally known to the public or to 02 Micro's competitors." FAC ¶ 14. 02 Micro repeated this assertion word-for-word in the proposed Second Amended Complaint (SAC) it submitted to the Court as an attachment to its previous motion for leave to amend. Then, in the SAC actually filed, 02 Micro changed the language of ¶ 14, adding the sentence, "Some of these trade secrets were not disclosed in the '615 patent." MPS now moves to strike this additional sentence in ¶ 14 of the SAC.

The Court DENIES MPS' motion to strike. The additional sentence in ¶ 14 of the SAC does not, as MPS asserts, contradict the version of ¶ 14 submitted in the proposed SAC. MPS asserts that the added sentence contradicts 02 Micro's implicit admission in the FAC that any alleged trade secrets at issue became generally known to the public upon the June, 2001 publication of the '615 patent. However, 02 Micro did not make such an implicit admission. Stating that trade secrets were not generally known before a certain date does not necessarily concede that all of the trade secrets were generally known after that date.

Although ¶ 14 of 02 Micro's SAC deviates from the proposed SAC that the Court had allowed it to file, the Court will allow it. It describes the additional trade secrets that the Court had allowed it to allege in its SAC. MPS' motion to strike is DENIED.

IV. 02 Micro's Motion to Strike Unauthorized Affirmative Defenses in MPS' Answer to Second Amended Complaint

In its answer to 02 Micro's FAC in C 01-3995, MPS raised seven affirmative defenses. 02 Micro subsequently was granted leave to

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file a SAC. When MPS filed its answer to the SAC, it added six additional "affirmative defenses" not raised in its previous answer: (1) Failure to Comply with California Code of Civil Procedure § 2019(d); (2) Failure to Conduct Pre-Lawsuit Investigation; (3) Lawful Receipt of Information; (4) Independent Derivation; (5) Competition Privilege; and (6) Estoppel by Prior Admission. 02 Micro argues that these should be stricken.

MPS admits that, although the new allegations appeared in the "affirmative defenses" section of its answer, the first five of the new allegations listed above are not affirmative defenses at all. Rather, they are allegations of deficiencies in 02 Micro's trade secret claims. Because the first five of the new allegations are not affirmative defenses, they are inappropriately set out in the "affirmative defenses" section of MPS' answer. Accordingly, the Court GRANTS 02 Micro's motion to strike the first five additional affirmative defenses. Although the Court orders such allegations stricken from the "affirmative defenses" section of the answer, the Court does not reject the underlying theories articulated in the purported affirmative defenses.

MPS argues that its sixth additional affirmative defense, Estoppel by Prior Admission, is properly asserted without leave of the Court because it addresses the new assertion raised by 02 Micro in ¶ 14 of the SAC. Because the Court denies MPS' motion to strike the new assertion in 02 Micro's SAC, 02 Micro's motion to strike the sixth additional affirmative defense is DENIED.

V. 02 Micro's Motion to Amend Complaint in 01-3995 and Re-Open Discovery Regarding Trade Secret Claims

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In determining whether to allow amendment, the Court must consider undue delay, bad faith or dilatory motive, futility of amendment, and prejudice to the opposing party. Foman v. Davis, 371 U.S. 178, 182 (1962). Because here the trade secret claims are alleged as supplemental to 02 Micro's patent claims, the Court must also consider the jurisdictional question of whether the additional trade secret claims arise from the same transaction or occurrence as the patent claims.

A. Jurisdiction

MPS contends that the Court does not have subject matter jurisdiction over the proposed additional claims. The Court rejects this argument. The current trade secret claims are based on data sheets for 02 Micro's product, the OZ960. 02 Micro contends that MPS misappropriated 02 Micro's data sheets which contained trade secrets. The proposed new claims are based on data sheets for different 02 Micro products, including the OZ9RC, OZ1RC and OZ9RR. 02 Micro claims to have discovered that MPS misappropriated its trade secrets in the OZ9RC, OZ1RC and OZ9RR data sheets after reviewing MPS' June 30, 2003 production of emails.

MPS argues the claims are not related because they are based on actions taken at a different point in time with respect to different products. However, the proposed new claims arise out of an alleged pattern of behavior by MPS. The proposed new claims also involve overlapping technology, and testimony by the same witnesses as the current claims. Thus, the Court finds that it has supplemental jurisdiction over the trade secret claims regarding

the OZ9RC, OZ1RC and OZ9RR data sheets.

B. Undue Delay, Bad Faith, Futility and Prejudice

02 Micro did not unduly delay bringing these additional trade secret violation claims. It asserted these claims immediately after it reviewed MPS' email production which it argues revealed the violations.

MPS argues that it would be prejudiced by the delay that would be caused by accommodating 02 Micro's additional claims. However, MPS has not met its burden to show prejudice. Many of the concerns MPS raised about this delay are now moot. At the time this motion was briefed, trial was set for February 2, 2004. Since then, the parties have stipulated to a later trial date. Accordingly, the Court GRANTS 02 Micro's motion to amend the complaint in C 01-3995 and to re-open discovery with regard to the new trade secret claims.

CONCLUSION

For the foregoing reasons, the Court GRANTS MPS' cross-motion for summary adjudication of non-infringement of the '615 patent as set forth above. (Docket no. 456) The Court DENIES as moot 02 Micro's motion for summary adjudication of infringement of the '615 patent. (Docket no. 428). The Court DENIES both 02 Micro's motion and MPS' cross-motion for summary adjudication of trade secret misappropriation. (Docket nos. 428 and 456). The Court DENIES MPS' motion to strike the contradictory assertion in 02 Micro's second amended complaint. (Docket no. 397). The Court GRANTS in part and DENIES in part 02 Micro's motion to strike unauthorized affirmative defenses in MPS' answer to the second amended complaint

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and counterclaim. (Docket no. 470).

02 Micro's motion to amend the complaint and reopen discovery regarding trade secret claims is GRANTED. (Docket no. 498). 02 Micro may file a third amended complaint in C 01-3995, in accordance with this order, within five days of the date of this order. MPS shall answer no later than twenty days from the date the third amended complaint is filed, or it may rest on its prior answer. The parties may conduct additional discovery necessitated by the amended complaint. The parties shall attempt to agree on the scope and schedule for this discovery. If the parties are unable to agree, they shall seek a ruling from the Magistrate Judge.

IT IS SO ORDERED.

Dated: FEB 11 2004

CLAUDIA WILKEN
United States District Judge

Copies mailed to counsel
as noted on the following page

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