EXHIBIT 2

File History Report

☐ Paper number _____ is missing from the United States Patent Trademark Office's copy of the file History. No additional information is available.

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- ☐ **PTO 1449**
- ☐ **PTO 892**
- ☐ **PTO 948**
- ☐ **PTO 1474**
- ☐ **Assignment**
- ☐ **Cover page**

Additional comments: Wrapper Jacket 7203788

7203788

USB-TO-VGA CONVERTER

Transaction History

Date	Transaction Description
12/11/2002	Initial Exam Team nn
12/14/2002	IFW Scan & PACR Auto Security Review
1/27/2003	Application Dispatched from OIPE
1/27/2003	Application Is Now Complete
2/11/2003	Case Docketed to Examiner in GAU
12/16/2003	Case Docketed to Examiner in GAU
5/24/2004	IFW TSS Processing by Tech Center Complete
11/30/2004	Case Docketed to Examiner in GAU
3/16/2005	Mail Non-Final Rejection
3/16/2005	Non-Final Rejection
6/16/2005	Response after Non-Final Action
6/21/2005	Date Forwarded to Examiner
8/31/2005	Final Rejection
9/1/2005	Mail Final Rejection (PTOL - 326)
1/17/2006	Request for Continued Examination (RCE)
1/17/2006	Request for Extension of Time - Granted
1/17/2006	Workflow - Request for RCE - Begin
1/26/2006	Date Forwarded to Examiner
1/26/2006	Date Forwarded to Examiner
1/26/2006	DISPOSAL FOR A RCE/CPA/129 (express abandonment if CPA)
3/1/2006	Examiner Interview Summary Record (PTOL - 413)
3/3/2006	Supplemental Response
3/29/2006	Date Forwarded to Examiner
4/24/2006	Miscellaneous Communication to Applicant - No Action Count
5/12/2006	Notice of Allowance Data Verification Completed
5/15/2006	Mail Miscellaneous Communication to Applicant
5/16/2006	Mail Notice of Allowance
6/13/2006	Information Disclosure Statement considered
6/13/2006	Reference capture on IDS
6/13/2006	Information Disclosure Statement (IDS) Filed
6/13/2006	Information Disclosure Statement (IDS) Filed
6/26/2006	Miscellaneous Communication to Applicant - No Action Count
6/29/2006	Mail Miscellaneous Communication to Applicant
8/16/2006	Information Disclosure Statement considered
8/16/2006	Reference capture on IDS
8/16/2006	Information Disclosure Statement (IDS) Filed
8/16/2006	Information Disclosure Statement (IDS) Filed
8/16/2006	Request for Continued Examination (RCE)
8/16/2006	Workflow - Request for RCE - Begin

8/25/2006	Date Forwarded to Examiner
8/25/2006	DISPOSAL FOR A RCE/CPA/129 (express abandonment if CPA)
10/12/2006	Notice of Allowance Data Verification Completed
10/23/2006	Mail Notice of Allowance
11/1/2006	Issue Fee Payment Verified
11/1/2006	Issue Fee Payment Received
11/6/2006	Application Is Considered Ready for Issue
2/6/2007	Pubs Case Remand to TC
2/20/2007	TC Return to Pubs
2/27/2007	Case Docketed to Examiner in GAU
3/6/2007	Dispatch to FDC
3/21/2007	Issue Notification Mailed
4/10/2007	Recordation of Patent Grant Mailed
4/10/2007	Patent Issue Date Used in PTA Calculation

Search Notes	Application No.	Applicant(s)
	10/315,013	LIU, PEI-CHUNG
	Examiner	Art Unit
	Kim T. Huynh	2112

SEARCHED			
Class	Subclass	Date	Examiner
710	315	3/5/2005	KH
710	22	3/5/2005	KH
710	308	3/5/2005	KH
710	310	3/5/2005	KH
710	100	8/22/2005	KH
710	305-306	8/22/2005	KH

INTERFERENCE SEARCHED			
Class	Subclass	Date	Examiner

SEARCH NOTES (INCLUDING SEARCH STRATEGY)		
	DATE	EXMR
East search uspat, uspgpub, epo, jpo, derwent	3/5/2005	KH
Updated prior search	8/22/2005	KH

U.S. Patent and Trademark Office

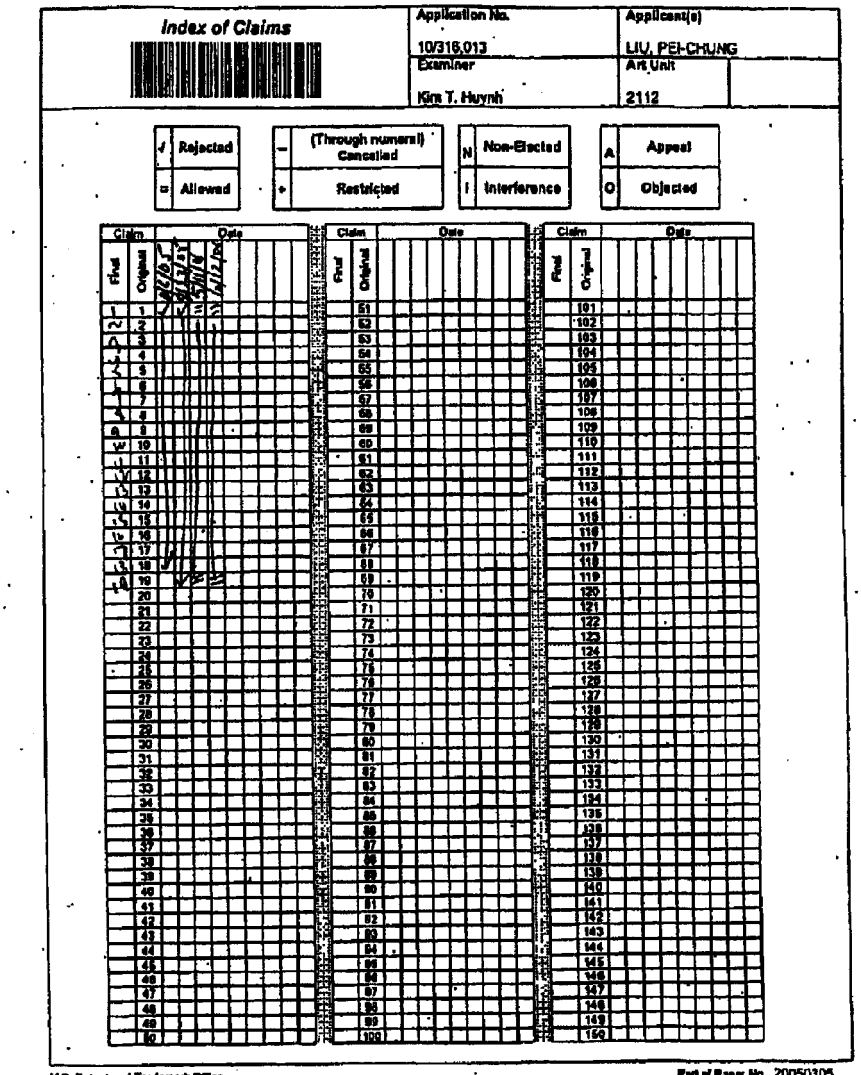
Part of Paper No. 20050305

Index of Claims

Application No.	Applicant(s)
10/316,013	LIU, PEI-CHUNG
Examiner	**Art Unit**
Kim T. Huynh	2112

√	Rejected	–	(Through numeral) Cancelled	N	Non-Elected	A	Appeal
=	Allowed	+	Restricted	I	Interference	O	Objected

| Claim | | Date | | | | | | |



Index of Claims	Application No.	Applicant(s)
	10/316,013	LIU, PEI-CHUNG
	Examiner	Art Unit
	Kim T. Huynh	2112

√	Rejected	–	(Through numeral) Cancelled	N	Non-Elected	A	Appeal
=	Allowed	+	Restricted	I	Interference	O	Objected

Claim Final	Claim Original	Date	Claim Final	Claim Original	Date	Claim Final	Claim Original	Date
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3	3	11/5/11		53			103	
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U.S. Patent and Trademark Office

Part of Paper No. 20050305

Issue Classification	Application/Control No. 10/316,013	Applicant(s)/Patent under Reexamination LIU, PEI-CHUNG
	Examiner Kim T. Huynh	Art Unit 2112

ISSUE CLASSIFICATION

ORIGINAL CLASS	ORIGINAL SUBCLASS	INTERNATIONAL CLASSIFICATION CLAIMED	NON-CLAIMED
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CROSS REFERENCES					
CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)				
710	107	100	~~365.200~~	/	/
710	305	306		/	/
				/	/
				/	/
				/	/

KH
Kim T. Huynh 5/11/06
(Assistant Examiner) (Date)

REHANA PERVEEN
SUPERVISORY PATENT EXAMINER
(Primary Examiner) (Date) 10/12/06

(Legal Instruments Examiner) (Date) 10-12-06

Total Claims Allowed: 19

O.G. Print Claim(s)	O.G. Print Fig.
1	3

☒ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

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US007203788B2

(12) **United States Patent**
Liu

(10) **Patent No.: US 7,203,788 B2**
(45) **Date of Patent: Apr. 10, 2007**

(54) **USB-TO-VGA CONVERTER**

(75) Inventor: **Pei Chung Liu**, Chungtlo (TW)

(73) Assignee: **Magic Control Technology Corporation**, Taipei (TW)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 392 days.

(21) Appl. No.: **10/316,013**

(22) Filed: **Dec. 11, 2002**

(65) **Prior Publication Data**

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(51) **Int. Cl.**
G06F 13/36 (2006.01)

(52) **U.S. Cl.** **710/315**; 710/107; 710/100; 710/305; 710/306

(58) **Field of Classification Search** 710/315, 710/22, 308, 310, 100, 305–306
See application file for complete search history.

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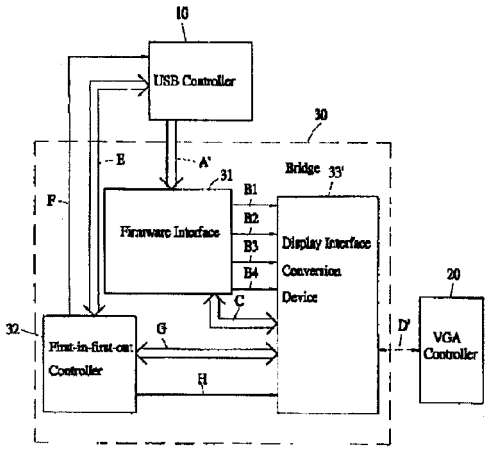
Primary Examiner—Rehana Perveen
Assistant Examiner—Kim T. Huynh
(74) *Attorney, Agent, or Firm*—Rosenberg, Klein & Lee

(57) **ABSTRACT**

A USB-to-VGA converter includes a USB controller connectable to a USB port of a computer for receiving USB based display signals from the computer, a VGA controller connectable to a display device for conveying VGA signals to the display device and a bridge connected between the USB controller and the VGA controller. The bridge receives a bus control command from the USB controller and issues a first-in-first-out control signal to the USB controller to receive the USB based display signals from the USB controller in a first-in-first-out manner. The bridge circuit converts the USB based display signals into corresponding VGA signals and forwarding the VGA signals to the VGA controller, which in turn applies the VGA signals to the display device. No display interface card is required inside the host computer for generation of the VGA signals.

19 Claims, 6 Drawing Sheets



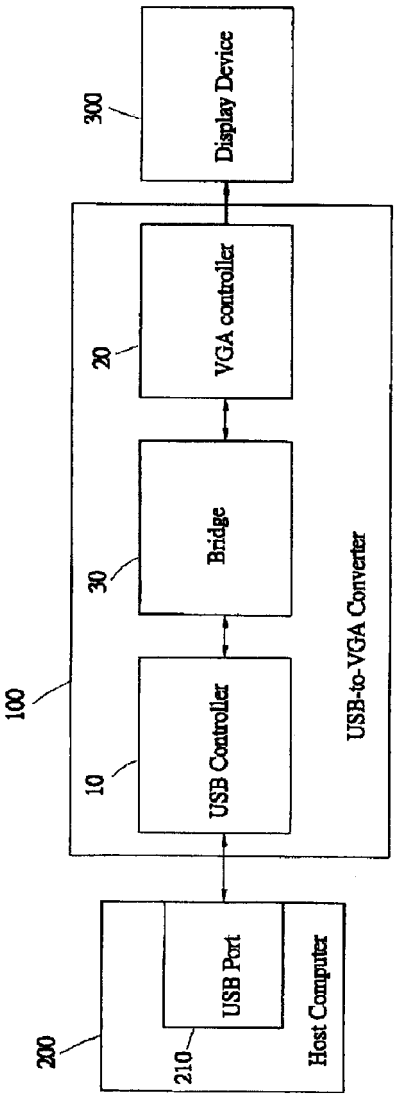

300
Display Device
20
VGA controller
30
Bridge
100
USB Controller
10
USB-to-VGA Converter
200
USB Port
210
Host Computer

FIG.1

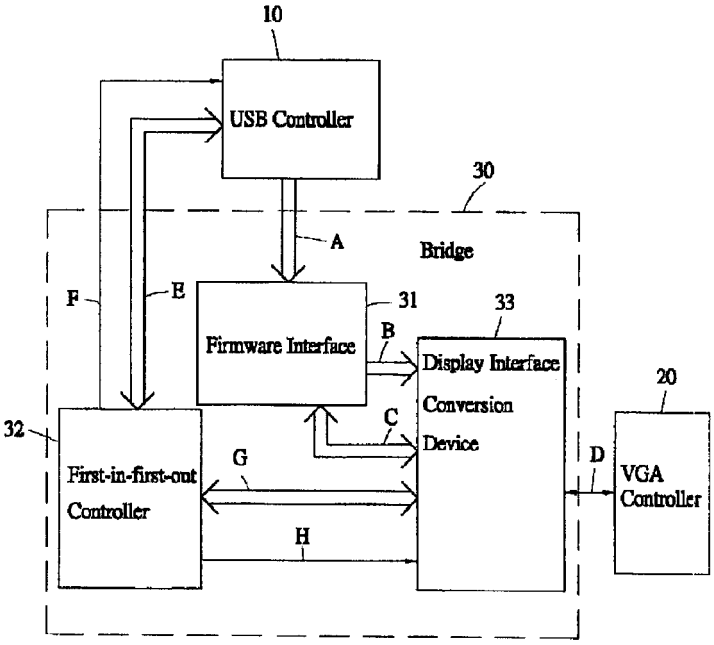

10
USB Controller
30
A
Bridge
F
E
31
33
Firmware Interface
B
Display Interface
Conversion
Device
20
32
C
First-in-first-out
Controller
G
D
VGA
Controller
H

FIG.2

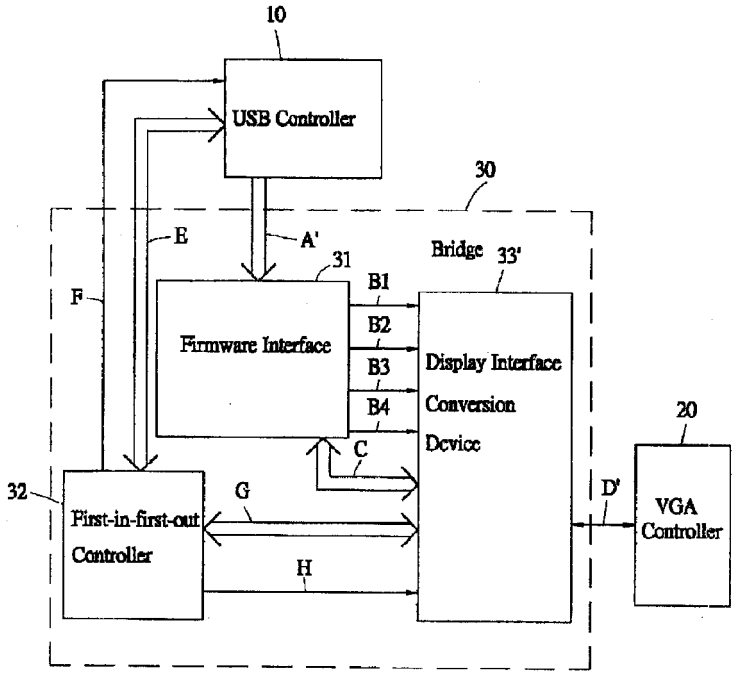

10
USB Controller
30
E
A'
Bridge
33'
31
B1
F
Firmware Interface
B2
B3
Display Interface
Conversion
Device
B4
20
C
32
G
D'
VGA
Controller
First-in-first-out
Controller
H

FIG.3

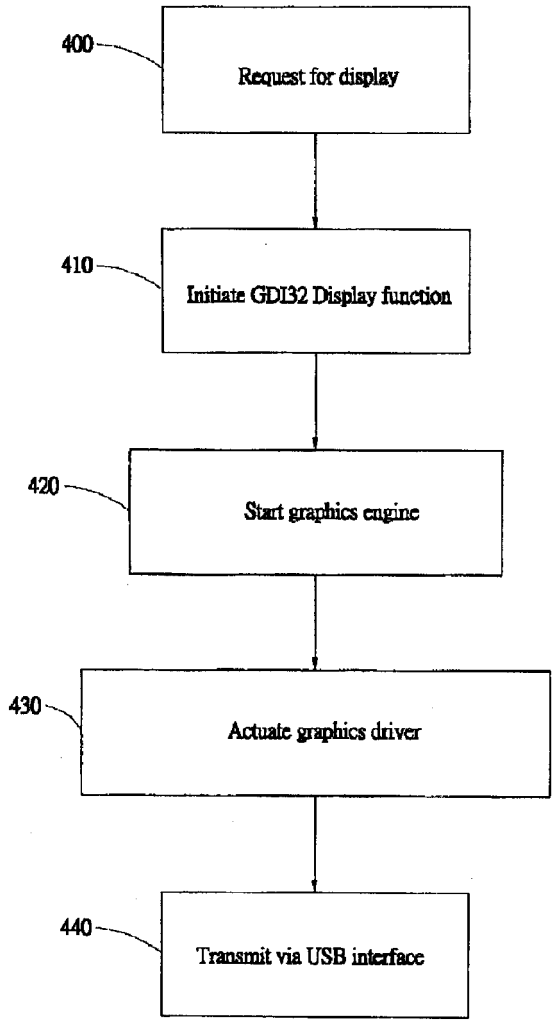

400
Request for display
410
Initiate GDI32 Display function
420
Start graphics engine
430
Actuate graphics driver
440
Transmit via USB interface

FIG.4

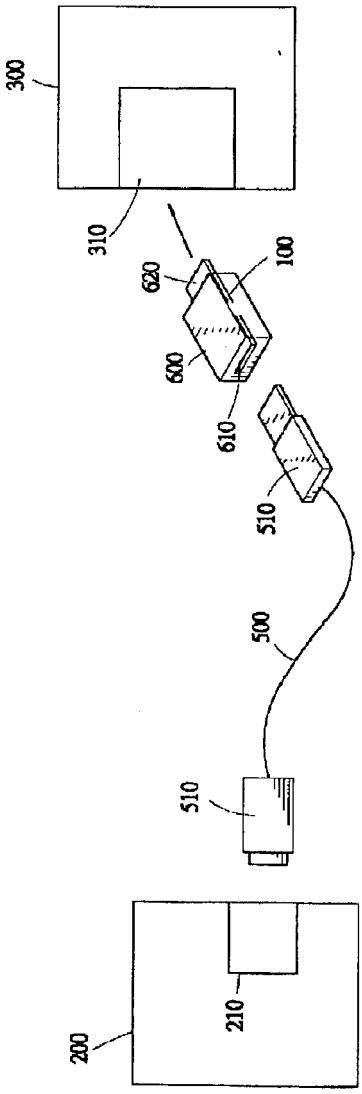


FIG.5

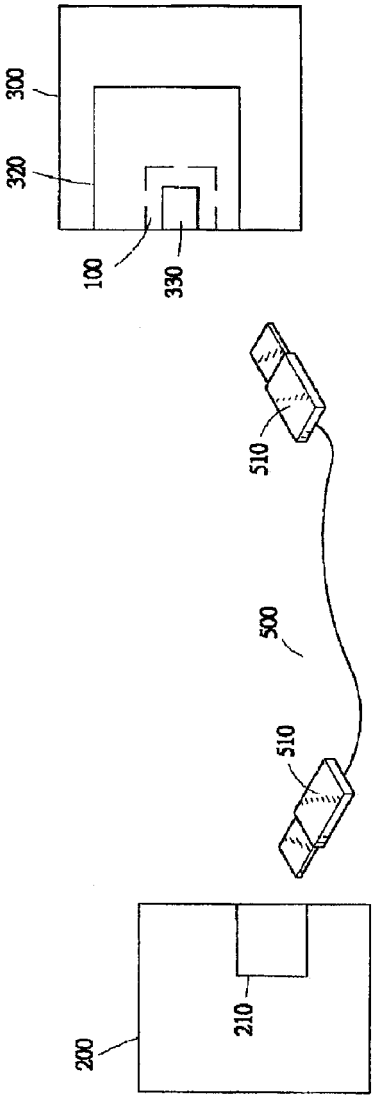


FIG.6

USB-TO-VGA CONVERTER

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates generally to a USB (Universal Serial Bus) to VGA (Video Graphics Array) converter, and in particular to a USB-to-VGA converter connectable between a USB port of a computer and a VGA display device.

2. The Related Art

A computer system comprises a display device connected to a host machine of the computer system for receiving display signals from the host computer and displaying messages associated with the display signals. The connection between the display device and the host computer is provided by an interface circuit built in the host computer, such as a PCI (Peripheral Component Interconnect) display interface and an AGP (Accelerated Graphics Port) display interface. A display interface card is mounted on a main board of the host computer for transmission of VGA signals to the display device. The display interface card occupies a portion of the limited space inside the host computer and in addition, increases the overall costs of the computer system. The display interface card is often connected to the display device by a cable for transmission of the display signals. The cable is adverse to the management of peripheral devices of the computer system and limits the distance that the display signals can be transmitted therethrough.

SUMMARY OF THE INVENTION

Thus, an object of the present invention is to provide a USB-to-VGA converter which converts USB based display signals issued from a host computer into VGA signals that can be received and recognized by a display device whereby image to be displayed can be transmitted from the host computer in USB form.

Another object of the present invention is to provide a USB-to-VGA converter that converts USB based display signals from a host computer into VGA signals in a first-in-first-out manner for display in a VGA display device.

A further object of the present invention is to provide a USB-to-VGA converter that allows for direct transmission of USB signals from a host computer to a display device without adding any display interface card inside the host computer.

To achieve the above objects, in accordance with the present invention, there is provided a USB-to-VGA converter comprising a USB controller connectable to a USB port of a computer for receiving USB based display signals from the computer, a VGA controller connectable to a display device for conveying VGA signals to the display device and a bridge connected between the USB controller and the VGA controller. The bridge receives a bus control command from the USB controller and issues a first-in-first-out control signal to the USB controller to receive the USB based display signals from the USB controller in a first-in-first-out manner. The bridge circuit converts the USB based display signals into corresponding VGA signals and forwarding the VGA signals to the VGA controller, which in turn applies the VGA signals to the display device. No display interface card is required inside the host computer for generation of the VGA signals.

BRIEF DESCRIPTION OF THE DRAWINGS

The present invention will be apparent to those skilled in the art by reading the following description of preferred embodiments thereof, with reference to the attached drawings, in which.

FIG. 1 is a system block diagram of a USB-to-VGA converter constructed in accordance with the present invention;

FIG. 2 is a block diagram of a bridge circuit of the USB-to-VGA converter of the present invention,

FIG. 3 is a block diagram of a bridge circuit of the USB-to-VGA converter in accordance with a different embodiment of the present invention;

FIG. 4 is a flow chart illustrating a process for a host computer to issue USB display signals to a USB controller;

FIG. 5 is a schematic view illustrating an application of the USB-to-VGA converter in connecting a display device to a host computer; and

FIG. 6 is a schematic view illustrating a different application of the USB-to-VGA converter in connecting a display device to a host computer.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

With reference to the drawings and in particular to FIG. 1, a USB-to-VGA converter constructed in accordance with the present invention, generally designated with reference numeral 100, comprises a USB controller 10, a VGA controller 20 and a bridge 30 connected between the USB controller 10 and the VGA controller 20. The USB controller 10 is connectable to a USB port 210 of a host computer 200 for receiving USB based display signals from the host computer 200. The VGA controller 20 is connectable to a display device 300 whereby the USB-to-VGA converter 100 provides a signal conversion and connection between the host computer 200 and the display device 300.

The bridge 30 that is connected between the USB controller 10 and the VGA controller 20 receives the USB based display signals from the USB controller 10 in a first-in-first-out (FIFO) manner and converts the USB based display signals into corresponding standard VGA signals which is then applied to the VGA controller 20. The VGA controller 20 in turn forwards the VGA signals to the display device 300 for display by the display device 300.

Also referring to FIG. 2, the bridge 30 comprises a firmware interface 31, a first-in-first-out (FIFO) controller 32 and a display interface conversion device 33. The firmware interface 31 is connected to the USB controller 10 and receives a bus control command A from the USB controller 10. The firmware interface 31 is also connected to the display interface conversion device 33 by a control bus B and a data bus C for transmission of a DMA control signal, a firmware control signal and a control command therebetween for allowing the display interface conversion device 33 to convert the USB based display signals into the corresponding VGA signals D which can be of PCI type or AGP type, but is not limited thereto.

The FIFO controller 32 is connected to the USB controller 10 by a data bus E and a control line F. The FIFO controller 32 issues control instructions to the USB controller 10 via the control line F for controlling the USB controller 10 to forward the USB based display signals received from the host computer 200 to the FIFO controller 32 in a FIFO manner via the data bus E. The FIFO controller 32 is connected to the display interface conversion device 33 by a data bus G and a control line H whereby the FIFO controller 32 issues FIFO control instruction to the display interface conversion device 33 via the control line H in order to convey the USB based display signals from the FIFO controller 32 to the display interface conversion device 33 in a FIFO manner via the data bus G. The display interface

conversion device 33 then converts the USB based display signals into the corresponding VGA signals D and applies the VGA signals D to the display device 300.

FIG. 3 shows a block diagram of a different embodiment of the bridge 30 in which the display interface conversion device, which is designated with reference numeral 33' for distinction, is embodied as a PCI interface. The firmware interface 31 receives a PIO bus control command A' that is issued by the USB controller 10. The firmware interface 31 is connected to the display interface conversion device 33' by a DMA address control line B1, a DMA length control line B2, a DMA trigger control line B3, a firmware trigger control line B4 and a data bus C whereby the firmware interface 31 controls DMA address, data length and trigger signal of the display interface conversion device 33' and the triggering of the firmware by means of the DMA address control line B1, the DMA length control line B2, the DMA trigger control line B3, and the firmware trigger control line B4 and forwards control instructions and data to the display interface conversion device 33' via the data bus C.

In the embodiment illustrated in FIG. 3, similar to that shown in FIG. 2, the FIFO controller 32 is connected to the USB controller 10 by a data bus E and a control line F. The FIFO controller 32 issues control instructions to the USB controller 10 via the control line F for controlling the USB controller 10 to forward the USB based display signals received from the host computer 200 to the FIFO controller 32 in a FIFO manner via the data bus E. The FIFO controller 32 is connected to the display interface conversion device 33' by a data bus G and a control line H whereby the FIFO controller 32 issues a FIFO control instruction to the display interface conversion device 33' via the control line H in order to convey the USB based display signals from the FIFO controller 32 to the display interface conversion device 33' in a FIFO manner via the data bus G. The display interface conversion device 33', based on the control signals including the DMA address, the data length, the trigger signal and the firmware triggering signal issued by the firmware interface 31 via the DMA address control line B1, the DMA length control line B2, the DMA trigger control line B3 and the firmware trigger control line B4, converts the USB based display signals into the corresponding PCI type VGA signals D' and applies the VGA signals D' to the display device 300.

The bridge 30 comprised of the USB-to-VGA converter of the present invention is embodied in for example a FPGA (Field Programmable Gate Array) chip. However, it can also be embodied in a single chip integrated circuit of different form, such as an ASIC, in which the firmware interface 31, the FIFO controller 32 and the display interface conversion device 33 (33') are integrated.

FIG. 4 shows an operation process of the USB-to-VGA converter 100 working with a host computer 200 to control the display device 300. The operation process discussed herein is based on the WINDOWS operation system released by Microsoft Company, comprising the following steps: In step 400, application software of the host computer 200 issues a request for display of messages. In step 410, the host computer 200 initiates GDI32 display control function and forward the display messages of the application software to a graphics engine. The graphics engine is started in step 420 for processing the messages to be displayed. In step 430, a graphics driver is actuated to process and drive the displayed screen information. In step 440, the information is transmitted via the USB interface.

Based on the above description of the operation process of the USB-to-VGA converter 100, the USB-to-VGA converter 100 can work with any computer systems running under any operation systems. No hardware based display card is required inside the computer 200. The space that is traditionally occupied by the display card inside the computer 200 is thus saved. In addition, no large cable connected between the display device and the host computer is needed.

FIG. 5 shows an application of the USB-to-VGA converter of the present invention in a computer system comprising a display device 300 and a host computer 200. The USB-to-VGA converter 100 is encased in and embodied as an "adaptor" 600. In other words, the USB controller 10, the VGA controller 20 and the bridge 30 are arranged inside the adaptor 600. The adaptor 600 forms a VGA plug 620 releasably mating a signal inlet port 310 of the display device 300 and a USB socket 610 into which a USB plug 510 formed on an end of a USB cable 500 is plugged. An opposite end of the USB cable 500 forms another USB plug 510 for engaging a USB port 210 of the host computer 200 thereby connecting the host computer 200 to the display device 300.

FIG. 6 shows a different application of the USB-to-VGA converter of the present invention in a computer system comprising a display device 300 and a host computer 200 connected by a USB cable 500. The USB controller 10, the VGA controller 20 and the bridge 30 of the USB-to-VGA converter 100 of the present invention are integrated with a display control circuit 320 built inside the display device 300. The display control circuit 320 comprises a USB socket 330 exposed for engagement with a USB plug 510 formed on an end of the USB cable 500. An opposite end of the USB cable 500 forms another USB plug 510 for engaging a USB port 210 of the host computer 200 thereby connecting the host computer 200 to the display device 300. The VGA controller 20 is coupled to the display control circuit 320 for direct supply of VGA signals to the display device 300.

The present invention is aimed to provide a simple and low cost measure for connecting a host computer to a display device without a hardware based display interface card mounted inside the host computer. A USB cable can simply connect the display device to the host computer and allows for transmission of display signals in USB form that has a broad bandwidth and low signal lose. The USB signal is then converted into a VGA signal for proper display by the display device. Costs of the cable itself and the installation of the cable between the computer and the display device are thus substantially reduced. Flexibility of the arrangement of the display device with respect to the computer is also enhanced.

Although the present invention has been described with reference to the preferred embodiments thereof, it is apparent to those skilled in the art that a variety of modifications and changes may be made without departing from the scope of the present invention which is intended to be defined by the appended claims.

The invention claimed is:

1. A USB-to-VGA converter interconnecting through a USB port of a computer a display device controlled the computer comprising:

a USB controller disposed external to the computer and adapted to detachably connect to a USB port of the computer for receiving exclusively therethrough USB based display signals from the computer, the USB controller issuing a bus control command;

a VGA controller disposed external to the computer and adapted to connect to the display device for conveying VGA signals to the display device; and

a bridge disposed external to the computer and connecting the USB controller and the VGA controller one to the other for the passage of data therebetween, the bridge receiving the bus control command and issuing a first-in-first-out control signal to the USB controller to receive the USB based display signals from the USB controller in a first-in-first-out manner, the bridge circuit converting the USB based display signals into corresponding VGA signals and forwarding the VGA signals to the VGA controller which in turn applies the VGA signals to the display device.

2. The USB-to-VGA converter as claimed in claim 1, wherein the USB controller comprises a USB socket.

3. The USB-to-VGA converter as claimed in claim 1, wherein the VGA controller comprises a VGA plug.

4. The USB-to-VGA converter as claimed in claim 1, wherein the converter is encased in an adaptor which comprises a USB socket for connection with the USB port of the computer.

5. The USB-to-VGA converter as claimed in claim 4, wherein the adaptor further comprises a VGA plug for connection with the display device.

6. The USB-to-VGA converter as claimed in claim 1, wherein the USB controller, the bridge circuit and the VGA controller are integrated with a display control circuit built inside the display device.

7. The USB-to-VGA converter as claimed in claim 6, wherein the USB controller comprises a USB socket for connection with the USB port of the computer.

8. The USB-to-VGA converter as claimed in claim 6, wherein the VGA controller is directly connected to the display control circuit of the display device.

9. The USB-to-VGA converter as claimed in claim 1, wherein the bridge circuit comprising:

a firmware interface connected to the USB controller for receiving the bus control signal from the USB controller and issuing a DMA control signal, a firmware control signal and control command data;

a first-in-first-out controller connected to the USB controller for issuing the first-in-first-out control signal to the USB controller to receive the USB based display signals from the USB controller in a first-in-first-out manner; and

a display interface conversion device connected to the firmware interface, the first-in-first-out controller and the VGA controller for receiving the DMA control signal, the firmware control signal and the control command data from the firmware interface and being controlled by the first-in-first-out control signal from the first-in-first-out controller to receive the USB based display signals from the USB controller in a first-in-first-out manner, the display interface conversion device converting the USB based display signals into the corresponding VGA signals and forwarding the VGA signals to the VGA controller.

10. The USB-to-VGA converter as claimed in claim 9, wherein the bus control signal from the USB controller to the firmware interface comprises a PIO bus control signal.

11. The USB-to-VGA converter as claimed in claim 9, wherein the firmware interface is connected to the display interface conversion device by a control bus and a data bus.

12. The USB-to-VGA converter as claimed in claim 9, wherein the firmware interface is connected to the display interface conversion device by a DMA address control line, a DMA length control line, a DMA trigger control line, a firmware trigger control line and a data bus.

13. The USB-to-VGA converter as claimed in claim 9, wherein the first-in-first-out controller is connected to the USB controller by a control line and a data bus.

14. The USB-to-VGA converter as claimed in claim 9, wherein the first-in-first-out controller is connected to the display interface conversion device by a control line and a data bus.

15. The USB-to-VGA converter as claimed in claim 9, wherein the VGA signals comprise PCI type VGA display signals.

16. The USB-to-VGA converter as claimed in claim 9, wherein the firmware interface, the first-in-first-out controller and the display interface conversion device are integrated in a single chip integrated circuit.

17. The USB-to-VGA converter as claimed in claim 16, wherein the integrated circuit comprises a field programmable gate array integrated circuit.

18. The USB-to-VGA converter as claimed in claim 16, wherein the integrated circuit comprises an ASIC integrated circuit.

19. A discrete USB-to-VGA converter externally interconnecting in detachable manner through a USB port of a computer a display device controlled the computer comprising:

a USB controller disposed external to the computer and detachably connected to a USB port of the computer for receiving exclusively therethrough USB based display signals from the computer, the USB controller issuing a bus control command;

a VGA controller disposed external to the computer for connection to the display device for conveying VGA signals to the display device; and

a bridge disposed external to the computer and interconnecting the USB controller and the VGA controller one to the other for the passage of data therebetween, the bridge receiving the bus control command and issuing a first-in-first-out control signal to the USB controller to receive the USB based display signals from the USB controller in a first-in-first-out manner, the bridge circuit converting the USB based display signals into corresponding VGA signals and forwarding the VGA signals to the VGA controller which in turn applies the VGA signals to the display device.

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ADDRESS
04586

TITLE
USB-TO-VGA CONVERTER

FILING FEE RECEIVED	FEES: Authority has been given in Paper
370	No. _____ to charge/credit DEPOSIT ACCOUNT No. _____ for following:

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USB-TO-VGA CONVERTER

ABSTRACT OF THE DISCLOSURE

A USB-to-VGA converter includes a USB controller connectable to a USB port of a computer for receiving USB based display signals from the computer, a VGA controller connectable to a display device for conveying VGA signals to the display device and a bridge connected between the USB controller and the VGA controller. The bridge receives a bus control command from the USB controller and issues a first-in-first-out control signal to the USB controller to receive the USB based display signals from the USB controller in a first-in-first-out manner. The bridge circuit converts the USB based display signals into corresponding VGA signals and forwarding the VGA signals to the VGA controller, which in turn applies the VGA signals to the display device. No display interface card is required inside the host computer for generation of the VGA signals.

USB-TO-VGA CONVERTER

BACKGROUND OF THE INVENTION

1. Field of the Invention

[0001] The present invention relates generally to a USB (Universal Serial Bus) to VGA (Video Graphics Array) converter, and in particular to a USB-to-VGA converter connectable between a USB port of a computer and a VGA display device.

2. The Related Art

[0002] A computer system comprises a display device connected to a host machine of the computer system for receiving display signals from the host computer and displaying messages associated with the display signals. The connection between the display device and the host computer is provided by an interface circuit built in the host computer, such as a PCI (Peripheral Component Interconnect) display interface and an AGP (Accelerated Graphics Port) display interface. A display interface card is mounted on a main board of the host computer for transmission of VGA signals to the display device. The display interface card occupies a portion of the limited space inside the host computer and in addition, increases the overall costs of the computer system. The display interface card is often connected to the display device by a cable for transmission of the display signals. The cable is adverse to the management of peripheral devices of the computer system and limits the distance that the display signals can be transmitted therethrough.

SUMMARY OF THE INVENTION

[0003] Thus, an object of the present invention is to provide a USB-to-VGA converter which converts USB based display signals issued from a host computer into VGA signals that can be received and recognized by a display device whereby image to be displayed can be transmitted from the host computer in USB form.

[0004] Another object of the present invention is to provide a USB-to-VGA converter that converts USB based display signals from a host computer into VGA signals in a first-in-first-out manner for display in a VGA display device.

[0005] A further object of the present invention is to provide a USB-to-VGA converter that allows for direct transmission of USB signals from a host computer to a display device without adding any display interface card inside the host computer.

[0006] To achieve the above objects, in accordance with the present invention, there is provided a USB-to-VGA converter comprising a USB controller connectable to a USB port of a computer for receiving USB based display signals from the computer, a VGA controller connectable to a display device for conveying VGA signals to the display device and a bridge connected between the USB controller and the VGA controller. The bridge receives a bus control command from the USB controller and issues a first-in-first-out control signal to the USB controller to receive the USB based display signals from the USB controller in a first-in-first-out manner. The bridge circuit converts the USB based display signals into corresponding VGA signals and forwarding the VGA signals to the VGA controller, which in turn applies the VGA signals to the display device. No display interface card is required inside the host computer for generation of the VGA signals.

BRIEF DESCRIPTION OF THE DRAWINGS

[0007] The present invention will be apparent to those skilled in the art by reading the following description of preferred embodiments thereof, with reference to the attached drawings, in which:

[0008] Figure 1 is a system block diagram of a USB-to-VGA converter constructed in accordance with the present invention;

[0009] Figure 2 is a block diagram of a bridge circuit of the USB-to-VGA converter of the present invention;

[0010] Figure 3 is a block diagram of a bridge circuit of the USB-to-VGA converter in accordance with a different embodiment of the present invention;

[0011] Figure 4 is a flow chart illustrating a process for a host computer to issue USB display signals to a USB controller;

[0012] Figure 5 is a schematic view illustrating an application of the USB-to-VGA converter in connecting a display device to a host computer; and

[0013] Figure 6 is a schematic view illustrating a different application of the USB-to-VGA converter in connecting a display device to a host computer.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0014] With reference to the drawings and in particular to Figure 1, a USB-to-VGA converter constructed in accordance with the present invention, generally designated with reference numeral 100, comprises a USB controller 10, a VGA controller 20 and a bridge 30 connected between the USB controller 10 and the VGA controller 20. The USB controller 10 is connectable to a USB port 210 of a host computer 200 for receiving USB based display signals from the host computer 200. The VGA controller 20 is connectable to a display device 300 whereby the USB-to-VGA converter 100 provides a signal conversion and connection between the host computer 200 and the display device 300.

[0015] The bridge 30 that is connected between the USB controller 10 and the VGA controller 20 receives the USB based display signals from the USB controller 10 in a first-in-first-out (FIFO) manner and converts the USB based display signals into corresponding standard VGA signals which is then applied to the VGA controller 20. The VGA controller 20 in turn forwards the VGA signals to the display device 300 for display by the display device 300.

[0016] Also referring to Figure 2, the bridge 30 comprises a firmware interface 31, a first-in-first-out (FIFO) controller 32 and a display interface conversion device 33. The firmware interface 31 is connected to the USB controller 10 and receives a

bus control command **A** from the USB controller 10. The firmware interface 31 is also connected to the display interface conversion device 33 by a control bus **B** and a data bus **C** for transmission of a DMA control signal, a firmware control signal and a control command therebetween for allowing the display interface conversion device 33 to convert the USB based display signals into the corresponding VGA signals **D** which can be of PCI type or AGP type, but is not limited thereto.

[0017] The FIFO controller 32 is connected to the USB controller 10 by a data bus **E** and a control line **F**. The FIFO controller 32 issues control instructions to the USB controller 10 via the control line **F** for controlling the USB controller 10 to forward the USB based display signals received from the host computer 200 to the FIFO controller 32 in a FIFO manner via the data bus **E**. The FIFO controller 32 is connected to the display interface conversion device 33 by a data bus **G** and a control line **H** whereby the FIFO controller 32 issues FIFO control instruction to the display interface conversion device 33 via the control line **H** in order to convey the USB based display signals from the FIFO controller 32 to the display interface conversion device 33 in a FIFO manner via the data bus **G**. The display interface conversion device 33 then converts the USB based display signals into the corresponding VGA signals **D** and applies the VGA signals **D** to the display device 300.

[0018] Figure 3 shows a block diagram of a different embodiment of the bridge 30 in which the display interface conversion device, which is designated with reference numeral 33' for distinction, is embodied as a PCI interface. The firmware interface 31 receives a PIO bus control command **A'** that is issued by the USB controller 10. The firmware interface 31 is connected to the display interface conversion device 33' by a DMA address control line **B1**, a DMA length control line **B2**, a DMA trigger control line **B3**, a firmware trigger control line **B4** and a data bus **C** whereby the firmware interface 31 controls DMA address, data length and trigger signal of the display interface conversion device 33' and the triggering of the firmware by means of the DMA address control line **B1**, the DMA length control line **B2**, the DMA trigger control line **B3**, and the firmware trigger control line **B4** and forwards control instructions and data to the display interface conversion device 33' via the data bus **C**.

[illegible]

[0019] In the embodiment illustrated in Figure 3, similar to that shown in Figure 2, the FIFO controller 32 is connected to the USB controller 10 by a data bus E and a control line F. The FIFO controller 32 issues control instructions to the USB controller 10 via the control line F for controlling the USB controller 10 to forward the USB based display signals received from the host computer 200 to the FIFO controller 32 in a FIFO manner via the data bus E. The FIFO controller 32 is connected to the display interface conversion device 33' by a data bus G and a control line H whereby the FIFO controller 32 issues a FIFO control instruction to the display interface conversion device 33' via the control line H in order to convey the USB based display signals from the FIFO controller 32 to the display interface conversion device 33' in a FIFO manner via the data bus G. The display interface conversion device 33', based on the control signals including the DMA address, the data length, the trigger signal and the firmware triggering signal issued by the firmware interface 31 via the DMA address control line B1, the DMA length control line B2, the DMA trigger control line B3 and the firmware trigger control line B4, converts the USB based display signals into the corresponding PCI type VGA signals D' and applies the VGA signals D' to the display device 300.

[0020] The bridge 30 comprised of the USB-to-VGA converter of the present invention is embodied in for example a FPGA (Field Programmable Gate Array) chip. However, it can also be embodied in a single chip integrated circuit of different form, such as an ASIC, in which the firmware interface 31, the FIFO controller 32 and the display interface conversion device 33 (33') are integrated.

[0021] Figure 4 shows an operation process of the USB-to-VGA converter 100 working with a host computer 200 to control the display device 300. The operation process discussed herein is based on the WINDOWS operation system released by Microsoft Company, comprising the following steps: In step 400, application software of the host computer 200 issues a request for display of messages. In step 410, the host computer 200 initiates GDI32 display control function and forward the display messages of the application software to a graphics engine. The graphics engine is started in step 420 for processing the messages to be displayed. In step 430, a graphics driver is actuated to process and drive the displayed screen information. In step 440, the information is transmitted via the USB interface.

[0022] Based on the above description of the operation process of the USB-to-VGA converter 100, the USB-to-VGA converter 100 can work with any computer systems running under any operation systems. No hardware based display card is required inside the computer 200. The space that is traditionally occupied by the display card inside the computer 200 is thus saved. In addition, no large cable connected between the display device and the host computer is needed.

[0023] Figure 5 shows an application of the USB-to-VGA converter of the present invention in a computer system comprising a display device 300 and a host computer 200. The USB-to-VGA converter 100 is encased in and embodied as an "adaptor" 600. In other words, the USB controller 10, the VGA controller 20 and the bridge 30 are arranged inside the adaptor 600. The adaptor 600 forms a VGA plug 620 releasably mating a signal inlet port 310 of the display device 300 and a USB socket 610 into which a USB plug 510 formed on an end of a USB cable 500 is plugged. An opposite end of the USB cable 500 forms another USB plug 510 for engaging a USB port 210 of the host computer 200 thereby connecting the host computer 200 to the display device 300.

[0024] Figure 6 shows a different application of the USB-to-VGA converter of the present invention in a computer system comprising a display device 300 and a host computer 200 connected by a USB cable 500. The USB controller 10, the VGA controller 20 and the bridge 30 of the USB-to-VGA converter 100 of the present invention are integrated with a display control circuit 320 built inside the display device 300. The display control circuit 320 comprises a USB socket 330 exposed for engagement with a USB plug 510 formed on an end of the USB cable 500. An opposite end of the USB cable 500 forms another USB plug 510 for engaging a USB port 210 of the host computer 200 thereby connecting the host computer 200 to the display device 300. The VGA controller 20 is coupled to the display control circuit 320 for direct supply of VGA signals to the display device 300.

[0025] The present invention is aimed to provide a simple and low cost measure for connecting a host computer to a display device without a hardware based display interface card mounted inside the host computer. A USB cable can simply connect the display device to the host computer and allows for transmission of display signals

in USB form that has a broad bandwidth and low signal lose. The USB signal is then converted into a VGA signal for proper display by the display device. Costs of the cable itself and the installation of the cable between the computer and the display device are thus substantially reduced. Flexibility of the arrangement of the display device with respect to the computer is also enhanced.

[0026] Although the present invention has been described with reference to the preferred embodiments thereof, it is apparent to those skilled in the art that a variety of modifications and changes may be made without departing from the scope of the present invention which is intended to be defined by the appended claims.

WHAT IS CLAIMED IS

1. A USB-to-VGA converter comprising:
   a USB controller adapted to connect to a USB port of a computer for receiving USB based display signals from the computer, the USB controller issuing a bus control command;
   a VGA controller adapted to connect to a display device for conveying VGA signals to the display device; and
   a bridge connected between the USB controller and the VGA controller, the bridge receiving the bus control command and issuing a first-in-first-out control signal to the USB controller to receive the USB based display signals from the USB controller in a first-in-first-out manner, the bridge circuit converting the USB based display signals into corresponding VGA signals and forwarding the VGA signals to the VGA controller which in turn applies the VGA signals to the display device.

2. The USB-to-VGA converter as claimed in Claim 1, wherein the USB controller comprises a USB socket.

3. The USB-to-VGA converter as claimed in Claim 1, wherein the VGA controller comprises a VGA plug.

4. The USB-to-VGA converter as claimed in Claim 1, wherein the converter is encased in an adaptor which comprises a USB socket for connection with the USB port of the computer.

5. The USB-to-VGA converter as claimed in Claim 4, wherein the adaptor further comprises a VGA plug for connection with the display device.

6. The USB-to-VGA converter as claimed in Claim 1, wherein the USB controller, the bridge circuit and the VGA controller are integrated with a display control circuit built inside the display device.

7. The USB-to-VGA converter as claimed in Claim 6, wherein the USB controller comprises a USB socket for connection with the USB port of the computer.

8. The USB-to-VGA converter as claimed in Claim 6, wherein the VGA controller is directly connected to the display control circuit of the display device.

9. The USB-to-VGA converter as claimed in Claim 1, wherein the bridge circuit comprising:

a firmware interface connected to the USB controller for receiving the bus control signal from the USB controller and issuing a DMA control signal, a firmware control signal and control command data;

a first-in-first-out controller connected to the USB controller for issuing the first-in-first-out control signal to the USB controller to receive the USB based display signals from the USB controller in a first-in-first-out manner; and

a display interface conversion device connected to the firmware interface, the first-in-first-out controller and the VGA controller for receiving the DMA control signal, the firmware control signal and the control command data from the firmware interface and being controlled by the first-in-first-out control signal from the first-in-first-out controller to receive the USB based display signals from the USB controller in a first-in-first-out manner, the display interface conversion device converting the USB based display signals into the corresponding VGA signals and forwarding the VGA signals to the VGA controller.

10. The USB-to-VGA converter as claimed in Claim 9, wherein the bus control signal from the USB controller to the firmware interface comprises a PIO bus control signal.

11. The USB-to-VGA converter as claimed in Claim 9, wherein the firmware interface is connected to the display interface conversion device by a control bus and a data bus.

12. The USB-to-VGA converter as claimed in Claim 9, wherein the firmware interface is connected to the display interface conversion device by a DMA address control line, a DMA length control line, a DMA trigger control line, a firmware trigger control line and a data bus.

13. The USB-to-VGA converter as claimed in Claim 9, wherein the first-in-first-out controller is connected to the USB controller by a control line and a data bus.

14. The USB-to-VGA converter as claimed in Claim 9, wherein the first-in-first-out controller is connected to the display interface conversion device by a control line and a data bus.

15. The USB-to-VGA converter as claimed in Claim 9, wherein the VGA signals comprise PCI type VGA display signals.

16. The USB-to-VGA converter as claimed in Claim 9, wherein the firmware interface, the first-in-first-out controller and the display interface conversion device are integrated in a single chip integrated circuit.

17. The USB-to-VGA converter as claimed in Claim 16, wherein the integrated circuit comprises a field programmable gate array integrated circuit.

18. The USB-to-VGA converter as claimed in Claim 16, wherein the integrated circuit comprises an ASIC integrated circuit.

10316013 .121102

DECLARATION FOR PATENT APPLICATION

Docket Number (Optional)
MR1115-429

As a below named inventor, I hereby declare that:

My residence, post office address, and citizenship are as stated below next to my name.

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled: USB-TO-VGA CONVERTER, the specification of which is attached hereto unless the following box is checked.

☐ was filed on _____ as United States Application Number or PCT International Application Number _____ and was amended on _____ (if applicable)

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment specifically referred to above.
I acknowledge the duty to disclose information which is material to patentability as defined in 37 CFR 1.56.
I hereby claim foreign priority benefits under 35 U.S.C. 119(a)-(d) or 365(b) of any foreign application(s) for patent or inventor's certificate, or 365(a) of any PCT international application which designated at least one country other than the United States of America, listed below and have also identified below, by checking the box, any foreign application for patent or inventor's certificate, or of any PCT international application having a filing date before that of the application on which priority is claimed.

Prior Foreign Application(s)			Priority Not Claimed
(Number)	(Country)	(Day/Month/Year Filed)	☐
(Number)	(Country)	(Day/Month/Year Filed)	☐

I hereby claim the benefit under 35 U.S.C. 119(e) of any United States provisional application(s) listed below.

(Application Number) (Filing Date)

(Application Number) (Filing Date)

I hereby claim the benefit under 35 U.S.C. 120 of any United States application(s), or 365(c) of any PCT international application designating the United States of America, listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States or PCT International application in the manner provided by the first paragraph of 35 U.S.C. 112,
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(Application Number) (Filing Date) (Status-*patented, pending, abandoned*)

I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and to transact all business in the Patent and Trademark Office connected therewith: MORTON J. ROSENBERG, ESQ., REG. # 26,049
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I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under 18 U.S.C. 1001 and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

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Full name of second joint inventor, if any (given name, family name) _____
Second Inventor's signature _____ Date _____
Citizenship _____
Mailing Address _____

☐ Additional inventors are being named on separately numbered sheets attached hereto.

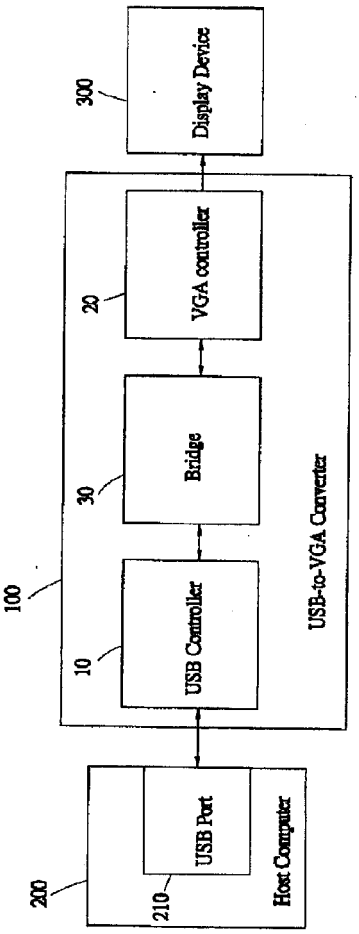
Display Device
300
VGA controller
20
Bridge
30
USB Controller
10
USB-to-VGA Converter
100
USB Port
210
Host Computer
200

FIG.1

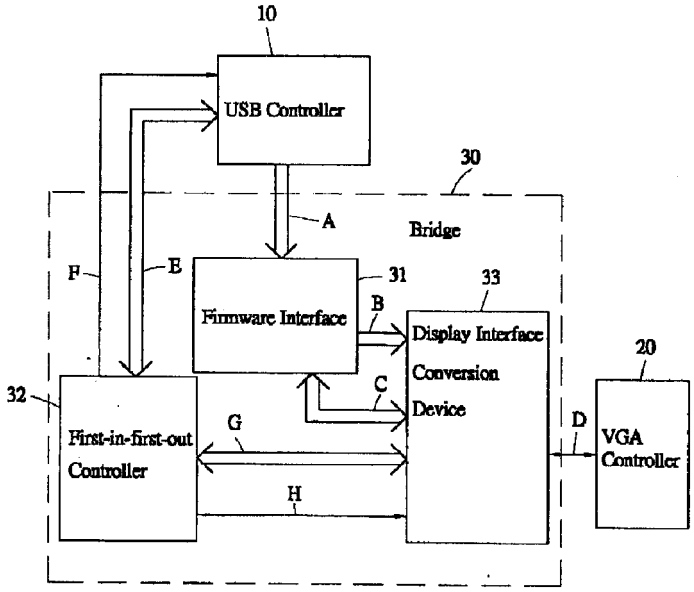
10
USB Controller
30
Bridge
A
F
E
31
33
Firmware Interface
B
Display Interface
Conversion
Device
20
32
C
G
D
VGA
Controller
First-in-first-out
Controller
H

FIG.2

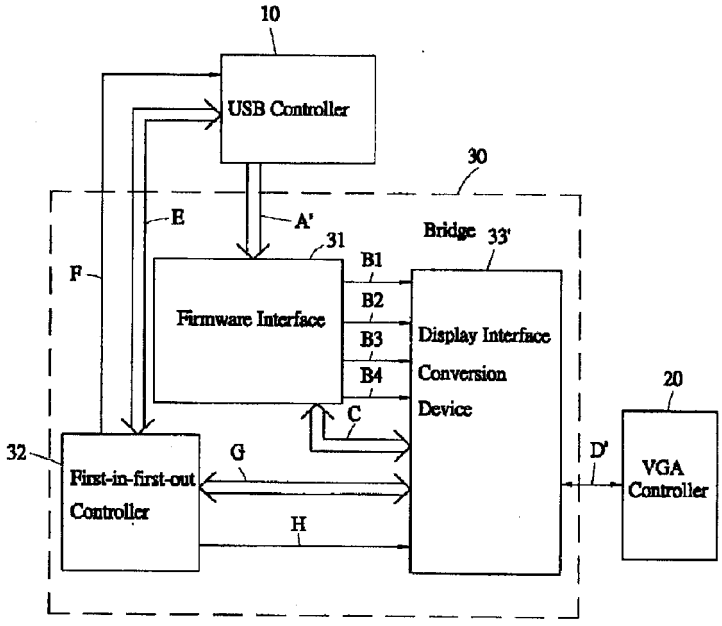
10
USB Controller
30
E
A'
Bridge
33'
31
B1
B2
B3
B4
F
Firmware Interface
Display Interface
Conversion
Device
20
C
32
G
D'
VGA
Controller
First-in-first-out
Controller
H

FIG.3

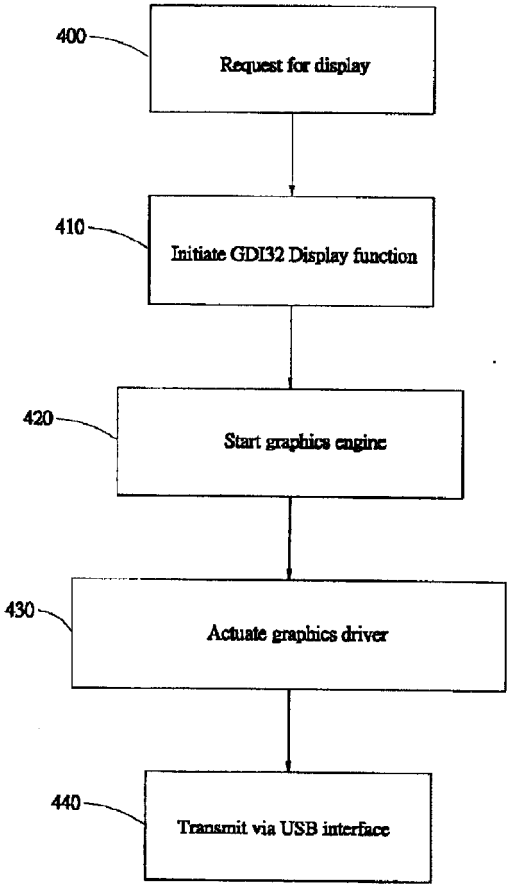
400
Request for display
410
Initiate GDI32 Display function
420
Start graphics engine
430
Actuate graphics driver
440
Transmit via USB interface

FIG.4

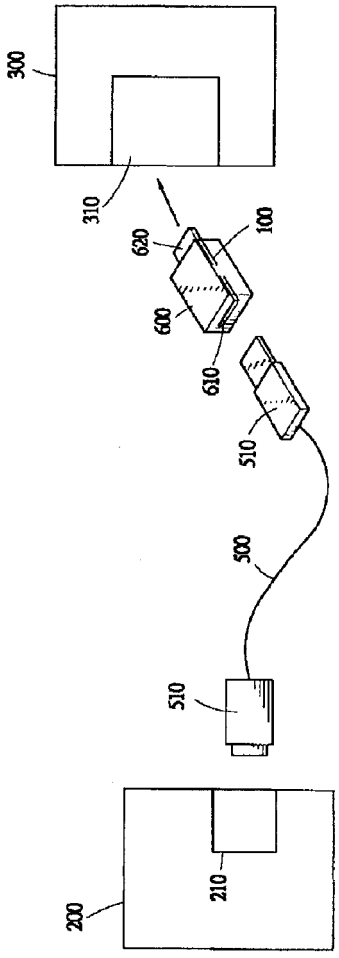

FIG.5

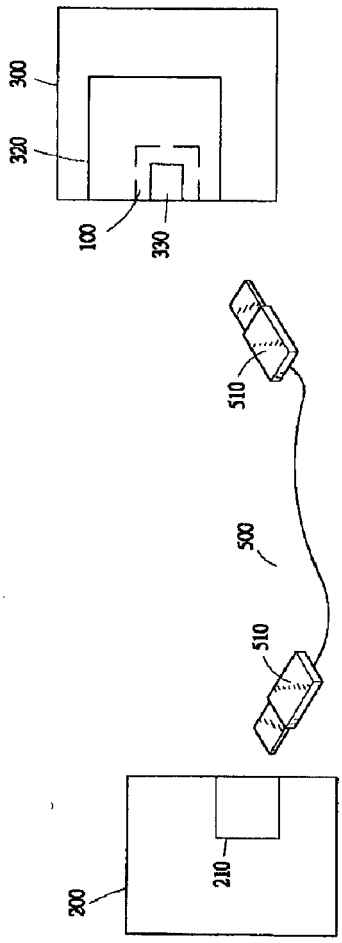

FIG.6

12/11/02 jc923 U.S. PTO

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UTILITY PATENT APPLICATION TRANSMITTAL

(Only for new nonprovisional applications under 37 CFR 1.53(b))

Attorney Docket No.	MR1115-429
First Inventor	PEI-CHUNG LIU
Title	USB-TO-VGA CONVERTER
Express Mail Label No.	

10/316013 U.S. PTO 12/11/02

APPLICATION ELEMENTS

See MPEP chapter 600 concerning utility patent application contents.

ADDRESS TO: Assistant Commissioner for Patents
Box Patent Application
Washington, DC 20231

1. [X] Fee Transmittal Form (e.g., PTO/SB/17) (Submit an original, and a duplicate for fee processing)
2. [X] Applicant claims small entity status. See 37 CFR 1.27.
3. [X] Specification [Total Pages 11] (preferred arrangement set forth below)
   - Descriptive title of the invention
   - Cross Reference to Related Applications
   - Statement Regarding Fed sponsored R & D
   - Reference to sequence listing, a table, or a computer program listing appendix
   - Background of the Invention
   - Brief Summary of the Invention
   - Brief Description of the Drawings (if filed)
   - Detailed Description
   - Claim(s)
   - Abstract of the Disclosure
4. [X] Drawing(s) (35 U.S.C. 113) [Total Sheets 6]
5. Oath or Declaration [Total Pages 1]
   a. [X] Newly executed (original or copy)
   b. [ ] Copy from a prior application (37 CFR 1.63 (d)) (for continuation/divisional with Box 18 completed)
      i. [ ] DELETION OF INVENTOR(S) Signed statement attached deleting inventor(s) named in the prior application, see 37 CFR 1.63(d)(2) and 1.33(b).
6. [ ] Application Data Sheet. See 37 CFR 1.76
7. [ ] CD-ROM or CD-R in duplicate, large table or Computer Program (Appendix)
8. Nucleotide and/or Amino Acid Sequence Submission (if applicable, all necessary)
   a. [ ] Computer Readable Form (CRF)
   b. Specification Sequence Listing on:
      i. [ ] CD-ROM or CD-R (2 copies); or
      ii. [ ] paper
   c. [ ] Statements verifying identity of above copies

ACCOMPANYING APPLICATION PARTS

9. [X] Assignment Papers (cover sheet & document(s))
10. [ ] 37 CFR 3.73(b) Statement (when there is an assignee) [X] Power of Attorney
11. [ ] English Translation Document (if applicable)
12. [ ] Information Disclosure Statement (IDS)/PTO-1449 [ ] Copies of IDS Citations
13. [ ] Preliminary Amendment
14. [X] Return Receipt Postcard (MPEP 503) (Should be specifically itemized)
15. [ ] Certified Copy of Priority Document(s) (if foreign priority is claimed)
16. [ ] Request and Certification under 35 U.S.C. 122 (b)(2)(B)(i). Applicant must attach form PTO/SB/35 or its equivalent.
17. [ ] Other: .....

18. If a CONTINUING APPLICATION, check appropriate box, and supply the requisite information below and in a preliminary amendment, or in an Application Data Sheet under 37 CFR 1.76:

[ ] Continuation [ ] Divisional [ ] Continuation-in-part (CIP) of prior application No.: ____/____

Prior application information: Examiner: _____ Group Art Unit: _____

For CONTINUATION OR DIVISIONAL APPS only: The entire disclosure of the prior application, from which an oath or declaration is supplied under Box 5b, is considered a part of the disclosure of the accompanying continuation or divisional application and is hereby incorporated by reference. The incorporation can only be relied upon when a portion has been inadvertently omitted from the submitted application parts.

19. CORRESPONDENCE ADDRESS

[X] Customer Number or Bar Code Label [barcode] or [X] Correspondence address below

Name	Morton J. Rosenberg, Esq.				
	Rosenberg, Klein & Lee				
Address	3458 Ellicott Center Drive - Suite 101				
City	Ellicott City	State	MD	Zip Code	21043
Country	USA	Telephone	410-465-6678	Fax	410-461-3067

Name (Print/Type)	Morton J. Rosenberg	Registration No. (Attorney/Agent)	26,049
Signature	Morton J. Rosenberg	Date	12/9/02

Burden Hour Statement: This form is estimated to take 0.2 hours to complete. Time will vary depending upon the needs of the individual case. Any comments on the amount of time you are required to complete this form should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, Washington, DC 20231. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Assistant Commissioner for Patents, Box Patent Application, Washington, DC 20231.

10814813.111108

PTO/SB/17 (10-01)
Approved for use through 10/31/2002. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

FEE TRANSMITTAL for FY 2002

Patent fees are subject to annual revision.

TOTAL AMOUNT OF PAYMENT ($) 410.00

Complete if Known	
Application Number	
Filing Date	
First Named Inventor	PEI-CHUNG LIU
Examiner Name	
Group Art Unit	
Attorney Docket No.	MR1115-429

METHOD OF PAYMENT

1. [X] The Commissioner is hereby authorized to charge indicated fees and credit any overpayments to:
   Deposit Account Number: 18-2011
   Deposit Account Name:
   [X] Charge Any Additional Fee Required Under 37 CFR 1.16 and 1.17
   [X] Applicant claims small entity status. See 37 CFR 1.27
2. [X] Payment Enclosed: [X] Check [ ] Credit card [ ] Money Order [ ] Other

FEE CALCULATION

1. BASIC FILING FEE

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
101	740	201	370	Utility filing fee	$370
106	330	206	165	Design filing fee	
107	510	207	255	Plant filing fee	
108	740	208	370	Reissue filing fee	
114	150	214	75	Provisional filing fee	

SUBTOTAL (1) ($) $370

2. EXTRA CLAIM FEES

	Extra Claims		Fee from below	Fee Paid
Total Claims	18 - 20** = 0	X	9	0
Independent Claims	1 - 3** = 0	X	42	0
Multiple Dependent			140	0

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description
103	18	203	9	Claims in excess of 20
102	84	202	42	Independent claims in excess of 3
104	280	204	140	Multiple dependent claim, if not paid
109	84	209	42	** Reissue independent claims over original patent
110	18	210	9	** Reissue claims in excess of 20 and over original patent

SUBTOTAL (2) ($) 0

*or number previously paid, if greater; For Reissues, see above

FEE CALCULATION (continued)

3. ADDITIONAL FEES

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
105	130	205	65	Surcharge - late filing fee or oath	
127	50	227	25	Surcharge - late provisional filing fee or cover sheet	
139	130	139	130	Non-English specification	
147	2,520	147	2,520	For filing a request for ex parte reexamination	
112	920*	112	920*	Requesting publication of SIR prior to Examiner action	
113	1,840*	113	1,840*	Requesting publication of SIR after Examiner action	
115	110	215	55	Extension for reply within first month	
116	400	216	200	Extension for reply within second month	
117	920	217	460	Extension for reply within third month	
118	1,440	218	720	Extension for reply within fourth month	
128	1,960	228	980	Extension for reply within fifth month	
119	320	219	160	Notice of Appeal	
120	320	220	160	Filing a brief in support of an appeal	
121	280	221	140	Request for oral hearing	
138	1,510	138	1,510	Petition to institute a public use proceeding	
140	110	240	55	Petition to revive - unavoidable	
141	1,280	241	640	Petition to revive - unintentional	
142	1,280	242	640	Utility issue fee (or reissue)	
143	460	243	230	Design issue fee	
144	620	244	310	Plant issue fee	
122	130	122	130	Petitions to the Commissioner	
123	50	123	50	Processing fee under 37 CFR 1.17(q)	
126	180	126	180	Submission of Information Disclosure Stmt	
581	40	581	40	Recording each patent assignment per property (times number of properties)	$ 40
146	740	246	370	Filing a submission after final rejection (37 CFR § 1.129(a))	
149	740	249	370	For each additional invention to be examined (37 CFR § 1.129(b))	
179	740	279	370	Request for Continued Examination (RCE)	
169	900	169	900	Request for expedited examination of a design application	

Other fee (specify)

*Reduced by Basic Filing Fee Paid SUBTOTAL (3) ($) 40

SUBMITTED BY				Complete (if applicable)	
Name (Print/Type)	Morton J. Rosenberg	Registration No. (Attorney/Agent)	26,049	Telephone	410-465-6678
Signature				Date	12/9/02

WARNING: Information on this form may become public. Credit card information should not be included on this form. Provide credit card information and authorization on PTO-2038.

Burden Hour Statement: This form is estimated to take 0.2 hours to complete. Time will vary depending upon the needs of the individual case. Any comments on the amount of time you are required to complete this form should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, Washington, DC 20231. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Assistant Commissioner for Patents, Washington, DC 20231.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
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www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/316,013	12/11/2002	Pei-Chung Liu	MR1115-429	2895

4586 7590 03/16/2005

ROSENBERG, KLEIN & LEE
3458 ELLICOTT CENTER DRIVE-SUITE 101
ELLICOTT CITY, MD 21043

EXAMINER	
HUYNH, KIM T	

ART UNIT	PAPER NUMBER
2112	

DATE MAILED: 03/16/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

PTO-90C (Rev. 10/03)

Office Action Summary	Application No.	Applicant(s)
	10/318,013	LIU, PEI-CHUNG
	Examiner	Art Unit
	Kim T. Huynh	2112

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on 11 December 2002.

2a)☐ This action is FINAL. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-18 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-18 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 11 December 2002 is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

U.S. Patent and Trademark Office
PTOL-326 (Rev. 1-04) Office Action Summary Part of Paper No./Mail Date 20050305

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1-8 are rejected under 35 U.S.C. 102(e) as being anticipated by Finger et al. (US Patent 6,629,926)

As per claim 1, Finger discloses a USB-to-VGA converter comprising:

- a USB controller(fig.2, 66 ie peripheral interface includes usb controller) adapted to connect to a USB port of a computer for receiving USB based display signals from the computer, the USB controller issuing a bus control command; (col.9, lines 22-51, ie the peripheral(usb) interfaces 66 connected to data processing system 52 allows communication from any peripherals via system bus 56 (col.8, lines 41-53) and stored data to memory 72, from memory 72 , data processing system process reconstruction and conversion and output to the display)
- a VGA controller(fig.5, 64 video controlling paths) adapted to connect to a display device for conveying VGA signals to the display device(fig.5, 34 ie display device); and (col.4, lines 12-21, ie data provide by peripherals to

data processing system 52 process and reconstruction and conversion and output to the display 34)

- a bridge(fig.2, 70, ie interface device) connected between the USB controller and the VGA controller the bridge receiving the bus control command and issuing a first-in-first-out control signal to the USB controller to receive the USB based display signals from the USB controller in a first-in-first-out manner (col.10, line 65-col.11, line 64, ie interface device 70 connected to data transfer controller 68 for converting USB signal to the display signals and output to the display 34, included event ID stored in buffer 308(FIFO) when a request for transfer is made, the control 300 uses the event ID to access transfer control parameters, including logical address which generated sequentially which implies FIFO manner) the bridge circuit converting the USB based display signals into corresponding VGA signals and forwarding the VGA signals to the VGA controller which in turn applies the VGA signals to the display device. (col.9, lines 22-51, ie the peripheral(usb) interfaces 66 connected to interface device 70 comprising data transfer controller 68 allows communication from any peripherals via system bus 56 and stored data to memory 72, from memory 72 , data transfer controller process reconstruction and conversion and output to the display 34 via video controlling path 64, col.5, lines 4-52)

As per claim 2, Finger discloses wherein the USB controller comprises a USB socket. (fig.7, 200, the adaptor module, col.10, lines 11-40)

As per claim 3, Finger discloses wherein the VGA controller comprises a VGA plug. (col.11, lines 40-65), (fig.5, 64, video controlling paths connected to display device 34 via controlling of fig.6, 68 ie data transfer controller)

As per claim 4, Finger discloses wherein the converter is encased in an adaptor which comprises a USB socket for connection with the USB port of the computer. (fig.7, 200, ie the adaptor module), (col.10, lines 11-40)

As per claim 5, Finger discloses wherein the adaptor further comprises a VGA plug for connection with the display device. (fig.5, 64, video controlling paths connected to display device 34 via fig.6, 68 ie data transfer controller)

As per claim 6, Finger discloses wherein the USB controller, the bridge circuit and the VGA controller are integrated with a display control circuit built inside the display device. (fig1, 62, ie data processing system)

As per claim 7, Finger discloses wherein the USB controller comprises a USB socket for connection with the USB port of the computer. (col.9, lines 22-51, ie

the peripheral(usb) interfaces 66 allow communication from any the various peripheral to data processing system 62)

As per claim 8, Finger discloses wherein the VGA controller is directly connected to the display control circuit of the display device. (fig.5, 64, video controlling paths connected to display device 34 via fig.6, 68 ie data transfer controller)

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 9-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Finger et al. (US Patent 6,629,926) in view of Cheng (Pub No US20040153778)

As per claim 9, Finger discloses wherein the bridge circuit comprising:

- a firmware interface (fig.2, 70 ie interface device) connected to the USB controller for receiving the bus control signal from the USB controller and; (col.9, lines 22-51, ie the peripheral(usb) interfaces 66 connected to interface device 70 comprising data transfer controller 68 allows communication from any peripherals via system bus 56 ,col.8, lines 41-53)
- a first-in-first-out controller connected to the USB controller for issuing the first-in-first-out control signal to the USB controller to receive the USB

based display signals from the USB controller in a first-in-first-out manner ; and (col.10, line 65-col.11, line 64, ie interface device 70 connected to data transfer controller 68 for converting usb signal into display signals and output to the display 34, included event ID stored in buffer 308(FIFO) when a request for transfer is made, the control 300 uses the event ID to access transfer control parameters, including logical address which generated sequentially which implies FIFO manner)

- a display interface conversion device connected to the firmware interface, the first-in-first-out controller and the VGA controller (fig.5, 64 video controlling paths) for receiving the control signal, the firmware control signal and the control command data from the firmware interface and being controlled by the first-in-first-out control signal from the first-in-first-out controller to receive the USB based display signals from the USB controller in a first-in-first-out manner(col.10, line 65-col.11, line 64, ie interface device 70 connected to data transfer controller 68 for converting usb signal to display signal output to display device included event ID stored in buffer 308(FIFO) when a request for transfer is made, the control 300 uses the event ID to access transfer control parameters, including logical address which generated sequentially and transfer to memory 72, AGP command generator requests transfer to or from the memory 72, the controller 300 writes the event ID into the interrupt buffer 304, the cpu indicate the availability of the data and the data transfer controller 68

arbitrate request and output to the display) the display interface conversion device converting the USB based display signals into the corresponding VGA signals and forwarding the VGA signals to the VGA controller. (col.9, lines 22-51, ie the peripheral(usb) interfaces 66 connected to interface device 70 comprising data transfer controller 38 allows communication from any peripherals via system bus 56 and stored data to memory 72, from memory 72 , data transfer controller process reconstruction and conversion and output to the display 34 via video controlling path 64, col.5, lines 4-52)

Finger discloses all the limitations as above except issuing a DMA control signal, a firmware control signal and control command data. However, Cheng discloses graphics data is transferred from system memory to graphics device using DMA bus-mastering and graphics commands from memory to device also use DMA bus-mastering. [0022]

It would have been obvious to one having ordinary skills in the art at the time the invention was made to incorporate Cheng's teaching into Finger's system so as it will be apparent that a solution to better integrate data buses within motherboards and graphics display devices is needed. [0006]

As per claim 10, Finger discloses wherein the bus control signal from the USB controller to the firmware interface comprises a PIO bus control signal. (fig.3, 70,

ie interface 66 provides I/O signals), (col.11, lines 40-65)

As per claim 11, Finger discloses wherein the firmware interface (fig.6, 68, ie data transfer controller) is connected to the display interface (fig.5, 64 video controlling paths) conversion device by a control bus and a data bus. (col.9, lines 22-51, ie the peripheral(usb) interfaces 66 connected to interface device 70 comprising data transfer controller 68 allows communication from any peripherals via system bus 56 (col.8, lines 41-53) and stored data to memory 72, from memory 72 , data processing system process reconstruction and conversion and output to the display)

As per claim 12, Finger discloses all the limitations as above except wherein the firmware interface is connected to the display interface conversion device by a DMA address control line, a DMA length control line, a DMA trigger control line, a firmware trigger control line and a data bus. However, Cheng discloses graphics data is transferred from system memory to graphics device using DMA bus-mastering and graphics commands from memory to device also use DMA bus-mastering. [0022]

It would have been obvious to one having ordinary skills in the art at the time the invention was made to incorporate Cheng's teaching into Finger's system so as it will be apparent that a solution to better integrate data buses within motherboards and graphics display devices is needed. [0006]

As per claim 13, Finger discloses wherein the first-in-first-out controller is connected to the USB controller by a control line and a data bus. (col.10, line 65-col.11, line 64, ie interface device 70 connected to data transfer controller 68 for converting usb signal to display signals and output to display 34, included event ID stored in buffer 308(FIFO) when a request for transfer is made, the control 300 uses the event ID to access transfer control parameters, including logical address which generated sequentially which implies FIFO manner)

As per claim 14, Finger discloses wherein the first-in-first-out controller is connected to the display interface conversion device by a control line and a data bus. (col.11, lines 40-65) (col.10, line 65-col.11, line 64, ie interface device 70 connected data transfer controller 68 for converting usb signal to display signals and output to the display 34 included event ID stored in buffer 308(FIFO) when a request for transfer is made, the control 300 uses the event ID to access transfer control parameters, including logical address transferring via data control line)

As per claim 15, Finger discloses wherein the VGA signals comprise PCI type VGA display signals. (col.12, lines 8-13)

As per claim 16, Finger discloses wherein the firmware interface, the first-in-first-out controller and the display interface conversion device are integrated in a

single chip integrated circuit. (fig.1, 62, data processing system)

As per claim 17, Finger discloses wherein the integrated circuit comprises a field programmable gate array integrated circuit. (fig.1, 62, data processing system)

As per claim 18, Finger discloses wherein the integrated circuit comprises an ASIC integrated circuit. (fig.1, 62, data processing system)

Conclusion

5. *Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kim Huynh whose telephone number is (571)272-3635 or via e-mail addressed to [kim.huynh3@uspto.gov]. The examiner can normally be reached on M-F 9.00AM- 6:00PM. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark Rinehart can be reached at (571)272-3632 or via e-mail addressed to [mark.Rinehart@uspto.gov].*

The fax phone numbers for the organization where this application or proceeding is assigned are (703)872-9306 for regular communications and After Final communications. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (571)272-2100.

Kim Huynh
March 6, 2005

TIM VO
PRIMARY EXAMINER

Notice of References Cited	Application/Control No. 10/316,013	Applicant(s)/Patent Under Reexamination LIU, PEI-CHUNG	
	Examiner Kim T. Huynh	Art Unit 2112	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
	A	US-6,824,797 B1	09-2003	Wheeler et al.	345/1.2
	B	US-2004/0153778 A1	08-2004	Cheng, Jeffrey Gongxian	714/026
	C	US-6,202,008 B1	03-2001	Beckert et al.	701/33
	D	US-2002/0135584 A1	09-2002	Lee, Eun Seog	345/531
	E	US-6,285,398 B1	09-2001	Shinsky et al.	348/223.1
	F	US-6,829,926 B1	10-2003	Finger et al.	600/437
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

2112

MR1115-429



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Pei-Chung Liu	:	Group
Serial No:	10/316,013	:	Art Unit #2112
Filed:	11 December 2002	:	Examiner:
Title:	USB-TO-VGA CONVERTER	:	K.T. Huynh

AMENDMENT

Mail Stop - Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Responsive to the Office Action dated 16 March 2005, please amend the above-referenced Patent Application as follows:

Amendments to the Claims are reflected in the Listing of Claims which begins on page 2 of this paper.

Remarks begin on page 7 of this paper.

IN THE CLAIMS:

This Listing of Claims will replace all prior versions, and listings, of claims in the subject Patent Application:

Listing of Claims:

1. (Currently amended) A USB-to-VGA converter for interconnecting a computer and a display device controlled thereby comprising:

a USB controller disposed external to the computer and adapted to connect to a USB port of a the computer for receiving USB based display signals from the computer, the USB controller issuing a bus control command;

a VGA controller disposed external to the computer and adapted to connect to a the display device for conveying VGA signals to the display device; and

a bridge disposed external to the computer and connected between the USB controller and the VGA controller, the bridge receiving the bus control command and issuing a first-in-first-out control signal to the USB controller to receive the USB based display signals from the USB controller in a first-in-first-out manner, the bridge circuit converting the USB based display signals into corresponding VGA signals and forwarding the VGA signals to the VGA controller which in turn applies the VGA signals to the display device.

2. (Original) The USB-to-VGA converter as claimed in Claim 1, wherein the USB controller comprises a USB socket.

3. (Original) The USB-to-VGA converter as claimed in Claim 1, wherein the VGA controller comprises a VGA plug.

4. (Original) The USB-to-VGA converter as claimed in Claim 1, wherein the converter is encased in an adaptor which comprises a USB socket for connection with the USB port of the computer.

5. (Original) The USB-to-VGA converter as claimed in Claim 4, wherein the adaptor further comprises a VGA plug for connection with the display device.

6. (Original) The USB-to-VGA converter as claimed in Claim 1, wherein the USB controller, the bridge circuit and the VGA controller are integrated with a display control circuit built inside the display device.

7. (Original) The USB-to-VGA converter as claimed in Claim 6, wherein the USB controller comprises a USB socket for connection with the USB port of the computer.

8. (Original) The USB-to-VGA converter as claimed in Claim 6, wherein the VGA controller is directly connected to the display control circuit of the display device.

9. (Original) The USB-to-VGA converter as claimed in Claim 1, wherein the bridge circuit comprising:

a firmware interface connected to the USB controller for receiving the bus control signal from the USB controller and issuing a DMA control signal, a firmware control signal and control command data;

a first-in-first-out controller connected to the USB controller for issuing the first-in-first-out control signal to the USB controller to receive the USB based display signals from the USB controller in a first-in-first-out manner; and

a display interface conversion device connected to the firmware interface, the first-in-first-out controller and the VGA controller for receiving the DMA control signal, the firmware control signal and the control command data from the firmware interface and being controlled by the first-in-first-out control signal from the first-in-first-out controller to receive the USB based display signals from the USB controller in a first-in-first-out manner, the display interface conversion device converting the USB based display signals into the corresponding VGA signals and forwarding the VGA signals to the VGA controller.

10. (Original) The USB-to-VGA converter as claimed in Claim 9, wherein the bus control signal from the USB controller to the firmware interface comprises a PIO bus control signal.

11. (Original) The USB-to-VGA converter as claimed in Claim 9, wherein the firmware interface is connected to the display interface conversion device by a control bus and a data bus.

12. (Original) The USB-to-VGA converter as claimed in Claim 9, wherein the firmware interface is connected to the display interface conversion device by a DMA address control line, a DMA length control line, a DMA trigger control line, a firmware trigger control line and a data bus.

13. (Original) The USB-to-VGA converter as claimed in Claim 9, wherein the first-in-first-out controller is connected to the USB controller by a control line and a data bus.

14. (Original) The USB-to-VGA converter as claimed in Claim 9, wherein the first-in-first-out controller is connected to the display interface conversion device by a control line and a data bus.

15. (Original) The USB-to-VGA converter as claimed in Claim 9, wherein the VGA signals comprise PCI type VGA display signals.

16. (Original) The USB-to-VGA converter as claimed in Claim 9, wherein the firmware interface, the first-in-first-out controller and the display interface conversion device are integrated in a single chip integrated circuit.

17. (Original) The USB-to-VGA converter as claimed in Claim 16, wherein the integrated circuit comprises a field programmable gate array integrated circuit.

18. (Original) The USB-to-VGA converter as claimed in Claim 16, wherein the integrated circuit comprises an ASIC integrated circuit.

19. (New) A discrete USB-to-VGA converter for externally interconnecting a computer and a display device controlled thereby comprising:

a USB controller disposed external to the computer and detachably connected to a USB port of the computer for receiving USB based display signals from the computer, the USB controller issuing a bus control command;

a VGA controller disposed external to the computer for connection to the display device for conveying VGA signals to the display device; and

a bridge disposed external to the computer and connected between the USB controller and the VGA controller, the bridge receiving the bus control command and issuing a first-in-first-out control signal to the USB controller to receive the USB based display signals from the USB controller in a first-in-first-out manner, the bridge circuit converting the USB based display signals into corresponding VGA signals and forwarding the VGA signals to the VGA controller which in turn applies the VGA signals to the display device.

REMARKS

This case has been carefully reviewed and analyzed in view of the Office Action dated 16 March 2005. Responsive to that Office Action, Claim 1 is now amended and Claim 19 newly-inserted for further prosecution with the other pending Claims. It is believed that with such amendment and insertion of Claims, there is a further clarification of the pending Claims' recitations.

In the Office Action, the Examiner rejected Claims 1-8 under 35 U.S.C. § 102(e) as being anticipated by the Finger, et al. reference. The Examiner also rejected Claims 9-18 under 35 U.S.C. § 103(a) as being unpatentable over Finger, et al. in view of the Cheng reference. In setting forth the latter rejection, the Examiner acknowledged that Finger, et al. fails to disclose the use of a DMA control signal, a firmware control signal, or control command data. The Examiner, however, cited Cheng for disclosing these features and concluded that it would have been obvious to one of ordinary skill in the art to have incorporated as much into the Finger, et al. system, so as to better integrate data buses within motherboards and graphics display devices. The Examiner also cited Cheng for disclosing various DMA control lines as well as a firmware trigger control line and a data bus, concluding again that it would have been obvious to one of ordinary skill in the art to have incorporated such features into the Finger, et al. system for better integration of data buses.

As each of the newly-amended independent Claim 1 and newly-inserted independent Claim 19 each now more clearly recite, Applicant's converter is one which "interconnect[s] a computer and a display device controlled thereby." The converter includes among its combination of features a USB controller, a VGA controller, and a bridge connected therebetween, each of which is "disposed external to the computer," as Claims 1 and 19 also now more clearly recite. The requisite interface capability for driving a display device typically provided through graphics cards or other such measures integrated into the controlling computer is thereby "disposed external to the computer."

The full combination of these and other features now more clearly recited by Applicant's pending Claims is nowhere disclosed by the cited references. Note in this regard that the peripheral interfaces 66, video/audio reconstruction pad 64, and memory port-containing interface device 70 – which the Examiner respectively correlated to the claimed USB controller, VGA controller, and bridge - are prescribed to be formed in the data processing system 52 itself. That is, these devices are built into the computer-based system 52 which controls the various external devices, including a display 34, connected directly thereto. This teaches quite plainly away from any USB-to-VGA converter having "a USB controller disposed external to the computer," "a VGA controller disposed external to the computer," and "a bridge disposed external to the computer," as Claims 1 and 19 each now more clearly recites.

Note also that within Finger, et al.'s data processing system 52, each of the internal devices 66, 64, and 70 are shown separately connected to a shared system bus, without direct interconnection therebetween. This teaches away from the operational structure of Applicant's converter, wherein "a bridge ... [is] connected between the USB controller and the VGA controller," as Claims 1 and 19 also now more clearly recite.

Given such contrary teachings of the primarily-cited Finger, et al. reference, the teachings of the secondarily-cited Cheng reference are found to be quite ineffectual to the present patentability analysis. The Examiner merely cited Cheng for disclosing DMA control capabilities, the reference's focus being the better integration of data buses within motherboard-equipped systems. Such actively departs from the features now more clearly recited by Applicant's pending independent Claims 1 and 19.

It is respectfully submitted, therefore, that the cited Finger, et al. and Cheng references, even when considered together, fail to disclose the unique combination of elements now more clearly recited by Applicant's pending Claims for the purposes and objectives disclosed in the subject Patent Application.

The other references cited by the Examiner but not used in the rejection are found to be further remote from Applicant's claimed converter when patentability considerations are taken properly into account.

It is now believed that the subject Patent Application has been placed in condition for allowance, and such action is respectfully requested.

Respectfully submitted,
For: ROSENBERG, KLEIN & LEE

Jun Y. Lee
Registration #40,262

Dated: 15 June 2005

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/316,013	12/11/2002	Pei-Chung Liu	MR1115-429	2895

4586 7590 09/01/2005

ROSENBERG, KLEIN & LEE
3458 ELLICOTT CENTER DRIVE-SUITE 101
ELLICOTT CITY, MD 21043

EXAMINER	
HUYNH, KIM T	

ART UNIT	PAPER NUMBER
2112	

DATE MAILED: 09/01/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

PTO-90C (Rev. 10/03)

Office Action Summary	Application No.	Applicant(s)	
	10/316,013	LIU, PEI-CHUNG	
	Examiner	Art Unit	
	Kim T. Huynh	2112	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 June 2005*.

2a)☒ This action is FINAL. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12/11/02* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

U.S. Patent and Trademark Office
PTOL-326 (Rev. 1-04) Office Action Summary Part of Paper No./Mail Date 20050823

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-8, 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Finger et al. (US Patent 6,629,926) in view of Beckert et al. (US Patent 6,175,789)

As per claims 1, 19, Finger discloses a USB-to-VGA converter for interconnecting computer and a display device controlled thereby comprising:

- a USB controller(fig.2, 66 ie peripheral interface includes usb controller) adapted to connect to a USB port of a computer for receiving USB based display signals from the computer, the USB controller issuing a bus control command; (col.9, lines 22-51, ie the peripheral(usb) interfaces 66 connected to data processing system 52 allows communication from any peripherals via system bus 56 (col.8, lines 41-53) and stored data to memory 72, from memory 72 , data processing system process reconstruction and conversion and output to the display)
- a VGA controller(fig.5, 64 video controlling paths) adapted to connect to a display device for conveying VGA signals to the display device(fig.5, 34 ie display device); and (col.4, lines 12-21, ie data provide by peripherals to

data processing system 52 process and reconstruction and conversion and output to the display 34)

- a bridge(fig.2, 70, ie interface device) connected between the USB controller and the VGA controller the bridge receiving the bus control command and issuing a first-in-first-out control signal to the USB controller to receive the USB based display signals from the USB controller in a first-in-first-out manner (col.10, line 65-col.11, line 64, ie interface device 70 connected to data transfer controller 68 for converting USB signal to the display signals and output to the display 34, included event ID stored in buffer 308(FIFO) when a request for transfer is made, the control 300 uses the event ID to access transfer control parameters, including logical address which generated sequentially which implies FIFO manner) the bridge circuit converting the USB based display signals into corresponding VGA signals and forwarding the VGA signals to the VGA controller which in turn applies the VGA signals to the display device. (col.9, lines 22-51, ie the peripheral(usb) interfaces 66 connected to interface device 70 comprising data transfer controller 68 allows communication from any peripherals via system bus 56 and stored data to memory 72, from memory 72 , data transfer controller process reconstruction and conversion and output to the display 34 via video controlling path 64, col.5, lines 4-52)

Finger discloses all the limitations as above except features of a USB controller, a VGA controller and a bridge each of which is disposed external to the computer. However, Berkert discloses the support module 62 resides in stationary base unit 46(disposed external to the computer) which includes a USB interface 92 is driven from the bus and provides the interconnection to the various usb peripherals and a VGA controller 94 is provides on the support module 62 to drive the display 24. The usb interface and VGA controller incorporated into the logic 90. (col.5, lines 39-67, figures 1 and 3)

It would have been obvious to one having ordinary skills in the art at the time the invention was made to incorporate Berkert's teaching into Finger's system so as to offer a general purpose computing platform that allows for easy expandability. (col.2, lines 8-17)

As per claim 2, Finger discloses wherein the USB controller comprises a USB socket. (fig.7, 200, the adaptor module, col.10, lines 11-40)

As per claim 3, Finger discloses wherein the VGA controller comprises a VGA plug. (col.11, lines 40-65), (fig.5, 64, video controlling paths connected to display device 34 via controlling of fig.6, 68 ie data transfer controller)

As per claim 4, Finger discloses wherein the converter is encased in an adaptor which comprises a USB socket for connection with the USB port of the computer.

(fig.7, 200, ie the adaptor module), (col.10, lines 11-40)

As per claim 5, Finger discloses wherein the adaptor further comprises a VGA plug for connection with the display device. (fig.5, 64, video controlling paths connected to display device 34 via fig.6, 68 ie data transfer controller)

As per claim 6, Finger discloses wherein the USB controller, the bridge circuit and the VGA controller are integrated with a display control circuit built inside the display device. (fig1, 62, ie data processing system)

As per claim 7, Finger discloses wherein the USB controller comprises a USB socket for connection with the USB port of the computer. (col.9, lines 22-51, ie the peripheral(usb) interfaces 66 allow communication from any the various peripheral to data processing system 62)

As per claim 8, Finger discloses wherein the VGA controller is directly connected to the display control circuit of the display device. (fig.5, 64, video controlling paths connected to display device 34 via fig.6, 68 ie data transfer controller)

3. Claims 9-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Finger et al. (US Patent 6,629,926) in view of Beckert et al. (US Patent 6,175,789) and further in view of Cheng (Pub No US20040153778)

As per claim 9, the modified of Finger discloses wherein the bridge circuit comprising:

- a firmware interface (fig.2, 70 ie interface device) connected to the USB controller for receiving the bus control signal from the USB controller and; (col.9, lines 22-51, ie the peripheral(usb) interfaces 66 connected to interface device 70 comprising data transfer controller 68 allows communication from any peripherals via system bus 56 ,col.8, lines 41-53)
- a first-in-first-out controller connected to the USB controller for issuing the first-in-first-out control signal to the USB controller to receive the USB based display signals from the USB controller in a first-in-first-out manner ; and (col.10, line 65-col.11, line 64, ie interface device 70 connected to data transfer controller 68 for converting usb signal into display signals and output to the display 34, included event ID stored in buffer 308(FIFO) when a request for transfer is made, the control 300 uses the event ID to access transfer control parameters, including logical address which generated sequentially which implies FIFO manner)
- a display interface conversion device connected to the firmware interface, the first-in-first-out controller and the VGA controller (fig.5, 64 video controlling paths) for receiving the control signal, the firmware control signal and the control command data from the firmware interface and being controlled by the first-in-first-out control signal from the first-in-first-out controller to receive the USB based display signals from the USB

controller in a first-in-first-out manner(col.10, line 65-col.11, line 64, ie interface device 70 connected to data transfer controller 68 for converting usb signal to display signal output to display device included event ID stored in buffer 308(FIFO) when a request for transfer is made, the control 300 uses the event ID to access transfer control parameters, including logical address which generated sequentially and transfer to memory 72, AGP command generator requests transfer to or from the memory 72, the controller 300 writes the event ID into the interrupt buffer 304, the cpu indicate the availability of the data and the data transfer controller 68 arbitrate request and output to the display) the display interface conversion device converting the USB based display signals into the corresponding VGA signals and forwarding the VGA signals to the VGA controller. (col.9, lines 22-51, ie the peripheral(usb) interfaces 66 connected to interface device 70 comprising data transfer controller 38 allows communication from any peripherals via system bus 56 and stored data to memory 72, from memory 72 , data transfer controller process reconstruction and conversion and output to the display 34 via video controlling path 64, col.5, lines 4-52)

Finger discloses all the limitations as above except issuing a DMA control signal, a firmware control signal and control command data. However, Cheng discloses graphics data is transferred from system

memory to graphics device using DMA bus-mastering and graphics commands from memory to device also use DMA bus-mastering. [0022]

It would have been obvious to one having ordinary skills in the art at the time the invention was made to incorporate Cheng's teaching into Finger's system so as it will be apparent that a solution to better integrate data buses within motherboards and graphics display devices is needed. [0006]

As per claim 10, Finger discloses wherein the bus control signal from the USB controller to the firmware interface comprises a PIO bus control signal. (fig.3, 70, ie interface 66 provides I/O signals), (col.11, lines 40-65)

As per claim 11, Finger discloses wherein the firmware interface (fig.6, 68 ie data transfer controller) is connected to the display interface (fig.5, 64 video controlling paths) conversion device by a control bus and a data bus. (col.9, lines 22-51, ie the peripheral(usb) interfaces 66 connected to interface device 70 comprising data transfer controller 68 allows communication from any peripherals via system bus 56 (col.8, lines 41-53) and stored data to memory 72, from memory 72 , data processing system process reconstruction and conversion and output to the display)

As per claim 12, Finger discloses all the limitations as above except wherein the

firmware interface is connected to the display interface conversion device by a DMA address control line, a DMA length control line, a DMA trigger control line, a firmware trigger control line and a data bus. However, Cheng discloses graphics data is transferred from system memory to graphics device using DMA bus-mastering and graphics commands from memory to device also use DMA bus-mastering. [0022]

It would have been obvious to one having ordinary skills in the art at the time the invention was made to incorporate Cheng's teaching into Finger's system so as it will be apparent that a solution to better integrate data buses within motherboards and graphics display devices is needed. [0006]

As per claim 13, Finger discloses wherein the first-in-first-out controller is connected to the USB controller by a control line and a data bus. (col.10, line 65-col.11, line 64, ie interface device 70 connected to data transfer controller 68 for converting usb signal to display signals and output to display 34, included event ID stored in buffer 308(FIFO) when a request for transfer is made, the control 300 uses the event ID to access transfer control parameters, including logical address which generated sequentially which implies FIFO manner)

As per claim 14, Finger discloses wherein the first-in-first-out controller is connected to the display interface conversion device by a control line and a data bus. (col.11, lines 40-65) (col.10, line 65-col.11, line 64, ie interface device 70

connected data transfer controller 68 for converting usb signal to display signals and output to the display 34 included event ID stored in buffer 308(FIFO) when a request for transfer is made, the control 300 uses the event ID to access transfer control parameters, including logical address transferring via data control line)

As per claim 15, Finger discloses wherein the VGA signals comprise PCI type VGA display signals. (col.12, lines 8-13)

As per claim 16, Finger discloses wherein the firmware interface, the first-in-first-out controller and the display interface conversion device are integrated in a single chip integrated circuit. (fig.1, 62, data processing system)

As per claim 17, Finger discloses wherein the integrated circuit comprises a field programmable gate array integrated circuit. (fig.1, 62, data processing system)

As per claim 18, Finger discloses wherein the integrated circuit comprises an ASIC integrated circuit. (fig.1, 62, data processing system)

Response to Amendment

4. Applicant's amendment filed on 6/16/05 have been fully considered but are moot in view of the new ground(s) of rejection.

Conclusion

5. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL.** See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

6. *Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kim Huynh whose telephone number is (571)272-3635 or via e-mail addressed to [kim.huynh3@uspto.gov]. The examiner can normally be reached on M-F 9:00AM- 6:00PM. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rehana Perveen can be reached at (571)272-3676 or via e-mail addressed to [rehana.perveen@uspto.gov].*

The fax phone numbers for the organization where this application or proceeding is assigned are (571)273-8300 for regular communications and After Final communications. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (571)272-2100.

Kim Huynh

August 22, 2005

Khanh Dang
Primary Examiner

Notice of References Cited	Application/Control No. 10/316,013	Applicant(s)/Patent Under Reexamination LIU, PEI-CHUNG	
	Examiner Kim T. Huynh	Art Unit 2112	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
	A	US-6,175,789 B1	01-2001	Beckert et al.	701/33
	B	US-2001/0032280	10-2001	Osakada et al.	710/129
	C	US-			
	D	US-			
	E	US-			
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

OIPE JAN 17 2006 PATENT & TRADEMARK OFFICE

MR1115-429

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Pei-Chung Liu	:	Group
Serial No:	10/316,013	:	Art Unit #2112
Filed:	11 December 2002	:	Examiner:
Title:	USB-TO-VGA CONVERTER	:	K.T. Huynh

REQUEST FOR EXTENSION OF TIME UNDER RULE 1.136

Honorable Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Applicant hereby requests an Extension of Time for two (2) months to respond to the outstanding Official Action dated 1 September 2005. With this Request for Extension of Time being granted, the Applicant shall have to and including 1 February 2006 to respond to the outstanding Official Action. In fact, an Amendment is being filed concurrently with this Request for Extension of Time.

A check in the amount of $225.00 is hereby enclosed to cover the filing fees associated with this Extension of Time. If there are any further fees necessary in this filing, the Director of Patents and Trademarks is hereby authorized to charge Deposit Account #18-2011 for such additional charges.

Respectfully submitted,
For: ROSENBERG, KLEIN & LEE

Jun Y. Lee
Registration #40,262

Dated: 1/16/2006

01/18/2006 HALI11 00000008 10316013
01 FC:2252 225.00 OP

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Customer No. 04586

RCE

PTO/SB/30 (04-05)
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Request for Continued Examination (RCE) Transmittal

Address to:
Mail Stop RCE
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

JAN 17 2006 PATENT & TRADEMARK OFFICE USPTO

Application Number	10/316,013
Filing Date	11 DECEMBER 2002
First Named Inventor	PEI-CHUNG LIU
Art Unit	2112
Examiner Name	K.T. HUYNH
Attorney Docket Number	MR1115-429

This is a Request for Continued Examination (RCE) under 37 CFR 1.114 of the above-identified application.
Request for Continued Examination (RCE) practice under 37 CFR 1.114 does not apply to any utility or plant application filed prior to June 8, 1995, or to any design application. See Instruction Sheet for RCEs (not to be submitted to the USPTO) on page 2.

1. Submission required under 37 CFR 1.114 Note: If the RCE is proper, any previously filed unentered amendments and amendments enclosed with the RCE will be entered in the order in which they were filed unless applicant instructs otherwise. If applicant does not wish to have any previously filed unentered amendment(s) entered, applicant must request non-entry of such amendment(s).

   a. ☐ Previously submitted. If a final Office action is outstanding, any amendments filed after the final Office action may be considered as a submission even if this box is not checked.
      i. ☐ Consider the arguments in the Appeal Brief or Reply Brief previously filed on _____
      ii. ☐ Other _____

   b. ☑ Enclosed
      i. ☑ Amendment/Reply
      ii. ☐ Affidavit(s)/ Declaration(s)
      iii. ☐ Information Disclosure Statement (IDS)
      iv. ☑ Other 2-Month Extension of Time

2. Miscellaneous
   a. ☐ Suspension of action on the above-identified application is requested under 37 CFR 1.103(c) for a period of _____ months. (Period of suspension shall not exceed 3 months; Fee under 37 CFR 1.17(i) required)
   b. ☐ Other _____

3. Fees The RCE fee under 37 CFR 1.17(e) is required by 37 CFR 1.114 when the RCE is filed.
   The Director is hereby authorized to charge the following fees, any underpayment of fees, or credit any overpayments, to
   a. ☑ Deposit Account No. 18-2011. I have enclosed a duplicate copy of this sheet.
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      ii. ☐ Extension of time fee (37 CFR 1.136 and 1.17)
      iii. ☑ Other deficiencies associated with this filing only.
   b. ☑ Check in the amount of $ 620.00 enclosed ($395 - RCE Fee; $225 - Extension Fee)
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SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT REQUIRED

Signature		Date	1/16/2006
Name (Print/Type)	Jun Y. Lee	Registration No.	40,262

CERTIFICATE OF MAILING OR TRANSMISSION

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to: Mail Stop RCE, Commissioner for Patents, P. O. Box 1450, Alexandria, VA 22313-1450 or facsimile transmitted to the U.S. Patent and Trademark Office on the date shown below.

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This collection of information is required by 37 CFR 1.114. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: **Mail Stop RCE, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**
If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

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MR1115-429

OIPE JAN 17 2006 PATENT & TRADEMARK OFFICE

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Pei-Chung Liu	:	Group
Serial No:	10/316,013	:	Art Unit #2112
Filed:	11 December 2002	:	Examiner:
Title:	USB-TO-VGA CONVERTER	:	K.T. Huynh

AMENDMENT AFTER FINAL OFFICE ACTION

Mail Stop - AF
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

The Examiner issued a Final Office Action dated 1 September 2005 in the above-referenced Patent Application. In that Office Action, the Examiner set a three-month shortened statutory period for reply. The reply period having now expired, a Request and Fee for a Two-month Extension of Time is concurrently filed herewith to ensure timely filing.

Responsive to the Office Action dated 1 September 2005 and the discussions had at the interview, please amend the above-referenced Patent Application as follows:

Amendments to the Claims are reflected in the Listing of Claims which begins on page 2 of this paper.

Remarks begin on page 8 of this paper.

IN THE CLAIMS:

This Listing of Claims will replace all prior versions, and listings, of claims in the subject Patent Application:

Listing of Claims:

1. (Currently amended) A USB-to-VGA converter for interconnecting a computer and a display device controlled thereby comprising:

a USB controller disposed external to the computer and adapted to detachably connect to a USB port of the computer for receiving USB based display signals from the computer, the USB controller issuing a bus control command;

a VGA controller disposed external to the computer and adapted to connect to the display device for conveying VGA signals to the display device; and

a bridge disposed external to the computer and connecting ~~connected between~~ the USB controller and the VGA controller one to the other for the passage of data therebetween, the bridge receiving the bus control command and issuing a first-in-first-out control signal to the USB controller to receive the USB based display signals from the USB controller in a first-in-first-out manner, the bridge circuit converting the USB based display signals into corresponding VGA signals and forwarding the VGA signals to the VGA controller which in turn applies the VGA signals to the display device.

2. (Original) The USB-to-VGA converter as claimed in Claim 1, wherein the USB controller comprises a USB socket.

3. (Original) The USB-to-VGA converter as claimed in Claim 1, wherein the VGA controller comprises a VGA plug.

4. (Original) The USB-to-VGA converter as claimed in Claim 1, wherein the converter is encased in an adaptor which comprises a USB socket for connection with the USB port of the computer.

5. (Original) The USB-to-VGA converter as claimed in Claim 4, wherein the adaptor further comprises a VGA plug for connection with the display device.

6. (Original) The USB-to-VGA converter as claimed in Claim 1, wherein the USB controller, the bridge circuit and the VGA controller are integrated with a display control circuit built inside the display device.

7. (Original) The USB-to-VGA converter as claimed in Claim 6, wherein the USB controller comprises a USB socket for connection with the USB port of the computer.

8. (Original) The USB-to-VGA converter as claimed in Claim 6, wherein the VGA controller is directly connected to the display control circuit of the display device.

9. (Original) The USB-to-VGA converter as claimed in Claim 1, wherein the bridge circuit comprising:

a firmware interface connected to the USB controller for receiving the bus control signal from the USB controller and issuing a DMA control signal, a firmware control signal and control command data;

a first-in-first-out controller connected to the USB controller for issuing the first-in-first-out control signal to the USB controller to receive the USB based display signals from the USB controller in a first-in-first-out manner; and

a display interface conversion device connected to the firmware interface, the first-in-first-out controller and the VGA controller for receiving the DMA control signal, the firmware control signal and the control command data from the firmware interface and being controlled by the first-in-first-out control signal from the first-in-first-out controller to receive the USB based display signals from the USB controller in a first-in-first-out manner, the display interface conversion device converting the USB based display signals into the corresponding VGA signals and forwarding the VGA signals to the VGA controller.

10. (Original) The USB-to-VGA converter as claimed in Claim 9, wherein the bus control signal from the USB controller to the firmware interface comprises a PIO bus control signal.

11. (Original) The USB-to-VGA converter as claimed in Claim 9, wherein the firmware interface is connected to the display interface conversion device by a control bus and a data bus.

12. (Original) The USB-to-VGA converter as claimed in Claim 9, wherein the firmware interface is connected to the display interface conversion device by a DMA address control line, a DMA length control line, a DMA trigger control line, a firmware trigger control line and a data bus.

13. (Original) The USB-to-VGA converter as claimed in Claim 9, wherein the first-in-first-out controller is connected to the USB controller by a control line and a data bus.

14. (Original) The USB-to-VGA converter as claimed in Claim 9, wherein the first-in-first-out controller is connected to the display interface conversion device by a control line and a data bus.

15. (Original) The USB-to-VGA converter as claimed in Claim 9, wherein the VGA signals comprise PCI type VGA display signals.

16. (Original) The USB-to-VGA converter as claimed in Claim 9, wherein the firmware interface, the first-in-first-out controller and the display interface conversion device are integrated in a single chip integrated circuit.

17. (Original) The USB-to-VGA converter as claimed in Claim 16, wherein the integrated circuit comprises a field programmable gate array integrated circuit.

18. (Original) The USB-to-VGA converter as claimed in Claim 16, wherein the integrated circuit comprises an ASIC integrated circuit.

19. (Currently amended) A discrete USB-to-VGA converter for externally interconnecting in detachable manner a computer and a display device controlled thereby comprising:

a USB controller disposed external to the computer and detachably connected to a USB port of the computer for receiving USB based display signals from the computer, the USB controller issuing a bus control command;

a VGA controller disposed external to the computer for connection to the display device for conveying VGA signals to the display device; and

a bridge disposed external to the computer and interconnecting ~~connected between~~ the USB controller and the VGA controller one to the other for the passage of data therebetween, the bridge receiving the bus control command and issuing a first-in-first-out control signal to the USB controller to receive the USB based display signals from the USB controller in a first-in-first-out manner, the bridge circuit converting the USB based display signals into corresponding VGA signals and

forwarding the VGA signals to the VGA controller which in turn applies the VGA signals to the display device.

REMARKS

Responsive to the Final Office Action dated 1 September 2005, Claims 1 and 19 are amended for further prosecution with the other pending Claims. It is believed that with such amendment of Claims, there is a further clarification of the pending Claims' recitations.

In the Office Action, the Examiner rejected Claims 1-8 and 19 under 35 U.S.C. § 103(a) as being unpatentable over the Finger, et al. reference in view of the Beckert, et al. reference. The Examiner acknowledged in this regard that Finger, et al. fails to disclose a USB controller, VGA controller, and bridge disposed external to a computer, cut cited Beckert, et al. for disclosing as much in its support module 62. The Examiner stated that Becker, et al.'s support module 62 resides in a stationary base unit 46 which is disposed external to the computer (referring presumably to the computer module 64). The Examiner then concluded that it would have been obvious to one of ordinary skill in the art to have incorporated Beckert, et al.'s disclosed features into the Finger, et al. system to arrive at the claimed apparatus.

Also in the Office Action, the Examiner rejected Claims 9-18 under 35 U.S.C. § 103(a) as being unpatentable over Finger, et al. in view of Beckert, et al., further in view of the Cheng reference. In this regard, the Examiner cited Cheng for disclosing the use of DMA bus-mastering commands, and concluded that it

would have been obvious to one of ordinary skill in the art to have incorporated such feature into the Finger, et al. system.

As newly-amended independent Claims 1 and 19 each now more clearly recite, Applicant's USB-TO-VGA converter includes among its combination of features "a USB controller disposed external" to the given "computer" which "detachably connect[s] to a USB port of the computer," as well as a VGA controller also "disposed external to the computer." The USB-TO-VGA converter includes in addition a bridge disposed external to the computer that connects "the USB controller and the VGA controller one to the other for the passage of data therebetween," as each of the newly-amended independent Claims 1 and 19 also now more clearly recites.

The full combination of these and other features now more clearly recited by Applicant's pending Claims is nowhere disclosed by the cited references. As the Examiner readily acknowledged, the primarily-cited Finger, et al. reference fails to disclose any USB controller, VGA controller, and bridge disposed external to the given computer. Even beyond this, though, Finger, et al.'s peripheral interfaces 66, video/audio reconstruction and output 64, and interface device 70 (which the Examiner correlated respectively to the claimed USB controller, VGA, controller and bridge) merely share the same system bus 50. It does not follow that because they utilize the same system bus 50 for their respective purposes that

these functional components necessarily interact during operation in the manner now more clearly set forth in each of the newly-amended independent Claims 1 and 19. Indeed, Finger, et al. makes apparent that these system components 66, 64, and 70 typically operate rather independently. This teaches plainly away from a bridge that actually interconnects "the USB controller and the VGA controller one to the other for the passage of data therebetween," as Claims 1 and 19 now more clearly recite.

Referring to the Beckert, et al. reference which the Examiner cited for disclosing the disposition of certain components external to the computer, the reference discloses a computer system 22 prescribed to be mounted in a vehicle's dashboard. As such, such functional modules of Becker, et al. as the support module 62 and computer module 64 are both integrated into the "centralized computer 22." As Beckert, et al. specifically prescribes, not only does the "support module 62 reside[ ] in the typically stationary base unit 46 ... that is mounted in the vehicle dashboard, ... the computer module 64 resides in the dashboard-mounted base unit 46" as well (column 5; lines 40-42 and column 6; lines 47-48).

Thus, Becker, et al.'s support module 62, which the Examiner cited for containing the USB controller, VGA controller, and bridge of Applicant's Claims, is necessarily provided as a built-in part of Becker, et al.'s dashboard-mounted

computer system, not as a separate part "external" thereto. Even if the computer module 64, rather than the actual centralized computer 22, were taken to be the given "computer," that support module 62 is built into the same dashboard-mounted base unit 46 with the computer module 64. It could hardly be considered "detachably connect[ed]" to such computer module 64, as Claims 1 and 19 recite.

If these were not significant departures enough from the claimed subject matter, the USB interface 92 and VGA controller 94 of Becker, et al.'s support module 62 are not in any way prescribed by the reference to be, nor are they intended to be, connected "one to the other for the passage of data therebetween" (as Claims 1 and 19 also now more clearly recite). To the contrary, Becker, et al. plainly prescribes each to serve separate, not necessarily related, purposes. The reference notes that the "USB interface 92 is driven from the PCI bus 66 and provides the interconnection to the various USB peripherals shown in Fig. 2," whereas the "VGA controller 94 is provided on the support module 62 to drive the display 24," (column 5; lines 57-59 and lines 62-63).

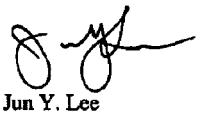
Given such contrary teachings of the Finger, et al. and Beckert, et al. references, the secondarily-cited Cheng reference is found to be quite ineffectual to the present patentability analysis. Cheng was merely cited for disclosing the use of DMA bus-mastering commands. The reference nowhere relates otherwise to any other deficiencies of the Finger, et al. and Beckert, et al. disclosures.

It is respectfully submitted, therefore, that the cited Finger, et al., Beckert, et al., and Cheng references, even when considered together, fail to disclose the unique combination of elements now more clearly recited by Applicant's pending Claims for the purposes and objectives disclosed in the subject Patent Application. In fact, the references teach quite clearly away from the claimed subject matter in certain notable respects.

The other references cited by the Examiner but not used in the rejection are believed to be further remote from Applicant's claimed apparatus when patentability considerations are taken properly into account.

It is now believed that the subject Patent Application has been placed fully in condition for allowance, and such action is respectfully requested.

Respectfully submitted,
For: ROSENBERG, KLEIN & LEE



Jun Y. Lee
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Dated: 1/16/2006

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TGW 2112

MR1115-429



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Pei-Chung Liu	:	Group
Serial No:	10/316,013	:	Art Unit #2112
Filed:	11 December 2002	:	Examiner:
Title:	USB-TO-VGA CONVERTER	:	K.T. Huynh

SUPPLEMENTAL AMENDMENT AND STATEMENT OF THE SUBSTANCE OF INTERVIEW

Mail Stop - AMENDMENT
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

An interview of the Examiner her supervising Examiner was conducted by the undersigned Attorney at the U.S. Patent and Trademark Office on 1 March 2006. Responsive to the discussions had at the interview, and as a supplement to the earlier-filed 16 January 2006 Amendment, please further amend the above-referenced Patent Application as follows:

Amendments to the Claims are reflected in the Listing of Claims which begins on page 2 of this paper.

Remarks begin on page 8 of this paper.

IN THE CLAIMS:

This Listing of Claims will replace all prior versions, and listings, of claims in the subject Patent Application:

Listing of Claims:

1. (Currently amended) A USB-to-VGA converter ~~for~~ interconnecting through a USB port of a computer ~~and~~ a display device controlled ~~thereby~~ the computer comprising:

a USB controller disposed external to the computer and adapted to detachably connect to a USB port of the computer for receiving exclusively therethrough USB based display signals from the computer, the USB controller issuing a bus control command;

a VGA controller disposed external to the computer and adapted to connect to the display device for conveying VGA signals to the display device; and

a bridge disposed external to the computer and connecting the USB controller and the VGA controller one to the other for the passage of data therebetween, the bridge receiving the bus control command and issuing a first-in-first-out control signal to the USB controller to receive the USB based display signals from the USB controller in a first-in-first-out manner, the bridge circuit converting the USB based display signals into corresponding VGA signals and forwarding the VGA signals to the VGA controller which in turn applies the VGA signals to the display device.

2. (Original) The USB-to-VGA converter as claimed in Claim 1, wherein the USB controller comprises a USB socket.

3. (Original) The USB-to-VGA converter as claimed in Claim 1, wherein the VGA controller comprises a VGA plug.

4. (Original) The USB-to-VGA converter as claimed in Claim 1, wherein the converter is encased in an adaptor which comprises a USB socket for connection with the USB port of the computer.

5. (Original) The USB-to-VGA converter as claimed in Claim 4, wherein the adaptor further comprises a VGA plug for connection with the display device.

6. (Original) The USB-to-VGA converter as claimed in Claim 1, wherein the USB controller, the bridge circuit and the VGA controller are integrated with a display control circuit built inside the display device.

7. (Original) The USB-to-VGA converter as claimed in Claim 6, wherein the USB controller comprises a USB socket for connection with the USB port of the computer.

8. (Original) The USB-to-VGA converter as claimed in Claim 6, wherein the VGA controller is directly connected to the display control circuit of the display device.

9. (Original) The USB-to-VGA converter as claimed in Claim 1, wherein the bridge circuit comprising:

a firmware interface connected to the USB controller for receiving the bus control signal from the USB controller and issuing a DMA control signal, a firmware control signal and control command data;

a first-in-first-out controller connected to the USB controller for issuing the first-in-first-out control signal to the USB controller to receive the USB based display signals from the USB controller in a first-in-first-out manner; and

a display interface conversion device connected to the firmware interface, the first-in-first-out controller and the VGA controller for receiving the DMA control signal, the firmware control signal and the control command data from the firmware interface and being controlled by the first-in-first-out control signal from the first-in-first-out controller to receive the USB based display signals from the USB controller in a first-in-first-out manner, the display interface conversion device converting the USB based display signals into the corresponding VGA signals and forwarding the VGA signals to the VGA controller.

10. (Original) The USB-to-VGA converter as claimed in Claim 9, wherein the bus control signal from the USB controller to the firmware interface comprises a PIO bus control signal.

11. (Original) The USB-to-VGA converter as claimed in Claim 9, wherein the firmware interface is connected to the display interface conversion device by a control bus and a data bus.

12. (Original) The USB-to-VGA converter as claimed in Claim 9, wherein the firmware interface is connected to the display interface conversion device by a DMA address control line, a DMA length control line, a DMA trigger control line, a firmware trigger control line and a data bus.

13. (Original) The USB-to-VGA converter as claimed in Claim 9, wherein the first-in-first-out controller is connected to the USB controller by a control line and a data bus.

14. (Original) The USB-to-VGA converter as claimed in Claim 9, wherein the first-in-first-out controller is connected to the display interface conversion device by a control line and a data bus.

15. (Original) The USB-to-VGA converter as claimed in Claim 9, wherein the VGA signals comprise PCI type VGA display signals.

16. (Original) The USB-to-VGA converter as claimed in Claim 9, wherein the firmware interface, the first-in-first-out controller and the display interface conversion device are integrated in a single chip integrated circuit.

17. (Original) The USB-to-VGA converter as claimed in Claim 16, wherein the integrated circuit comprises a field programmable gate array integrated circuit.

18. (Original) The USB-to-VGA converter as claimed in Claim 16, wherein the integrated circuit comprises an ASIC integrated circuit.

19. (Currently amended) A discrete USB-to-VGA converter ~~for~~ externally interconnecting in detachable manner through a USB port of a computer ~~and~~ a display device controlled ~~thereby~~ the computer comprising:

a USB controller disposed external to the computer and detachably connected to a USB port of the computer for receiving exclusively therethrough USB based display signals from the computer, the USB controller issuing a bus control command;

a VGA controller disposed external to the computer for connection to the display device for conveying VGA signals to the display device; and

a bridge disposed external to the computer and interconnecting the USB controller and the VGA controller one to the other for the passage of data therebetween, the bridge receiving the bus control command and issuing a first-in-first-out control signal to the USB controller to receive the USB based display signals from the USB controller in a first-in-first-out manner, the bridge circuit converting the USB based display signals into

corresponding VGA signals and forwarding the VGA signals to the VGA controller which in turn applies the VGA signals to the display device.

REMARKS

At the outset, the courtesies extended by the Examiner and her supervising Examiner in granting the 1 March 2006 interview are appreciatively noted. At the interview, certain of the references cited by the Examiner in the 1 September 2005 Office Action were discussed in light of the Claims amendments incorporated by the 16 January 2006 Amendment, and the further clarifying amendments to Claims 1 and 19 proposed by the undersigned Attorney, as set forth herein.

As Claims 1 and 19 each now even more clearly recite, Applicant's USB-to-VGA converter "interconnect[s] through a USB port of a computer a display device" that is then controlled by such computer. The converter includes among its combination of features that of a USB controller "external to the computer" which "detachably" connects to the computer's USB port for "receiving exclusively therethrough" the "USB based display signals from the computer," as each of these independent Claims 1 and 19 also now more clearly recites.

The Examiners acknowledged at the interview that the primarily-cited Finger, et al. reference fails to actually disclose the full combination of features recited by the pending Claims, as distinguished in the earlier-filed Amendment. The Examiners further acknowledged that the Beckert, et al. reference appears to be overcome by the Claims as amended.

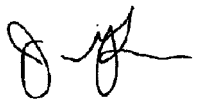
Turning more specifically to Beckert et al., the reference is generally directed to an in-dash computer system 22 for a vehicle, within which the support module 62 and computer module 64 are fixedly integrated. Apart from the fact that the disclosed in-dash structure explicitly negates any detachability feature between the computer module 64 and any component of support module 62 (as addressed in the 16 January 2006 Amendment), the modules 62 and 64 are coupled specifically through a PCI bus interconnect 66. The full interoperability prescribed for these modules contemplate and depend as much on such interconnect means. Quite telling in this regard is that the reference explicitly notes the VGA controller 94 itself to be directly "driven from the PCI bus" (column 5, line 64), rather than through any USB-to-VGA converter interconnected to a computer "through a USB port of ...[that] computer," as Claims 1 and 19 recite. Hence, the reference hardly teaches the claimed converter, much less one connected through a USB port of the given computer to receive the computer's "USB based display signals" "exclusively therethrough," as Claims 1 and 19 further clarify.

As pointed out in the earlier-filed Amendment, moreover, Beckert et al.'s USB interface 92 and VGA controller 94 are not themselves interconnected "one to the other for the passage of data therebetween" (as Claims 1 and 19 also recite). They are specified to serve separate, not necessarily related, purposes, with the USB interface 92 – like the VGA controller 94 - being "driven from the PCI bus

66," so as to "provide[ ] the interconnection to the various USB peripherals shown in Fig. 2," while the "VGA controller 94" serves separately "to drive the display 24," (column 5; lines 57-59 and lines 62-63).

It is now believed that the subject Patent Application has been placed fully in condition for allowance, and such action is respectfully requested.

Respectfully submitted,
For: ROSENBERG, KLEIN & LEE



Jun Y. Lee
Registration #40,262

Dated: 3/2/2006

Suite 101
3458 Ellicott Center Drive
Ellicott City, MD 21043
(410) 465-6678
Customer No. 04586

Interview Summary	Application No.	Applicant(s)	
	10/316,013	LIU, PEI-CHUNG	
	Examiner	Art Unit	
	Kim T. Huynh	2112	

All participants (applicant, applicant's representative, PTO personnel):

(1) *Kim T. Huynh, USPTO*. (3) *Jun Lee, 40,262*.

(2) *John Cottingham, USPTO*. (4)_____.

Date of Interview: _____.

Type: a)☐ Telephonic b)☐ Video Conference
c)☒ Personal [copy given to: 1)☐ applicant 2)☐ applicant's representative]

Exhibit shown or demonstration conducted: d)☒ Yes e)☐ No.
If Yes, brief description: *showed the product*.

Claim(s) discussed: *1*.

Identification of prior art discussed: *Finger and Becker*.

Agreement with respect to the claims f)☐ was reached. g)☐ was not reached. h)☒ N/A.

Substance of interview including description of the general nature of what was agreed to if an agreement was reached, or any other comments: *Discussed the proposed amendment which may appeared to be overcomed the cited prior arts. Examiner will further search and reconsider*.

(A fuller description, if necessary, and a copy of the amendments which the examiner agreed would render the claims allowable, if available, must be attached. Also, where no copy of the amendments that would render the claims allowable is available, a summary thereof must be attached.)

THE FORMAL WRITTEN REPLY TO THE LAST OFFICE ACTION MUST INCLUDE THE SUBSTANCE OF THE INTERVIEW. (See MPEP Section 713.04). If a reply to the last Office action has already been filed, APPLICANT IS GIVEN A NON-EXTENDABLE PERIOD OF THE LONGER OF ONE MONTH OR THIRTY DAYS FROM THIS INTERVIEW DATE, OR THE MAILING DATE OF THIS INTERVIEW SUMMARY FORM, WHICHEVER IS LATER, TO FILE A STATEMENT OF THE SUBSTANCE OF THE INTERVIEW. See Summary of Record of Interview requirements on reverse side or on attached sheet.

Examiner Note: You must sign this form unless it is an Attachment to a signed Office action.

Examiner's signature, if required

U.S. Patent and Trademark Office
PTOL-413 (Rev. 04-03) Interview Summary Paper No. 20080301

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/316,013	12/11/2002	Pei-Chung Liu	MR1115-429	2895

4586 7590 05/15/2006

ROSENBERG, KLEIN & LEE
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ELLICOTT CITY, MD 21043

EXAMINER
HUYNH, KIM T

ART UNIT	PAPER NUMBER
2112	

DATE MAILED: 05/15/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

PTO-90C (Rev. 10/03)

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Rosenberg, Klein & Lee
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APR 24 2006

In re Application of: Pei-Chung Liu	)	
Application No. 10/316,013	)	
Filed: December 11, 2002	)	**NOTIFICATION OF**
U.S. Publication No. 2004/0117538	)	**IDENTIFICATION OF PRIOR**
Published: June 17, 2004	)	**ART IN LATE PROTEST**
For: USB-TO-VGA CONVERTER	)	**UNDER 37 C.F.R. § 1.291(a)**

The protest filed April 19, 2006 under 37 C.F.R. §1.291(a) was filed after the June 17, 2004, publication date of the application.

Because the protest was filed after publication of the application it is untimely and it is not being entered in the application file. A copy of the protest was served on applicant and the original submitted to the Office by the protestor is being discarded. (MPEP § 1901.06)

If appropriate, Applicant may wish to consider submitting prior art from the protest pursuant to 37 C.F.R. §1.97 and 37 C.F.R. §1.56 during the prosecution of the application.

Pinchus M. Laufer
Special Programs Examiner
Technology Center 2100
Computer Architecture, Software, and Information Security
(571) 272-3599

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APR 24 2006

In re Application of: Pei-Chung Liu	)	
Application No. 10/316,013	)	
Filed: December 11, 2002	)	**NOTIFICATION OF**
U.S. Publication No. 2004/0117538	)	**IDENTIFICATION OF PRIOR**
Published: June 17, 2004	)	**ART IN LATE PROTEST**
For: USB-TO-VGA CONVERTER	)	**UNDER 37 C.F.R. § 1.291(a)**

The protest filed April 19, 2006 under 37 C.F.R. §1.291(a) was filed after the June 17, 2004, publication date of the application.

Because the protest was filed after publication of the application it is untimely and it is not being entered in the application file. A copy of the protest was served on applicant and the original submitted to the Office by the protestor is being discarded. (MPEP § 1901.06)

If appropriate, Applicant may wish to consider submitting prior art from the protest pursuant to 37 C.F.R. §1.97 and 37 C.F.R. §1.56 during the prosecution of the application.

Pinchus M. Laufer
Special Programs Examiner
Technology Center 2100
Computer Architecture, Software, and Information Security
(571) 272-3599

Notice of Allowability	Application No. 10/316,013	Applicant(s) LIU, PEI-CHUNG
	Examiner Kim T. Huynh	Art Unit 2112

– The MAILING DATE of this communication appears on the cover sheet with the correspondence address–

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS. This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to 4/24/06.

2. ☒ The allowed claim(s) is/are 1-19.

3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____.
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).
   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.
   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)
1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____.
7. ☐ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

U.S. Patent and Trademark Office
PTOL-37 (Rev. 7-05) Notice of Allowability Part of Paper No./Mail Date 20060511

DETAILED ACTION

Allowable Subject Matter

1. Applicant's amendment filed on 4/24/06 have been fully considered and are persuasive.

2. The following is an examiner's statement of reasons for allowance:

Applicant's claimed invention is deemed allowable over the prior art of record as the prior art, alone or in combination, fails to teach or suggest a USB controller external to the computer which detachably connects to the computer's USB port for receiving exclusively therethrough the USB based display signals from the computer, the USB controller issuing a bus control command in combination with other limitations as recited in independent claims and further in view of the specification and applicant's arguments.

3. Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

4. *Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kim Huynh whose telephone number is (571)272-3635 or via e-mail addressed to [kim.huynh3@uspto.gov]. The examiner can normally be reached on M-F 9.00AM- 6:00PM. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rehana Perveen can be reached at (571)272-3676 or via e-mail addressed to [rehana.perveen@uspto.gov].*

The fax phone numbers for the organization where this application or proceeding is assigned are (571)273-8300 for regular communications and After Final communications. Any inquiry of a general

nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (571)272-2100.

Kim Huynh

May 11, 2006

REHANA PERVEEN
SUPERVISORY PATENT EXAMINER
5/12/06

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

NOTICE OF ALLOWANCE AND FEE(S) DUE

04586 7590 05/16/2006

ROSENBERG, KLEIN & LEE
3458 ELLICOTT CENTER DRIVE-SUITE 101
ELLICOTT CITY, MD 21043

EXAMINER	
HUYNH, KIM T	
ART UNIT	PAPER NUMBER
2182	

DATE MAILED: 05/16/2006

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/316,013	12/11/2002	Pei-Chung Liu	MR1135-429	2895

TITLE OF INVENTION: USB-TO-VGA CONVERTER

APPLN. TYPE	SMALL ENTITY	ISSUE FEE	PUBLICATION FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	YES	$700	$300	$1000	08/16/2006

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE REFLECTS A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE APPLIED IN THIS APPLICATION. THE PTOL-85B (OR AN EQUIVALENT) MUST BE RETURNED WITHIN THIS PERIOD EVEN IF NO FEE IS DUE OR THE APPLICATION WILL BE REGARDED AS ABANDONED.

HOW TO REPLY TO THIS NOTICE:

I. Review the SMALL ENTITY status shown above.

If the SMALL ENTITY is shown as YES, verify your current SMALL ENTITY status:

A. If the status is the same, pay the TOTAL FEE(S) DUE shown above.

B. If the status above is to be removed, check box 5b on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and twice the amount of the ISSUE FEE shown above, or

If the SMALL ENTITY is shown as NO:

A. Pay TOTAL FEE(S) DUE shown above, or

B. If applicant claimed SMALL ENTITY status before, or is now claiming SMALL ENTITY status, check box 5a on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and 1/2 the ISSUE FEE shown above.

II. PART B - FEE(S) TRANSMITTAL should be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). Even if the fee(s) have already been paid, Part B - Fee(s) Transmittal should be completed and returned. If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

PTOL-85 (Rev. 01/06) Approved for use through 04/30/2007.

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail **Mail Stop ISSUE FEE**
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax **(571)-273-2885**

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

04586 7590 05/16/2006

ROSENBERG, KLEIN & LEE
3458 ELLICOTT CENTER DRIVE-SUITE 101
ELLICOTT CITY, MD 21043

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission
I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/316,013	12/11/2002	Pei-Chang Liu	MR1115-429	2895

TITLE OF INVENTION: USB-TO-VGA CONVERTER

APPLN. TYPE	SMALL ENTITY	ISSUE FEE	PUBLICATION FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	YES	$700	$300	$1000	08/16/2006

EXAMINER	ART UNIT	CLASS-SUBCLASS
HUYNH, KIM T	2112	710-315000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).
☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. Use of a Customer Number is required.

2. For printing on the patent front page, list
(1) the names of up to 3 registered patent attorneys or agents OR, alternatively,
(2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.
1 _____
2 _____
3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE (B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent): ☐ Individual ☐ Corporation or other private group entity ☐ Government

4a. The following fee(s) are enclosed:
☐ Issue Fee
☐ Publication Fee (No small entity discount permitted)
☐ Advance Order - # of Copies _____

4b. Payment of Fee(s):
☐ A check in the amount of the fee(s) is enclosed.
☐ Payment by credit card. Form PTO-2038 is attached.
☐ The Director is hereby authorized by charge the required fee(s), or credit any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).

5. Change in Entity Status (from status indicated above)
☐ a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27. ☐ b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

The Director of the USPTO is requested to apply the Issue Fee and Publication Fee (if any) or to re-apply any previously paid issue fee to the application identified above.
NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature _____ Date _____

Typed or printed name _____ Registration No. _____

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

PTOL-85 (Rev. 01/06) Approved for use through 04/30/2007. OMB 0651-0033 U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/316,013	12/11/2002	Pei-Chung Liu	MR1115-429	2895

04586 7590 05/16/2006

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ELLICOTT CITY, MD 21043

EXAMINER	
HUYNH, KIM T	
ART UNIT	PAPER NUMBER
2112	

DATE MAILED: 05/16/2006

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

The Patent Term Adjustment to date is 352 day(s). If the issue fee is paid on the date that is three months after the mailing date of this notice and the patent issues on the Tuesday before the date that is 28 weeks (six and a half months) after the mailing date of this notice, the Patent Term Adjustment will be 352 day(s).

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

PTOL-85 (Rev. 01/06) Approved for use through 04/30/2007.

MR1115-429

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

OIPE JUN 13 2006 PATENT & TRADEMARK OFFICE

Applicant:	Pei-Chung Liu	:	Group
Serial No:	10/316,013	:	Art Unit #2112
Filed:	11 December 2002	:	Examiner:
Title:	USB-TO-VGA CONVERTER	:	K.T. Huynh

INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

The Applicant wishes to make the following art reference of record in the above-identified Patent Application pursuant to 37 C.F.R. §§ 1.97 and 1.98, and to the Duty of Disclosure set forth in 37 C.F.R. § 1.56.

Although the information submitted herewith may be "material" to the Examiner's consideration of the subject Patent Application, this submission is not intended to constitute an admission that such information is "prior art" as to the claimed invention.

In accordance with 37 C.F.R. § 1.97(g), the filing of this Information Disclosure Statement (IDS) shall not be construed to mean that a search was made or that no other material information, as defined in 37 C.F.R. § 1.56(b), exists.

06/14/2006 HALI11 00000008 10316013
01 FC:1806 180.00 OP

The cited Patent References are:

Ref. No.	Patent/Appl. No.	Issue/Pub. Date	Inventor(s)/Applicant(s)
A1	2004/0021615	02/05/2004	Benson, et al.
A2	2002/0135584	09/26/2002	Lee

The cited Non-Patent References are:

Ref. No.	Pub. Title.	Pub. Date	Name(s)
B1	"VinChip Announces Release of USB-PCI Device Bridge IP"	(uncertain)	K. Subramaniam
B2	USBN9602 (Universal Serial Bus) Full Speed Function Controller With DMA Support	11/1998	National Semiconductor

A Form PTO/SB/08A (Substitute for Form 1449/PTO) is submitted along with this document. Reference A1was not cited in a communication from a foreign patent office in a counterpart foreign application; however, it was not known to Applicant or any other individual designated in 37 C.F.R. § 1.56(c) more than three months prior to the filing of this IDS. It is requested that the Examiner consider the reference and make it of record in the above-referenced Patent Application.

This IDS is being submitted after the mailing of a Notice of Allowance. Accordingly, a check in the amount of $180.00 is attached to cover the fee due for this IDS. Should there be any additional fees due in connection with this filing, the Director Patents and Trademarks is hereby authorized to charge Deposit Account #18-2011 for such additional fees.

Respectfully submitted,
FOR: ROSENBERG, KLEIN & LEE

Jun Y. Lee
Registration No. 40,262

Dated: 6/13/2006

Suite 101
3458 Ellicott Center Drive
Ellicott City, MD 21043
(410) 465-6678

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
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Alexandria, Virginia 22313-1450
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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/316,013	12/11/2002	Pei-Chung Liu	MR1115-429	2895

4586 7590 06/29/2006

ROSENBERG, KLEIN & LEE
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ELLICOTT CITY, MD 21043

EXAMINER	
HUYNH, KIM T	

ART UNIT	PAPER NUMBER
2112	

DATE MAILED: 06/29/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

PTO-90C (Rev. 10/03)

UNITED STATES DEPARTMENT OF COMMERCE
U.S. Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450

APPLICATION NO./ CONTROL NO.	FILING DATE	FIRST NAMED INVENTOR / PATENT IN REEXAMINATION	ATTORNEY DOCKET NO.
10 316 013			

EXAMINER	
ART UNIT	PAPER

10/316,013

DATE MAILED:

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner for Patents

The IDS filed on 6/13/06 has been considered and made of record. Copies of the PTO form 1449 have been attached with this communication.

Kim Huynh
AU 2112

REHANA PERVEEN
SUPERVISORY PATENT EXAMINER
6/26/06

PTO-90C (Rev.04-03)

PTO/SB/08A (07-06)
Approved for use through 07/31/2006. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Substitute for form 1449/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Sheet 2 of 2

Complete if Known	
Application Number	10/316,013
Filing Date	11 DECEMBER 2002
First Named Inventor	PEI-CHUNG LIU
Art Unit	2112
Examiner Name	K.T. HUYNH
Attorney Docket Number	MR1115-429

U.S. PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Document Number Number-Kind Code[2] (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
KH	A1	US- 2004/0021615	02/05/2004	BENSON, ET AL.	
KH	A2	US- 2002/0135584	09/26/2002	LEE	
		US-			
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		US-			

FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Foreign Patent Document Country Code[3] Number[4] Kind Code[5] (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages Or Relevant Figures Appear	T[6]

Examiner Signature	/Kim Huynh/	Date Considered	06/16/2006

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. [1] Applicant's unique citation designation number (optional). [2] See Kinds Codes of USPTO Patent Documents at www.uspto.gov or MPEP 901.04. [3] Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). [4] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [5] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [6] Applicant is to place a check mark here if English language Translation is attached.

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 (1-800-786-9199) and select option 2.

PTO/SB/08B (07-05)
Approved for use through 07/31/2006. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Substitute for form 1449/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Sheet 1 of 2

	Complete if Known
Application Number	10/316,013
Filing Date	11 DECEMBER 2002
First Named Inventor	PEI-CHUNG LIU
Art Unit	2112
Examiner Name	K.T. HUYNH
Attorney Docket Number	MR1115-429

NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
KH	B1	SUBRAMANIAM, K,"VinChip Announces Release of USB-PCI Device Bridge IP", San Jose, CA	
KH	B2	NATIONAL SEMICONDUCTOR, USBN9602 (Universal Serial Bus) Full Speed Function Controller With DMA Support, 11/1998	

Examiner Signature	/Kim Huynh/	Date Considered	06/26/2006

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

1 Applicant's unique citation designation number (optional). 2 Applicant is to place a check mark here if English language Translation is attached.

This collection of information is required by 37 CFR 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 (1-800-786-9199) and select option 2.

MR1115-429



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Pei-Chung Liu	:	Group
Serial No:	10/316,013	:	Art Unit #2112
Filed:	11 December 2002	:	Examiner:
Title:	USB-TO-VGA CONVERTER	:	K.T. Huynh

RESUBMISSION OF INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Applicant wishes to resubmit the Information Disclosure Statement which was previously submitted to the USPTO on 13 June 2006. The resubmission of the Information Disclosure Statement is being made due to the fact that subsequent to the filing of the original Information Disclosure Statement on 13 June 2006, the undersigned attorney became aware that one of the references cited, namely, the Lee Patent Application Publication 2002/0135584, having a publication date of 26 September 2002 (now abandoned) was found to be an application which was filed by the undersigned attorney's firm of Rosenberg, Klein & Lee (RKL).

However, in the original Information Disclosure Statement filed on 13 June 2006, a statement was made that the references were "not known to Applicant or any other individual designated in 37 CFR § 1.56(c) more than three months prior

to the filing of this IDS." In fact, the original IDS was filed responsive to a protest made by a third party and at the time the IDS was filed with the USPTO, the attorneys for Applicant, namely, RKL did not notice that the Lee Patent Application was filed by RKL.

Subsequent to the filing of the original IDS, it was noticed that RKL were the attorneys for the Lee application.

Thus, in order to remove even the remotest appearance of impropriety, an RCE has been requested in the above-referenced patent application with this resubmission of the Information Disclosure Statement being made.

The cited Patent References which are the same as those filed in the original Information Disclosure are:

Ref. No.	Patent/Appl. No.	Issue/Pub. Date	Inventor(s)/Applicant(s)
A1	2004/0021615	02/05/2004	Benson, et al.
A2	2002/0135584	09/26/2002	Lee

The cited Non-Patent References are:

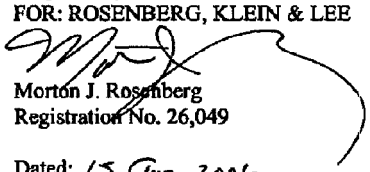
Ref. No.	Pub. Title.	Pub. Date	Name(s)
B1	"VinChip Announces Release of USB-PCI Device Bridge IP"	(uncertain)	K. Subramaniam
B2	USBN9602 (Universal Serial Bus) Full Speed Function Controller With DMA Support	11/1998	National Semiconductor

A Form PTO/SB/08A (Substitute for Form 1449/PTO) is submitted along with this document.

This resubmission of the IDS is being submitted after the mailing of the Notice of Allowance. It is not known whether a further check in the amount of $180.00 is payable to the USPTO for this resubmission of the IDS.

Should there be any fees due in connection with this filing, the Honorable Director of Patents and Trademarks is hereby authorized to charge Deposit Account 18-2011 for such additional fees.

Respectfully submitted,
FOR: ROSENBERG, KLEIN & LEE



Morton J. Rosenberg
Registration No. 26,049

Dated: 15 Aug. 2006

Suite 101
3458 Ellicott Center Drive
Ellicott City, MD 21043
(410) 465-6678

OIPE AUG 16 2006 PATENT & TRADEMARK OFFICE

PTO/SB/08A (07-05)
Approved for use through 07/31/2006. OMB 0651-0031
U.S. Patent and Trademark Office: U.S. DEPARTMENT OF COMMERCE
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Substitute for form 1449/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Sheet 1 of 2

Complete if Known	
Application Number	10/316,013
Filing Date	11 DECEMBER 2002
First Named Inventor	PEI-CHUNG LIU
Art Unit	2112
Examiner Name	K.T. HUYNH
Attorney Docket Number	MR1115-429

U.S. PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Document Number Number-Kind Code[2] (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
KH	A1	US- 2004/0021615	02/05/2004	BENSON, ET AL.	
KH	A2	US- 2002/0135584	09/26/2002	LEE	
		US-			
		US-			
		US-			
		US-			
		US-			
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		US-			
		US-			

FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Foreign Patent Document Country Code[3] Number[4] Kind Code[5] (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages Or Relevant Figures Appear	T[6]

Examiner Signature	/Kim Huynh/	Date Considered	10/11/2006

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. [1] Applicant's unique citation designation number (optional). [2] See Kinds Codes of USPTO Patent Documents at www.uspto.gov or MPEP 901.04. [3] Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). [4] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [5] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [6] Applicant is to place a check mark here if English language Translation is attached.

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 (1-800-786-9199) and select option 2.

PTO/SB/08B (07-05)
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OIPE
AUG 16 2006
PATENT & TRADEMARK OFFICE

Substitute for form 1449/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Sheet 2 of 2

Complete if Known	
Application Number	10/318,013
Filing Date	11 DECEMBER 2002
First Named Inventor	PEI-CHUNG LIU
Art Unit	2112
Examiner Name	K.T. HUYNH
Attorney Docket Number	MR1115-429

NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
KH	B1	SUBRAMANIAM, K,"VinChip Announces Release of USB-PCI Device Bridge IP", San Jose, CA	
KH	B2	NATIONAL SEMICONDUCTOR, USBN9602 (Universal Serial Bus) Full Speed Function Controller With DMA Support, 11/1998	

Examiner Signature	/Kim Huynh/	Date Considered	10/17/2006

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.
[1] Applicant's unique citation designation number (optional). [2] Applicant is to place a check mark here if English language Translation is attached.

This collection of information is required by 37 CFR 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing the burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 (1-800-786-9199) and select option 2.

RCE$

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Request for Continued Examination (RCE) Transmittal

Address to:
Mail Stop RCE
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

AUG 16 2006
PATENT & TRADEMARK OFFICE

Application Number	10/316,013
Filing Date	11 December 2002
First Named Inventor	Pei-Chung Liu
Art Unit	2112
Examiner Name	K. T. Huynh
Attorney Docket Number	MR1115-429

This is a Request for Continued Examination (RCE) under 37 CFR 1.114 of the above-identified application.
Request for Continued Examination (RCE) practice under 37 CFR 1.114 does not apply to any utility or plant application filed prior to June 8, 1995, or to any design application. See Instruction Sheet for RCEs (not to be submitted to the USPTO) on page 2.

1. Submission required under 37 CFR 1.114 Note: If the RCE is proper, any previously filed unentered amendments and amendments enclosed with the RCE will be entered in the order in which they were filed unless applicant instructs otherwise. If applicant does not wish to have any previously filed unentered amendment(s) entered, applicant must request non-entry of such amendment(s).

a. ☐ Previously submitted. If a final Office action is outstanding, any amendments filed after the final Office action may be considered as a submission even if this box is not checked.
   i. ☐ Consider the arguments in the Appeal Brief or Reply Brief previously filed on _____
   ii. ☐ Other _____

b. ☑ Enclosed
   i. ☐ Amendment/Reply
   ii. ☐ Affidavit(s)/ Declaration(s)
   iii. ☑ Information Disclosure Statement (IDS)
   iv. ☐ Other _____

2. Miscellaneous
a. ☐ Suspension of action on the above-identified application is requested under 37 CFR 1.103(c) for a period of _____ months. (Period of suspension shall not exceed 3 months; Fee under 37 CFR 1.17(i) required)
b. ☐ Other _____

3. Fees The RCE fee under 37 CFR 1.17(e) is required by 37 CFR 1.114 when the RCE is filed.
a. ☑ The Director is hereby authorized to charge ~~the following fees~~ any underpayment of fees, or credit any overpayments, to Deposit Account No. 18-2011. I have enclosed a duplicate copy of this sheet.
   i. ☐ RCE fee required under 37 CFR 1.17(e)
   ii. ☐ Extension of time fee (37 CFR 1.136 and 1.17)
   iii. ☐ Other _____
b. ☑ Check in the amount of $ 395.00 enclosed
c. ☐ Payment by credit card (Form PTO-2038 enclosed)

WARNING: Information on this form may become public. Credit card information should not be included on this form. Provide credit card information and authorization on PTO-2038.

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT REQUIRED

Signature	Morton J. Rosenberg	Date	8/15/2006
Name (Print/Type)	Morton J. Rosenberg	Registration No.	26,049

CERTIFICATE OF MAILING OR TRANSMISSION [illegible] 395.00 DP

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to: Mail Stop RCE, Commissioner for Patents, P. O. Box 1450, Alexandria, VA 22313-1450 or facsimile transmitted to the U.S. Patent and Trademark Office on the date shown below.

Signature	
Name (Print/Type)	Date

This collection of information is required by 37 CFR 1.114. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Mail Stop RCE, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.
If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Customer No.
04586

Notice of Allowability	Application No.	Applicant(s)	
	10/318,013	LIU, PEI-CHUNG	
	Examiner	Art Unit	
	Kim T. Huynh	2112	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to 8/16/06.

2. ☒ The allowed claim(s) is/are 1-19.

3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).
   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.
   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)
1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☒ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date 8/16/06
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____.
7. ☐ Examiner's Amendment/Comment
8. ☐ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

REHANA PERVEEN
SUPERVISORY PATENT EXAMINER
10/12/06

U.S. Patent and Trademark Office
PTOL-37 (Rev. 08-06) Notice of Allowability Part of Paper No./Mail Date 20061011

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

NOTICE OF ALLOWANCE AND FEE(S) DUE

04586 7590 10/23/2006

ROSENBERG, KLEIN & LEE
3458 ELLICOTT CENTER DRIVE-SUITE 101
ELLICOTT CITY, MD 21043

EXAMINER	
HUYNH, KIM T	
ART UNIT	PAPER NUMBER
2812	

DATE MAILED: 10/23/2006

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/316,013	12/11/2002	Pei-Chung Liu	MR1115-429	2895

TITLE OF INVENTION: USB-TO-VGA CONVERTER

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	YES	$700	$300	$0	$1000	01/23/2007

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the SMALL ENTITY status shown above.

If the SMALL ENTITY is shown as YES, verify your current SMALL ENTITY status:

A. If the status is the same, pay the TOTAL FEE(S) DUE shown above.

B. If the status above is to be removed, check box 5b on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and twice the amount of the ISSUE FEE shown above, or

If the SMALL ENTITY is shown as NO:

A. Pay TOTAL FEE(S) DUE shown above, or

B. If applicant claimed SMALL ENTITY status before, or is now claiming SMALL ENTITY status, check box 5a on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and 1/2 the ISSUE FEE shown above.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

PTOL-85 (Rev. 07/06) Approved for use through 04/30/2007.

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail Mail Stop ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

04586 7590 10/23/2006

ROSENBERG, KLEIN & LEE
3458 ELLICOTT CENTER DRIVE-SUITE 101
ELLICOTT CITY, MD 21043

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission
I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/316,913	12/11/2002	Pei-Chung Liu	MR1115-429	2895

TITLE OF INVENTION: USB-TO-VGA CONVERTER

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	YES	$700	$300	$0	$1000	01/23/2007

EXAMINER	ART UNIT	CLASS-SUBCLASS
HUYNH, KIM T	2112	710-315000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).
☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. Use of a Customer Number is required.

2. For printing on the patent front page, list
(1) the names of up to 3 registered patent attorneys or agents OR, alternatively,
(2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.
1 _____
2 _____
3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE (B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent): ☐ Individual ☐ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:
☐ Issue Fee
☐ Publication Fee (No small entity discount permitted)
☐ Advance Order - # of Copies _____

4b. Payment of Fee(s): (Please first reapply any previously paid issue fee shown above)
☐ A check is enclosed.
☐ Payment by credit card. Form PTO-2038 is attached.
☐ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).

5. Change in Entity Status (from status indicated above)
☐ a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27.
☐ b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature _____ Date _____

Typed or printed name _____ Registration No. _____

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

PTOL-85 (Rev. 07/06) Approved for use through 04/30/2007. OMB 0651-0033 U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/316,013	12/11/2002	Pei-Chung Liu	MR1115-429	2895

04586 7590 10/23/2006

ROSENBERG, KLEIN & LEE
3458 ELLICOTT CENTER DRIVE-SUITE 101
ELLICOTT CITY, MD 21043

EXAMINER	
HUYNH, KIM T	
ART UNIT	PAPER NUMBER
2112	

DATE MAILED: 10/23/2006

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

The Patent Term Adjustment to date is 352 day(s). If the issue fee is paid on the date that is three months after the mailing date of this notice and the patent issues on the Tuesday before the date that is 28 weeks (six and a half months) after the mailing date of this notice, the Patent Term Adjustment will be 352 day(s).

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

PTOL-85 (Rev. 07/06) Approved for use through 04/30/2007.

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail Mail Stop ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

04586 7590 10/23/2006

ROSENBERG, KLEIN & LEE
3458 ELLICOTT CENTER DRIVE-SUITE 101
ELLICOTT CITY, MD 21043



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Certificate of Mailing or Transmission
I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/316,013	12/11/2002	Pei-Chung Lin	MR1115-429	2895

TITLE OF INVENTION: USB-TO-VGA CONVERTER

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	YES	$700	$300	$0	$1000	01/23/2007

EXAMINER	ART UNIT	CLASS-SUBCLASS
HUYNH, KIM T	2112	710-315000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).
- ☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
- ☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. Use of a Customer Number is required.

2. For printing on the patent front page, list
(1) the names of up to 3 registered patent attorneys or agents OR, alternatively,
(2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 Rosenberg, Klein & Lee
2
3

11/02/2006 MBERHE1 00000002 10316013
01 FC:2501 300.00 OP
02 FC:1504 700.00 OP

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE: Magic Control Technology Corporation
(B) RESIDENCE: (CITY and STATE OR COUNTRY): Taipei, Taiwan, R.O.C.

Please check the appropriate assignee category or categories (will not be printed on the patent): ☐ Individual ☒ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:
- ☒ Issue Fee
- ☒ Publication Fee (No small entity discount permitted)
- ☐ Advance Order - # of Copies _____

4b. Payment of Fee(s): (Please first reapply any previously paid issue fee shown above)
- ☒ A check is enclosed.
- ☐ Payment by credit card. Form PTO-2038 is attached.
- ☒ The Director is hereby authorized to charge [redacted], any deficiency, or credit any overpayment, to Deposit Account Number 18-2011 (enclose an extra copy of this form).

5. Change in Entity Status (from status indicated above)
- ☐ a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27.
- ☐ b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature _____ Date 31 Oct 2006

Typed or printed name Morton J. Rosenberg Registration No. 26,049

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

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APPLICATION NO.	ISSUE DATE	PATENT NO.	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/316,013	04/10/2007	7203788	MR1115-429	2895

4586 7590 03/21/2007

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ELLICOTT CITY, MD 21043

ISSUE NOTIFICATION

The projected patent number and issue date are specified above.

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

The Patent Term Adjustment is 392 day(s). Any patent to issue from the above-identified application will include an indication of the adjustment on the front page.

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at (571)-272-4200.

APPLICANT(s) (Please see PAIR WEB site http://pair.uspto.gov for additional applicants):

Pei-Chung Liu, ChungHo City, TAIWAN;

IR103 (Rev. 11/05)

BEST AVAILABLE COPY

PATENT APPLICATION FEE DETERMINATION RECORD
Effective October 1, 2001

Application or Docket Number: 10,316,013

CLAIMS AS FILED - PART I

	(Column 1)	(Column 2)
TOTAL CLAIMS 16		
FOR	NUMBER FILED	NUMBER EXTRA
TOTAL CHARGEABLE CLAIMS	16 minus 20=	* 0
INDEPENDENT CLAIMS	1 minus 3 =	* 0
MULTIPLE DEPENDENT CLAIM PRESENT		☐

* If the difference in column 1 is less than zero, enter "0" in column 2

SMALL ENTITY TYPE ☐		OR	OTHER THAN SMALL ENTITY	
RATE	FEE		RATE	FEE
BASIC FEE	370.00	OR	BASIC FEE	740.00
X$ 9=		OR	X$18=	
X42=		OR	X84=	
+140=		OR	+280=	
TOTAL	370	OR	TOTAL	

CLAIMS AS AMENDED - PART II

AMENDMENT A	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA
Total	*	Minus	**	=
Independent	*	Minus	***	=
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM				☐

SMALL ENTITY		OR	OTHER THAN SMALL ENTITY	
RATE	ADDITIONAL FEE		RATE	ADDITIONAL FEE
X$ 9=		OR	X$18=	
X42=		OR	X84=	
+140=		OR	+280=	
TOTAL ADDIT. FEE		OR	TOTAL ADDIT. FEE	

AMENDMENT B	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA
Total	*	Minus	**	=
Independent	*	Minus	***	=
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM				☐

		OR		
RATE	ADDITIONAL FEE		RATE	ADDITIONAL FEE
X$ 9=		OR	X$18=	
X42=		OR	X84=	
+140=		OR	+280=	
TOTAL ADDIT. FEE		OR	TOTAL ADDIT. FEE	

AMENDMENT C	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA
Total	*	Minus	**	=
Independent	*	Minus	***	=
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM				☐

		OR		
RATE	ADDITIONAL FEE		RATE	ADDITIONAL FEE
X$ 9=		OR	X$18=	
X42=		OR	X84=	
+140=		OR	+280=	
TOTAL ADDIT. FEE		OR	TOTAL ADDIT. FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20."
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3."
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

FORM PTO-875 (Rev. 8/01) — Patent and Trademark Office, U.S. DEPARTMENT OF COMMERCE

Application or Docket Number 10,316,013

PATENT APPLICATION FEE DETERMINATION RECORD
Effective October 1, 2001

CLAIMS AS FILED - PART I

	(Column 1)	(Column 2)
TOTAL CLAIMS 16		
FOR	NUMBER FILED	NUMBER EXTRA
TOTAL CHARGEABLE CLAIMS	16 minus 20= *	0
INDEPENDENT CLAIMS	1 minus 3 = *	0
MULTIPLE DEPENDENT CLAIM PRESENT		☐

* If the difference in column 1 is less than zero, enter "0" in column 2

SMALL ENTITY TYPE ☐		OR	OTHER THAN SMALL ENTITY	
RATE	FEE		RATE	FEE
BASIC FEE	370.00	OR	BASIC FEE	740.00
X$ 9=		OR	X$18=	
X42=		OR	X84=	
+140=		OR	+280=	
TOTAL	370	OR	TOTAL	

IFW Amdt 61605

CLAIMS AS AMENDED - PART II

AMENDMENT A

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA
Total	* 19	Minus	** 20	0
Independent	* 2	Minus	*** 3	0
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM				☐

SMALL ENTITY		OR	OTHER THAN SMALL ENTITY	
RATE	ADDITIONAL FEE		RATE	ADDITIONAL FEE
X$ 9=		OR	X$18=	
X42=		OR	X84=	
+140=		OR	+280=	
TOTAL ADDIT. FEE		OR	TOTAL ADDIT. FEE	

AMENDMENT B

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA
Total	*	Minus	**	=
Independent	*	Minus	***	=
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM				☐

RATE	ADDITIONAL FEE		RATE	ADDITIONAL FEE
X$ 9=		OR	X$18=	
X42=		OR	X84=	
+140=		OR	+280=	
TOTAL ADDIT. FEE		OR	TOTAL ADDIT. FEE	

AMENDMENT C

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA
Total	*	Minus	**	=
Independent	*	Minus	***	=
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM				☐

RATE	ADDITIONAL FEE		RATE	ADDITIONAL FEE
X$ 9=		OR	X$18=	
X42=		OR	X84=	
+140=		OR	+280=	
TOTAL ADDIT. FEE		OR	TOTAL ADDIT. FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20."
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3."
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

FORM PTO-875 (Rev. 8/01) — Patent and Trademark Office, U.S. DEPARTMENT OF COMMERCE

MPI Family Report (Family Bibliographic and Legal Status)

In the MPI Family report, all publication stages are collapsed into a single record, based on identical application data. The bibliographic information displayed in the collapsed record is taken from the latest publication.

Report Created Date: 2007-08-09

Name of Report:

Number of Families: 1

Comments:

Table of Contents

1. **US7203788B2** 20070410 MAGIC CONTROL TECHNOLOGY CORP TW
USB-to-VGA converter 1

Family1

2 records in the family, collapsed to 1 records.

US7203788B2 20070410
US2004117538A1 20040617

(ENG) USB-to-VGA converter

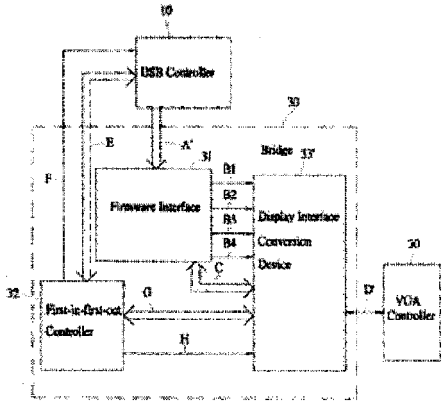
Assignee: MAGIC CONTROL TECHNOLOGY CORP TW

Inventor(s): LIU PEI CHUNG TW

Application No: US 31601302 A

Filing Date: 20021211

Issue/Publication Date: 20070410



Abstract: (ENG) A USB-to-VGA converter includes a USB controller connectable to a USB port of a computer for receiving USB based display signals from the computer, a VGA controller connectable to a display device for conveying VGA signals to the display device and a bridge connected between the USB controller and the VGA controller. The bridge receives a bus control command from the USB controller and issues a first-in-first-out control signal to the USB controller to receive the USB based display signals from the USB controller in a first-in-first-out manner. The bridge circuit converts the USB based display signals into corresponding VGA signals and forwarding the VGA signals to the VGA controller, which in turn applies the VGA signals to the display device. No display interface card is required inside the host computer for generation of the VGA signals.

Priority Data: US 31601302 20021211 A;

Related Application(s): 10/316013 20021211 20040117538 20040617 US

IPC (International Class): G06F01336

ECLA (European Class): G06F00314; G09G00500

US Class: 710315; 710100; 710107; 710305; 710306

Publication Language: ENG

Filing Language: ENG

Agent(s): Rosenberg, Klein & Lee

Examiner Primary: Perveen, Rehana

Examiner Assistant: Huynh, Kim T.

US Post Issuance:
--US Litigations: Displaylink Corporation Displaylink Corporation 20070410
N.D. California 3:07cv1998 ; Displaylink Corporation Displaylink Corporation 20070410
N.D. California 5:07cv1998

Assignments Reported to USPTO:
Reel/Frame: 13564/0969 **Date Signed:** 20021203 **Date Recorded:** 20021211
Assignee: MAGIC CONTROL TECHNOLOGY CORPORATION 6F, NO. 120-11, CHUNGSHAN ROAD SECTION 3 CHUNGHO CITY TAIPEI R.O.C. TAIWAN

Assignor: LIU, PEI-CHUNG

Corres. Addr: ROSENBERG, KLEIN & LEE MORTON J. ROSENBERG 3458 ELLICOTT CENTER DRIVE, SUITE 101 ELLICOTT CITY, MD 21043

Brief: ASSIGNMENT OF ASSIGNORS INTEREST (SEE DOCUMENT FOR DETAILS).

Legal Status: There is no Legal Status information available for this patent

USPTO Maintenance Report					
Patent Bibliographic Data			08/09/2007 01:41 PM		
Patent Number:	7203788		Application Number:	10316013	
Issue Date:	04/10/2007		Filing Date:	12/11/2002	
Title:	USB-TO-VGA CONVERTER				
Status:	4th year fee window opens: 04/12/2010			Entity:	Small
Window Opens:	04/12/2010	Surcharge Date:	10/13/2010	Expiration:	N/A
Fee Amt Due:	Window not open	Surchg Amt Due:	Window not open	Total Amt Due:	Window not open
Fee Code:	2551	MAINTENANCE FEE DUE AT 3.5 YEARS			
Surcharge Fee Code:					
Most recent events (up to 7):		No Maintenance History Found --- End of Maintenance History ---			
Address for fee purposes:	ROSENBERG, KLEIN & LEE 3458 ELLICOTT CENTER DRIVE-SUITE 101 ELLICOTT CITY, MD 21043				