QUINN EMANUEL URQUHART
& SULLIVAN, LLP
James R. Asperger (Bar No. 083188)
jimasperger@quinnemanuel.com
Bryan C. Hathorn (Bar No. 294413)
bryanhathorn@quinnemanuel.com
865 S. Figueroa St., 10th Floor
Los Angeles, California 90017
Telephone: (213) 443-3000
Facsimile: (213) 443-3100

Kevin P.B. Johnson (Bar No. 177129)
kevinjohnson@quinnemanuel.com
Mark Yeh-Kai Tung (Bar No. 245782)
marktung@quinnemanuel.com
555 Twin Dolphin Drive, 5th Floor
Redwood Shores, California 94065
Telephone: (650) 801-5000
Facsimile: (650) 801-5100

Kathy Ke Peng (Bar No. 296113)
kathypeng@quinnemanuel.com
50 California Street 22nd Floor
San Francisco, California 94111
Telephone: (415) 875-6600
Facsimile: (415) 875-6700

Attorneys for Plaintiff California Institute of Technology

UNITED STATES DISTRICT COURT

CENTRAL DISTRICT OF CALIFORNIA

CALIFORNIA INSTITUTE OF TECHNOLOGY, a California corporation,

Plaintiff,

vs.

HUGHES COMMUNICATIONS, INC., a Delaware corporation, HUGHES NETWORK SYSTEMS, LLC, a Delaware limited liability company, DISH NETWORK CORPORATION, a Nevada corporation, DISH NETWORK L.L.C., a Colorado limited liability company, and DISHNET SATELLITE BROADBAND L.L.C., a Colorado limited liability company,

Defendants.

CASE NO. 2:13-CV-07245-MRP (JEMx)

DECLARATION OF KATHY PENG IN SUPPORT OF PLAINTIFF'S OPENING CLAIM CONSTRUCTION BRIEF

Date: July 9, 2014
Time: 1:30 p.m.
Place: Courtroom 12

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I. INTRODUCTION

Plaintiff California Institute of Technology ("Caltech") respectfully submits this brief on claim construction issues. Caltech's proposed constructions should be adopted because they are consistent with the intrinsic evidence and the ordinary meaning to a person of ordinary skill in the art. In contrast, in order to support its purported non-infringement positions, Defendants (collectively "Hughes") improperly attempt to limit the meaning of the claim terms in a way that is inconsistent with the evidence. Furthermore, none of the disputed claim terms are indefinite because they inform a person of ordinary skill in the art of the scope of the claims with reasonable certainty. Hughes will not be able to meet its burden to prove any of these claim terms indefinite by clear and convincing evidence.[1]

II. OVERVIEW OF THE TECHNOLOGY[2]

The patents-in-suit each claim priority to the same patent application U.S. Serial Application No. 09/861,102.[3] The inventions of these patents cover a revolutionary coding technique used in digital communications known as "irregular repeat and accumulate codes" or "IRA codes." These inventions were developed in 1999 at Caltech by Hui Jin, Aamod Khandekar and Professor Bob McEliece. IRA codes are used in a variety of digital communications applications, including standardized satellite communications.

At the time of the invention, different techniques were used to increase the amount of data that a channel—such as a cellular link—can carry to approach a theoretical limit, known as the Shannon Limit. One such prior approach that was particularly effective is known as turbocoding. This technique allowed for a robust

[1] Hughes has taken the position that three of the six terms in dispute are indefinite under 35 U.S.C. § 112(b).

[2] Per the Court's orders, Caltech will submit a separate technology tutorial.

[3] Each patent-in-suit shares the same disclosure as this application, which issued as U.S. Patent 7,116,710 ("the '710 patent").

error correction, but was complex to encode and decode. Information is translated into a code that can be transmitted or stored then later recovered, either after receiving a transmission or when retrieving information from storage. Any errors can be corrected during the decoding process to recover the original information from the code. Turbocoding required more output bits to be transmitted than the original information bits input to turbocoding, and more complex circuitry.

The IRA codes of the patents-in-suit allow for error correction as effective as turbocoding but use simpler algorithms and circuitry. The patented technique involves creating a code from the information bits (sometimes referred to as message bits) by reordering repeated instances of information bits in a randomized but known way and performing logical operations on the reordered bits. The code can be represented using a diagram, called a Tanner graph, that shows the relationship of a code to the information bits using "parity checks." Figure 3 of the patent is an example of a Tanner graph, generalized to show the types of relationships that comprise the codes of the invention:

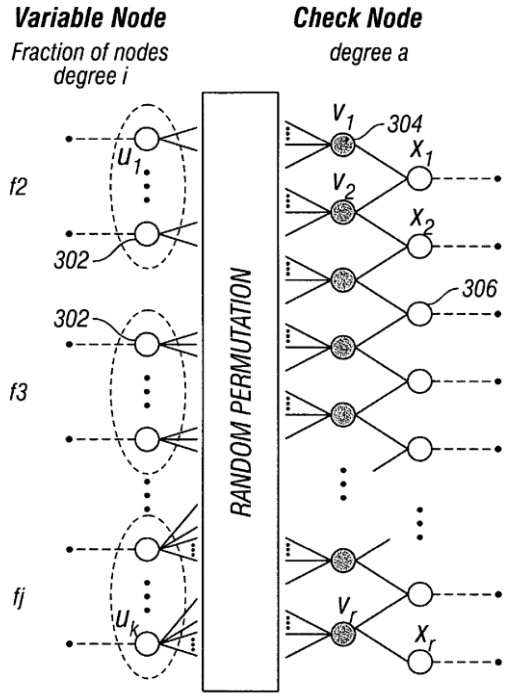


FIG. 3

The graph uses ellipses to show the variation in parity check relationships within the genus of the invention, which are described in detail in the specification, including the number (k) of information nodes (U_k), the number (j) of subsets (f_j) of nodes, the number of repeats (q, not shown on figure but described in patent) of each information node within a subset, the number (r) of check nodes (Vr), the number (a) of connections at each check node, and the number of parity bits (Xr). U.S. Patent 7,421,032, 3:30 – 4:18.

III. LEGAL STANDARDS

A. Law of Claim Construction

"When the parties present a fundamental dispute regarding the scope of a claim term, it is the court's duty to resolve it." *O2 Micro Int'l Ltd. v. Beyond Innovation Tech. Co.*, 521 F.3d 1351, 1362 (Fed. Cir. 2008). The "bedrock principle of patent law" is that "the claims of the patent define the invention." *Phillips v. AWH Corp.*, 415 F.3d 1303, 1312 (Fed. Cir. 2005) (en banc) (quoting *Innova/Pure Water, Inc. v. Safari Water Filtration Sys., Inc.*, 381 F.3d 1111, 1115 (Fed. Cir. 2004)). Thus, "the claims are 'of primary importance' in the effort to ascertain precisely what it is that is patented." *Id.* (quoting *Merrill v. Yeomans*, 94 U.S. 568, 570 (1876)). Claims are interpreted "with an eye toward giving effect to all terms in the claim." *Bicon, Inc. v. Diro, Inc.*, 441 F.3d 945, 950 (Fed. Cir. 2006). Claims are construed from the perspective of a person of ordinary skill in the art at the time of the invention. *Phillips*, 415 F.3d at 1312-13. "[T]he ordinary and customary meaning of a claim term is the meaning that the term would have to a person of ordinary skill in the art in question at the time of the invention." *Id.* at 1313.

The specification is "intrinsic" evidence and "the single best guide to the meaning of a disputed term." *Id.* at 1315 (quoting *Vitronics Corp. v. Conceptronic, Inc.*, 90 F.3d 1576, 1582 (Fed. Cir. 1996)). Claims should also be construed in light of the prosecution history before the U.S. Patent and Trademark Office, which is

also intrinsic evidence. *See Computer Docking Station Corp. v. Dell, Inc.*, 519 F.3d 1366, 1374-75 (Fed. Cir. 2008). "The plain meaning of claim language ordinarily controls unless the patentee acts as his own lexicographer and provides a special definition for a particular claim term or the patentee disavows the ordinary scope of a claim term either in the specification or during prosecution." *InterDigital Commc'ns, LLC v. Int'l Trade Comm'n,* 690 F.3d 1318, 1324 (Fed. Cir. 2012) *on reh'g*, 707 F.3d 1295 (Fed. Cir. 2013).

Courts may also consider extrinsic evidence, such as dictionaries, treatises and expert testimony, to provide technology background, to explain the invention, or to explain the meaning of a term as it would be understood by a person of ordinary skill in the art at the time of the invention. *See Phillips*, 415 F.3d at 1317-18.

Claims should generally be construed to preserve their validity. *Id.* at 1327.

B. Law of Indefiniteness

The Patent Act requires that a patent specification contains "such full, clear, concise, and exact terms" to "point[] out and distinctly claim[] the subject matter which the [applicant] regards as the invention." 35 U.S.C. § 112(a), (b) (2012). To meet this definiteness requirement, when "viewed in light of the specification and prosecution history," the patent's claims must "inform those skilled in the art about the scope of the invention with reasonable certainty." *Nautilus, Inc. v. Biosig Instruments, Inc.*, 134 S. Ct. 2120, 2129 (2014). The court's ability "to ascribe *some* meaning" to a patent's claims is insufficient. *Id.* "[T]he definiteness inquiry trains on the understanding of a skilled artisan at the time of the patent application, not that of a court viewing matters *post hoc*." *Id.* A claim that is "hard to understand when viewed without benefit of the specification" is not indefinite when the specification shows the claim's intended meaning. *S3 Inc. v. NVIDIA Corp.*, 259 F.3d 1364, 1369 (Fed. Cir. 2001).

Whether a patent claim complies with the definiteness requirement of section 112 is a question of law. *Noah Sys., Inc. v. Intuit, Inc.*, 675 F3d 1302, 1311

(Fed. Cir. 2012), *citing Intellectual Prop. Dev., Inc. v. UA-Columbia Cablevision of Westchester, Inc.*, 336 F.3d 1308, 1318 (Fed Cir. 2003). A patent is presumed valid, and the party asserting invalidity has the burden to show the patent is invalid by clear and convincing evidence. 35 U.S.C. § 282(a) (2012); *Microsoft Corp. v i4i Ltd. P'ship*, 131 S. Ct. 2238, 2242 (2011).

IV. ARGUMENT

A. "repeat" ('710 patent, claims 1, 6, 11, 15,16 & 19)

Caltech's Proposed Construction	Hughes's Proposed Construction
"re-use in forming a code"	"sequential duplication"

The term "repeat" appears in claims 1, 6, 11, 15, 16, and 19 of the '710 Patent and claims 1 and 13 of the '032 Patent. Claim 1 of the '710 Patent is recited below:

> 1. A method of encoding a signal, comprising:
>
> obtaining a block of data in the signal to be encoded;
>
> partitioning said data block into a plurality of sub-blocks, each sub-block including a plurality of data elements;
>
> first encoding the data block to from a first encoded data block, ***said first encoding including repeating the data elements in different sub-blocks a different number of times***;
>
> ***interleaving the repeated data elements*** in the first encoded data block; and
>
> second encoding said first encoded data block using an encoder that has a rate close to one.

1. The Intrinsic Evidence Supports Caltech's Construction

The intrinsic evidence—the claims and the specification[4]—suggest a broad meaning for the term "repeat," one that is certainly broader than Defendants' narrow construction.

[4] The prosecution history does not require a narrower construction of "repeat." The term was not the subject of an amendment or traverse of a claim rejection.

The claims of the '710 patent support reading "repeat" to mean "re-use in forming a code." The patent gives the same meaning to the different forms of "repeat" – "repeating" and "repeated." Certain dependent claims require that low-density generator matrix ("LDGM") encoding is a method of "repeating" message bits. *Compare* '710 pat., claims 1 *with* 3, 7; claim 11 *with* 13.[5] A person of ordinary skill in the art would understand that the claimed LDGM coder or transformation performs "repeating" in the broadest sense of that word – re-use in forming a code—not narrowly limited to sequential duplication. *See* Tanner Decl. ¶¶ 17-18.[6]

The specification also supports this reading of the term. Figure 3 of the '710 patent shown below depicts an IRA code as a set of parity checks; the code is the collective output of open circles (parity bits) on the right side of the figure.

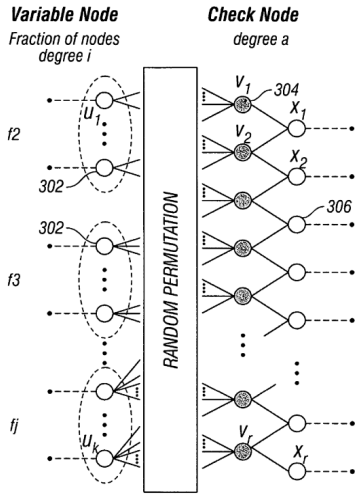


FIG. 3

[5] Claim 1 recites a "first encoding including repeating the data elements" that dependent claim 3 recites is performed by a "first coder," and dependent claim 7 further recites, "wherein the first coder comprises a low-density generator matrix coder." Similarly, Claim 11 recites a method of encoding a signal where the first encoding step requires data blocks to be "repeated," and dependent claim 13 further recites "the first encoding is via a low-density generator matrix transformation."

[6] "Tanner Decl." refers to the Declaration of R. Michael Tanner In Support Of Caltech's Opening Claim Construction Brief, submitted herewith.

Figure 3 clearly shows that message bits are re-used in forming an IRA code. '710 pat., fig. 3, 3:23-43. Each message bit is connected to an information node (open circles on the left side of the figure). *Id*. 3:31-32. The information nodes are arranged in Figure 3 to show subsets of message bits ($f_1, \ldots, f_j$) that each represent bits re-used a specific number of times. Each information node (U_k) is connected randomly to a number of check nodes (closed circles labeled $v_1, v_2, \ldots, v_k$), corresponding to the number of times the message bit at that information node is re-used. *Id*. 3:37-38. The multiple lines entering each check node (closed circles) from the left represent multiple message bits at each check node, which suggest to a person of ordinary skill that the re-use of message bits is not limited to "sequential duplication" as Hughes suggests. Tanner Decl. ¶ 18. The lines merely show that re-use of bits, but not how those bits are re-used.

2. **Hughes's Construction of "Repeat" Is Too Narrow**

Hughes incorrectly asserts that "repeat" should be limited to "sequential duplication"—which is but *one* form of repeating data—to the exclusion of other ways of "repeating" bits described in the specification.

As noted above, the claims suggest a broader meaning for "repeat" because dependent claims recite structure—an LGDM coder—that a person of ordinary skill would understand to support a broader reading of "repeat." *See* Tanner Decl. ¶¶ 17-18. *Compare* '710 pat. claims 1, 3, 11 *with* claims 7, 13. Furthermore, the specification also describes an alternate embodiment of coding using a "low-density generator matrix (LDGM) coder" that "***performs the irregular repeat*** of the k bits in the block."[7] '710 pat. 3:52-55. A generator matrix coder operates by multiplying a set of message bits with a generator matrix to produce a set of encoded bits. *See*

[7] The parties have agreed that the term "irregular" means "a different number of times." Dkt. No. 60. The term "irregular" refers to the number of times bits in one subset are re-used as compared to bits in another subset.

Tanner Decl. ¶ 16. A person of ordinary skill in the art would understand that a LDGM encoder would not perform repeating by sequential duplication but would re-use message bits in forming the code. *See id.* ¶ 18. There is no suggestion in the specification that Hughes's unduly narrow interpretation is warranted.

Because Hughes's proposed construction is unduly narrow and not supported by the intrinsic evidence, it should be rejected.

B. Equation Used in Claim 1 of the '032 patent

Caltech's Proposed Construction	Hughes's Proposed Construction
The parity bit Xj is the sum of (a) the parity bit Xj-1 and (b) the sum of a number, "a," of randomly chosen irregular repeats of the message bits.	This term is indefinite under 35 U.S.C. §112, ¶2. In the alternative, plain meaning.

The disputed equation appears in claim 1 of the '032 patent. It is well defined in the claim and its meaning would be clear to a person of ordinary skill in the art. Claim 1 recites:

> 1. A method comprising:
>
> receiving a collection of message bits having a first sequence in a source data stream;
>
> generating a sequence of parity bits, wherein each parity bit "x_j" in the sequence is in accordance with the formula
>
> $$x_j = x_{j-1} + \sum_{i=1}^{a} v_{(j-1)a+i}$$
>
> where
>
> "x_{j-1}" is the value of the parity bit "j-1," and
>
> $$\sum_{i=1}^{a} v_{(j-1)a+i}$$
>
> is the value of a sum of "a" randomly chosen irregular repeats of the message bits; and
>
> making the sequence of parity bits available for transmission in a transmission data stream.

The equation in claim 1 has been corrected as stated in the Certificate of Correction issued July 27, 2010, and attached to the patent.

1. **The Claims and Intrinsic Evidence Support Caltech's Definition**

Caltech's proposed construction is the plain meaning of this term as used in the '032 patent.[8] Claim 1 of the '032 patent claims a method of generating parity bits using a process of adding together randomly chosen subsets from a collection of incoming message bits, and then performing a recursive "accumulation" operation on the resulting collection of intermediate bits.[9] '032 pat., 2:43-60; 2:66-3:20;3:56-64. Claim 1 of the '032 patent describes both of these steps—generating intermediate bits and then accumulating them—in the disputed equation. Specifically, the claim states that "x_j" is a parity bit, the jth parity bit in the collection. Its value is defined as the sum of "x_{j-1}"—explicitly defined as "the value of the parity bit '*j-1*'"—and the summation ($\sum$) of $v_{(j-1)a+i}$. This summation is also explicitly defined, as "the value of a sum of 'a' randomly chosen irregular repeats of the message bits." Caltech's proposed construction embraces these exact definitions from the claim. The value of the current bit (X_j) is the sum of the previous bit (X_{j-1}) and the sum of "*a*" randomly chosen irregular repeats of the message bits, where "a" is the number of total bits summed.

The specification also supports Caltech's proposed construction for this equation. The specification of the '032 Patent contains an explanation of the exact equation in dispute here. The patent states:

> The value of a parity bit is determined uniquely by the condition that the mod-2 sum of the values of the variable nodes connected to each of

[8] The disputed equation is not addressed in the prosecution history, and therefore is not limited by it.

[9] A recursive formula is a formula that requires the computation of all previous terms for a sequence (e.g., a_1, a_2, a_3, . . . , a_n) in order to find the value of the current term of the sequence, a_n .

> the check nodes is zero. To see this, set $x_0 = 0$. Then if the values of the bits on the *ra* edges coming out of the permutation box are (v_1, . . . , v_{ra}), then we have the recursive formula
>
> $$x_j = x_{j-1} + \sum_{i=1}^{a} v_{(j-1)a+i}$$
>
> for j =1, 2, . . ., r. This is in effect the encoding algorithm.

'032 pat., 4:4-19 (emphasis added). This passage in the specification explains how the claimed equation is used, and conforms with Caltech's proposed construction.

The parties did not cite any extrinsic dictionary definitions or literature for this claim. Accordingly, the claim should be understood by the definitions provided for it in the intrinsic evidence.

2. **The Equation Is Not Indefinite**

Hughes asserts that this equation is indefinite because "the claim does not define the value of the first parity bit in the sequence." (Dkt. 55 at 81.) The intrinsic evidence and the common understanding of a person of ordinary skill in the art demonstrates that Hughes is incorrect.

Where a claim term is a mathematical equation, it is permissible for a person of ordinary skill to look to the specification to understand its meaning. *See Ex Parte Nishioka*, Appeal 2009-001507, 2010 WL 191205, at *4 (B.P.A.I. Jan. 10, 2010) ("[T]he attachment of meaning to the variable expressed in the equations of the claims, ***either through definitions in the specification or in the claims themselves***, adds necessary clarity to the claims to be able to properly appreciate the metes and bounds of the protected invention.") (emphasis added); *Johnson & Johnson Vision Care, Inc. v. CIBA Vision Corp.*, 648 F. Supp. 2d 1294, 1336-37 (M.D. Fla. 2009) (finding a term definite when it relied on a disputed equation if the person of ordinary skill could understand and apply the correct equation).

The specification here explains that the claimed equation defines a set of parity bits, (x_1, . . . x_j), given a set of irregular repeats of message bits, (v_1, . . . v_{ra}).

'032 pat., 3:65-4:19. x_0 is a starting condition for the recursive equation, not a parity bit. The specification describes ***an example*** where x_0 is set equal to zero. *Id.*, 4:6-7. A person of ordinary skill would understand that, here, a bit can only be one of two values—a "0" or a "1." *See* Tanner Decl. ¶ 30. Choosing to set x_0 to 1 instead of to 0 would in effect add 1 to ***all*** of the generated parity bits. A person of ordinary skill would understand that ***both*** cases are covered by the claimed method. *See id.*

Furthermore, a claim is not indefinite merely because it broadly embraces multiple possibilities, where a person of ordinary skill has reasonable certainty as to what is covered. *See Nautilis*, 134 S. Ct. at 2129; *Ultimax Cement Mfg. v. CTS Cement Mfg.*, 587 F.3d 1339, 1352 (Fed. Cir. 2010) ("[A] formula containing over 5000 possible combinations is not necessarily ambiguous if it sufficiently notifies the public of the scope of the claims."). Here, the specification clearly informs a person of ordinary skill in the art of the bounds of the claim. *See* '032 pat., 4:6-7.

Because the equation is well defined by the '032 patent and Caltech's proposed construction accurately embraces the meaning in the patent, that construction should be adopted.

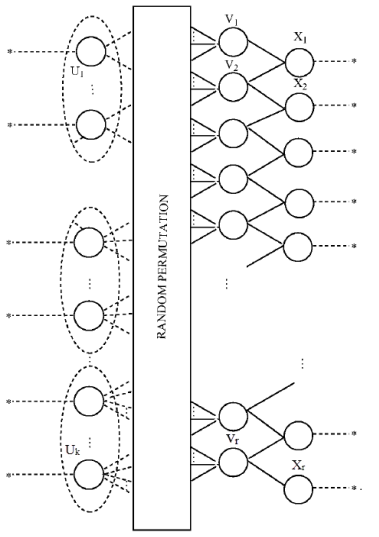
C. Diagram Used in Claims 11 & 18 of '032 patent

Caltech's Proposed Construction[10]	Hughes's Proposed Construction
A graph representing an IRA code as a set of parity checks where every message bit is repeated, at least two different subsets of message bits are repeated a different number of times, and check nodes, randomly connected to the repeated message bits, enforce constraints that determine the parity bits.	This term is indefinite under 35 U.S.C. §112, ¶2. At a minimum, however, this limitation requires "at least three information bits, where each of the three information bits contributes to a different number of parity checks."

The disputed term (a graph) is claimed in independent claims 11 and 18 of the '032 Patent. Claim 11 illustrates how the graph is used in the claims:

> 11. A device comprising:
>
> an encoder configured to receive a collection of message bits and encode the message bits to generate a collection of parity bits in accordance with the following Tanner graph:

[10] Caltech has revised its construction from the proposal set forth in the June 4 Joint Claim Construction Statement. (Dkt. 60). Its construction accurately reflects Caltech's position and highlights the dispute between the parties. Specifically, on June 8, four days after the joint statement was filed, Caltech discovered a transcription error that omitted the words "for example" from its proposal. As a result, Caltech decided to remove the exemplary clause from its June 4 proposal, and informed Hughes counsel of this on June 9. On June 10, Hughes counsel indicated by e-mail that it objected to Caltech's changes. On June 11, Caltech advised Hughes that Caltech's proposed construction will be further revised to more clearly describe Caltech's proposal and clarify the dispute between Caltech and Hughes. Caltech considered filing a motion to amend the joint statement but decided it made more sense to address this issue directly in the opening briefs on disputed claim terms rather than burden the Court with unnecessary motion practice that would further delay the claim construction process.



The claimed graph from the '032 patent shown above was altered to replace "U_1," "V_1," and "X_1" with "U_k," "V_r," and "X_r," respectively, as stated in the Certificate of Correction issued Feb. 17, 2009, and attached to the patent.

1. **The Intrinsic Evidence Supports Caltech's Construction**

The claims of the '032 Patent support Caltech's proposed construction. First, claim 11 states that the Tanner graph represents "a collection of parity bits" encoding "a collection of message bits" received by the encoder. Dependent claim 13 explains that the encoder may comprise a low-density generator matrix (LDGM) coder that performs irregular repeats on the message bits, and comprise an accumulator that sums the bits to create the final parity bits. Therefore, independent claim 11 describes broadly a method of creating an IRA code.

Caltech's proposed construction is grounded directly in the language of the specification in describing the invention and representative figure. First, the patent explains that the parity bits generated by the claimed method form "an irregular repeat and accumulate (IRA) code." '032 pat., 3:30-31. An IRA code "may be represented by a set of parity checks." *Id.*, 3:32-33. That set of parity checks may further "be represented in a bipartite graph, called the Tanner graph, of the code." *Id.*, 3:33-34. Figure 3 is an exemplary Tanner graph depicting a set of parity bits

generated according to the claimed method. *Id.*, 3:35-36. Accordingly, Caltech begins its construction by explaining that the disputed figure is "a graph representing an IRA code as a set of parity checks."

Next, the claimed figure shows that the received message bits are repeated, and different subsets are repeated different numbers of times. The specification explains that the Tanner graph may be used to represent "IRA code[s] with parameters (f_1, . . . , f_j; a), where $f_i \geq 0$, $\sum_i f_i = 1$ and "a" is a positive integer." *Id.*, 3:35-37. In less mathematical terms, a particular IRA code is defined by number of times each subset of bits is repeated (i), what fraction of bits is included in each subset (f_i), and the number of connections incoming to each check node (a). The specification explains, "Each information node is connected to a number of check nodes. The fraction of information nodes connected to exactly i check nodes is f_i." *Id.*, 3:42-45. As stated in Caltech's construction, different subsets of messages bits are repeated different numbers of times. *Id.*, 2:54-56; 3:57-58.

The specification clearly provides a specific example where there are only two subsets of bits, f_2 and f_3. *See id.*, 3:44-49. "The fraction of information nodes connected to exactly i check nodes is f_i. For example, in the Tanner graph 300, each of the f_2 information nodes are connected to two check nodes, corresponding to a repeat of q=2, and each of the f_3 information nodes are connected to three check nodes, corresponding to q=3." *Id.* As a result of the message bits being repeated, they are connected to check nodes in a random manner. The specification explains with respect to Figure 3, "Each check node 304 is connected to exactly "a" information nodes 302. These connections can be made in many ways as indicated by the permutation block 310, which re-orders the "edges" (i.e., connections) joining information nodes 302 and check nodes 304, as shown in Figure 3. These connections correspond to the scrambling performed by the interleaver 204." *Id.*, 3:49-55. The check nodes enforce the constraint that all bits connected to them sum to zero, thus determining the value of the connected parity bits. *Id.*, 4:1-7.

Caltech's proposed construction accurately captures the disclosure in the specification.

2. **The Extrinsic Evidence Supports Caltech's Construction**

The extrinsic evidence also supports Caltech's proposed construction. At the time of the filing of the first patent application that led to the '032 Patent, Tanner graphs had a well-understood meaning in the digital communications coding art. Tanner graphs were introduced by Michael Tanner in his 1981 paper, "A Recursive Approach to Low Complexity Codes." Tanner Decl., Ex. I ("Tanner paper"). Codes may be represented as bipartite graphs, where information nodes are connected to "subcode" nodes, which each may "represent a simple parity check." Tanner paper, at 2. Such graphs were used consistently in the art to describe codes. *See* Dkt. 55-5 at 3, 26, 33. The '032 patent cites publications that use bipartite graphs to describe codes. *See, e.g.*, '032 pat, References Cited—Other Publications; Declaration of Kathy Peng Ex. 5 (using a bipartite graph to show an LDPC code).

3. **The Figure Is Not Indefinite**

Hughes incorrectly argues the figure in the claims is indefinite because the claims do not "provide any explanation of how the image may be interpreted." Dkt. 55, at 82. However, the detailed explanation of every component of figure 3 provides ample information for a person of ordinary skill to understand the scope of codes covered by the claimed invention with reasonable certainty. *Nautilus*, 134 S. Ct. at 2129. And a person of ordinary skill in the art at the time of the invention would have been familiar with Tanner graphs. *See* Tanner Decl. ¶ 25.

The elements of the Tanner graph are described in the specification. For example, the message bits (on the left) are labeled U_1 through U_k, and the generated parity bits are labeled X_1 through X_r, as described in the specification. '032 pat., 3:39-41; Tanner Decl. ¶¶ 20-21. The nodes V_1 through V_r are defined as check nodes, constraining the connected nodes to sum to zero. '032 pat., 3:41-43, 4:5-7;

Tanner Decl. ¶¶ 20-21. The method in which the message bits are connected to the check nodes—via a random permutation—is clearly labeled in the figure. '032 pat., Fig. 3; Tanner Decl. ¶ 26. The graph represents a class of codes, called IRA codes, that define how to generate parity bits for a given set of message bits. *See* Tanner Decl. ¶ 25. A person of ordinary skill would readily understand the figure and its scope. *See id.* ¶ 27. Because the figure provides "reasonable certainty" to those of ordinary skill, the claims are not indefinite.

4. **Hughes's Alternative Construction Conflicts with the Specification**

In the alternative, Hughes proposes that the figure be limited to "at least three" bits, where *each* of the bits contributes to a different number of parity checks. Hughes's alternative is inconsistent with the description in the specification that the claimed graph is defined by a set of parameters (f_1, . . . f_j; a), where each of f_i is greater than or equal to zero, and the sum of all of the f_i is equal to one. '032 pat., 3:33-36. The patent only describes two subsets f when describing Figure 3. *Id.*, 3:44-49. The claimed graph (which is based on Figure 3) is merely a description of a genus of codes. Although the graph shows three different subsets (f_2, f_3, and f_j), the graph and the explanation in the specification clearly allow for two subsets, as long as the bits are irregularly repeated, i.e., the sum of all fractions, f_i, equals one. *See id.*, 3:35-37. The ellipses between bits and subsets of bits indicate that the claimed graph is exemplary and that the number of subsets is not set, subject to the definitional parameters described in the specification. Caltech's construction takes this into account.

Even Hughes recognizes the nature of the graph as a description of a genus. Its proposed alternative construction is not limited to f_2, f_3, and f_j. There is no support for limiting the claims artificially here.

D. "codeword" ('781 patent, claims 1-4, 11, 13-16 & 19-21)

Caltech's Proposed Construction	Hughes's Proposed Construction
"a discrete encoded sequence of data elements"	"a discrete sequence of data elements encoded for transmission"

The term "codeword" appears in claims 1-4, 11, 13-16, 19-21 of the '781 patent. Exemplary claim 1 of the '781 patent is reproduced below:

> 1. A method of encoding a signal, comprising:
>
> receiving a block of data in the signal to be encoded, the block of data including information bits;
>
> performing a first encoding operation on at least some of the information bits, the first encoding operation being a linear transform operation that generates L transformed bits; and
>
> performing a second encoding operation using the L transformed bits as an input, the second encoding operation including an accumulation operation in which the L transformed bits generated by the first encoding operation are accumulated, said second encoding operation producing at least a portion of a **codeword**, wherein L is two or more.

The parties agree that the proposed construction of this term should include "a discrete [encoded] sequence of data elements." The dispute here can be narrowed to whether the meaning of this term should be limited to a discrete sequence of data elements "encoded for transmission," as Hughes contends.

1. Caltech's Proposed Construction Is Consistent with the Intrinsic Evidence

The claims of the '781 patent do not require that codeword be "transmitted" or "encoded for transmission." At most, the claims suggest that a codeword may be "output." *See* '781 pat., claims 2-4, 14-15, 21. The outputting of codewords is distinct from transmission. *See, e.g., id.*, 3:3-5 ("In an embodiment, the inner coder is an accumulator which produces outputs that are the modulo two (mod-2) partial sums of its inputs"). But no claim language suggests that the term "codeword" is limited to transmission.

The specification of the '781 patent similarly does not limit the term to encoding "for transmission." There is nothing in the specification, nor the prosecution history, that suggests such a limitation. At most, the specification states that the "[t]he encoded data output from the inner coder ***may*** be transmitted on a channel and decoded in linear time at a destination using iterative decoding techniques." *Id.*, 2:11-13 (emphasis added). However, this is just an example of what to do with a codeword (i.e., transmit it) after it has been generated. This does not require that the codeword ***must*** be encoded for transmission. Absent any definitional or limiting language in the intrinsic record, Hughes's proposed construction must be rejected. *See Dealertrack v. Huber*, 674 F.3d 1315, 1322 (Fed. Cir. 2012) ("To specifically exclude the Internet would thus require a waiver of claim scope that is both so clear as to show reasonable clarity and deliberateness, and so unmistakable as to be unambiguous evidence of disclaimer.").

2. **Caltech's Construction is Supported by Extrinsic Evidence**

The extrinsic evidence supports the ordinary meaning proposed by Caltech. Persons of ordinary skill in the art use the term "codeword" broadly. *See* Tanner Decl. ¶ 41; Tanner Decl. Ex. H (Shu Lin *et al.*, *Error Control Coding: Fundamentals & Applications* 2 (1983) ("The design and implementation of channel encoders to combat the noisy environment in which code words must be ***transmitted or stored*** is one of the major topics of this book.") (emphasis added)). In fact, a "codeword" need not be transmitted at all, as channel coding techniques such as the invention here are used in storage applications to help ensure that errors in retrieved data from storage (such as a hard drive) can be corrected. *Id.* ¶ 40. Codewords can be used with channel coding techniques in data compression applications, where data is coded then compressed to allow for error correction of recovered data after decompression. *Id*. Such applications do not require transmission.

3. Hughes' Proposed Construction Improperly Imports Limitation into the Claims

As discussed above, there is ample evidence to show that "codeword" is not limited to "encoded for transmission." Although codewords can and often are used in channel coding for transmission, Hughes's proposed construction improperly adds this limitation in violation of the prohibition importing limitations from the specification. *See CollegeNet, Inc. v. ApplyYourself, Inc.*, 418 F.3d 1225, 1231 (Fed. Cir. 2005) ("In examining the specification for proper context, however, this court will not at any time import limitations from the specification into the claims."); *Intervet America, Inc. v. Kee-Vet Laboratories, Inc.*, 887 F.2d 1050, 1053 (Fed. Cir. 1989) ("[T]his court has consistently adhered to the proposition that courts cannot alter what the patentee has chosen to claim as his invention, that limitations appearing in the specification will not be read into claims, and the interpreting what is meant by a word in a claim is not to be confused with adding an extraneous limitation appearing in the specification, which is improper.") (internal quotations omitted). Hughes's proposal should be rejected.

E. "combine" / "combining" ('833 patent, claims 1, 2, 3, 8, 9, 10 & 13)

Caltech's Proposed Construction[11]	Hughes's Proposed Construction
Plain and ordinary meaning—"performing logical operations on"	This term is indefinite under 35 U.S.C. §112, ¶2. In the alternative, plain meaning.

[11] Caltech has also revised its construction for this term from the proposal set forth in the June 4 Joint Claim Construction Statement (Dkt. 60). This change was made to move Caltech's construction closer to the alternative construction proposed by Hughes of plain meaning. Hughes was informed of this proposal on June 9, and it indicated on June 10 that it objected to the new proposed construction. Similar to the construction for the figure in the '032 patent claims, Caltech did not wish to burden the Court with motion practice on this term.

The term "combine" or "combining" appears in claims 1, 2, 3, 8, 9, 10, and 13 of the '833 patent. Exemplary claims 1 and 2 of the '833 patent are reproduced below:

> 1. An apparatus for performing encoding operations, the apparatus comprising:
>
> a first set of memory locations to store information bits;
>
> a second set of memory locations to store parity bits;
>
> a permutation module to read a bit from the first set of memory locations and **combine** the read bit to a bit in the second set of memory locations based on a corresponding index of the first set of memory locations and a corresponding index of the second set of memory locations; and
>
> an accumulator to perform accumulation operations on the bits stored in the second set of memory locations, wherein two or more memory locations of the first set of memory locations are read by the permutation module different times from one another.
>
> 2. The apparatus of claim 1, wherein the permutation module is configured to perform the **combine** operation to include performing mod-2 or exclusive-OR sum.

In an effort to narrow the dispute between the parties, Caltech has revised the proposed construction of this term to be consistent with Hughes' alternative construction—the plain and ordinary meaning.

1. **Caltech's Construction Is Supported by the Intrinsic Evidence**

The claims of the '833 patent support Caltech's proposed construction. This term is associated with the portion of the encoding operation that occurs before the accumulation operation. *See* '833 pat., claims 1 and 8. According to the doctrine of claim differentiation, dependent claims may aid in interpreting the scope of the independent claims. *See Laitram Corp. v. NEC Corp.*, 62 F.3d 1388, 1392 (Fed. Cir. 1995) (using dependent claims to hold that printing by "strobing" expressly claimed in the dependent claim was covered by more general language in the independent claim). Here, claim 1 recites "a permutation module to read a bit from the first set of memory locations and ***combine the read bit to a bit in the second set***

of memory locations based on a corresponding index of the first set of memory locations and a corresponding index of the second set of memory locations." Claim 2, which depends from claim 1, recites "the permutation module is configured to perform the combine operation ***to include performing mod-2 or exclusive-OR sum***." Independent claim 8 and dependent claim 9 recite the same language regarding "combine/combining." Accordingly, based on the doctrine of claim differentiation, the "combine/combining" term includes performing logical operations but is not limited to just mod-2 or exclusive-OR sum. Caltech's broader statement of ordinary meaning is consistent with the limitations as set forth in these claims.

Caltech's proposed construction is also consistent with the specification. The specification discusses the bits recited in the claims as follows:

> Each of the information bits is associated with one of the information nodes **302**, and each of the parity bits is associated with one of the parity nodes **306**. The value of a parity bit is determined uniquely by the condition that the mod-2 sum of the values of the variable nodes connected to each of the check nodes **304** is zero. To see this, set x_0=0. Then if the values of the bits on the ra edges coming out the permutation box are (v_1, . . . , v_{ra}), then we have the recursive formula for j=1, 2, . . . , r. This is in effect the encoding algorithm.
>
> $$x_j = x_{j-1} + \sum_{i=1}^{a} v_{(j-1)a+i} ,$$

According to the above equation, x_{j-1} is the value of a parity bit "*j-1*" and the summation (∑) of $v_{(j-1)a+i}$ is the value of a sum of "*a*" randomly chosen irregular repeats of the message bits. *See* '833 pat., 3:65- 4:20; '032 pat., claim 1. This summation disclosed in the patent is an example of the combining step recited in claims 1 and 2. In other words, the '833 patent implements the encoding algorithm described above in an operation that generates parity bits by (i) "combining" randomly chosen sets of message bits to form intermediate bits and then (ii) performing an accumulation operation on the intermediate bits (i.e., a recursive operation on the resulting collection of intermediate bits).

The specification describing mod-2 sum is an example of a logical operation that may be performed on the bits during the encoding operation. *See* '833 pat., 4:1-10; 3:5-24; 2:10-12. A specification need not set out every conceivable example of logical operations for the claims to encompass logical operations generally. *See Phillips v. AWH Corp.*, 415 F.3d 1303, 1323 (Fed. Cir. 2005); *Woods v. DeAngelo Marine Exhaust, Inc.*, 692 F.3d 1272, 1283 (Fed. Cir. 2012). The patent does not expressly limit the operations that would meet the term "combine." Thus, it should be given its ordinary meaning, which Caltech's proposed construction describes – "performing logical operations on." The prosecution history does not address this term.

2. **Caltech's Construction Is Supported by Extrinsic Evidence**

The understanding of this term by one of ordinary skill in the art as reflected in prior art patents also supports Caltech's construction and is consistent with the intrinsic record. *See* Tanner Decl. ¶¶ 34-36. For example, U.S. Patent 3,222,506 relates to digital computers and a logic unit that performs logical operations on bits. It describes combining bits P and Q by using "logical AND", "logical OR", "EXCLUSIVE OR", or "identity" operations. U.S. Patent No. 3,222,506 at 2:9-31. As another example, U.S. Patent 5,386,523 relates to a system and method of generating address for a computer memory. It describes "overlapped bits . . . logically combined in a boolean operation" including logical OR. U.S. Patent 5,386,523 at 2:40-52. Accordingly, those of ordinary skill in the art at the time of the invention understood "combine"/"combining" of bits to mean "performing logical operations on" the bits.

3. **This Term Is Not Indefinite under 35 U.S.C. §112, ¶2**

In its invalidity contentions, Hughes incorrectly alleges that this term is indefinite because "[o]ne of ordinary skill in the art would not be able to ascertain

how the bits are combined (e.g., Boolean AND, Boolean OR, Boolean XOR, mod-2 addition, concatenation, etc.)." Dkt. No. 55, at 83-84.

First, by identifying illustrative logical operations that can be performed on bits, Hughes's own statement of invalidity position shows that the scope of the term is ascertainable with reasonable certainty. *See Nautilus*, 134 S. Ct. at 2129. Here, one of ordinary skill in the art would understand the scope of the term "combine/combining" with reasonably certainty based on the claims viewed in light of the intrinsic evidence. *See* Tanner Decl. ¶ 37.

Second, it is unnecessary to provide every example of how bits can be "combined" to satisfy the definiteness test. *Nautilus*, 134 S. Ct. at 2123 ("Section 112's definiteness requirement must take into account the inherent limitations of language. . . . some modicum of uncertainty is the price of ensuring the appropriate incentives for innovation.") (internal quotations omitted). Here, the plain and ordinary meaning of the term "combine" and the scope of this term is clear to one of ordinary skill in the art. Accordingly, this term is not indefinite.

F. "transmitting" / "transmission" ('032 patent, claims 1, 8 & 10)

Caltech's Proposed Construction	Hughes's Proposed Construction
"sending over a channel"	"sending over a physical channel"

The terms "transmission" and "transmitting" appear in claims 1, 8, and 10 of the '032 patent. Claim 1 is set forth below for context:

> 1. A method comprising:
>
> receiving a collection of message bits having a first sequence in a source data stream;
>
> generating a sequence of parity bits, wherein each parity bit "x_j" in the sequence is in accordance with the formula
>
> $$x_j = x_{j-1} + \sum_{i=1}^{a} v_{(j-1)a+i}$$
>
> where
>
> "x_{j-1}" is the value of the parity bit "j-1," and

$$\sum_{i=1}^{a} v_{(j-1)a+i}$$

is the value of a sum of "a" randomly chosen irregular repeats of the message bits; and

making the sequence of parity bits available for transmission in a transmission data stream.

Claim 8 goes on to claim "the method of claim 1, further comprising ***transmitting the sequence of parity bits***," and claim 10 further claims "the method of claim 8, wherein transmitting the sequence of parity bits comprises ***transmitting the sequence of parity bits*** as part of a systematic code." The dispute here can be narrowed to whether the meaning of this term should include the extraneous word "physical," as Hughes contends.

1. **The Intrinsic Evidence Supports Caltech's Construction**

The specification supports Caltech's construction, which broadly captures the different manners of transmission without unnecessary language.[12] The specification repeatedly refers to transmitting in connection with a channel, without limiting transmissions to a particular channel. *See, e.g.*, '032 pat., 2:8-10 ("the encoded data output from the inner coder may be transmitted ***on a channel*** and decoded in linear time at a destination using iterative decoding techniques"); 6:10-15 (discussing performance of encoding methods on "three memoryless channel models: a binary erasure channel (BEC); a binary symmetric channel (BSC); and an additive white Gaussian noise (AGWN) channel"); 6:15-20(stating for the BEC, "When 0 is transmitted, the receiver can receive either 0 or an erasure E. An erasure E output means that the receiver does not know how to demodulate the output. Similarly, when 1 is transmitted, the receiver can receive either 1 or E"). There is no need to add the word "physical" to the construction of this term. *See also id.*,

2:38-40 ("format[ting] blocks of data for transmission, introducing redundancy into the stream of data to protect the data from loss due to transmission errors,"); *id.*, 7:1-3 ("The selection of a degree profile for use in a particular transmission channel is a design parameter, which may be affected by various attributes of the channel."). Thus the disclosures of transmitting in the patent support a broad construction of "sending over a channel."

2. To the Extent Hughes Seeks to Exclude Satellite Communications, Its Construction Is Incorrect

While "transmissions" may be described as taking place over a physical channel, the definition of a transmission need not do so. At no point does the patent state that a channel must be "physical"—in fact, the patent ***never uses the word "physical" at all.*** The use of "physical" in Hughes's construction is extraneous and not necessary to allow a jury to understand the scope of the claimed invention. And to the extent that Hughes proposes this extraneous limitation to exclude satellite communications such as those accused here, Caltech disagrees. The extrinsic evidence demonstrating the understanding of a person of ordinary skill in the art at the time of the alleged invention shows that satellite communications are squarely within the understanding of the term "transmission." *See* Tanner Decl. Ex. H, at 2-3 (describing "satellite links" as an example of a "typical transmission channel"). Thus Hughes's proposed construction should be rejected.

V. CONCLUSION

For the foregoing reasons, Defendants' proposed claim constructions should be rejected and Caltech's proposed claim constructions should be adopted.

[12] This term is not discussed in the prosecution history.

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QUINN EMANUEL URQUHART & SULLIVAN, LLP

By */s/ James R. Asperger*
James R. Asperger
Kevin P.B. Johnson
Mark Yeh-Kai Tung

Attorneys for Plaintiff California Institute of Technology