ATTACHMENT 5

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Paper 18
Entered: April 27, 2015

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

HUGHES NETWORK SYSTEMS, LLC and
HUGHES COMMUNICATIONS, INC.,
Petitioner,

v.

CALIFORNIA INSTITUTE OF TECHNOLOGY,
Patent Owner.

Case IPR2015-00068
Patent 7,116,710 B1

Before KALYAN K. DESHPANDE, GLENN J. PERRY, and TREVOR M. JEFFERSON, *Administrative Patent Judges*.

JEFFERSON, *Administrative Patent Judge*.

DECISION
Denying Institution of *Inter Partes* Review
37 C.F.R. § 42.108

I. INTRODUCTION

Hughes Network Systems, LLC and Hughes Communications, Inc. (collectively, "Petitioner") filed a Corrected Petition requesting an *inter partes* review of claims 1, 3, 4, 5, 6, 15, 16, 20, 21, and 22 of U.S. Patent No. 7,116,710 B1 (Ex. 1001, "the '710 patent"). Paper 4 ("Pet."). California Institute of Technology ("Patent Owner") timely filed a Preliminary Response. Paper 13 ("Prelim. Resp."). We have jurisdiction under 35 U.S.C. § 314(a), which provides that an *inter partes* review may not be instituted "unless . . . there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition." After considering the Petition, the Preliminary Response, and associated evidence, we conclude that Petitioner has not demonstrated a reasonable likelihood that it would prevail in showing unpatentability of all the challenged claims. Thus, we deny institution of an *inter partes* review of claims 1, 3, 4, 5, 6, 15, 16, 20, 21, and 22 of the '710 patent.

A. Related Proceedings

Petitioner indicates that the '710 patent is the subject of the proceedings in *California Institute of Technology v. Hughes Communications, Inc. et al.*, No. 13-cv-07245 (C.D. Cal.). Pet. 1–2.

The '710 patent is also the subject of IPR2015-00067. Additionally, Petitioner indicates that the '710 patent is related to U.S. Patent No. 7,421,032, U.S. Patent No. 7,916,781, and U.S. Patent No. 8,284,833, which are the subject of IPR2015-00059, IPR2015-00060, IPR2015-00061, and IPR2015-00081. Paper 7, 1–2.

B. The '710 Patent

The '710 patent describes the serial concatenation of interleaved convolutional codes forming turbo-like codes. Ex. 1001, Title. It explains some of the prior art with reference to its Figure 1, reproduced below.

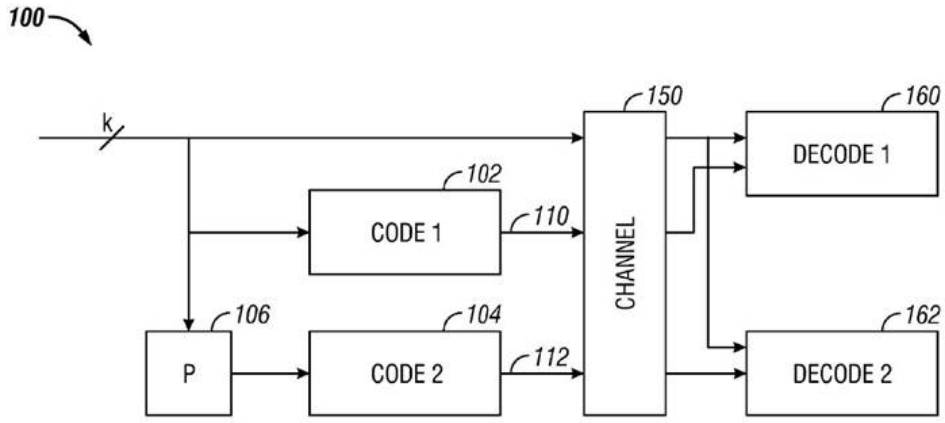


FIG. 1
(Prior Art)

Figure 1 is a schematic diagram of a prior "turbo code" system. *Id.* at 2:14–15. The '710 patent Specification describes Figure 1 as follows:

> A standard turbo coder 100 is shown in FIG. 1. A block of k information bits is input directly to a first coder 102. A k bit interleaver 106 also receives the k bits and interleaves them prior to applying them to a second coder 104. The second coder produces an output that has more bits than its input, that is, it is a coder with rate that is less than 1. The coders 102,104 are typically recursive convolutional coders.
>
> Three different items are sent over the channel 150: the original k bits, first encoded bits 110, and second encoded bits 112. At the decoding end, two decoders are used: a first constituent decoder 160 and a second constituent decoder 162. Each receives both the original k bits, and one of the encoded portions 110, 112. Each decoder sends likelihood estimates of the decoded bits to the other decoders. The estimates are used to decode the uncoded information bits as corrupted by the noisy channel.

Id. at 1:38–53 (emphasis omitted).

A coder 200, according to a first embodiment of the invention, is described with respect to Figure 2, reproduced below.

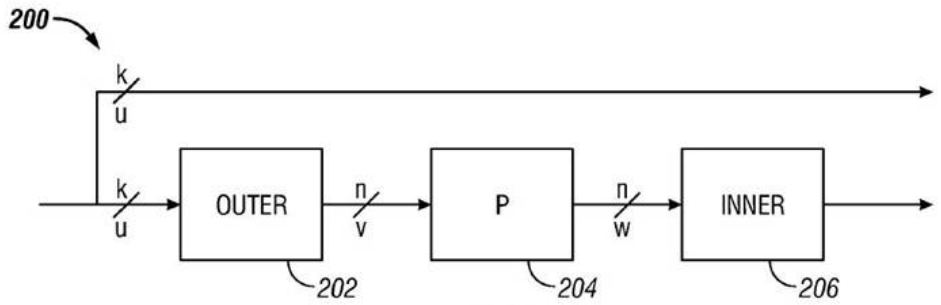


FIG. 2

Figure 2 of the '710 patent is a schematic diagram of coder 200. *Id*. at2:16–17.

The Specification states that "coder 200 may include an outer coder 202, an interleaver 204, and inner coder 206." *Id*. at 2:34–35 (emphasis omitted). It further states as follows.

> The outer coder 202 receives the uncoded data. The data may be partitioned into blocks of fixed size, say k bits. The outer coder may be an (n,k) binary linear block coder, where n>k. The coder accepts as input a block u of k data bits and produces an output block v of n data bits. The mathematical relationship between u and v is $v=T_0u$, where T_0 is an n x k matrix, and the rate[1] of the coder is k/n.
>
> The rate of the coder may be irregular, that is, the value of T_0 is not constant, and may differ for sub-blocks of bits in the data block. In an embodiment, the outer coder 202 is a repeater that repeats the k bits in a block a number of times q to produce a block with n bits, where n=qk. Since the repeater has an irregular output, different bits in the block may be repeated a

[1] The "rate" of an encoder refers to the ratio of the number of input bits to the number of resulting encoded output bits related to those input bits. *See* Ex. 1010 ¶ 19.

> different number of times. For example, a fraction of the bits in the block may be repeated two times, a fraction of bits may be repeated three times, and the remainder of bits may be repeated four times. These fractions define a degree sequence or degree profile, of the code.
>
> The inner coder 206 may be a linear rate-1 coder, which means that the n-bit output block x can be written as $x=T_I w$, where T_I is a nonsingular n x n matrix. The inner coder 210 can have a rate that is close to 1, e.g., within 50%, more preferably 10% and perhaps even more preferably within 1% of 1.

Id. at 2:41–64 (emphasis omitted and footnote added). Codes characterized by a regular repeat of message bits into a resulting codeword are referred to as "regular repeat," whereas codes characterized by irregular repeat of message bits into a resulting codeword are referred to as "irregular repeat." The second ("inner") encoder 206 performs an "accumulate" function. Thus, the two step encoding process illustrated in Figure 2, including a first encoding ("outer encoding") followed by a second encoding ("inner encoding"), results in either a "regular repeat accumulate" ("RRA") code or an "irregular repeat accumulate ("IRA") code, depending upon whether the repetition in the first encoding is regular or irregular.

Figure 4 of the '710 patent, reproduced below, shows an alternative embodiment in which the first encoding is carried out by a low density generator matrix.

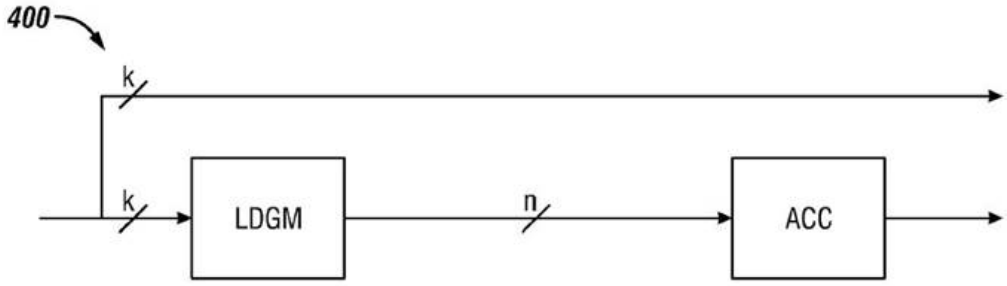


FIG. 4

Figure 4 of the '710 patent is a schematic of an irregular repeat and accumulate coder using a Low density generator matrix (LDGM)[2] coder. *Id.* at 2:20–21, 3:25. The LDGM coder "performs an irregular repeat of the k bits in the block, as shown in FIG. 4." *Id.* at 3:52–54. LDGM codes are a special class of low density parity check codes that allow for less encoding and decoding complexity. LDGM codes are systematic linear codes generated by a "sparse" generator matrix. No interleaver (as in the Figure 2 embodiment) is required in the Figure 4 embodiment because the LDGM provides scrambling otherwise provided by the interleaver.

C. Illustrative Claim

Petitioner challenges claims 1, 3, 4, 5, 6, 15, 16, 20, 21, and 22 of the '710 patent. Pet. 3–4. Claim 1 is illustrative of the claims at issue and is reproduced below:

> 1. A method of encoding a signal, comprising:
> obtaining a block of data in the signal to be encoded;

[2] A "generator" matrix (typically referred to by "G") is used to create (generate) codewords. A parity check matrix (typically referred to by "H") is used to decode a received message.

> partitioning said data block into a plurality of sub-blocks, each sub-block including a plurality of data elements;
>
> first encoding the data block to from a first encoded data block, said first encoding including repeating the data elements in different sub-blocks a different number of times;
>
> interleaving the repeated data elements in the first encoded data block; and
>
> second encoding said first encoded data block using an encoder that has a rate close to one.

D. The Alleged Grounds of Unpatentability

The information presented in the Petition sets forth proposed grounds of unpatentability of claims 1, 3, 4, 5, 6, 15, 16, 21, and 223 of the '710 patent as follows (*see* Pet. 14–43):

References	Basis	Claim(s) Challenged
Divsalar[3] and Luby[4]	§ 103(a)	1, 3, 4, 5, 6, 15, 16, 21, and 22
Divsalar, Luby, and Hall[5]	§ 103(a)	15, 16, 21, and 22
Divsalar, Luby, and Ping[6]	§ 103(a)	20
Divsalar, Luby, Ping, and Hall	§ 103(a)	20

[3] Dariush Divsalar, et al., *Coding Theorems for "Turbo-Like" Codes*, THIRTY-SIXTH ANNUAL ALLERTON CONFERENCE ON COMMUNICATION, CONTROL, AND COMPUTING, Sept. 23–25, 1998, at 201–209 (Ex. 1011, "Divsalar").
[4] U.S. Patent No. 6,081,909, issued June 27, 2000 (Ex. 1016, "Luby").
[5] Eric K. Hall, et al., *Stream-Oriented Turbo Codes*, 48TH IEEE VEHICULAR TECHNOLOGY CONFERENCE 1998 at 71-75 (Ex. 1013, "Hall").
[6] L. Ping, et al., *Low Density Parity Check Codes with Semi-Random Parity Check Matrix*, 35 ELECTRONIC LETTERS 38–39, 1999 (Ex. 1014, "Ping").

II. ANALYSIS[7]

A. Claim Construction

The Board will interpret claims of an unexpired patent using the broadest reasonable construction in light of the specification of the patent in which they appear. *See* 37 C.F.R. § 42.100(b); Office Patent Trial Practice Guide, 77 Fed. Reg. 48756, 48766 (Aug. 14, 2012). Under the broadest reasonable construction standard, claim terms are given their ordinary and customary meaning, as would be understood by one of ordinary skill in the art in the context of the entire disclosure. *In re Translogic Tech. Inc.*, 504 F.3d 1249, 1257 (Fed. Cir. 2007).

Petitioner discusses several claim terms and the District Court's construction of those terms, but does not offer proposed constructions. Pet. 12–14. We determine that no claim construction is necessary for the purposes of this decision.

B. Divsalar (Ex. 1011) and Luby (Ex. 1016)

Petitioner contends that claims 1, 3, 4, 5, 6, 15, 16, 21, and 22 are unpatentable under 35 U.S.C. § 103(a) over Divsalar and Luby (Pet. 14–33) and that each of the remaining challenged claims 15, 16, 20, 21, and 22 are unpatentable under 35 U.S.C. § 103(a) as obvious over Divsalar and Luby in combination with other asserted prior art (Pet. 34–43).

[7] Patent Owner argues that, as a threshold matter, the Petition should be dismissed because Petitioner fails to identify all real parties in interest. Prelim. Resp. 3. Because we have determined that Petitioner has not demonstrated a reasonable likelihood of prevailing, we need not address the real parties in interest issue in this Decision.

1. Divsalar (Ex. 1011) as a Printed Publication

Petitioner states that Divsalar was "published no later than April 30, 1999 at the University of Texas library." Pet. iii; *see also* Pet. 2 (stating that Divsalar was "published at least by April 30, 1999 and available as prior art under 35 U.S.C. § 102(b)"). In support, Petitioner proffers the declaration testimony of a Univ. of Texas librarian (Ex. 1064) including an acquisition record pasted into an email. According to Petitioner's expert, Dr. Henry D. Pfister, The Allerton Conference is generally regarded as one of the main conferences in the field of information theory and communications. Ex. 1010 ¶ 28.

Patent Owner argues that Petitioner has not established that Divsalar is a printed publication within the meaning of § 311(b). Prelim. Resp. 21–23. Patent Owner states that the acquisition record of the University of Texas library does not state that the paper was actually shelved or otherwise displayed and accessible to those of "ordinary skill." Prelim. Resp. 22–23.

According to the Divsalar cover page, it was presented at the Allerton Conference held on September 23–25, 1998. The acquisition record of the University of Texas indicating acquisition in April, 1999 lends credence to the actual presentation and publication of the paper at the September 1998 Allerton Conference and dissemination of the paper to the interested public. *See* Ex. 1064 (Declaration of Robin Fradenburgh) 4–6. Given Dr. Pfister's testimony that the Allerton Conference is the premier conference for information theorists, we find sufficient evidence to establish Divsalar as a printed publication within the meaning of the AIA statute.[8]

[8] We also note that Divsalar is listed as being of record among the "References Cited" in U.S. Patent No. 7,916,781 (the '781 patent) that is the

Accordingly, we are persuaded by Petitioner and the supporting evidence that Divsalar is prior art for the purposes of this Decision. Patent Owner may rebut Petitioner's contentions and supporting evidence with evidence that Divsalar was not presented and published at the Allerton Conference.

2. Divsalar (Ex. 1011)

Divsalar discloses "turbo-like" coding systems that are built from fixed convolutional codes interconnected with random interleavers, including both parallel concatenated convolutional codes and serial concatenated convolutional codes as special cases. Ex. 1011, 3. With fixed component codes and interconnection topology, Divsalar demonstrates that as the block length approaches infinity, the ensemble (over all possible interleaves) maximum likelihood error probability approaches zero, if the ratio of energy per bit to noise power spectral density exceeds some threshold. *Id*.

The general class of concatenated coding systems is depicted in Figure 1 of Divsalar as follows:

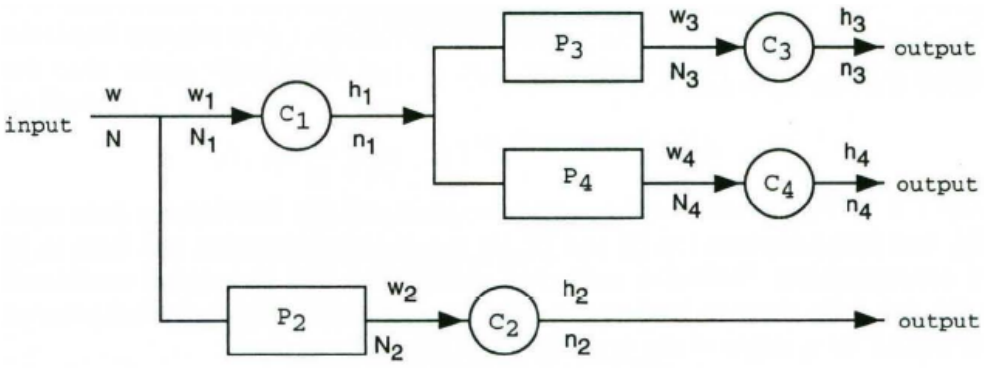


Figure 1. A "turbo-like" code with $s_I = \{1,2\}$, $s_O = \{2,3,4\}$, $\bar{s}_O = \{1\}$.

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subject of IPR2015-00059. It was cited by the Applicant in an IDS apparently filed with the application on June 30, 2008.

Figure 1 illustrates that encoders C2, C3, and C4 are preceded by interleavers (permuters) P2, P3, and P4, except C1, which is connected to an input rather than an interleaver. *Id*. at 4–5. The overall structure must have no loops and, therefore, is called a "turbo-like" code. *Id*.

Divsalar further discloses that "turbo-like" codes are repeat and accumulate (RA) codes. *Id*. at 7. The general scheme is depicted in Figure 3 as follows:

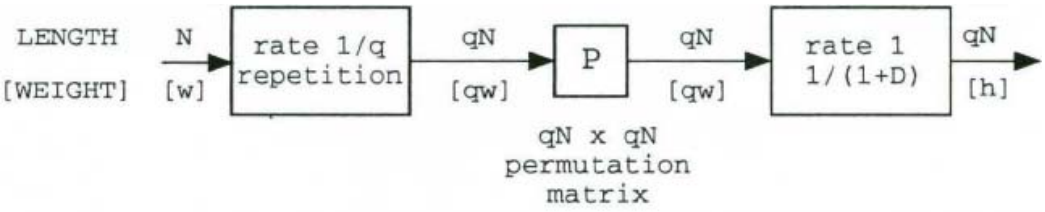


Figure 3. Encoder for a (qN, N) repeat and accumulate code. The numbers above the input-output lines indicate the length of the corresponding block, and those below the lines indicate the weight of the block.

Figure 3 illustrates that information block of length N is repeated q times, scrambled by interleaver of size qN, and then encoded by a rate 1 accumulator. *Id*. The accumulator can be viewed as a truncated rate-1 recursive convolutional encoder. *Id*. Figure 3 further illustrates a simple class of rate 1/q serially concatenated codes where the outer code is a q-fold repetition code and the inner code is a rate 1 convolutional code with a transfer function 1/(1+ D). *Id*. at 3, 7.

3. Luby (Ex. 1016)

Luby discloses a technique for creating loss resilient and error correcting codes having irregular graphing between the message data and the redundant data. Ex. 1016, 1:5–9. Luby teaches a technique for creating encoded messages, which when decoded, facilitate recover and/or correcting

of message data that has been lost or corrupted during transmission or storage. *Id.* at 2:56–60.

4. Analysis – Divsalar and Luby (independent claims 1 and 15)

Independent claim 1 recite encoding that required "repeating the data elements in different sub-blocks a different number of times." In addition irregular repeating, claim 1 further recites partitioning the data block into sub-blocks.

Although Divsalar teaches obtaining a block of data (Pet. 14), Petitioner admits that "*Divsalar* teaches a method that includes repeating each input bit the same number of []times" and not an irregular or different number of times. Pet. 16 (citing Ex. 1011 at 5; Ex. 1010 ¶ 118); *see also* Pet. 24 (stating that Divsalar "does not 'repeat said stream of bits *irregularly*,' as required by claim 15"). Petitioner relies on Luby to teach the irregular repeating recited in claims 1 and 15. Pet. 24–25. According to Petitioner, this is demonstrated by Luby's Figure 17, reproduced below.

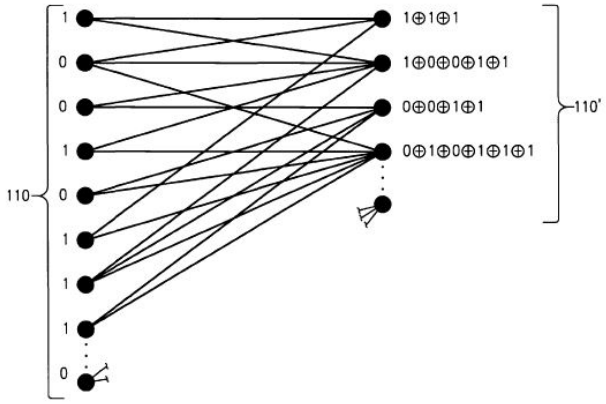


FIG. 17

Figure 17 depicts an irregular graphing of the edges between node layers in an error correcting cascading encoding structure. Ex. 1016, 5:42–46. According to Petitioner, the circles (nodes) in the left column represent

information bits to be encoded and the circles (nodes) in the right column represent parity bits computed from the information bits. Pet. 17 (citing Ex. 1010 ¶ 119). Each parity bit on the right is computed by summing together (modulo 2) all of the information bits connected to that parity bits by an edge. *Id*.

According to Petitioner, if d_i is the degree (or the number of adjacent edges) of the i-th information bit, then some information bits are connected to two parity bits (i.e., have a degree of two) and other information bits are connected to three parity bits (i.e., have a degree of three). *Id*. Petitioner argues that a person of ordinary skill in the art would understand that Luby's assignment of a first group to a degree of two and a second group of input bits to a degree of three is "partitioning said data block into a plurality of sub-blocks, each sub-block including a plurality of elements," as recited in claim 1. Pet. 17; *see also* Pet. 24. Petitioner contends that in Figure 17 of the Luby, "the input bits with a degree of two are one sub-block and the input bits with a degree of three are a second sub-block" of at least two input bits. *Id*.

With respect to the parity bits of Figure 17 of Luby, Petitioner argues that "the parity bits are computed by first repeating the i-th information bit d_i times and then interleaving the repeated bits based on the edge connection in the graph." Pet. 17–18 (citing Ex. 1010 ¶ 146). "Next, each parity bit with degree d is computed as the modulo-2 sum of d repeated bits." *Id*. Petitioner contends that Luby teaches "partitioning said data block into a plurality of sub-blocks, each sub-block including a plurality of data elements" because some bits have different degrees, either two or three. *Id*.

Based on the record before us, we agree with Patent Owner that Petitioner has not sufficiently shown that Luby discloses "partitioning said data block into a plurality of sub-blocks, each sub-block including a plurality of data elements," as recited in claim 1. Prelim. Resp. 26. In addition, the Petition fails to adequately show how the combination of Luby and Divsalar teach "said first encoding including repeating the data elements in different sub-blocks a different number of times" as recited in claim 1.

Petitioner has neither provided sufficient citation to evidence, nor adequately explained how one of ordinary skill in the art applies irregular graphing of the edges between node layers as disclosed in Luby to partition the block of data in Divsalar into "a plurality of sub-blocks, each sub-block including a plurality of data elements," as recited in claim 1. Indeed, the Petition claim chart does not adequately explain how parity bits are computed based on the edge graphing disclosed in Luby.[9]

With respect to claim 15, Petitioner has failed to provide sufficient evidence and testimony to support the combination of the Luby and Divsalar. Although Luby discusses that "sparse graph codes" can be improved by use of "'irregular graphing'" (Pet. 24–25 (citing Ex. 1016, Fig. 17; 11:23–49)), Petitioner has not shown that the irregular graphing of Luby

[9] Even assuming that Petitioner intended to cite Dr. Pfister's declaration testimony on information bits and parity bits in Figure 17 to explain the teaching of Luby (*see* Prelim. Resp. 29), we are not persuaded. The Pfister declaration states that Figure 17 of Luby describes the functional relationship between the information bits and the parity bits without any reference to Luby. Ex. 1010 ¶ 120. Petitioner failed to cite this testimony, which does not adequately show how Figure 17 of Luby teaches one of ordinary skill in the art the partitioning and irregular encoding of sub-blocks limitations recited in claim 1.

combined with the regular repeat codes of block of length N in Divsalar teaches the limitations of claim 15.

In sum, Petitioner has not provided sufficient evidence or argument to support the contention that "irregular graphing" of Luby teaches the irregular stream of bits as required in claim 15. In addition, we note that Petitioner provides only conclusory statements that Divsalar has inputs configured to receive a stream of bits as recited in claim 15. Pet. 24.

On the record before us, we are not persuaded by Petitioner's contentions that Luby in combination with Divsalar teaches irregular repeating as required in independent claims 1 and 15. Petitioner's arguments and evidence with respect to claim limitations for partitioning and assignment and irregular encoding in claim 1 and the limitation for an irregular stream of bits in claim 15 are presented confusingly and are not persuasive. *See* Pet. 15–18; 23–25. Petitioner relies on the same arguments presented for independent claims 1 and 15 to support the unpatentability of dependent claims 3, 4, 5, 6, 16, 21, and 22. Pet. 14–33.

For the reasons stated above, we conclude that on this record Petitioner has not demonstrated a reasonable likelihood that Petitioner would prevail in showing that claims 1, 3, 4, 5, 6, 15, 16, 21, and 22 are unpatentable as obvious over Divsalar and Luby.

5. *Analysis—Remaining Grounds based, in part, on Divsalar and Luby (claims 15, 16, 20, 21, and 22)*

Petitioner relies on the same arguments presented for claim 15 with respect to Divsalar and Luby (Pet. 23–25) in the grounds of unpatentability asserted for claims 15, 16, 21, and 22 based on obviousness over Divsalar, Luby and Hall (Pet. 35–36); and the grounds of unpatentability asserted for

claim 20 based on (i) Divsalar, Luby, and Ping and (ii) Divsalar, Luby, Ping and Hall (Pet. 37–43).

For the reasons discussed above, we conclude that on this record Petitioner has not demonstrated a reasonable likelihood that Petitioner would prevail in showing that claims 15, 16, 21, and 22 are unpatentable for obviousness over Divsalar, Luby, and Hall; claim 20 is unpatentable for obviousness over Divsalar, Luby, and Ping; and claim 20 is unpatentable for obviousness over Divsalar, Luby, Ping, and Hall.

III. CONCLUSION

For the foregoing reasons, we determine that the information presented in the Petition does not establish a reasonable likelihood that Petitioner would prevail in establishing the unpatentability of: (1) claims 1, 3, 4, 5, 6, 15, 16, 21, and 22 as obvious over Divsalar and Luby; (2) claims 15, 16, 21, and 22 as obvious over Divsalar, Luby, and Hall; (4) claim 20 as obvious over Divsalar, Luby, and Ping; and (5) claim 20 as obvious over Divsalar, Luby, Ping, and Hall.

IV. ORDER

Accordingly, it is

ORDERED that pursuant to 35 U.S.C. § 314, an *inter partes* review is hereby denied as to all grounds raised in the Petition for the reasons stated above and no trial is instituted.

Case IPR2015-00068
Patent 7,116,710 B1

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