ATTACHMENT 3

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Paper 18
Entered: April 27, 2015

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

HUGHES NETWORK SYSTEMS, LLC and
HUGHES COMMUNICATIONS, INC.,
Petitioner,

v.

CALIFORNIA INSTITUTE OF TECHNOLOGY,
Patent Owner.

Case IPR2015-00061
Patent 8,284,833 B2

Before KALYAN K. DESHPANDE, GLENN J. PERRY, and TREVOR M. JEFFERSON, *Administrative Patent Judges*.

DESHPANDE, *Administrative Patent Judge*.

DECISION
Denying Institution of *Inter Partes* Review
37 C.F.R. § 42.108

I. INTRODUCTION

Hughes Network Systems, LLC and Hughes Communications, Inc. (collectively, "Petitioner") filed a Corrected Petition requesting an *inter partes* review of claims 1, 2, 4, 6, 8, 9, 10, 11, and 13 of U.S. Patent No. 8,284,833 B2 (Ex. 1007, "the '833 patent"). Paper 4 ("Pet."). California Institute of Technology ("Patent Owner") timely filed a Preliminary Response. Paper 10 ("Prelim. Resp."). We have jurisdiction under 35 U.S.C. § 314(a), which provides that an *inter partes* review may not be instituted "unless . . . there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition." After considering the Petition, the Preliminary Response, and associated evidence, we conclude that Petitioner has not demonstrated a reasonable likelihood that it would prevail in showing unpatentability of all the challenged claims. Thus, we deny institution of an *inter partes* review of claims 1, 2, 4, 6, 8, 9, 10, 11, and 13 of the '833 patent.

A. Related Proceedings

Petitioner indicates that the '833 patent is the subject of the proceedings in *California Institute of Technology v. Hughes Communications, Inc. et al.*, No. 13-cv-07245 (Ca.C.D.). Pet. 1–2.

The '833 patent is also the subject of IPR2015-00081. Additionally, Petitioner indicates that the '833 patent is related to U.S. Patent No. 7,116,710, U.S. Patent No. 7,421,032, and U.S. Patent No. 7,916,781, which are the subject of IPR2015-00059, IPR2015-00060, IPR2015-00067, and IPR2015-00068.

B. The '833 Patent

The '833 patent describes the serial concatenation of interleaved convolutional codes forming turbo-like codes. Ex. 1007, Title. It explains some of the prior art with reference to its Figure 1, reproduced below.

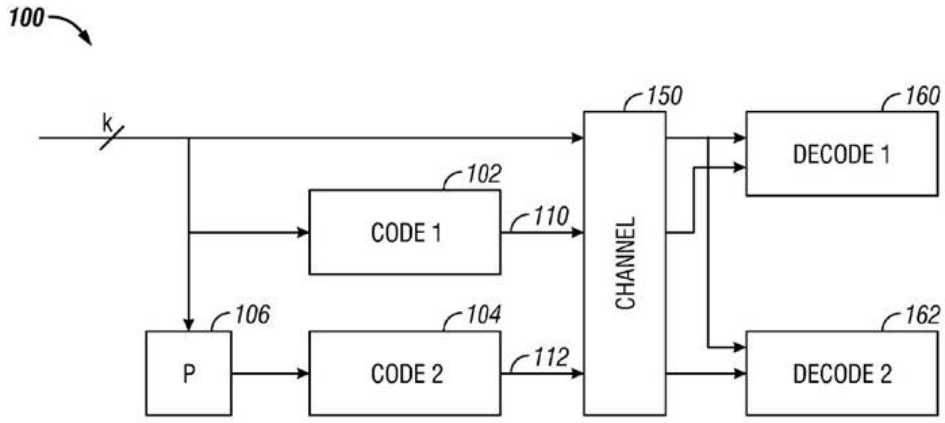

FIG. 1
(Prior Art)

Figure 1 is a schematic diagram of a prior "turbo code" system. *Id.* at 2:20–21. The '833 patent specification describes Figure 1 as follows:

> A block of k information bits is input directly to a first coder 102. A k bit interleaver 106 also receives the k bits and interleaves them prior to applying them to a second coder 104. The second coder produces an output that has more bits than its input, that is, it is a coder with rate that is less than 1. The coders 102,104 are typically recursive convolutional coders.
>
> Three different items are sent over the channel 150: the original k bits, first encoded bits 110, and second encoded bits 112. At the decoding end, two decoders are used: a first constituent decoder 160 and a second constituent decoder 162. Each receives both the original k bits, and one of the encoded portions 110, 112. Each decoder sends likelihood estimates of the decoded bits to the other decoders. The estimates are used to decode the uncoded information bits as corrupted by the noisy channel.

Id. at 1:46–60 (emphasis omitted).

A coder 200, according to a first embodiment of the invention, is described with respect to Figure 2, reproduced below.

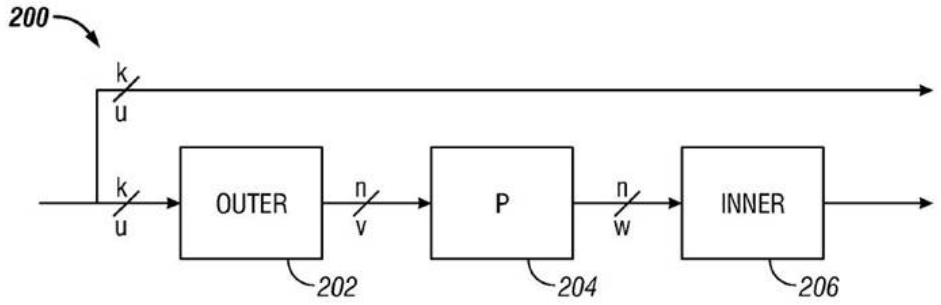

FIG. 2

Figure 2 of the '781 patent is a schematic diagram of coder 200.

> The coder 200 may include an outer coder 202, an interleaver 204, and inner coder 206… The outer coder 202 receives uncoded data. The data may be partitioned into blocks of fixed size, say k bits. The outer coder may be an (n,k) binary linear block coder, where n>k. The coder accepts as input a block u of k data bits and produces an output block v of n data bits and produces an output block v of n data bits. The mathematical relationship between u and v is $v=T_0u$, where T_0 is an n x k matrix, and the rate[1] of the coder is k/n.
>
> The rate of the coder may be irregular, that is, the value of T_0 is not constant, and may differ for sub-blocks of bits in the data block. In an embodiment, the outer coder 202 is a repeater that repeats the k bits in a block a number of times q to produce a block with n bits, where n=qk. Since the repeater has an irregular output, different bits in the block may be repeated a different number of times. For example, a fraction of the bits in the block may be repeated two times, a fraction of bits may be repeated three times, and the remainder of bits may be repeated four times. These fractions define a degree sequence, or degree profile, of the code.

[1] The "rate" of an encoder refers to the ratio of the number of input bits to the number of resulting encoded output bits related to those input bits.

> The inner coder 206 may be a linear rate-1 coder, which means that the n-bit output block x can be written as $x=T_I w$, where T_I is a nonsingular n x n matrix. The inner coder 210 can have a rate that is close to 1, e.g., within 50%, more preferably 10% and perhaps even more preferably within 1% of I.

Id. at 2:41–3:3 (emphasis omitted). Codes characterized by a regular repeat of message bits into a resulting codeword are referred to as "regular repeat," whereas codes characterized by irregular repeat of message bits into a resulting codeword are referred to as "irregular repeat." The second ("inner") encoder 206 performs an "accumulate" function. Thus, the two step encoding process illustrated in Figure 2, including a first encoding ("outer encoding") followed by a second encoding ("inner encoding"), results in either a "regular repeat accumulate" ("RRA") code or an "irregular repeat accumulate ("IRA") code, depending upon whether the repetition in the first encoding is regular or irregular.

Figure 4 of the '833 patent reproduced below.

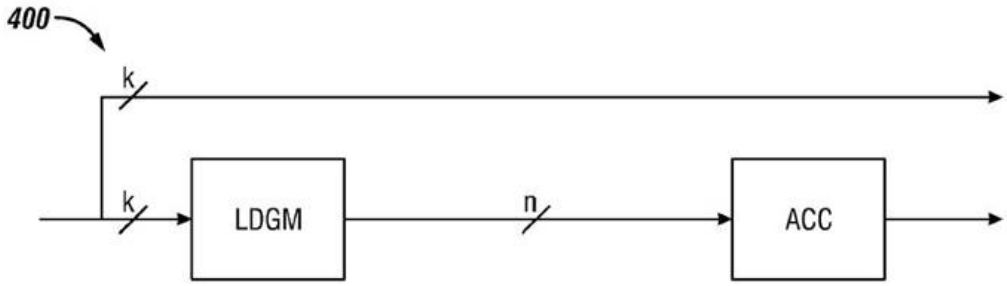

FIG. 4

Figure 4 shows an alternative embodiment in which the first encoding is carried out by a low density generator matrix. Low density generator matrix (LDGM)[2] codes are a special class of low density parity check codes that

[2] A "generator" matrix (typically referred to by "G") is used to create

allow for less encoding and decoding complexity. LDGM codes are systematic linear codes generated by a "sparse" generator matrix. No interleaver (as in the Figure 2 embodiment) is required in the Figure 4 embodiment because the LDGM provides scrambling otherwise provided by the interleaver in the Figure 2 embodiment. Ex. 1003, 3:55–64.

C. Illustrative Claim

Petitioner challenges claims 1, 2, 4, 6, 8, 9, 10, 11, and 13 of the '833 patent. Pet. 13–59. Independent claim 1 is illustrative of the claims at issue and is reproduced below:

> 1. An apparatus for performing encoding operations, the apparatus comprising:
>
> a first set of memory locations to store information bits;
>
> a second set of memory locations to store parity bits;
>
> a permutation module to read a bit from the first set of memory locations and combine the read bit to a bit in the second set of memory locations based on a corresponding index of the first set of memory locations and a corresponding index of the second set of memory locations; and
>
> an accumulator to perform accumulation operations on the bits stored in the second set of memory locations,
>
> wherein two or more memory locations of the first set of memory locations are read by the permutation module different times from one another.

D. The Alleged Grounds of Unpatentability

The information presented in the Petition sets forth proposed grounds of unpatentability of claims 1, 2, 4, 6, 8, 9, 10, 11, and 13 of the '833 patent as follows (*see* Pet. 13–59):

(generate) codewords. A parity check matrix (typically referred to by "H") is used to decode a received message.

Reference(s)	Basis	Claims Challenged
Ping[3] and Hennessy[4]	§ 103(a)	1, 2, 4, 6, 8, 9, 10, 11, and 13
Ping, Hennessy, and Luby '09[5]	§ 103(a)	1, 2, 4, 6, 8, 9, 10, 11, and 13
Divsalar[6] and Hennessy	§ 103(a)	1, 4, 6, 8, 11, and 13
Divsalar, Hennessy, and Luby '09	§ 103(a)	1, 2, 4, 6, 8, 9, 10, 11, and 13

II. ANALYSIS[7]

A. Claim Construction

The Board will interpret claims of an unexpired patent using the broadest reasonable construction in light of the specification of the patent in which they appear. *See* 37 C.F.R. § 42.100(b); Office Patent Trial Practice Guide, 77 Fed. Reg. 48,756, 48,766 (Aug. 14, 2012). Under the broadest reasonable construction standard, claim terms are given their ordinary and customary meaning, as would be understood by one of ordinary skill in the art in the context of the entire disclosure. *In re Translogic Tech. Inc.*,

[3] Li Ping et al., "Low Density Parity Check Codes with Semi-random Parity Check Matrix," ELECTRONIC LETTERS, THE INSTITUTION OF ELECTRICAL ENGINEERS, Jan. 7, 1999 (Ex. 1014, "Ping").
[4] Hennessy et al., COMPUTER ORGANIZATION & DESIGN, THE HARDWARE / SOFTWARE INTERFACE, Morgan Kaufmann Publishers, Nov. 8, 1994 (Ex. 1020, "Hennessy").
[5] U.S. Patent No. 6,081,909, issued June 27, 2000 (Ex. 1016, "Luby '09").
[6] Divsalar et al., "Coding Theorems for 'Turbo-Like' Codes," THIRTY-SIXTH ANNUAL ALLERTON CONFERENCE ON COMMUNICATION, CONTROL, AND COMPUTING, Sept. 23–25, 1998, at 201–209 (Ex. 1011, "Divsalar").
[7] Patent Owner argues that, as a threshold matter, the Petition should be dismissed because Petitioner fails to identify all real parties in interest. Prelim. Resp. 3. Because we have determined that Petitioner has not demonstrated a reasonable likelihood of prevailing, we need not address the real parties in interest issue in this Decision.

504 F.3d 1249, 1257 (Fed. Cir. 2007). We determine that only the following claim construction is necessary for the purposes of this decision.

1. *"wherein two or more memory locations of the first set of memory locations are read by the permutation module different times from one another"*

Petitioner contends that both Petitioner and Patent Owner agreed that "wherein two or more memory locations of the first set of memory locations are read by the permutation module different times from one another," as recited in claims 1 and 8, means "where two or more memory locations of the first set of memory locations are read by the permutation module a different number of times from one another." Pet. 11. Petitioner further presents an alternative construction, and proposes that this limitation means "where two or more memory locations of the first set of memory locations are read by the permutation module a different *number of* times from one another." Pet. 28 (citing Ex. 1010 ¶ 68). Petitioner argues that the distinction between the two proposed constructions is whether the limitation encompasses both regular and irregular encoding methods, or whether the limitation specifically requires irregular reading of memory locations. *See* Pet. 28; Ex. 1010 ¶ 68; Prelim. Resp. 20. Patent Owner argues that Petitioner is arguing for two inconsistent interpretations of this limitation, and, therefore, Petitioner's proposed interpretations should be rejected. Prelim. Resp. 18–21. Patent Owner, however, does not propose a meaning for this limitation.

We agree with Petitioner that the limitation "wherein two or more memory locations of the first set of memory locations are read by the permutation module different times from one another," under the broadest reasonable construction, does not require irregular readings of the memory

locations. We do not find anything in the '833 patent specification or the claims that limit the scope of this limitation to require irregular encoding. We are also not persuaded by Patent Owner that Petitioner has provided two inconsistent interpretations to this limitation. Rather, Petitioner has provided a broadest reasonable construction and, as an alternative construction, a narrower construction that is encompassed by the broader construction. Accordingly, we interpret the limitation "wherein two or more memory locations of the first set of memory locations are read by the permutation module different times from one another" to mean "wherein two or more memory locations of the first set of memory locations are read by the permutation module a different number of times from one another."

B. Claims 1, 2, 4, 6, 8, 9, 10, 11, and 13 — Obvious over Ping and Hennessey

Petitioner contends that claims 1, 2, 4, 6, 8, 9, 10, 11, and 13 are unpatentable under 35 U.S.C. § 103(a) as obvious over Ping and Hennessey. Pet. 13–27.

1. Ping (Ex. 1014)

Ping discloses a semi-random approach to low density parity check ("LDPC") code design that achieves essentially the same performance as an existing method, but with considerably reduced complexity. Ex. 1014, 6.[8] An LDPC code is defined by a randomly generated parity check matrix H. Ping utilizes a semi-random technique, where only H is generated randomly, and the remaining part is deterministic. *Id.* Codeword c is decomposed to c = $[p, d]^t$, where p and d contain the parity bits and information bits. *Id.*

[8] Ex. 1014 includes page numbers indicated by the publication itself, and different page numbers provided by Petitioner. Our references are to the page numbers provided by Petitioner.

Accordingly, H is decomposed in to $H = [H^p, H^d]$. H^p is constructed in a deterministic form. *Id.* H^d is partitioned in to *t* equal sub-blocks, where *t* is constrained by *n–k / t* and *kt / n–k* (where *n–k* are the number of rows). *Id.* In each sub-block, one element is randomly created 1 per column and *kt/(n–k)* 1s per row. *Id.* The resultant H^d has a column weight of t and a row weight of *kt/(n–k)*. *Id.*

This method is much simpler than a full Gaussian elimination. *Id.* Furthermore, a random H^d can be singular, causing additional programming complexity in realizing a specified rate. Even further, there is a memory saving because it requires little memory to store H^d in the encoder if H^d is sparse. *Id.*

2. Hennessy (Ex. 1020)

Hennessy discloses the performance of arithmetic operations in a computer. Ex. 1020, 9.[9] Hennessy discloses that operands of arithmetic instructions must be from registers. *Id.* at 11. A process can store small amounts of data in registers, but computer memory stores millions of data elements, and, therefore, data structures, like arrays, are kept in memory. *Id.* at 12. Because arithmetic operations occur in registers, there must be instructions that transfer data between meory and registers, i.e. data transfer instructions. *Id.* "To access a word in memory, the instruction must supply its *address*." *Id.*

[9] Ex. 1020 includes page numbers indicated by the publication itself, and different page numbers provided by Petitioner. Our references are to the page numbers provided by Petitioner.

3. Analysis

The evidence set forth by Petitioner indicates there is not a reasonable likelihood that Petitioner will prevail in showing that claims 1, 2, 4, 6, 8, 9, 10, 11, and 13 are unpatentable under 35 U.S.C. § 103(a) as obvious over Ping and Hennessey. Pet. 13–27. Independent claim 1 recites, *inter alia*, "a first set of memory locations," "a second set of memory locations," and "a permutation module to read a bit from the first set of memory locations and combine the read bit to a bit in the second set of memory locations." Independent claim 8 recites similar limitations. Petitioner argues that Ping discloses a "simulation study," which would be performed by a computer, and, therefore, Petitioner suggests that Ping inherently discloses the use of a computer. Pet. 13.

"[W]hen the reference is silent about the asserted inherent characteristic, such gap in the reference may be filled with recourse to extrinsic evidence. Such evidence must make clear that the missing descriptive matter is necessarily present in the thing described in the reference, and that it would be so recognized by persons of ordinary skill." *Continental Can Co. v. Monsanto Co.*, 948 F.2d 1264, 1268 (Fed. Cir. 1991). "Inherency, however, may not be established by probabilities or possibilities. The mere fact that a certain thing *may* result from a given set of circumstances is not sufficient." *Id.* at 1269. Petitioner has not established that Ping inherently discloses the use of a computer, much less "a first set of memory locations," "a second set of memory locations," and a "permutation module" that reads from the first memory and combines it with a bit in the second memory location. Petitioner relies on the testimony of Dr. Pfister, who conclusively asserts

> Ping states 'Fig. 1 contains the simulated performances of the proposed encoding method for various rates (1/3, 1/2, 2/3) using t=4.' A person of ordinary skill would recognize that Ping is describing the performance of [a] device, such as a computer, that implements Ping's proposed encoding and decoding."

Ex. 1010 ¶ 55 (quoting Ex. 1014, 39). Although Dr. Pfister's testimony suggests that a computer *may* be used for various encoding rates, Dr. Pfister fails to set forth persuasive evidence or rationale to demonstrate that encoding at various rates necessarily requires the use of a computer or memory. Accordingly, we are not persuaded from Dr. Pfister's testimony that Ping inherently discloses "a first set of memory locations," "a second set of memory locations," and a "permutation module" that reads from the first memory and combines it with a bit in the second memory location.

Petitioner further provides Hennessy to disclose these limitations, in the event that the "Board concludes a computer is not inherent in *Ping*." Pet. 13. Petitioner specifically argues that "it would be obvious to implement the *Ping* technique in a general purpose computer as taught in *Hennessy*." Pet. 13 (citing Ex. 1010 ¶¶ 75–76). Petitioner further argues that "[s]uch a combination would be obvious because computers are known to be effective at arithmetic computations, such as those in *Ping*." Pet. 13–14 (citing Ex. 1020, 95; Ex. 1010 ¶ 75). Patent Owner argues that Petitioner's proposed combination of Ping and Hennessy does not disclose "combining bits from two memory locations used to store information bits and parity bits." Prelim. Resp. 24. Patent Owner further argues that Petitioner "manufactures an arbitrary 'second memory location' purported to contain both data which is combined with information bits and (eventually) parity bits." Prelim. Resp. 24–25.

Although Hennessy discloses memory and characterizes memory as a large, single–dimensional array (Ex. 1020, 12), we are not persuaded by Petitioner that the combination of Ping and Hennessy discloses the claimed "a first set of memory locations," "a second set of memory locations," and a "permutation module" that reads from the first memory and combines it with a bit in the second memory location. Hennessey only discloses the use of memory to store memory and the use of a computer to perform arithmetic computations. Ex. 1020, 9, 12. As discussed above, we are not persuaded that Ping discloses a "permutation module" that reads from the first memory and combines it with a bit in the second memory location. Accordingly, we are not persuaded that the merely addition of a "computer" or "memory" capable of performing arithmetic, as disclosed by Hennessey, to Ping's method teaches or suggests "a first set of memory locations," "a second set of memory locations," and a "permutation module" that reads from the first memory and combines it with a bit in the second memory location.

Furthermore, Petitioner has not provided an articulated reasoning with a rational underpinning to support its conclusion of obviousness. Petitioner conclusively asserts that "[s]uch a combination would be obvious because computers are known to be effective at arithmetic computations." Pet. 13–14. Petitioner's conclusory statement does not sufficiently articulate why a person of ordinary skill in the art would have combined Ping and Hennessy in the manner proposed by Petitioner, and, therefore, is insufficient for a conclusion of obviousness.

4. Conclusion

Independent claim 8 recites similar limitations to claim 1, and dependent claims 2, 4, 6, 9, 10, 11, and 13 incorporate these limitations.

Accordingly, the evidence set forth by Petitioner indicates there is not a reasonable likelihood that Petitioner will prevail in showing that claims 1, 2, 4, 6, 8, 9, 10, 11, and 13 are unpatentable under 35 U.S.C. § 103(a) as obvious over Ping and Hennessey.

C. Claims 1, 2, 4, 6, 8, 9, 10, 11, and 13 — Obvious over Ping, Hennessey, and Luby '09

Petitioner contends that claims 1, 2, 4, 6, 8, 9, 10, 11, and 13 are unpatentable under 35 U.S.C. § 103(a) as obvious over Ping, Hennessey, and Luby '09. Pet. 27–33.

1. Luby '09 (Ex. 1016)

Luby '09 discloses a technique for creating loss resilient and error correcting codes having irregular graphing between the message data and the redundant data. Ex. 1016, 1:5–9. Luby '09 teaches a technique for creating encoded messages, which when decoded, facilitate recover and/or correcting of message data that has been lost or corrupted during transmission or storage. *Id.* at 2:56–60.

2. Analysis

The evidence set forth by Petitioner indicates there is not a reasonable likelihood that Petitioner will prevail in showing that claims 1, 2, 4, 6, 8, 9, 10, 11, and 13 are unpatentable under 35 U.S.C. § 103(a) as obvious over Ping, Hennessey, and Luby '09. Pet. 27–33. Claim 1 recites, *inter alia*, "wherein two or more memory locations of the first set of memory locations are read by the permutation module different times from one another." Independent claim 8 recites similar limitations. As discussed above, Petitioner proposes a broadest, reasonable interpretation for this limitation, and further proposes an alternate interpretation. *See* Section II.A.1. Petitioner argues that Ping discloses the broadest, reasonable interpretation

of this limitation, and further provides Luby '09 in the event that this limitation is determined to require irregular encoding. Pet. 28.

Luby '09, however, is not provided to discloses "a first set of memory locations," "a second set of memory locations," and a "permutation module" that reads from the first memory and combines it with a bit in the second memory location. Petitioner again relies on the combination of Ping and Hennessy to disclose these limitations. As discussed above, we are not persuaded that that the combination of Ping and Hennessy discloses these limitations. *See* Section II.B.3. For the same reasons stated above, we are not persuaded that the combination of Ping, Hennessy, and Luby '09 teaches or suggests "a first set of memory locations," "a second set of memory locations," and a "permutation module" that reads from the first memory and combines it with a bit in the second memory location. *Id.*

3. Conclusion

Independent claim 8 recites similar limitations to claim 1, and dependent claims 2, 4, 6, 9, 10, 11, and 13 incorporate these limitations. Accordingly, the evidence set forth by Petitioner indicates there is not a reasonable likelihood that Petitioner will prevail in showing that claims 1, 2, 4, 6, 8, 9, 10, 11, and 13 are unpatentable under 35 U.S.C. § 103(a) as obvious over Ping, Hennessey, and Luby '09.

D. Claims 1, 4, 6, 8, 11, and 13 — Obvious over Divsalar and Hennessey

Petitioner contends that claims 1, 4, 6, 8, 11, and 13 are unpatentable under 35 U.S.C. § 103(a) as obvious over Divsalar and Hennessey. Pet. 33–43.

1. Divsalar (Ex. 1011)

Divsalar discloses "turbo-like" coding systems that are built from

fixed convolutional codes interconnected with random interleavers, including both parallel concatenated convolutional codes and serial concatenated convolutional codes as special cases. Ex. 1011, 3.[10] With fixed component codes and interconnection topology, Divsalar demonstrates that as the block length approaches infinity, the ensemble (over all possible interleaves) maximum likelihood error probability approaches zero, if the ratio of energy per bit to noise power spectral density exceeds some threshold. *Id*.

The general class of concatenated coding systems is depicted in Figure 1 of Divsalar, as follows:

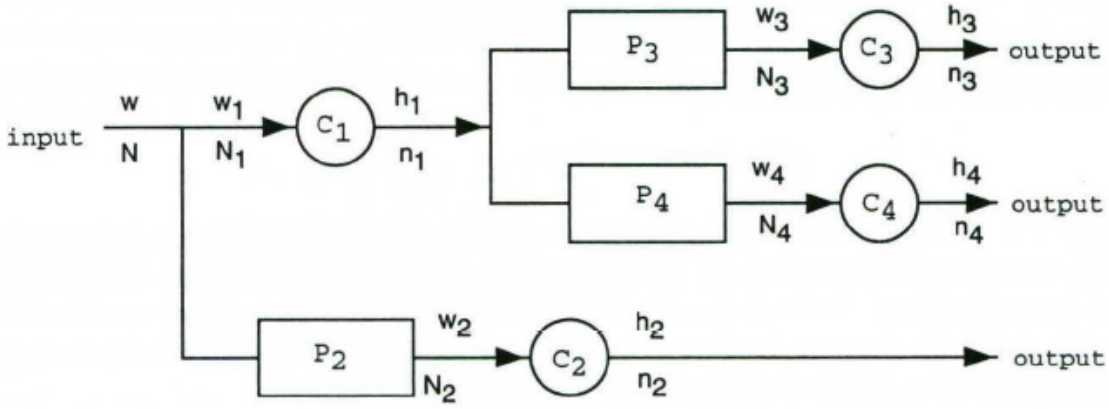

Figure 1. A "turbo-like" code with $s_I = \{1,2\}$, $s_O = \{2,3,4\}$, $\bar{s}_O = \{1\}$.

Figure 1 illustrates that encoders C_2, C_3, and C_4 are preceded by interleavers (permuters) P_2, P_3, and P_4, except C_1 which is connected to an input rather than an interleaver. *Id.* at 4. The overall structure must have no loops and, therefore, is called a "turbo-like" code. *Id.*

Divsalar further discloses that "turbo-like" codes are repeat and

[10] Ex. 1011 includes page numbers indicated by the publication itself, and different page numbers provided by Petitioner. Our references are to the page numbers provided by Petitioner.

accumulate (RA) codes. *Id.* at 7. The general scheme is depicted in Figure 3 as follows:

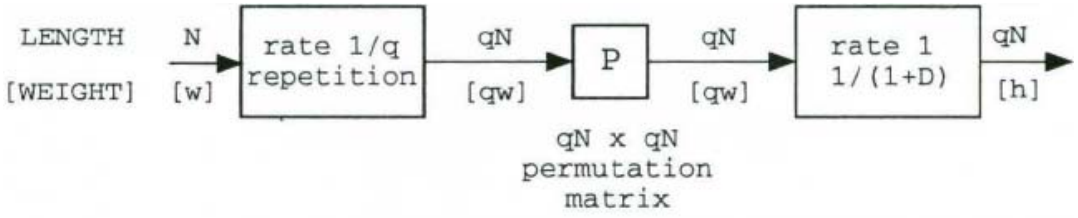

Figure 3. Encoder for a (qN, N) repeat and accumulate code. The numbers above the input-output lines indicate the length of the corresponding block, and those below the lines indicate the weight of the block.

Figure 3 illustrates that information block of length N is repeated q times, scrambled by interleaver of siz qN, and then encoded by a rate 1 accumulator. *Id.* The accumulator can be viewed as a truncated rate-1 recursive convolutional encoder. *Id.* Figure 3 further illustrates a simple class of rate 1/q serially concatenated codes where the outer code is a q-fold repetition code and the inner code is a rate 1 convolutional code with a transfer function 1/(1+ D). *Id.* at 3, 7.

2. Divsalar as Prior Art

Petitioner states that Divsalar was "published no later than April 30, 1999 at the University of Texas library." Pet. 2. In support, Petitioner proffers the declaration testimony of the Univ. of Texas librarian (Ex. 1064), including an acquisition record pasted into an email. According to Dr. Pfister, Petitioner's expert, The Allerton Conference is generally regarded as one of the main conferences in the field of information theory and communications. Ex. 1010 ¶ 29.

Patent Owner argues that Petitioner has not established that Divsalar is a publication within the meaning of 35 U.S.C. § 311(b). Patent Owner states that Divsalar is "undated" and that the library acquisition record does

not state that the paper was actually shelved or otherwise displayed and accessible to those of "ordinary skill." Prelim. Resp. 33–34.

According to the Divsalar cover page, it was presented at the Allerton Conference held Sept 23–25, 1998. Ex. 1011, 1. The acquisition record of the University of Texas indicating acquisition in April, 1999 lends credence to the actual presentation of the paper at the September 1998 Allerton Conference. Ex. 1064 ¶ 5. Given, Dr. Pfister's testimony that the Allerton Conference is the premier conference for information theorists, we find sufficient evidence to establish Divsalar as a publication within the meaning of 35 U.S.C. § 311(b).

Accordingly, we are persuaded by Petitioner and the supporting evidence that Divsalar is prior art for the purposes of this Decision.

3. Analysis

The evidence set forth by Petitioner indicates there is not a reasonable likelihood that Petitioner will prevail in showing that claims 1, 4, 6, 8, 11, and 13 are unpatentable under 35 U.S.C. § 103(a) as obvious over Divsalar and Hennessey. Pet. 33–43.

Claim 1 recites, *inter alia*, "a first set of memory locations," "a second set of memory locations," and "a permutation module to read a bit from the first set of memory locations and combine the read bit in to a bit in the second set of memory locations." Independent claim 8 recites similar limitations. Petitioner argues that Divsalar discloses a "computer program implemented using a computer" and an "[e]ncoder." Pet. 33–34. Petitioner specifically argues that a "person of ordinary skill in the art would recognize that a computer's memory would be used to store both the information bits and the parity bits in memory locations." Pet. 34 (citing Ex. 1010 ¶113; Ex.

1020, 98). Petitioner concludes that "by teaching the computational manipulation of bits, *Divsalar* inherently teaches the use of memory locations and indexes to store and access those bits during the computations. *Id.*

We are not persuaded that Divsalar inherently discloses "a first set of memory locations," "a second set of memory locations," and a "permutation module" that reads from the first memory and combines it with a bit in the second memory location. Petitioner relies on the testimony of Dr. Pfister, who conclusively asserts that Divsalar inherently teaches the use of memory locations and indexes to store and access bits because Divsalar discloses the computational manipulation of bits. Ex. 1010 ¶ 114. Dr. Pfister fails to set forth persuasive evidence or rationale to demonstrate that the manipulation of bits necessarily discloses the manipulation of bits in "a first set of memory locations" and "a second set of memory locations," and the manipulation of bits reads from the first memory and combines it with a bit in the second memory location. Accordingly, we are not persuaded that Divsalar inherently discloses these limitations of claim 1.

Petitioner further provides Hennessy to disclose the memory limitations, in the event that the we are not persuaded that Divsalar discloses such limitations. Pet. 35. Petitioner specifically argues that "[t]o the extent the Board concludes this is not inherent [in Divsalar], it would be obvious to use memory locations and indexes to that memory access bits during computations, as taught in *Hennessy* as that would be desirable to permit the computer to operate on the data stored there." *Id.* Patent Owner argues that the combination of Divsalar and Hennessy fails to teach or suggest these

limitations for similar reasons as to those discussed above with respect to the combination of Ping and Hennessy. Prelim. Resp. 39.

Although Hennessy discloses memory and characterizes memory as a large, single–dimensional array (Ex. 1020, 12), we are not persuaded by Petitioner that the combination of Divsalar and Hennessy discloses the claimed "a first set of memory locations," "a second set of memory locations," and a "permutation module" that reads from the first memory and combines it with a bit in the second memory location. Hennessey only discloses the use of memory to store memory and the use of a computer to perform arithmetic computations. Ex. 1020, 9, 12. As discussed above, we are not persuaded that Divsalar discloses a "permutation module" that reads from the first memory and combines it with a bit in the second memory location. *See* Section II.B.3. Accordingly, we are not persuaded that the merely addition of a "computer" or "memory" capable of performing arithmetic, as disclosed by Hennessey, to Divsalar's method teaches or suggests "a first set of memory locations," "a second set of memory locations," and a "permutation module" that reads from the first memory and combines it with a bit in the second memory location.

Furthermore, Petitioner has not provided an articulated reasoning with a rational underpinning to support its conclusion of obviousness. Petitioner conclusively asserts that a person with ordinary skill in the art would have combined Divsalar and Hennessy in order "to permit the computer to operate on the data stored there." Pet. 35. Petitioner's conclusory statement does not sufficiently articulate why a person of ordinary skill in the art would have combined Divsalar and Hennessy in the manner proposed by Petitioner, and, therefore, is insufficient for a conclusion of obviousness.

4. Conclusion

Independent claim 8 recites similar limitations to claim 1, and dependent claims 4, 6, 11, and 13 incorporate these limitations. Accordingly, the evidence set forth by Petitioner indicates there is not a reasonable likelihood that Petitioner will prevail in showing that claims 1, 4, 6, 8, 11, and 13 are unpatentable under 35 U.S.C. § 103(a) as obvious over Divsalar and Hennessey.

E. Claims 1, 2, 4, 6, 8, 9, 10, 11, and 13 — Obvious over Divsalar, Hennessey, and Luby '09

Petitioner contends that claims 1, 2, 4, 6, 8, 9, 10, 11, and 13 are unpatentable under 35 U.S.C. § 103(a) as obvious over Divsalar, Hennessey and Luby '09. Pet. 43–59.

1. Analysis

The evidence set forth by Petitioner indicates there is not a reasonable likelihood that Petitioner will prevail in showing that claims 1, 2, 4, 6, 8, 9, 10, 11, and 13 are unpatentable under 35 U.S.C. § 103(a) as obvious over Divsalar, Hennessey, and Luby '09. Pet. 43–59. Claim 1 recites, *inter alia*, "wherein two or more memory locations of the first set of memory locations are read by the permutation module different times from one another." Independent claim 8 recites similar limitations. As discussed above, Petitioner proposes a broadest, reasonable interpretation for this limitation, and further proposes an alternate interpretation. *See* Section II.A.1. Petitioner argues that Divsalar discloses the broadest, reasonable interpretation of this limitation, and further provides Luby '09 in the event that this limitation is determined to require irregular encoding. Pet. 43.

Luby '09, however, is not provided to discloses "a first set of memory locations," "a second set of memory locations," and a "permutation module"

that reads from the first memory and combines it with a bit in the second memory location. Petitioner again relies on the combination of Divsalar and Hennessy to disclose these limitations. As discussed above, we are not persuaded that that the combination of Divsalar and Hennessy discloses these limitations. *See* Section II.D.3. For the same reasons stated above, we are not persuaded that the combination of Divsalar, Hennessy, and Luby '09 teaches or suggests "a first set of memory locations," "a second set of memory locations," and a "permutation module" that reads from the first memory and combines it with a bit in the second memory location. *Id.*

2. Conclusion

Independent claim 8 recites similar limitations to claim 1, and dependent claims 2, 4, 6, 9, 10, 11, and 13 incorporate these limitations. Accordingly, the evidence set forth by Petitioner indicates there is not a reasonable likelihood that Petitioner will prevail in showing that claims 1, 2, 4, 6, 8, 9, 10, 11, and 13 are unpatentable under 35 U.S.C. § 103(a) as obvious over Divsalar, Hennessey, and Luby '09.

III. ORDER

Accordingly, it is

ORDERED that pursuant to 35 U.S.C. § 314, an *inter partes* review is hereby denied as to all grounds raised in the Petition for the reasons stated above.

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