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MURATA MANUFACTURING CO., LTD.

UNITED STATES DISTRICT COURT

CENTRAL DISTRICT OF CALIFORNIA

SACV09-01124 JVS (ANx)

MURATA MANUFACTURING CO., LTD.,

Plaintiff,

v.

SAMSUNG ELECTRO-MECHANICS CO., LTD., and SAMSUNG ELECTRO-MECHANICS AMERICA, INC.,

Defendants.

Case No.

COMPLAINT FOR PATENT INFRINGEMENT AND DEMAND FOR JURY TRIAL

Plaintiff Murata Manufacturing Co., Ltd. ("Plaintiff" or "Murata") brings this action against defendants Samsung Electro-Mechanics Co., Ltd. ("SEMCO") and Samsung Electro-Mechanics America, Inc. ("SEMCO America") (collectively, "Defendants") for patent infringement under the patent laws of the United States, Title 35, United States Code §§ 101 *et seq*. In support of its claims, Plaintiff states and alleges as follows:

THE PARTIES

1. Plaintiff Murata is a Japanese corporation with its principal place of business at 10-1 Higashikotari 1-chome, Nagaokakyo-shi, Kyoto, Japan 617-8555.

2. Among other things, Murata is in the business of researching and developing, designing, manufacturing and selling ceramic capacitors.

3. Defendant SEMCO is a Korean corporation with its principal place of business at 314 Maetan-3-dong, Yeongtong-gu Suwon City 443-743, South Korea.

4. SEMCO is in the business of manufacturing, marketing and selling ceramic capacitors. SEMCO markets and sells ceramic capacitors in the United States.

5. Defendant SEMCO America is a California corporation with its principal place of business at 3345 Michelson Drive, Suite 350, Irvine, California 92612. SEMCO America is a wholly owned subsidiary of SEMCO.

6. SEMCO America is in the business of importing, marketing and selling SEMCO ceramic capacitors in the United States.

JURISDICTION AND VENUE

7. This action arises under the Patent Laws of the United States, 35 U.S.C. § 101 *et seq*. This Court has subject matter jurisdiction under 28 U.S.C. §§ 1331 and 1338.

8. Upon information and belief, Defendants place their products

related to this action into the stream of commerce throughout the United States, including California, and those products have been offered for sale and/or sold within this judicial district.

9. This Court has personal jurisdiction over Defendant SEMCO because SEMCO conducts business in the State of California and has infringed and continues to infringe Murata patents as alleged below.

10. As a California corporation, Defendant SEMCO America is subject to personal jurisdiction in this Court. This Court also has personal jurisdiction over SEMCO America because SEMCO America conducts business in the State of California, and has infringed and continues to infringe Murata patents as alleged below.

11. Venue is proper in this judicial district under 28 U.S.C. §§ 1391 and 1400(b) in that, among other things, acts of infringement complained of herein have been committed in the State of California, and Defendant SEMCO America is incorporated in California.

FACTUAL ALLEGATIONS

12. On July 24, 2001, United States Patent No. 6,266,229 B1 ("the '229 patent"), titled *Multilayer Capacitor*, was duly and legally issued to Yasuyuki Naito, Masaaki Taniguchi, Yoichi Kuroda, Takanori Kondo, Michihiro Murata and Yoshitaka Tanino. Murata is the assignee and owner of all right, title and interest in and to the '229 patent. The '229 patent is valid and in full force and effect. A copy of the '229 patent is attached hereto as Exhibit A.

13. On April 23, 2002, United States Patent No. 6,377,439 B1 ("the '439 patent"), titled *Electronic Multilayer Ceramic Component*, was duly and legally issued to Hiroshi Sekidou, Yoshikazu Takagi, and Yasunobu Yoneda. Murata is the assignee and owner of all right, title and interest in and to the '439 patent. The '439 patent is valid and in full force and effect. A copy of the '439 patent is attached hereto as Exhibit B.

14. On June 5, 2001, United States Patent No. 6,243,254 B1 ("the '254 patent"), titled *Dielectric Ceramic Composition and Laminated Ceramic Capacitor Using the Same*, was duly and legally issued to Nobuyuki Wada, Masamitsu Shibata, Takashi Hiramatsu, and Yukio Hamaji. Murata is the assignee and owner of all right, title and interest in and to the '254 patent. The '254 patent is valid and in full force and effect. A copy of the '254 patent is attached hereto as Exhibit C.

15. On January 11, 2000, United States Patent No. 6,014,309 ("the '309 patent"), titled *Laminated Ceramic Electronic Parts*, was duly and legally issued to Yasushi Ueno, Yoshikazu Takagi, Kazuaki Kawabata, and Nagato Omori. Murata is the assignee and owner of all right, title and interest in and to the '309 patent. The '309 patent is valid and in full force and effect. A copy of the '309 patent is attached hereto as Exhibit D.

16. SEMCO offers an extensive line of ceramic capacitor products of various specifications.

17. Products made, sold or offered for sale in the United States by or on behalf of Defendants embody the inventions disclosed and claimed in one or more of the patents-in-suit.

18. Specifically, Defendants manufacture, sell, and offer to sell ceramic capacitor products that infringe one or more claims of the patents-in-suit.

COUNT I

(Infringement of the '229 Patent)

19. Plaintiff realleges the above paragraphs as if fully set forth herein.

20. Defendants have infringed the '229 patent under one or more provisions of 35 U.S.C. § 271 by making, using, importing, offering for sale, or selling without license or authority in this district and elsewhere in the United States, infringing ceramic capacitor products.

21. Defendants have knowledge of the '229 patent and have willfully, deliberately and intentionally infringed one or more claims of this patent.

22. Unless Defendants and their agents, servants, subsidiaries, affiliates, employees, attorneys, representatives, and all others acting on their behalf are enjoined from infringing the patents-in-suit, Defendants will continue to infringe this patent and Murata will be greatly and irreparably harmed.

COUNT II

(Infringement of the '439 Patent)

23. Plaintiff realleges the above paragraphs as if fully set forth herein.

24. Defendants have infringed the '439 patent under one or more provisions of 35 U.S.C. § 271 by making, using, importing, offering for sale, or selling without license or authority in this district and elsewhere in the United States, infringing ceramic capacitor products.

25. Upon information and belief, Defendants have knowledge of the '439 patent and have willfully, deliberately and intentionally infringed one or more claims of this patent.

26. Unless Defendants and their agents, servants, subsidiaries, affiliates, employees, attorneys, representatives, and all others acting on their behalf are enjoined from infringing the patents-in-suit, Defendants will continue to infringe this patent and Murata will be greatly and irreparably harmed.

COUNT III

(Infringement of the '254 Patent)

27. Plaintiff realleges the above paragraphs as if fully set forth herein.

28. Defendants have infringed the '254 patent under one or more provisions of 35 U.S.C. § 271 by making, using, importing, offering for sale, or selling without license or authority in this district and elsewhere in the United

States, infringing ceramic capacitor products.

29. Defendants have knowledge of the '254 patent and have willfully, deliberately and intentionally infringed one or more claims of this patent.

30. Unless Defendants and their agents, servants, subsidiaries, affiliates, employees, attorneys, representatives, and all others acting on their behalf are enjoined from infringing the patents-in-suit, Defendants will continue to infringe this patent and Murata will be greatly and irreparably harmed.

COUNT IV

(Infringement of the '309 Patent)

31. Plaintiff realleges the above paragraphs as if fully set forth herein.

32. Defendants have infringed the '309 patent under one or more provisions of 35 U.S.C. § 271 by making, using, importing, offering for sale, or selling without license or authority in this district and elsewhere in the United States, infringing ceramic capacitor products.

33. Defendants have knowledge of the '309 patent and have willfully, deliberately and intentionally infringed one or more claims of this patent.

34. Unless Defendants and their agents, servants, subsidiaries, affiliates, employees, attorneys, representatives, and all others acting on their behalf are enjoined from infringing the patents-in-suit, Defendants will continue to infringe this patent and Murata will be greatly and irreparably harmed.

PRAYER FOR RELIEF

WHEREFORE, Plaintiff Murata respectfully requests the following relief:

A. A judgment that Defendants SEMCO and SEMCO America have infringed one or more claims of the patents-in-suit;

B. A judgment that Defendants SEMCO and SEMCO America's infringement of the patents-in-suit has been, and continues to be, willful and deliberate;

C. Permanent injunctive relief prohibiting Defendants SEMCO and SEMCO America and their respective subsidiaries, affiliates, officers, agents, servants, employees, licensees, and all other persons acting or attempting to act in active concert or participation with them or acting on their behalf, from infringement of the patents-in-suit;

D. A judgment that Defendants SEMCO and SEMCO America be ordered to account for and pay all damages caused by reason of their infringement pursuant to 35 U.S.C. § 284, including enhanced damages under 35 U.S.C. § 284 in an amount to be determined by the Court;

E. A judgment that Defendants SEMCO and SEMCO America be ordered to pay Murata's costs, expenses and reasonable attorneys' fees pursuant to 35 U.S.C. §§ 284 and 285;

F. An award of pre-judgment and post-judgment interest on the damages caused to Plaintiff by Defendants SEMCO and SEMCO America's infringement; and

G. Such other and further relief as the Court may deem just and proper under the circumstances.

JURY DEMAND

Plaintiff respectfully requests a jury trial on all issues so triable.

Dated: October 1, 2009

WILLIAM H. WRIGHT
Orrick, Herrington & Sutcliffe LLP

WILLIAM H. WRIGHT
Attorney for Plaintiff
MURATA MANUFACTURING CO., LTD.

EXHIBIT A



THE UNITED STATES OF AMERICA

TO ALL TO WHOM THESE PRESENTS SHALL COME:

UNITED STATES DEPARTMENT OF COMMERCE

United States Patent and Trademark Office

August 05, 2009

THIS IS TO CERTIFY THAT ANNEXED HERETO IS A TRUE COPY FROM THE RECORDS OF THIS OFFICE OF:

U.S. PATENT: *6,266,229*

ISSUE DATE: *July 24, 2001*

By Authority of the

Under Secretary of Commerce for Intellectual Property

and Director of the United States Patent and Trademark Office

M. K. CARTER

Certifying Officer

EXHIBIT A

08

US006266229B1

(12) **United States Patent**
Naito et al.

(10) **Patent No.: US 6,266,229 B1**
(45) **Date of Patent: Jul. 24, 2001**

(54) **MULTILAYER CAPACITOR**

(75) Inventors: **Yasuyuki Naito**, Takefu; **Masaaki Taniguchi**, Fukui; **Yoichi Kuroda**, Fukui; **Takanori Kondo**, Sabae; **Michihiro Murata**; **Yoshitaka Tanino**, both of Kyoto, all of (JP)

(73) Assignee: **Murata Manufacturing Co., LTD**, Kyoto (JP)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **09/501,084**

(22) Filed: **Feb. 9, 2000**

Related U.S. Application Data

(63) Continuation-in-part of application No. 09/042,379, filed on Mar. 13, 1998, now Pat. No. 6,072,687.

(30) **Foreign Application Priority Data**

Nov. 10, 1997 (JP) 9-306717
Dec. 27, 1999 (JP) 11-370803

(51) **Int. Cl.**[7] **H01G 4/228**; H01G 4/005

(52) **U.S. Cl.** **361/306.3**; 361/306.1; 361/308.1; 361/303

(58) **Field of Search** 361/303, 306.1, 361/306.3, 308.1, 309, 310, 311, 312, 313, 320, 321.1, 321.2, 321.3, 321.4, 321.5, 329, 330

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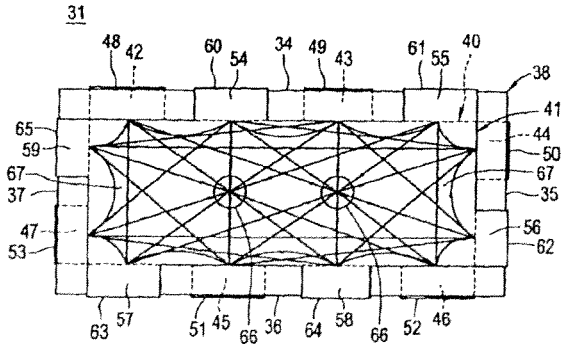
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Primary Examiner—Anthony Dinkins
(74) *Attorney, Agent, or Firm*—Keating & Bennett, LLP

(57) **ABSTRACT**

A multi-layer capacitor device includes a capacitor body including first electrode plates and a plurality of second electrode plates. The first and second electrode plates are interleaved with each other in opposed and spaced apart relation. A dielectric material is located between each opposed set of the first and second electrode plates. The first and second electrode plates each include a main electrode portion and a plurality of spaced apart lead structures extending therefrom. Respective lead structures of the first electrodes plates are located adjacent respective lead structures of the second electrode plates in an interdigitated arrangement. A plurality of electrical terminals are located on each of the opposed side surfaces of the capacitor body. A plurality of first polarity electrical terminals and a plurality of second polarity electrical terminals, respectively, located on the capacitor body. Each of the first polarity terminals is disposed opposite to another of the first polarity terminals across the capacitor body and each of the second polarity terminals is disposed opposite to another of the second polarity terminals across the capacitor body. Each of the lead structures of the first and second electrode plates have a length L and a width W and a ratio L/W is equal to about 3 or less, and preferably between 0.4 and 1.3.

60 Claims, 10 Drawing Sheets



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FIG. 1

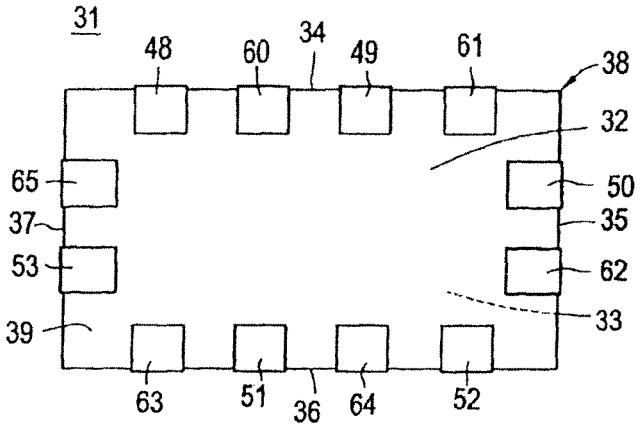
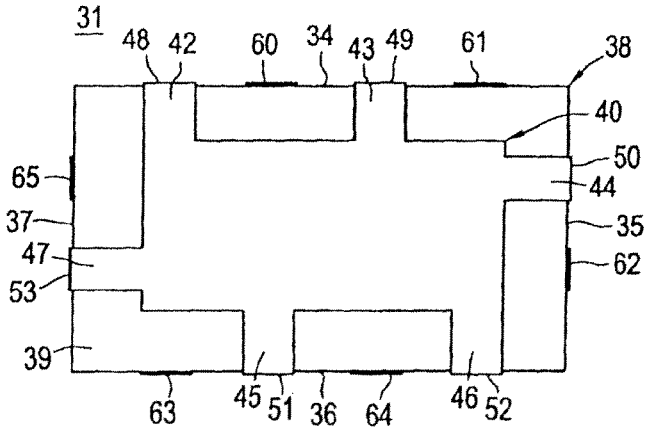


FIG. 2



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FIG. 3

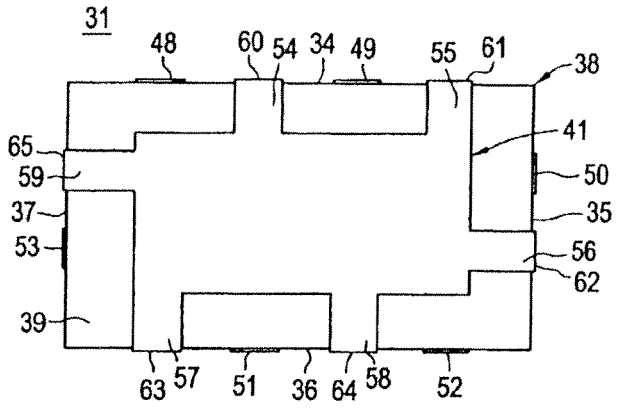
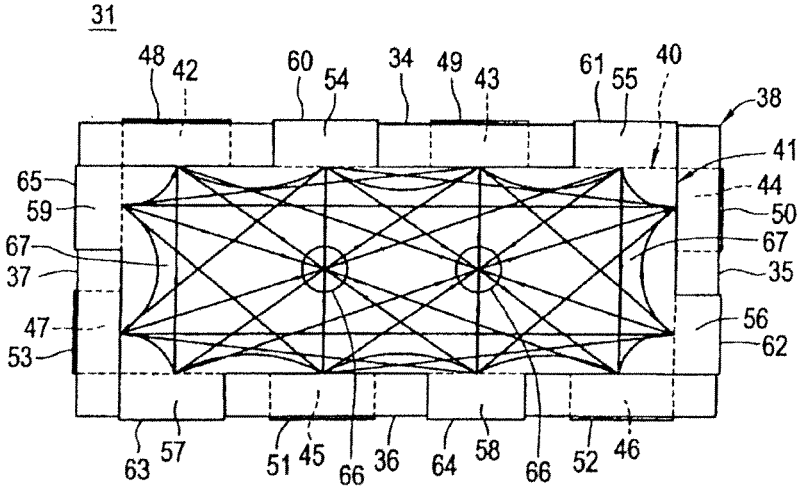


FIG. 4



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FIG. 5

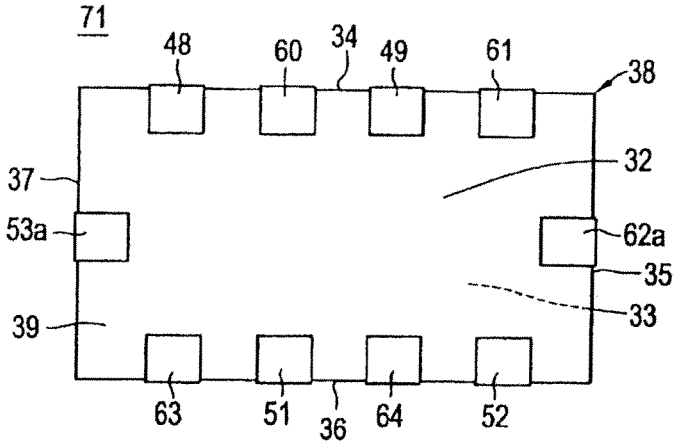
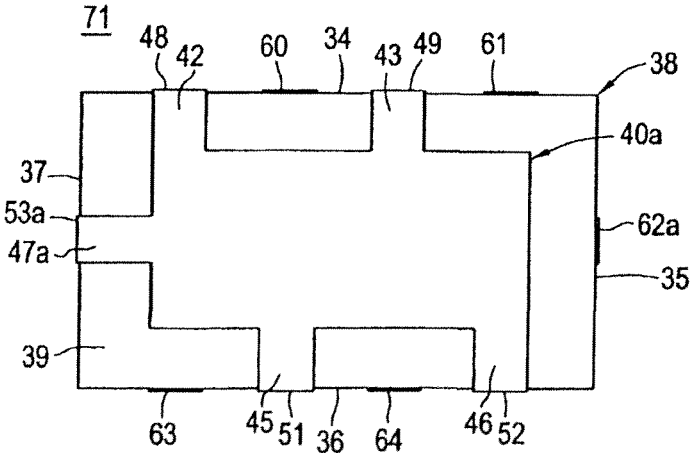


FIG. 6



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FIG. 7

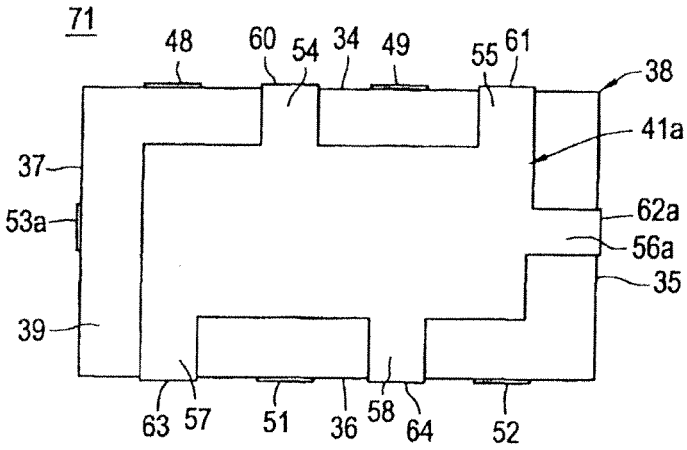
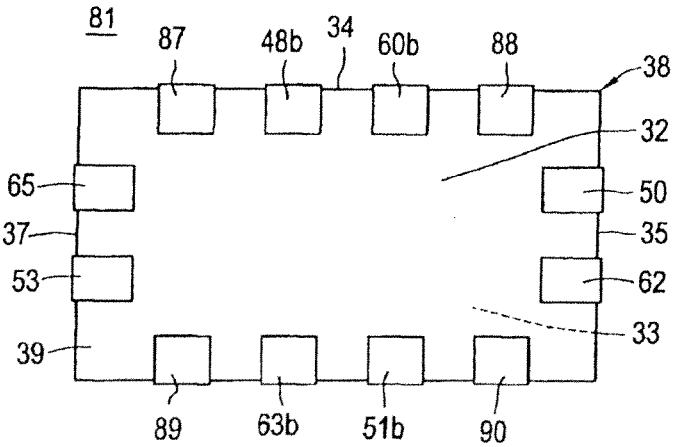


FIG. 8



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FIG. 9

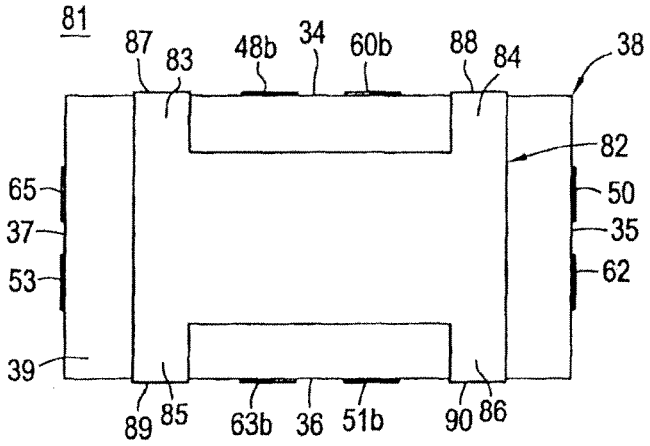
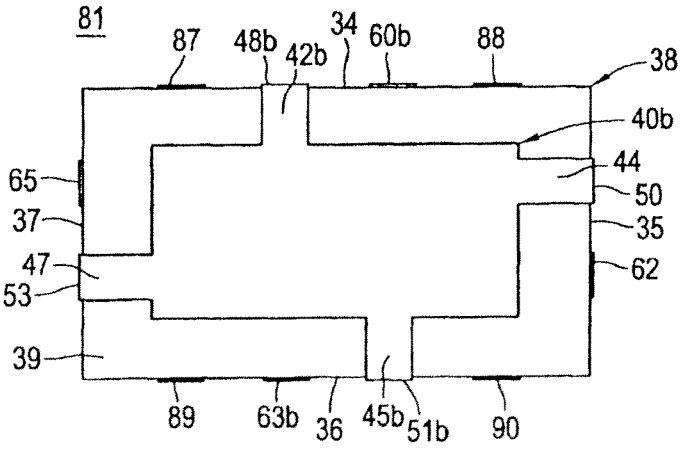


FIG. 10



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FIG. 11

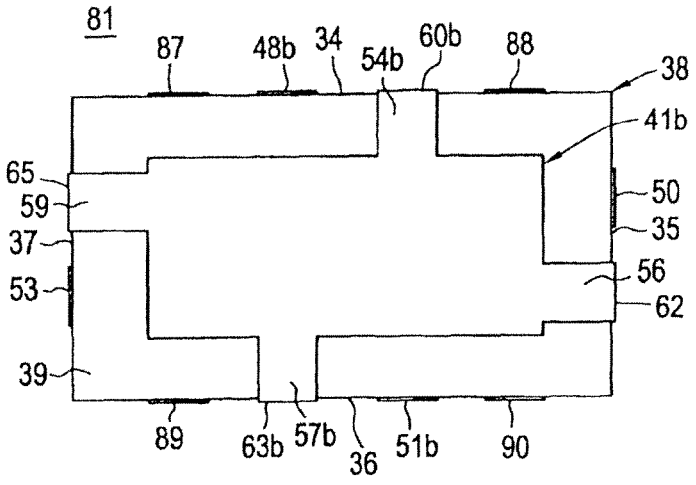
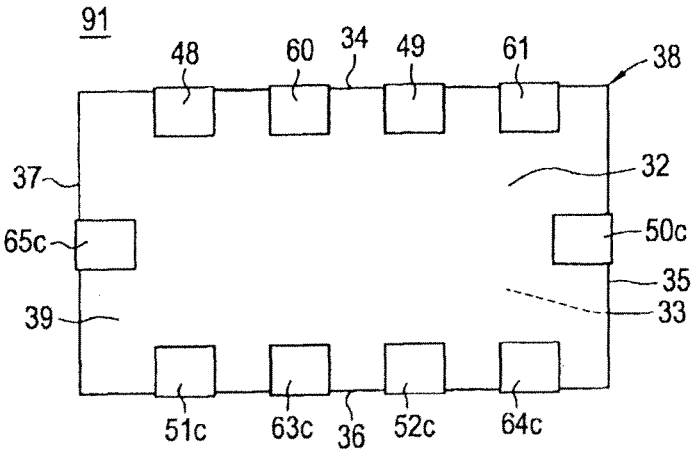


FIG. 12



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FIG. 13

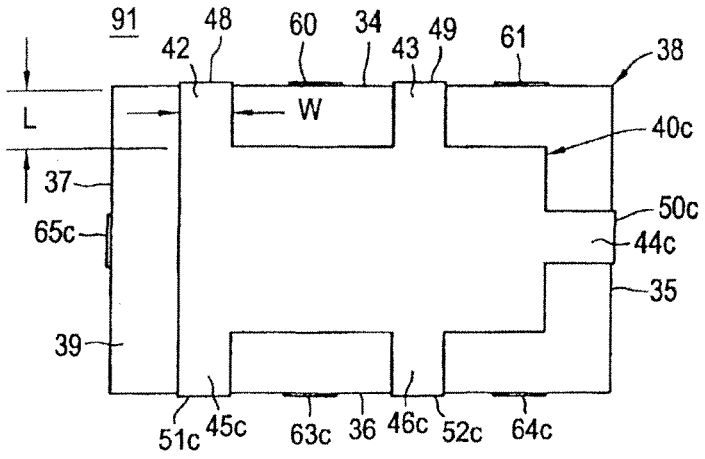
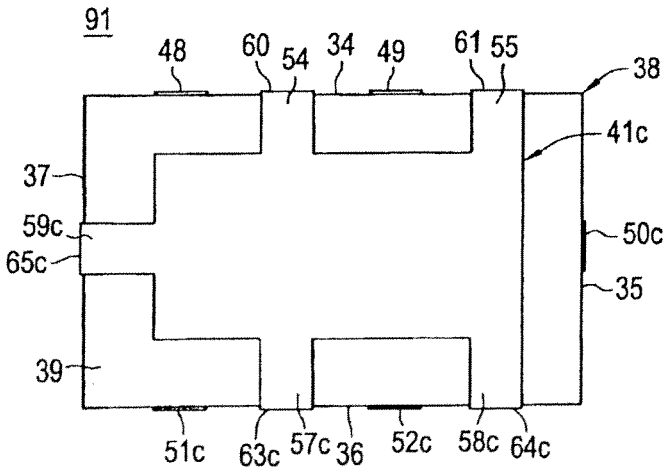


FIG. 14



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FIG. 15
PRIOR ART

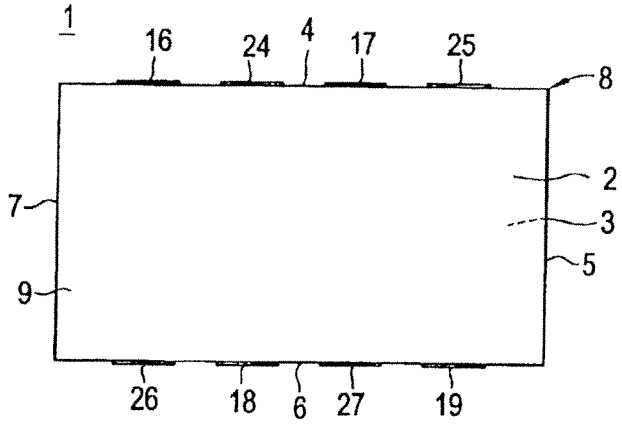
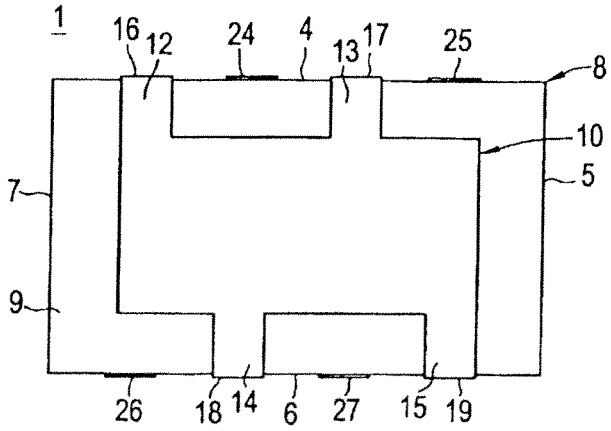


FIG. 16
PRIOR ART



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FIG. 17
PRIOR ART

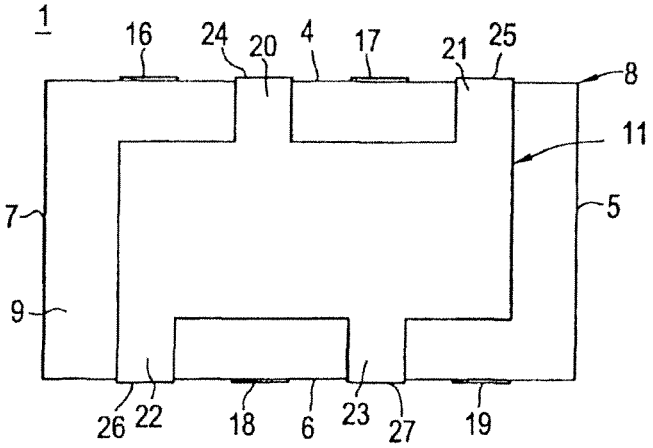
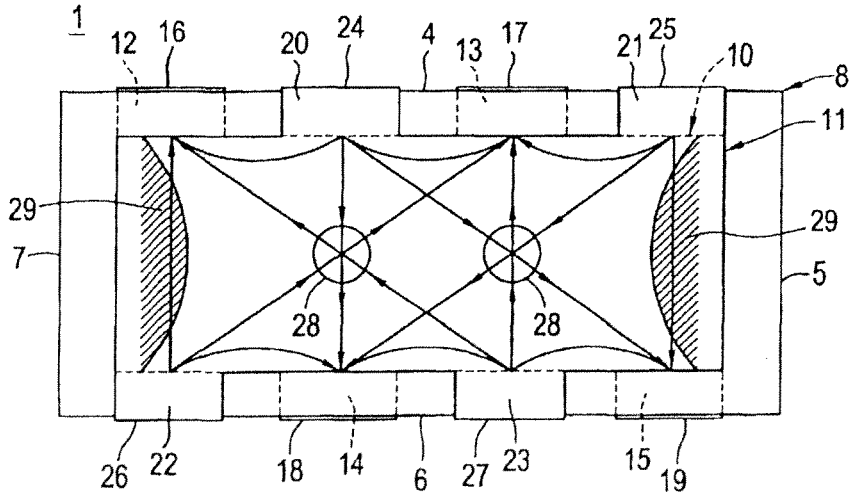


FIG. 18
PRIOR ART



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FIG. 19

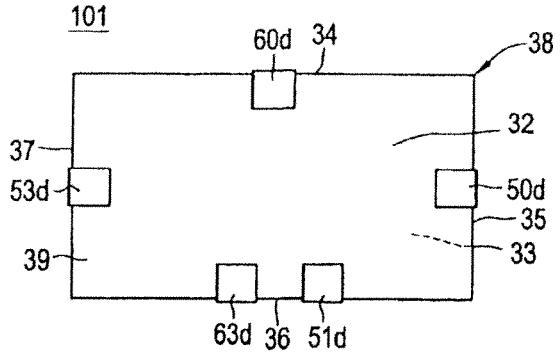


FIG. 20

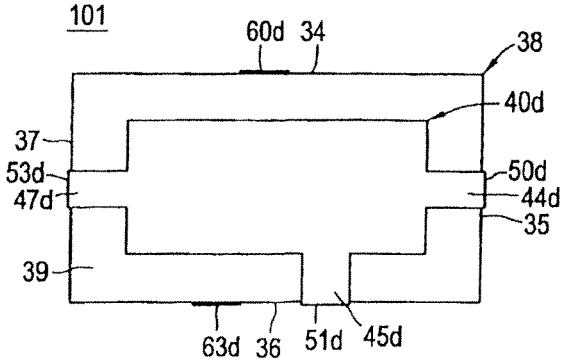
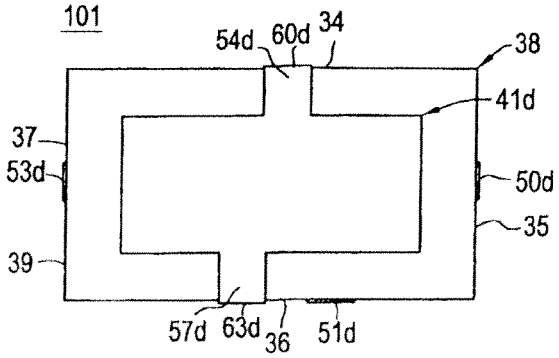


FIG. 21



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MULTILAYER CAPACITOR

This application is a Continuation-in-Part of U.S. patent application Ser. No. 09/042,379 filed on Mar. 13, 1998, now U.S. Pat. No. 6,072,687.

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to a multi-layer capacitor and, more particularly, to a multi-layer capacitor which can be advantageously used in high frequency circuits.

2. Description of the Related Art

Conventional multi-layer capacitors include those described in Japanese Unexamined Patent Publication No. H2-256216 in which a multi-layer capacitor **1**, as shown in FIGS. **15** through **17** of the present application, is disclosed. FIG. **15** is a plan view of the external appearance of the multi-layer capacitor **1**. FIG. **16** is a plan view of a first section of the multi-layer capacitor **1** showing a first electrode **10** located on one surface of one internal dielectric layer **9** of the capacitor **1**. FIG. **17** is a plan view of a second section of the multi-layer capacitor **1** showing a second electrode **11** located on one surface of a differential internal dielectric layer **9** of the capacitor **1**.

Referring to FIGS. **15–17**, the multi-layer capacitor **1** includes a capacitor main body **8** in the form of a rectangular parallelpiped having two principal surfaces **2** and **3** in a face-to-face relationship with each other and four side surfaces **4**, **5**, **6** and **7** connecting the principal surfaces **2** and **3**. The capacitor main body **8** includes a plurality of dielectric layers **9** (FIGS. **16–17**) made of, for example, a ceramic dielectric material. Each of the dielectric layers is generally planar in shape and lies generally parallel to the principal surfaces **2** and **3**. At least a pair of first and second internal electrodes **10** and **11** are provided on respective surfaces of the dielectric layers **9** in a face-to-face relationship with each other, with a dielectric layer **9** interposed therebetween to form a capacitor unit.

The first internal electrode **10** is formed with four lead electrodes **12**, **13**, **14** and **15** which extend to two opposing side surfaces **4** and **6**, as shown.

Each lead electrode **12**, **13**, **14** and **15** is coupled to a respective external terminal electrode **16**, **17**, **18** and **19** provided on the side surfaces **4** and **6** of the capacitor main body **8**. Specifically, the lead electrodes **12** and **13** are connected to the external terminal electrodes **16** and **17**, respectively, which are located on the side surface **4**, and the lead electrodes **14** and **15** are connected to the external terminal electrodes **18** and **19**, respectively, which are located on the side surface **6**.

Referring to FIG. **17**, the second internal electrode **11** is also formed with four lead electrodes **20**, **21**, **22** and **23** which extend to the side surfaces **4** and **6**, respectively. More specifically, the lead electrodes **20** and **21** extend to positions on the side surface **4** which are different from the positions to which the lead electrodes **12** and **13** extend, and the lead electrodes **22** and **23** extend to positions on the side surface **6** of the main body **8** which are different from the positions to which the lead electrodes **14** and **15** extend.

The lead electrodes **20** through **23** are electrically coupled to external terminal electrodes **24**, **25**, **26** and **27**, respectively. External terminal electrodes **24** and **25** are located on the side surface **4** at positions which are different from those of the external terminal electrodes **16** and **17**. External terminal electrodes **26** and **27** are located on the side surface **6** at positions which are different from the positions of the external terminal electrodes **18** and **19**.

Thus, the plurality of first external terminal electrodes **16** through **19** and the plurality of second external terminal electrodes **24** through **27** are arranged on the two side surfaces **4** and **6** such that they alternate adjacently to each other.

FIG. **18** illustrates current flowing through the multi-layer capacitor **1** as viewed in plan view corresponding to FIG. **17**. In FIG. **18**, first internal electrode **10** and second internal electrode **11**, shown with broken and solid lines, respectively, are shown in an overlapping relationship.

In FIG. **18**, the arrows indicate typical current paths and directions. In the state illustrated, current flows from each of the external terminal electrodes **24** through **27** to each of the external terminal electrodes **16** through **19**. Because an alternating current is used, the direction of current flow will reverse periodically.

When the currents flow, magnetic flux is induced. The direction of the flux is determined by the direction of the currents to produce self-inductance components. Since the currents flow in various directions at central regions **28** (indicated by circles) of the internal electrodes **10** and **11**, the induced magnetic flux generated by the various currents is canceled and substantially no net magnetic flux is produced in those regions.

The current in the vicinity of each of the external terminal electrodes **16** through **19** and **24** through **27** tends to flow toward each of the external terminal electrodes **16** through **19** and away from each of the external terminal electrodes **24** through **27**. There are currents that flow to the left and right as viewed in FIG. **18** to spread at an angle of about 180 degrees. As a result, a major part of magnetic flux is canceled and there is no significant generation of net magnetic flux in these areas.

Therefore, in the multi-layer capacitor **1** shown in FIGS. **15** through **17**, the generation of self-inductance is suppressed in the areas points described above to reduce equivalent series induction (hereinafter "ESL").

However, currents flow substantially in the same direction in the vicinity of each of the side surfaces **5** and **7** on which no external terminal electrodes are provided, i.e., at each of the left and right edge portions indicated by hatching in FIG. **18**. This results in substantially no cancellation of magnetic flux in these areas and significant net self-inductance is created. Therefore, the measures taken to reduce ESL in the multi-layer capacitor **1** shown in FIGS. **15** through **17** are less than desirable.

SUMMARY OF THE INVENTION

To overcome the problems described above, preferred embodiments of the present invention provide a multi-layer capacitor which more effectively reduces ESL.

In accordance with a preferred embodiment the present invention, a multi-layer capacitor includes a capacitor body including top and bottom surfaces and opposed side surfaces which have continuously flat surfaces and are disposed between the top and bottom surfaces and opposed end surfaces disposed between the top and bottom surfaces and the opposed side surfaces, the capacitor body including a plurality of first electrode plates and a plurality of second electrode plates, the first and second electrode plates being interleaved with each other in opposed and spaced apart relation, a dielectric material located between each opposed set of the first and second electrode plates, the first and

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second electrode plates each including a main electrode portion and a plurality of spaced apart lead structures extending therefrom, respective lead structures of the first electrodes plates being located adjacent respective lead structures of the second electrode plates in an interdigitated arrangement, and a plurality of electrical terminals located on each of the opposed side surfaces of the capacitor body, corresponding lead structures of the first electrode plates and corresponding lead structures of the second electrode plates being electrically connected together by respective ones of the electrical terminals to define a plurality of first polarity electrical terminals and a plurality of second polarity electrical terminals, respectively, located on the capacitor body; wherein each of the first polarity terminals is disposed opposite to another of the first polarity terminals across the capacitor body and each of the second polarity terminals is disposed opposite to another of the second polarity terminals across the capacitor body and at least one of the lead structures of the first and second electrode plates have a length L and a width W and a ratio L/W is equal to about 3 or less.

Another preferred embodiment of the present invention provides a multi-layer capacitor including a capacitor body including a pair of opposed side surfaces having continuously smooth surfaces and a pair of opposed end surfaces disposed between the pair of opposed side surfaces, at least four electrical terminals disposed on each of the opposed side surfaces, the capacitor body also including at least one first electrode plate having a generally substantially rectangular first main electrode portion with a plurality of first lead structures extending therefrom and at least one second electrode plate situated in opposed and spaced apart relation to the first electrode plate, the second electrode plate having a generally substantially rectangular second main electrode portion with a plurality of second lead structures extending therefrom, respective ones of the first lead structures being located adjacent respective ones of the second lead structures in an interdigitated arrangement and extending to respective ones of the electrical terminals; dielectric material disposed between each opposing set of first and second electrode plates, wherein each of the lead terminals of the at least one first electrode plate being disposed opposite to another of the lead terminals of the at least one first electrode plate across the capacitor body and each of the lead terminals of the at least one second electrode plate being disposed opposite to another of the lead terminals of the at least one second electrode plate across the capacitor body and at least one of the lead structures of the first and second electrode plates have a length L and a width W and a ratio L/W is equal to about 3 or less.

In other preferred embodiments based on the two preferred embodiments described above, it is preferred that the ratio L/W is equal to about 1.3 or less and equal to about 0.4 or greater.

Further, it is preferred that the width W of at least one of the lead electrodes is different from that of the other lead electrodes.

In other preferred embodiments, lead electrodes are provided on each of a first pair of opposed sides of the capacitor body and a lead electrode is provided on each of a second pair of opposed sides of the capacitor body, and the width W of at least one of the lead electrodes provided on a respective one of the second pair of opposed sides of the capacitor body is wider than the lead electrodes disposed on each of the first pair of opposed sides of the capacitor body.

Also, it is preferred that the lengths L of all of the lead electrodes are substantially equal to each other.

The internal and lead electrodes are preferably arranged in such a manner that when currents of different polarity are applied to the first and second internal electrodes, the net induced inductance in the area of all four of the side surfaces is substantially zero.

In a preferred embodiment of the present invention, the first internal electrode is formed with at least four first lead electrodes which extend respectively to respective ones of the four side surfaces. An equal number of first external terminal electrodes are provided. At least one of the first external terminal electrodes is located on each of the four side surfaces.

In this preferred embodiment, the second internal electrode is formed with at least four second lead electrodes which extend to respective ones of the four side surfaces. An equal number of second external terminal electrodes are provided. At least one of the second external terminal electrodes is located on each of the four side surfaces.

It is more advantageous if the above-described configuration is used for both of the first and second internal electrodes.

In another preferred embodiment, for each side surface which has both a first and a second external terminal electrode, each of the first external terminal electrodes located on that surface is located adjacent to one a corresponding second external terminal electrode located on that side surface. It is more advantageous if all of the first external terminal electrodes and all of the second external terminal electrodes are arranged such that they alternate with each other throughout the four side surfaces.

In yet another preferred embodiment, all of the external terminal electrodes are arranged such that they are not adjacent to any other external electrode which is connected to the same internal electrode.

In still another preferred embodiment, the first internal electrode is formed with three first lead electrodes which extend respectively to three of the side surfaces. The second internal electrode is formed with two second lead electrodes which extend respectively to two of the side surfaces, one of which does have a first external electrode.

In another preferred embodiment, at least one of the first and at least one of the second external terminal electrodes is provided on each of the four side surfaces.

A plurality of capacitor units can be provided in the multi-layer capacitor. Each capacitor unit includes a respective pair of first and second internal electrodes with a respective dielectric layer located therebetween.

According to various preferred the present invention, the effect of reducing ESL can be expected from effective cancellation of magnetic and reduction of the lengths of currents achieved by providing a third internal electrode facing at least either the first or second internal electrodes with a dielectric material layer interposed therebetween. The third internal electrode is formed with at least two third lead electrodes which extend to respective ones of the side surfaces. An equal number of third external terminal electrodes are provided on the corresponding side surfaces and are electrically coupled to respective ones of the third lead electrode.

In the above-described preferred embodiment, when all of the first, second and third external terminal electrodes are arranged in the same order of arrangement repeated throughout the four side surfaces, the various components of magnetic flux can be more effectively canceled and the lengths of the current paths can be shortened further for a further reduction of ESL.

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Other features, characteristics, elements and advantages of preferred embodiments of the present invention will be described in more detail below with reference to the figures attached hereto.

BRIEF DESCRIPTION OF THE DRAWINGS

For the purpose of illustrating the invention, there is shown in the drawing several forms which are presently preferred, it being understood, however, that the invention is not limited to the precise arrangements and instrumentalities shown.

FIG. **1** is a plan view of a multi-layer capacitor **31** according to a first preferred embodiment of the present invention;

FIG. **2** is a plan view of the multi-layer capacitor **31** shown in FIG. **1** showing an internal structure thereof in the form of a section along which a first internal electrode **40** extends;

FIG. **3** is a plan view of the multi-layer capacitor shown **31** in FIG. **1** showing an internal structure thereof in the form of a section along which a second internal electrode **41** extends;

FIG. **4** is a plan view illustrating currents flowing in the multi-layer capacitor **31**;

FIG. **5** is a plan view of a multi-layer capacitor **71** according to a second preferred embodiment of the invention showing the external appearance thereof;

FIG. **6** is a plan view of the multi-layer capacitor **71** shown in FIG. **5** showing an internal structure thereof in the form of a section along which a first internal electrode **40***a* extends;

FIG. **7** is a plan view of the multi-layer capacitor **71** shown in FIG. **5** showing an internal structure thereof in the form of a section along which a second internal electrode **41***a* extends;

FIG. **8** is a plan view of a multi-layer capacitor **81** according to a third preferred embodiment of the invention showing the external appearance thereof;

FIG. **9** is a plan view of the multi-layer capacitor **81** shown in FIG. **8** showing an internal structure thereof in the form of a section along which a third internal electrode **82** extends;

FIG. **10** is a plan view of the multi-layer capacitor **81** shown in FIG. **8** showing an internal structure thereof in the form of a section along which a first internal electrode **40***b* extends;

FIG. **11** is a plan view of the multi-layer capacitor **81** shown in FIG. **8** showing an internal structure thereof in the form of a section along which a second internal electrode **41***b* extends;

FIG. **12** is a plan view of a multi-layer capacitor **91** according to a fourth preferred embodiment of the invention showing the external appearance thereof;

FIG. **13** is a plan view of the multi-layer capacitor **91** shown in FIG. **12** showing an internal structure thereof in the form of a section along which a first internal electrode **40***c* extends;

FIG. **14** is a plan view of the multi-layer capacitor **91** shown in FIG. **12** showing an internal structure thereof in the form of a section along which a second internal electrode **41***c* extends;

FIG. **15** is a plan view of a conventional multi-layer capacitor **1** which is of interest to the present invention showing the external appearance thereof;

FIG. **16** is a plan view of the multi-layer capacitor **1** shown in FIG. **15** showing an internal structure thereof in the form of a section along which a first internal electrode **10** extends;

FIG. **17** is a plan view of the multi-layer capacitor **1** shown in FIG. **15** showing an internal structure thereof in the form of a section along which a second internal electrode **11** extends;

FIG. **18** is a plan view illustrating currents flowing in the multi-layer capacitor **1** shown in FIG, **15**;

FIG. **19** is a plan view of a multi-layer capacitor **101** according to a fifth preferred embodiment of the present invention;

FIG. **20** is a plan view of the multi-layer capacitor **101** shown in FIG. **19** showing an internal structure thereof in the form of a section along which a first internal electrode **40***d* extends; and

FIG. **21** is a plan view of the multi-layer capacitor **101** shown in FIG. **10** showing an internal structure thereof in the form of a section along which a second internal electrode **41***d* extends.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

First Preferred Embodiment

Referring now to the drawings, wherein like numerals indicate like elements, there is shown in FIGS. **1** through **3** a first preferred embodiment of a multi-layer capacitor constructed in accordance with the principles of the present invention and designated generally as **31**. FIGS. **1** through **3** correspond to FIGS. **15** through **17**.

FIG. **1** is a plan view of the external appearance multi-layer capacitor **31**. FIG. **2** is a plan view multi-layer capacitor **31** showing a first internal electrode **40** located on one surface of a first internal dielectric layer **39** of the capacitor **31**. FIG. **3** is a plan view of a second section of the multi-layer capacitor **31** showing a second internal electrode **41** located on one surface of a second internal dielectric layer **39** of the capacitor **31**.

Multi-layer capacitor **31** includes a capacitor main body **38** in the form of a rectangular parallelpiped having two opposed principal surfaces **32** and **33** and four side surfaces **34**, **35**, **36** and **37** extending therebetween. The capacitor main body **38** includes a plurality of generally planar dielectric layers **39** made of, for example, a ceramic dielectric material. The main surfaces of the dielectric layers **39** are situated generally parallel to the principal surfaces **32**, **33** of the capacitor main body **38**. At least a pair of first and second internal electrodes **40** and **41** are provided in a face-to-face relationship with each other with a dielectric material layer **39** interposed therebetween, each such pair of internal electrodes forming a respective capacitor unit.

As shown in FIG. **2**, the first internal electrode **40** has six lead electrodes **42**, **43**, **44**, **45**, **46** and **47**, each of which extends to a respective one of the four side surfaces **34** through **37**. Particularly, the lead electrodes **42** and **43** extend to the side surface **34**; the lead electrode **44** extends to the side surface **35**; the lead electrodes **45** and **46** extend to the side surface **36**; and the lead electrode **47** extends to the side surface **37**.

Each lead electrode **42**–**47** is electrically coupled to a respective external terminal electrodes **48**–**53**. The external terminal electrodes **48** and **49**, connected to the lead electrodes **42** and **43**, respectively, are located on the side surface

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34; the external terminal electrode **50**, connected to the lead electrode **44**, is located on the side surface **35**; the external terminal electrodes **51** and **52**, connected to the lead electrodes **45** and **46**, respectively, are located on the side surface **36**; and the external terminal electrode **53**, connected to the lead electrode **47**, is located on the side surface **37**.

As shown in FIG. **3**, the internal electrode **41** is formed with six second lead electrodes **54**, **55**, **56**, **57**, **58** and **59**, each of which extends to a respective one of the four side surfaces **34** through **37**. More specifically, the lead electrodes **54** and **55** extend to side surface **34**; lead electrode **56** extends to side surface **35**; lead electrodes **57** and **58** extend to side surface **36**; and lead electrode **59** extends to the side surface **37**.

The positions on the side surfaces **34** through **37** to which the respective lead electrodes **54** through **59** extend are different from the positions to which the respective lead electrodes **42** through **47** extend.

External terminal electrodes **60**, **61**, **62**, **63**, **64** and **65**, which are electrically coupled to respective lead electrodes **54** through **59**, are provided on the side surfaces **34** through **37** at positions which are different than the positions of the external terminal electrodes **48** through **53**. External terminal electrodes **60** and **61**, connected to lead electrodes **54** and **55**, respectively, are located on side surface **34**; external terminal electrode **62**, connected to lead electrode **56**, is located on side surface **35**; external terminal electrodes **63** and **64**, connected to lead electrodes **57** and **58**, respectively, are located on side surface **36**; and external terminal electrode **65**, connected to lead electrode **59**, are located on side surface **37**.

The external terminal electrodes **48** through **53** are arranged in an interleaved manner such that no two external electrodes which are electrically coupled to the same internal electrode **40** or **41** are adjacent one another. In operation, the polarizations of the first and second internal electrodes **40**, **41** are preferably opposite to one another.

In order to increase the capacity of the multi-layer capacitor **31**, additional pairs of internal electrodes can be provided to define additional capacitor units. For example, the multi-layer capacitor **31** can include two sets of capacitor units, each set being defined by a respective pair of first and second internal electrodes **40**, **41** separated by a respective dielectric layer. The plurality of capacitor units are preferably connected in parallel by at least either appropriate ones of the first external terminal electrodes **48** through **53** or the second external terminal electrodes **60** through **65**.

Each of the external terminal electrodes **48** through **53** and **60** through **65** is preferably formed so as to extend not only on the side surfaces **34** through **37** but also onto a part of each of the principal surfaces **32** and **33**.

FIG. **4** illustrates various currents, flowing in the multi-layer capacitor **31**. In FIG. **4**, the first internal electrode **40** is indicated by a broken line and the second internal electrode **41** is indicated by a solid line, the two electrodes being illustrated in an overlapping relationship.

As apparent from these typical paths and the directions of current flow indicated by the arrows in FIG. **4** (the direction of current flow indicates that direction of each of the noted current paths at a given point in time, the direction of the flow of current through these paths will alternate periodically), a current flows from each of the second external terminal electrodes **60** through **65** to each of the first external terminal electrodes **48** through **53**. When such currents flow, induced magnetic flux is generated.

As in the prior art, the various components of the induced flux at the central regions **66** indicated by the circles cancel one another out because currents flow in various directions. Similarly, the various components of the induced flux in the areas of the side surfaces **34** and **36** tend to cancel one another. In this connection, current flow in the area of side surfaces **34** and **36** is very similar to that of the prior art of FIG. **18**.

However, the embodiment of FIGS. **1**–**4** produces a much more desirable result in the areas **67** adjacent the side surfaces **35**, **37**. Since the first external terminal electrodes **50** and **53** and the second external terminal electrodes **62** and **65** are provided at the side surfaces **34** and **36**, there is no significant net current flow in the areas **67** and no significant generation of net magnetic flux.

As a result, the degree of net induced magnetic flux generated over the entire region of the multi-layer capacitor **31** is significantly reduced, thereby allowing the ESL to be suppressed to a very low level.

Another advantage of this embodiment is that the current paths between each of the electrodes is reduced. Particularly, each of the first lead electrodes **42** through **47** (and the first external terminal electrodes **48** through **53**) is located relatively close to its adjacent second lead electrode **54** through **59** (and the second external terminal electrode **60** through **64**) compared to the prior art of FIG. **18**. This reduces the lengths of the current paths and thereby reduces self-inductance components produced between them.

Second Preferred Embodiment

FIGS. **5** through **7** show a multi-layer capacitor **71** according to a second preferred embodiment of the present invention. FIG. **5** is a plan view of the external appearance of the multi-layer capacitor **71**. FIG. **6** is a plan view showing one surface of an internal dielectric layer **39** of the multi-layer capacitor **71** having a first internal electrode **40***a* located thereon. FIG. **7** is a plan view showing one surface of a different one of the internal dielectric layers **39** of the multi-layer capacitor **71** having a second internal electrode **41***a* located thereon.

FIGS. **5** through **7** respectively correspond to FIGS. **1** through **3** of the first preferred embodiment. In FIGS. **5** through **7**, elements corresponding to elements shown in FIGS. **1** through **3** are indicated by like reference numbers and will not be described here to avoid duplication.

Referring to FIG. **6**, the first internal electrode **40***a* is formed with five lead electrodes **42**, **43**, **45**, **46** and **47***a* which extend to respective side surfaces **34**, **36** and **37**. The multi-layer capacitor **71** is different from the multi-layer capacitor **31** of the first embodiment in that the multi-layer capacitor **71** has no lead electrode extending to side surface **35**. Additionally, lead electrode **47***a* extends to the middle of the side surface **37**, whereas lead electrode **47** extends to the upper half of side surface **37**.

The five lead electrodes **42** through **47***a* are electrically coupled to five external terminal electrodes **48**, **49**, **51**, **52** and **53***a*, respectively. The five external electrodes **48**, **49**, **51**, **52** and **53***a*, are each located on one of the three side surfaces **34**, **36** and **37**. The multi-layer capacitor **71** is different from the multi-layer capacitor **31** of the first preferred embodiment in that the multi-layer capacitor **71** has no external terminal corresponding to the first external terminal electrode **50** and in that the external terminal electrode **53***a* is different in location from the external terminal electrode **53**.

Referring to FIG. **7**, a second internal electrode **41***a* has five lead electrodes **54**, **55**, **56***a*, **57** and **58** which extend to respective side surfaces **34** through **36**. The multi-layer

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capacitor **71** is different from the multi-layer capacitor **31** of the first preferred embodiment in that it has no lead electrode extending to the side surface **37** and in that the lead electrode **56***a* which extends to the side surface **35** extends to the middle of the side surface **35**, rather than the bottom of the side surface **35** as is the case with lead electrode **56** of the first preferred embodiment.

Each of the lead electrodes **54** through **58** is electrically coupled to a respective external terminal electrode **60**, **61**, **62***a*, **63** and **64**. Each of these terminal electrodes are provided on a respective side surface **34** through **36**. The multi-layer capacitor **71** is different from the multi-layer capacitor **31** of the first preferred embodiment in that it has no external terminal corresponding to the external terminal electrode **65** and in that the external terminal electrode **62***a* is located in a different position than the external terminal electrode **62**.

If desired, the capacity of multi-layer capacitor **71** can be increased by providing a plurality of capacitive units, each defined by a respective set of internal electrodes **40***a*, **41***a*, separated by a respective dielectric layer **38**. The plurality of capacitor units are then connected in parallel by appropriate ones of the external terminal electrodes **48** through **53***a* or **60** through **64**.

In the second preferred embodiment of the invention, each of the external terminal electrodes **48**, **49**, **51** and **52** coupled to the first internal electrode **40***a* is located adjacent to at least one of the external terminal electrodes **60**, **61**, **63** and **64** coupled to internal electrode **41***a*. Further, only the second external terminal electrode **62***a* is located on the side surface **35**, and only the first external terminal electrode **53***a* is located on the side surface **37**. By providing the external terminal electrodes **62***a* and **53***a* on the side surfaces **35** and **37**, respectively, it is possible to direct the flow of the currents on the internal electrodes **40***a* and **41***a* in various directions to achieve a level of cancellation of magnetic flux that is higher than that which is achievable in the conventional multi-layer capacitor **1** shown in FIGS. **15** through **17**. It is also possible to reduce the length of the path of these currents thereby further reducing the induced inductance components.

Third Preferred Embodiment

FIGS. **8** through **11** show a multi-layer capacitor **81** according to a third preferred embodiment of the present invention. FIG. **8** is a plan view of the external appearance of the multi-layer capacitor **81**. FIG. **9** is a plan view of the surface of one of the internal dielectric layers **39** of the multi-layer capacitor **81** having a first internal electrode **82** formed thereon. FIG. **10** is a plan view of the surface of one of the internal dielectric layers **39** of the multi-layer capacitor **81** having a second internal electrode **40***b* formed thereon. FIG. **11** is a plan view of the surface of one of the internal dielectric layers **39** of the multi-layer capacitor **81** having a third internal electrode **41***b* formed thereon.

In FIGS. **8** through **11**, elements corresponding to elements shown in FIGS. **1** through **3** are indicated by like reference numbers and will not be described here to avoid duplication.

The multi-layer capacitor **81** of the third preferred embodiment of the invention includes a third internal electrode **82** facing at least either the first internal electrode **40***b* or second internal electrode **41***b* with a dielectric material layer **39** interposed therebetween. The third internal electrode **82** is formed with four lead electrodes **83**, **84**, **85** and **86**, each of which extends to a respective side surface **34** and **36**. More specifically, lead electrodes **83** and **84** extend to side surface **34**, and lead electrodes **85** and **86** extend to side surface **36**.

External terminal electrodes **87**, **88**, **89** and **90**, which are electrically coupled to the lead electrodes **83** through **86**, respectively, are provided on respective side surfaces **34** and **36**. The multi-layer capacitor **81** is different from the multi-layer capacitor **31** of the first preferred embodiment in that it includes the third external terminal electrodes **87** and **90** provided, respectively, in the positions where the first external terminal electrodes **48** and **52** are provided on the multi-layer capacitor **31** of the first embodiment and includes the third external terminal electrodes **88** and **89** provided respectively in the positions where the second external terminal electrodes **61** and **63** are provided on the multi-layer capacitor **31**.

Referring to FIG. **10**, a first internal electrode **40***b* has four first lead electrodes **42***b*, **44**, **45***b* and **47** which extend to respective side surfaces **34** through **37**. The first internal electrode **40***b* of the multi-layer capacitor **81** is different from the multi-layer capacitor **31** of the first embodiment in that it has only one lead electrode **42***b* which extends to side surface **34** and one lead electrode **45***b* which extends to side surface **36**.

Four first external terminal electrodes **48***b*, **50**, **51***b* and **53** are electrically coupled to the four first lead electrodes **42***b* through **47**, respectively, and are provided on the four side surfaces **34** through **37**, respectively. The multi-layer capacitor **81** is different from the multi-layer capacitor **31** of the first preferred embodiment in that it includes the first external terminal electrodes **48***b* and **51***b* provided respectively in the positions where the second external terminal electrodes **60** and **64** are provided on the multi-layer capacitor **31**.

Referring to FIG. **11**, a second internal electrode **41***b* has four second lead electrodes **54***b*, **56**, **57***b* and **59** which extend to respective side surfaces **34** through **37**. The second internal electrode of the multi-layer capacitor **81** is different from the second internal electrode **41** of the multi-layer capacitor **31** of the first preferred embodiment in that only one lead electrode **54***b* extends to the side surface **34** and only one lead electrode **57***b* extends to side surface **36**.

Four second external terminal electrodes **60***b*, **62**, **63***b* and **65** are electrically coupled to the four first lead electrodes **54***b* through **59**, respectively. The four second external terminal electrodes are provided on the four side surfaces **34** through **37**, respectively. The multi-layer capacitor **81** is different from the multi-layer capacitor **31** of the first preferred embodiment in that the second external terminal electrodes **60***b* and **63***b* provided, respectively, in the positions where the first external terminal electrodes **49** and **51** are provided on the multi-layer capacitor **31**.

By way of example, the multi-layer capacitor **81** can be formed by locating the third internal electrode **82**, the first internal electrode **40***b* and the second internal electrode **41***b*, one above the other with respective dielectric layers being located therebetween. Irrespective of the relative locations of the internal electrodes, the external terminal electrodes are arranged such that each of the third external terminal electrodes **87** through **90** is followed by one of the first external terminal electrodes **48***b* through **53** and then followed by one of the second external terminal electrodes **60***b* through **65**. This alternating arrangement is repeated throughout the four side surfaces **34** through **37**. The above-described order of stacking the internal electrodes **82**, **40***b* and **41***b* may be changed arbitrarily.

In order to increase the capacity of the multi-layer capacitor **81**, a plurality of third internal electrodes **82**, first internal

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electrodes **40***b* and second internal electrodes **41***b* may be provided to form a plurality of capacitor units. For example, a plurality of third internal electrodes **82** and a plurality of first internal electrodes **40***b* may be provided; a plurality of second internal electrodes **41***b* and a plurality of third internal electrodes **82** may be provided; or a plurality of third internal electrodes **82**, a plurality of first internal electrodes **40***b* and a plurality of second internal electrodes **41***b* may be provided. The resultant capacitor units are connected in parallel by at least any of the third external terminal electrodes **87** through **90**, the first external terminal electrodes **48***b* through **53** and the second external terminal electrodes **60***b* through **65**.

Like the first preferred embodiment, external terminal electrodes connected to different internal electrodes (that is, external terminal electrodes having different polarities) are located on each of the four side surfaces **34** through **37**. More specifically, first external terminal electrode **48***b*, second external terminal electrode **60***b* and third external terminal electrodes **87** and **88** are located on the side surface **34**; first external terminal electrode **50** and second external terminal electrode **62** are located on side surface **35**; first external terminal electrode **51***b*, second external terminal electrode **63***b* and third external terminal electrodes **85** and **90** are located on side surface **36**; and first external terminal electrode **53** and second external terminal electrode **65** are located on side surface **37**.

Therefore, according to the third preferred embodiment of the invention, since the flow of currents on the internal electrodes **40***b* and **41***b* can be directed in various directions to effectively cancel magnetic flux and to reduce the lengths of the current paths, the induced inductance components can be reduced.

Although the arrangement of the third preferred embodiment is different from that in the first preferred embodiment in that external terminal electrodes having different polarities are not necessarily adjacent to each other in all locations, the directions of the current flows on the internal electrodes **40***b* and **41***b* is more diverse than those in the conventional multi-layer capacitor **1** shown in FIGS. **15** through **17** and the lengths of the current paths are shorter. This makes it possible to achieve a higher reduction of the induced inductance components.

As an alternative to the third preferred embodiment, a multi-layer capacitor may be provided in which only the first and second internal electrodes **40***b* and **41***b* are provided and the third internal electrode **82** is excluded. Further, the third internal electrode **82** may be formed with lead electrodes which extend to the side surfaces **35** and **37**.

Fourth Preferred Embodiment

FIGS. **12** through **14** show a multi-layer capacitor **91** according to a fourth preferred embodiment of the present invention. FIG. **12** is a plan view of the external appearance of the multi-layer capacitor **91**. FIG. **13** is a plan view of the surface of one of the dielectric layers of the multi-layer capacitor **91** having a first internal electrode **40***c* formed thereon. FIG. **14** is a plan view of the surface of one of the dielectric layers of the multi-layer capacitor **91** having a second internal electrode **41***c* formed thereon.

FIGS. **12** through **14** respectively correspond to FIGS. **1** through **3** of the first preferred embodiment. In FIGS. **12** through **14**, elements corresponding to elements shown in FIGS. **1** through **3** are indicated by like reference numbers and will not be described here to avoid duplication.

The multi-layer capacitor **91** of the fourth preferred embodiment of the invention resembles the multi-layer capacitor **71** of the second embodiment in its external appearance. A first internal electrode **40***c* has five first lead electrodes **42**, **43**, **44***c*, **45***c* and **46***c* which extend to respective side surfaces **34**, **35** and **36**. The multi-layer capacitor **91** is different from the multi-layer capacitor **31** of the first preferred embodiment in that does not include a lead electrode corresponding to the lead electrode **47** which extends to the side surface **37** and in that the positions at which the lead electrodes **44***c*, **45***c* and **46***c* respectively extends to the side surfaces **35** and **36** are different from the positions that the lead electrodes **44** through **46** extend to those surfaces.

Five external terminal electrodes **48**, **49**, **50***c*, **51***c* and **52***c* are electrically coupled to the five lead electrodes **42** through **46***c*, respectively. These external electrodes are provided on the side surfaces **34** through **36**. The multi-layer capacitor **91** is different from the multi-layer capacitor **31** of the first preferred embodiment in that it does not include an external terminal electrode corresponding to the first external terminal electrode **53** and in that the positions of the external terminal electrodes **50***c*, **51***c* and **52***c* are different from the positions of the external terminal electrodes **50** through **52**, respectively.

Referring to FIG. **14**, a second internal electrode **41***c* has five lead electrodes **54**, **55**, **57***c*, **58***c* and **59***c*, each of which extends to a respective side surfaces **34**, **36** and **37**. The multi-layer capacitor **91** is different from the multi-layer capacitor **31** of the first preferred embodiment in that it does not include a lead electrode corresponding to the lead electrode **59** which extends to the side surface **35** and in that the positions of the lead electrodes **57***c*, **58***c* and **59***c* are different from the positions of the lead electrodes **57** through **59**, respectively.

The external terminal electrodes **60**, **61**, **63***c*, **64***c* and **65***c* which are electrically coupled to second lead electrodes **54** through **59***c*, respectively, are provided on the side surfaces **34**, **36** and **37**. The multi-layer capacitor **91** is different from the multi-layer capacitor **31** of the first preferred embodiment in that it does not include an external terminal electrode corresponding to the second external terminal electrode **62** and in that the positions of the external terminal electrodes **63***c*, **64***c* and **65***c* are different from the positions of the external terminal electrodes **63** through **65**, respectively.

In order to increase the capacity of multi-layer capacitor **91**, a plurality of first internal electrodes **40***c* and a plurality of second internal electrodes **41***c* can be provided. Pairs of internal electrodes **40***c*, **41***c* will face one another with a dielectric layer formed therebetween so as to form respective capacitor units. These capacitor units will be connected in parallel by at least either the first external terminal electrodes **48** through **52***c* or the second external terminal electrodes **60** through **65***c*.

Like the first preferred embodiment described above, each of the first external terminal electrodes **48** through **52***c* of the fourth preferred embodiment of the invention is arranged so as to alternate with respective ones of the second external terminal electrodes **60** through **65***c* throughout the four side surfaces **34** through **37**. The fourth preferred embodiment is different from the second preferred embodiment in this regard.

Therefore, according to the fourth preferred embodiment of the invention, since the flow of currents on the internal electrodes **40***c* and **41***c* can be directed in various directions, the various components of induced magnetic flux will be cancelled and the lengths of the current paths will be shortened relative to the prior art of FIGS. **15**–**17**. The fourth

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preferred embodiment will effectively reduce the induced inductance components to a degree which is similar to that of the first preferred embodiment.

In relation to additional features and advantages of the fourth preferred embodiment, the inventors discovered that variations in dimensions and relationships between such dimensions of the lead electrodes materially affect the ESL of the capacitors of the fourth preferred embodiment and each of other preferred embodiments described herein. These further features and advantages described in the following paragraphs are shown as being incorporated in the fourth preferred embodiment of FIGS. **12–14** but can be applied and incorporated in any of the preferred embodiments disclosed herein.

More specifically, the length and the width of a lead-out portion are designated by reference characters L, W in FIG. **13**, for example. In each of the above-described preferred embodiments, currents in the main portions of the first internal electrodes and the second internal electrodes flow in different directions, so that the generation of a magnetic flux is prevented. However, in the respective lead electrodes, currents flow in a uniform direction. Therefore, a magnetic flux is generated, and an inductance is generated in accordance with the magnetic flux. Further, the state of currents flowing in the respective main portions of the first internal electrodes and the second internal electrodes is changed, depending on the lengths and the widths of the lead electrodes. Accordingly, the lengths and the widths of the lead electrodes significantly affect the ESL value of the capacitor.

To confirm the discovery described above, the lengths L and the widths W of all of the lead electrodes were varied in a multi-layer capacitor **91** according to a fourth preferred embodiment as shown in FIGS. **12** through **14**. The capacitor **91** preferably includes a total of **10** lead electrodes, for example, in which four lead electrodes **42**, **43**, **54**, **55** and four lead electrodes **45***c*, **46***c*, **57***c*, **58***c* are extended onto the side surfaces **34**, **36**, respectively, and moreover, and one lead electrode **44***c* and one lead electrode **59***c* are extended onto the side surfaces **35**, **37**, correspondingly.
TABLE 1 shows the results.

TABLE 1

	L = 0.1 mm	L = 0.2 mm	L = 0.3 mm	L = 0.5 mm
W = 0.08 mm	38 pH	65 pH	87 pH	106 pH
W = 0.16 mm	28 pH	35 pH	50 pH	81 pH
W = 0.24 mm	25 pH	32 pH	39 pH	58 pH

The numerical values listed in TABLE 1 are measurement values of the ESL obtained by a conventional publicly-known resonance method. As seen in the results, in the capacitors having plural lead electrodes, the ESL value is changed according to the ration of L/W. When the ratio L/W of the capacitors is about 3 or lower, the ESL value is less than about 80 pH. When the ratio L/W is about 1.3 or lower, the ESL value is less than about 40 pH.

In the above-described preferred embodiments, the widths of all of the plural lead electrodes are preferably substantially equal to each other. However, the above-described preferred range of the L/W value can be applied to capacitors having the structure in which the width of at least one of the lead electrodes is different from that of the respective remaining lead electrode(s). For example, this will be described in reference to FIGS. **13** and **14**. The above-described preferred range of the L/W value can be applied to capacitors each having the structure in which the widths of one lead electrode **44***c* and one lead electrode **59***c* extending onto the side surfaces **35**, **37**, correspondingly, are wider as compared with four lead electrodes **42**, **43**, **54**, **55** and four lead electrodes **45***c*, **46***c*, **57***c*, **58***c* extending onto the side surfaces **34**, **36**, respectively.

According to another preferred embodiment, a capacitor structure is similar to that of the multi-layer capacitor **91** according to the fourth preferred embodiment as shown in FIGS. **12** through **14**, except that the lead electrodes **44***c*, **59***c* are not provided. The lengths L and the widths W of all the lead electrodes of this preferred embodiment were also varied to provide further confirmation of the discovery with respect to the ratio L/W described above. In this capacitor, four lead electrodes are preferably extended onto the side surfaces **34**, **36**, respectively. That is, the capacitor has a total of **8** lead electrodes, for example. TABLE 2 shows the results.

TABLE 2

	L = 0.1 mm	L = 0.2 mm	L = 0.3 mm	L = 0.5 mm
W = 0.08 mm	79 pH	107 pH	131 pH	176 pH
W = 0.16 mm	68 pH	76 pH	95 pH	133 pH
W = 0.24 mm	55 pH	66 pH	77 pH	106 pH

The numerical values in TABLE 2 are measurement values of ESL obtained by a conventional publicly-known resonance method. In this capacitor, when the ratio L/W is about 3 or lower, the ESL value is about 120 pH or lower. When the ratio L/W is about 1.3 or lower, the ESL value is about 80 pH or lower. For the prior art structure described in the specification of this application, the same results are obtained.

In the above preferred embodiment, the widths of all the lead electrodes are preferably made substantially equal to each other. However, the above-described preferred range of the ratio L/W value can be applied to capacitors having the structure in which the width of at least one of the lead electrodes is wider than that of the respective remaining lead electrodes.

In recently developed microprocessing units (MPU), the operating frequency of nearly 1 GHz is to be used. Such an MPU contains an MPU chip and a capacitor. Capacitors combined with the MPU chip are required to have an ESL value of less than about 10 pH. If one capacitor can not satisfy the requirement, plural capacitors are connected in parallel. For the purpose of reducing an inductance component caused by the wiring being short-circuited between the plural capacitors and the MPU chip, the capacitors are arranged close to the four sides of the MPU chip. In the case that the total ESL value of the plurality of capacitors is less than about 10 pH, and one capacitor is arranged on each of the four sides of the MPU chip, it is required to provide capacitors each having an ESL value of less than about 40 pH. When two capacitors are arranged on each of the four sides of the MPU chip, it is required for each capacitor to have an ESL value of less than about 80 pH. When three capacitors are arranged on each of the four sides of a MPU chip, it is required for each capacitor to have an ESL value of less than about 120 pH. The L/W values which have been included in the above preferred embodiment are significant for providing capacitors satisfying such a requirement.

Accordingly, in preferred embodiments of the present invention, when the ratio L/W is about 3 or lower, low ESL capacitors which are practically useful can be obtained. Preferably, the ratio L/W is about 1.3 or lower. In general, when lead electrodes are widened, currents can flow smoothly from the portions of capacitors where charges are

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accumulated, that is, the respective main portions of the first internal electrodes and the second internal electrodes into the lead electrodes. However, preferably, the ratio L/W is about 0.4 or higher because when the ratio L/W is less than about 0.4, the lengths of lead electrodes are short and/or the widths are wide, and therefore, deterioration of the electrical insulation and moisture-proof properties occurs.

Further, another preferred embodiment is arranged such that the outside dimensions of all of the first internal electrodes and all of the second internal electrodes are preferably substantially equal to each other, and the lengths of all the lead electrodes are preferably substantially equal to each other. In this preferred embodiment, the lengths of all of the lead electrodes are preferably substantially equal, and moreover can be reduced as much as possible. The static capacitance can be also made as large as possible.

On the other hand, when the outside dimensions of the first internal electrodes are smaller than those of the second internal electrodes, for example, the lengths of the lead electrodes connected to the first internal electrodes become relatively longer as compared with those of the second internal electrodes. Then, the ESL value is increased, as compared with that in the preferred embodiments of the present application. In other words, the capacitors of the preferred embodiments of this application have a much lower ESL value than capacitors having the structure in which the outside dimensions of the first internal electrodes and those of the second internal electrodes are different from each other.

Fifth Preferred Embodiment

FIGS. **19** through **21** show a multi-layer capacitor **101** according to a fifth preferred embodiment of the present invention. FIG. **19** is a plan view of the external appearance of the multi-layer capacitor **101**. FIG. **20** is a plan view of the surface of one of the dielectric layers of the multi-layer capacitor **101** having a first internal electrode **40***d* formed thereon. FIG. **21** is a plan view of the surface of one of the dielectric layers of the multi-layer capacitor **101** having a second internal electrode **41***d* formed thereon.

FIGS. **19** through **21** respectively correspond to FIGS. **1** through **3** of the first preferred embodiment. In FIGS. **19** through **21**, elements corresponding to elements shown in FIGS. **1** through **3** are indicated by like reference numbers and will not be described here to avoid duplication.

Referring to FIG. **20**, a first internal electrode **40***d* has three first lead electrodes **44***d*, **45***d* and **47***d* which extend to respective side surfaces **35**, **36** and **37**. The multi-layer capacitor **101** is different from the multi-layer capacitor **31** of the first preferred embodiment in that it does not include lead electrodes **42** and **43** which extend to the side surface **34**, does not include a lead electrode **46** which extends to the side surface **36**, and in that the positions at which the lead electrodes **44***d*, **45***d*, and **47***d* respectively extend to the side surfaces **35**, **36** and **37** are different from the positions that the lead electrodes **44**, **45** and **47** extend to those surfaces.

The three lead electrodes **44***d*, **45***d* and **47***d* are electrically coupled to three external terminal electrodes **50***d*, **51***d* and **53***d* respectively. These external terminal electrodes are provided on the side surfaces **35** through **37**. The multi-layer capacitor **101** is different from the multi-layer **31** of the first preferred embodiment in that it does not include external terminal electrodes corresponding to the first external terminal electrodes **48**, **49** and **52** in that the positions of the external terminal electrodes **50***d*, **51***d* and **53***d* are different from the positions of the external terminal electrodes **50**, **51** and **53**, respectively.

Referring to FIG. **21**, a second internal electrode **41***d* has two lead electrodes **54***d* and **57***d*, each of which extends to respective side surfaces **34** and **36**. The multi-layer capacitor **101** is different from the multi-layer capacitor **31** of the first preferred embodiment in that it does not include lead electrodes corresponding to the lead electrodes **61**, **62**, **64** and **65** which extends to the side surfaces **34** through **37**, respectively, and in that the positions of the lead electrodes **54***d* and **57***d* are different from the positions of the lead electrodes **54** and **57**, respectively.

Two external terminal electrodes **60***d* and **63***d* are electrically coupled to the two lead electrodes **54***d* and **57***d*, respectively, and are provided on the side surfaces **34** and **36**. The multi-layer capacitor is different from the multi-layer capacitor **31** of the first preferred embodiment in that it does not include external terminal electrodes corresponding to the second external terminal electrodes **61**, **62**, **64** and **65**, and in that the positions of the external terminal electrodes **60***d* and **63***d* are different from the positions of the external terminal electrodes **60** and **63**, respectively.

In order to increase the capacity of multi-layer capacitor **101**, a plurality of first internal electrodes **40***d* and a plurality of second internal electrodes **41***d* can be provided. Therefore, according to the fifth preferred embodiment of the invention, since the flow of the currents on the internal electrodes **40***b* and **41***b* can be directed in various directions to effectively cancel magnetic flux and to reduce the lengths of the current paths, the induced inductance components can be reduced.

Although the arrangement of the fifth preferred embodiment is different from that in that first preferred embodiment in that external terminal electrodes having different polarities are not necessarily adjacent to each other in all locations the directions of the current flows on the internal electrodes **40***d* and **41***d* is more diverse that those in the conventional multi-layer capacitor **1** shown in FIGS. **15** and **17** and the lengths of the current paths are shorter. Therefore, this makes it possible to achieve a higher reduction of the induced inductance components.

Test Results

A sample of each of the multi-layer capacitor **31** according to the first preferred embodiment (preferred embodiment 1), the multi-layer capacitor **71** according to the second preferred embodiment (preferred embodiment 2), the multi-layer capacitor **81** according to the third preferred embodiment (preferred embodiment 3), the multi-layer capacitor **91** according to the fourth preferred embodiment (preferred embodiment 4) and the conventional multi-layer capacitor **1** (comparative example) was fabricated and ESL of each of them was evaluated.

Each sample was formed with outer plan dimensions of 3.2 mm×2.5 mm. For samples having six layers of internal electrodes in total, i.e., those having two kinds of internal electrodes such as the multi-layer capacitors **31**, **71**, **91** and **1** (embodiments 1, 2 and 4 and comparative example), the stacking of the two kinds of internal electrodes was repeated three times (i.e., three pairs of internal electrodes where used to form three capacitance units). For the sample having three kinds of internal electrodes, i.e., the multi-layer capacitor **81** (preferred embodiment 3), the stacking of the three kinds of internal electrodes was repeated twice.

ESL was obtained using the resonance method. The resonance method is a method wherein the impedance frequency characteristics of each of the sample multi-layer capacitor is measured and ESL is obtained from a frequency

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f_o at a minimum point (referred to as series resonance point between the capacity component C_s and ESL of the capacitor) using the following equation.

$$ESL = 1/[(2\pi f_o)^2 \times C_s]$$

The measured value of ESL of each sample is shown in the Table 3 below.

TABLE 3

	ESL Value (pH)
Embodiment 1	40
Embodiment 2	72
Embodiment 3	85
Embodiment 4	51
Comparative Example	95

It is apparent from Tables 1~3 that ESL was suppressed to a greater degree in the examples of preferred embodiment 4, especially those in Table 1. Also, preferred embodiment 1 produced lower ESL values than the examples in Table 2 of preferred embodiment 4 and than the preferred embodiments 2 and 3 While the present invention has been described with reference to the illustrated preferred embodiments, for example, it is possible to change positions and the number of the lead-out electrodes of the internal electrodes variously and to change the positions and number of the external terminal electrodes accordingly within the scope of the invention.

As described above, according to the preferred embodiments of the present invention, at least either a first or a second internal electrode is formed with at least three lead electrodes which extend respectively to at least three of the side surfaces of a capacitor main body, and external terminal electrodes which are electrically coupled to respective lead electrodes are provided on respective side surfaces. As a result, since the flow of currents on the internal electrodes can be directed in various directions to cancel magnetic flux and to reduce the lengths of the currents path effectively, ESL can be reduced.

With this structure, a high resonance frequency can be achieved and the frequency band of the capacitor can be increased. Accordingly, a multi-layer capacitor according to the invention can accommodate electronic circuits at higher frequencies than was possible with the comparative example and can be advantageously used, for example, as a bypass capacitor or decoupling capacitor in a high frequency circuit. Further, while a decoupling capacitor used in an MPU (microprocessing unit) must also have the function of a quick power supply (a function of supplying power from an amount of electricity charged in the capacitor when there is a sudden need for power as in the case of power-up), a multi-layer capacitor according to the invention can be used for such an application because it has low ESL.

In the preferred embodiments of the present invention below, the cancellation of magnetic fluxes as described above is further improved and the lengths of currents are further reduced to achieve more effective reduction of ESL.

It should be understood that the foregoing description is only illustrative of the invention. Various alternatives and modifications can be devised by those skilled in the art without departing from the invention. Accordingly, the present invention is intended to embrace all such alternatives, modifications and variances which fall within the scope of the appended claims.

What it is claimed is:

1. A multi-layer capacitor device comprising:

a capacitor body including top and bottom surfaces and opposed side surfaces which have continuously flat surfaces and are disposed between the top and bottom surfaces and opposed end surfaces disposed between the top and bottom surfaces and the opposed side surfaces, the capacitor body including a plurality of first electrode plates and a plurality of second electrode plates, the first and second electrode plates being interleaved with each other in opposed and spaced apart relation;

a dielectric material located between each opposed set of the first and second electrode plates;

the first and second electrode plates each including a main electrode portion and a plurality of spaced apart lead structures extending therefrom, respective lead structures of the first electrodes plates being located adjacent respective lead structures of the second electrode plates in an interdigitated arrangement; and

a plurality of electrical terminals located on each of the opposed side surfaces of the capacitor body, corresponding lead structures of the first electrode plates and corresponding lead structures of the second electrode plates being electrically connected together by respective ones of the electrical terminals to define a plurality of first polarity electrical terminals and a plurality of second polarity electrical terminals, respectively, located on the capacitor body; wherein

each of the first polarity terminals is disposed opposite to another of the first polarity terminals across the capacitor body and each of the second polarity terminals is disposed opposite to another of the second polarity terminals across the capacitor body; and

at least one of the lead structures of the first and second electrode plates have a length L and a width W and a ratio L/W is equal to about 3 or less.

2. The multi-layer capacitor according to claim 1, wherein the ratio L/W is equal to about 1.3 or less.

3. The multi-layer capacitor according to claim 1, wherein the ratio L/W is equal to about 0.4 or greater.

4. The multi-layer capacitor according to claim 1, wherein the ratio L/W is equal to or less than about 1.3 and greater than or equal to about 0.4.

5. The multi-layer capacitor according to claim 1, wherein the width W of at least one of the lead electrodes is different from that of the other lead electrodes.

6. The multi-layer capacitor according to claim 1, wherein lead electrodes are provided on each of a first pair of opposed sides of the capacitor body and a lead electrode is provided on each of a second pair of opposed sides of the capacitor body, and the width W of at least one of the lead electrodes provided on a respective one of the second pair of opposed sides of the capacitor body is wider than the lead electrodes disposed on each of the first pair of opposed sides of the capacitor body.

7. The multi-layer capacitor according to claim 1, wherein the lengths L of all of the lead electrodes are substantially equal to each other.

8. The multi-layer capacitor according to claim 1, wherein the capacitor body has a substantially rectangular shape.

9. The multi-layer capacitor according to claim 1, wherein the first polarity terminals and the second polarity terminals are provided only along the opposed side surfaces of the capacitor body.

10. The multi-layer capacitor according to claim 1, wherein at least one of the first polarity terminals is provided

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at one of the opposed end surfaces and one of the second polarity terminals is provided at another of the opposed end surfaces.

11. The multi-layer capacitor device according to claim 1, wherein the first polarity terminals are disposed opposite to each other across a width of the capacitor body.

12. The multi-layer capacitor device according to claim 1, wherein the second polarity terminals are disposed opposite to each other across a width of the capacitor body.

13. The multi-layer capacitor device according to claim 1, wherein each of the first polarity terminals is disposed opposite to another of the first polarity terminals only across a width of the capacitor body.

14. The multi-layer capacitor device according to claim 1, wherein each of the second polarity terminals is disposed opposite to another of the second polarity terminals only across a width of the capacitor body.

15. The multi-layer capacitor device according to claim 1, wherein each of the first polarity terminals and the corresponding another of the first polarity terminals are located at a common position along a length of the capacitor body.

16. The multi-layer capacitor device according to claim 1, wherein each of the second polarity terminals and the corresponding another of the second polarity terminals are located at a common position along a length of the capacitor body.

17. The multi-layer capacitor device according to claim 1, wherein each of the first polarity terminals is adjacent to one of the second polarity terminals and each of the second polarity terminals is adjacent to one of the first polarity terminals along each of the opposed side surfaces of the capacitor body.

18. The multi-layer capacitor device according to claim 1, wherein the electrical terminals extend to portions of the top and bottom surfaces.

19. The multi-layer capacitor device according to claim 1, wherein none of the first polarity terminals is adjacent to others of the first polarity terminals on the opposed side surfaces of the capacitor body.

20. The multi-layer capacitor device according to claim 1, wherein none of the second polarity terminals is adjacent to others of the second polarity terminals on the opposed side surfaces of the capacitor body.

21. The multi-layer capacitor device according to claim 1, wherein each of the first and second electrode plates includes two of the lead structures extending to each of the pair of opposed side surfaces of the capacitor body.

22. The multi-layer capacitor device according to claim 1, wherein each of the pair of opposed side surfaces of the capacitor body includes at least two of the electrical terminals disposed thereon.

23. The multi-layer capacitor device according to claim 1, wherein each of the pair of opposed side surfaces of the capacitor body includes at least four of the electrical terminals disposed thereon.

24. A multi-layer capacitor device according to claim 1, wherein the multi-layer capacitor device is arranged to define a decoupling capacitor for a multiprocessing unit.

25. A high frequency circuit comprising at least one multi-layer capacitor device according to claim 1.

26. The high frequency circuit according to claim 25, wherein the at least one multi-layer capacitor device is arranged to define one of a bypass capacitor and a decoupling capacitor.

27. A wiring substrate comprising at least one multi-layer capacitor device according to claim 1 mounted thereon.

28. A multi-layer capacitor device comprising:

a capacitor body including a pair of opposed side surfaces having continuously smooth surfaces and a pair of opposed end surfaces disposed between the pair of opposed side surfaces;

at least four electrical terminals disposed on each of the opposed side surfaces;

the capacitor body also including at least one first electrode plate having a substantially rectangular first main electrode portion with a plurality of first lead structures extending therefrom and at least one second electrode plate situated in opposed and spaced apart relation to the first electrode plate, the second electrode plate having a substantially rectangular second main electrode portion with a plurality of second lead structures extending therefrom, respective ones of the first lead structures being located adjacent respective ones of the second lead structures in an interdigitated arrangement and extending to respective ones of the electrical terminals; dielectric material disposed between each opposing set of first and second electrode plates; wherein

each of the lead terminals of the at least one first electrode plate being disposed opposite to another of the lead terminals of the at least one first electrode plate across the capacitor body and each of the lead terminals of the at least one second electrode plate being disposed opposite to another of the lead terminals of the at least one second electrode plate across the capacitor body; and

at least one of the lead structures of the first and second electrode plates have a length L and a width W and a ratio L/W is equal to about 3 or less.

29. The multi-layer capacitor device according to claim 28, wherein the ratio L/W is equal to about 1.3 or less.

30. The multi-layer capacitor device according to claim 28, wherein the ratio L/W is equal to about 0.4 or greater.

31. The multi-layer capacitor device according to claim 28, wherein the ratio L/W is equal to or less than about 1.3 and greater than or equal to about 0.4.

32. The multi-layer capacitor device according to claim 28, wherein the width W of at least one of the lead electrodes is different from that of the other lead electrodes.

33. The multi-layer capacitor device according to claim 28, wherein lead electrodes are provided on each of a first pair of opposed sides of the capacitor body and a lead electrode is provided on each of a second pair of opposed sides of the capacitor body, and the width W of at least one of the lead electrodes provided on a respective one of the second pair of opposed sides of the capacitor body is wider than the lead electrodes disposed on each of the first pair of opposed sides of the capacitor body.

34. The multi-layer capacitor device according to claim 28, wherein the lengths L of all of the lead electrodes are substantially equal to each other.

35. A multi-layer capacitor device according to claim 28, wherein each of the first polarity terminals is disposed opposite to another of the first polarity terminals across a width of the substantially rectangular capacitor body.

36. A multi-layer capacitor device according to claim 28, wherein each of the second polarity terminals is disposed opposite to another of the second polarity terminals across a width of the substantially rectangular capacitor body.

37. A multi-layer capacitor device according to claim 28, wherein each of the first polarity terminals is disposed opposite to another of the first polarity terminals across a

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width of the capacitor body and each of the second polarity terminals is disposed opposite to another of the second polarity terminals across a width of the capacitor body.

38. The multi-layer capacitor device according to claim 28, wherein the capacitor body has a substantially rectangular shape.

39. The multi-layer capacitor device according to claim 28, wherein the first polarity terminals and the second polarity terminals are provided only along the opposed side surfaces of the capacitor body.

40. The multi-layer capacitor device according to claim 28, wherein at least one of the first polarity terminals is provided at one of the opposed end surfaces and one of the second polarity terminals is provided at another of the opposed end surfaces.

41. The multi-layer capacitor device according to claim 28, wherein each of the first polarity terminals is adjacent to one of the second polarity terminals and each of the second polarity terminals is adjacent to one of the first polarity terminals along each of the opposed side surfaces of the capacitor body.

42. The multi-layer capacitor device according to claim 28, wherein none of the first polarity terminals is adjacent to others of the first polarity terminals on the opposed side surfaces of the capacitor body.

43. The multi-layer capacitor device according to claim 28, wherein none of the second polarity terminals is adjacent to others of the second polarity terminals on the opposed side surfaces of the capacitor body.

44. The multi-layer capacitor device according to claim 28, wherein each of the first and second electrode plates includes two of the lead structures extending to each of the pair of opposed side surfaces of the capacitor body.

45. The multi-layer capacitor device according to claim 28, wherein each of the pair of opposed side surfaces of the capacitor body includes at least two of the electrical terminals disposed thereon.

46. The multi-layer capacitor device according to claim 28, wherein each of the pair of opposed side surfaces of the capacitor body includes at least four of the electrical terminals disposed thereon.

47. A multi-layer capacitor device according to claim 28, wherein the multi-layer capacitor device is arranged to define a decoupling capacitor for a multiprocessing unit.

48. A high frequency circuit comprising at least one multi-layer capacitor device according to claim 28.

49. The high frequency circuit according to claim 48, wherein the at least one multi-layer capacitor device is arranged to define one of a bypass capacitor and a decoupling capacitor.

50. A wiring substrate comprising at least one multi-layer capacitor according to claim 28 mounted thereon.

51. A monolithic capacitor comprising:

a capacitor body having two opposed main surfaces and four side surfaces connected between the two main surfaces, said capacitor body including a plurality of dielectric layers extending in the direction in which the two opposed main surfaces extend, and at least one pair of first and second internal electrodes opposed to each other through one of the dielectric layers so as to define a capacitor unit, said capacitor body further including at least two first lead electrodes extending from one of the first internal electrodes to at least two positions on at least one of the side surfaces, and at least one second lead electrode extending from the second internal electrode to a position located between the positions to which the first lead electrodes extend;

first and second external terminal electrodes provided on the side surfaces onto which the first and second lead electrodes extend, and electrically connected to the first and second lead electrodes, respectively; wherein the ratio L/W of the length L to the width W of at least one of the first and second lead electrodes is within the range of about 0.4 to about 3.0

52. A monolithic capacitor according to claim 51, wherein the ratio L/W is in the range of about 0.4 to about 1.3.

53. A monolithic capacitor according to claim 51, wherein the first and second lead electrodes extend onto at least two of the side surfaces opposed to each other, respectively.

54. A monolithic capacitor according to claim 51, wherein at least one of the first and second lead electrodes extend onto the respective four side surfaces.

55. A monolithic capacitor according to claim 51, wherein the first lead electrodes and the second lead electrodes are alternately arranged as viewed in the peripheral directions of the main surfaces.

56. A monolithic capacitor according to claim 51, wherein the monolithic capacitor is arranged to define a decoupling capacitor connected to a power supply circuit of an microprocessing unit chip provided in a microprocessing unit.

57. A wiring substrate including the monolithic capacitor according to claim 51 mounted thereon.

58. A wiring substrate including the monolithic capacitor according to claim 57, further comprising an microprocessing unit chip of a microprocessing unit mounted on the wiring substrate.

59. A decoupling circuit including the monolithic capacitor according to claim 51.

60. A high frequency circuit including the monolithic capacitor according to claim 51.

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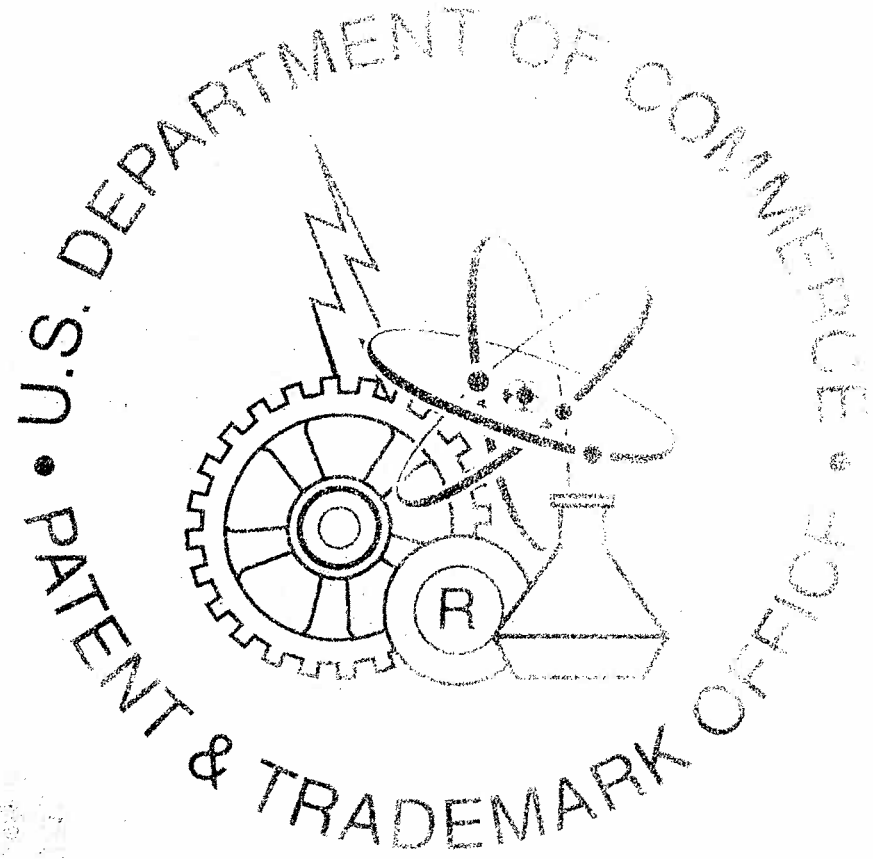


EXHIBIT A
32

EXHIBIT B

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U.S. PATENT: *6,377,439*

ISSUE DATE: *April 23, 2002*

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M. K. CARTER

Certifying Officer

US006377439B1

(12) **United States Patent**
Sekidou et al.

(10) **Patent No.: US 6,377,439 B1**
(45) **Date of Patent: Apr. 23, 2002**

(54) **ELECTRONIC MULTILAYER CERAMIC COMPONENT**

(75) Inventors: **Hiroshi Sekidou**, Takefu; **Yoshikazu Takagi**, Sabae; **Yasunobu Yoneda**, Takefu, all of (JP)

(73) Assignee: **Murata Manufacturing, Co.** (JP)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

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(22) Filed: **Jul. 13, 2000**

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(52) **U.S. Cl.** **361/303**; 361/306.3; 361/321.2; 428/210

(58) **Field of Search** 428/210; 361/303, 361/306.3, 311, 312, 313, 320, 321.1–321.5

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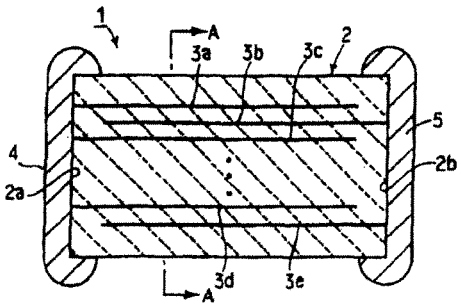
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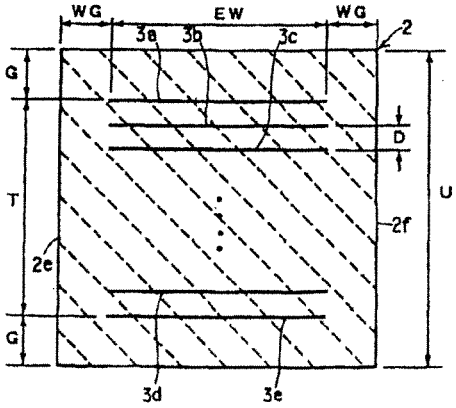
Primary Examiner—Cathy Lam
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(57) **ABSTRACT**

An electronic multilayer ceramic component is disclosed which is less susceptible to having a crack or delamination in a sintered ceramic block and has high thermal shock resistance, high humidity resistance, and high reliability. Dimensional parameters EW, WG, T, and G of the electronic multilayer ceramic component are determined such that the following conditions are satisfied: $WG/EW \geqq 0.3$; and $T/G \leqq 7.0$, where EW is the width of inner electrodes, WG is the width of a side gap region between the ends of the inner electrodes and one of side faces of a sintered ceramic block, T is the thickness of a region in which the plurality of inner electrodes are laminated, and G is the thickness of one of the outermost ceramic layers parallel to the plurality of inner electrodes and located outside the region in which the plurality of inner electrodes are laminated.

5 Claims, 2 Drawing Sheets





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FIG. 1A

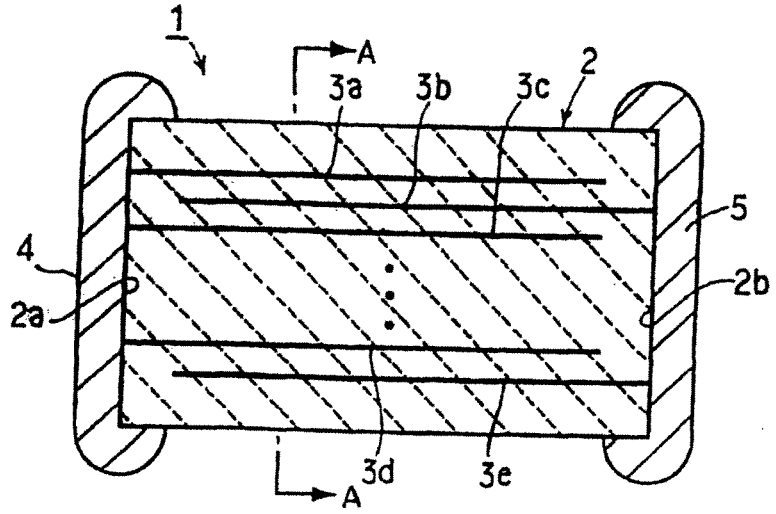
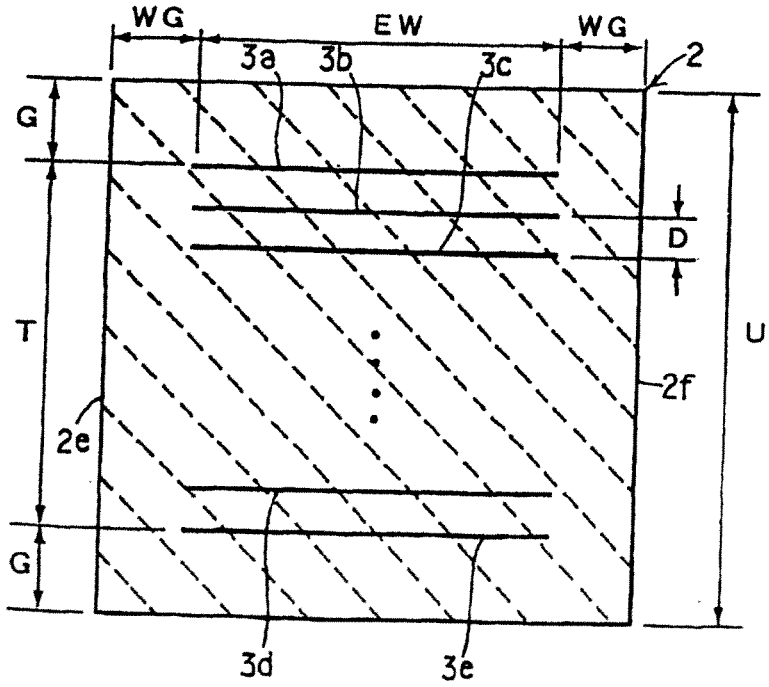
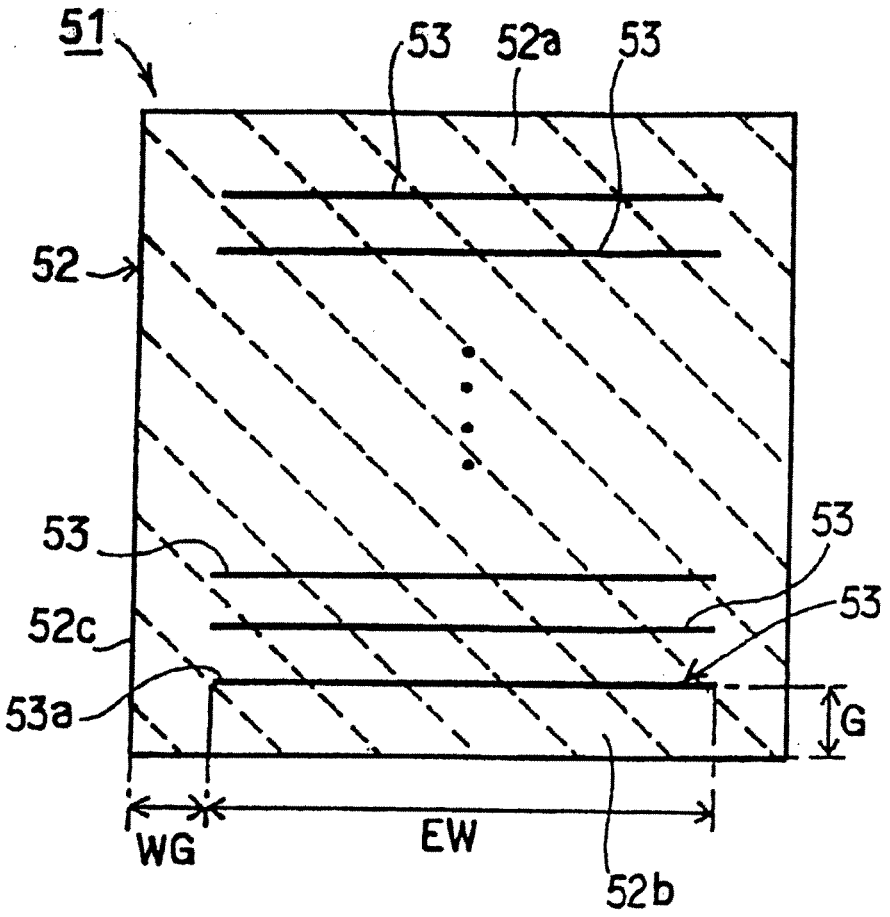


FIG. 1B



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FIG. 2



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ELECTRONIC MULTILAYER CERAMIC COMPONENT

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to an electronic multilayer ceramic component such as a multilayer capacitor, and more particularly to an electronic multilayer ceramic component in which the relationship between the size of a region in which inner electrodes are disposed in a multilayer fashion and the size of a part located outside that region is optimized.

2. Description of the Related Art

Electronic multilayer ceramic components, such as a multilayer capacitors are becoming increasingly smaller. Electronic multilayer ceramic components are constructed such that a plurality of inner electrodes are embedded in a sintered ceramic block, and outer electrodes are formed on outer side faces of the sintered ceramic block. With the reduction in size of electronic multilayer ceramic components, the size of the sintered ceramic block has become very small. For example, various types of sintered ceramic blocks with sizes smaller than 1.6 mm×0.8 mm×0.8 mm are commercially available.

In the case of multilayer ceramic capacitors, in order to reduce the size while maintaining the capacitance at a large value, the thickness of ceramic layers between adjacent inner electrodes is selected to be as small as 5 μm or 3 μm or still smaller, and as many as several hundred inner electrode layers are used.

FIG. 2 is a cross-sectional view of a conventional multilayer capacitor of the above-described type. As shown in FIG. 2, the multilayer capacitor 51 includes a plurality of inner electrodes 53 disposed in a sintered ceramic block 52 such that the plurality of inner electrodes 53 overlap with one another via ceramic layers. In order to achieve a greater capacitance with a smaller size, various attempts have been made to dispose a greater number of inner electrode layers within a sintered ceramic block with a smaller size.

To this end, the thickness G of outermost ceramic layers 52a and 52b parallel to the inner electrodes and located outside a region in which the plurality of inner electrodes 53 are laminated, is set to be as small as possible. However, if the thickness G of the outermost ceramic layers 52a and 52b is less than 100 μm, there is a possibility that the outermost ceramic layers 52a and 52b delaminate at an interface with an inner electrode 53 during a sintering process in which ceramic layers are sintered into a single block 52. For the above reason, the lower limit of the thickness of the outermost ceramic layers 52a and 52b is about 100 μm.

It is also required to minimize the width WG of a side gap region between side ends 53c of the inner electrodes 53 and an end face 52c of the sintered ceramic block 52. To this end, the ratio WG/EW is generally set to a value smaller than 0.3 where EW is the width of each inner electrode 53.

In the conventional multilayer capacitor 51, as described above, in order to obtain a greater capacitance with a smaller size, it has been attempted to minimize the thickness G of the outermost ceramic layers 52a and 52b and also minimize the ratio WG/EW.

However, when the size of the sintered ceramic block 52 is further reduced, if the ratio WG/EW is smaller than 0.3 and if G is set to be about 100 μm, various problems occur as described below. That is, during the sintering process for obtaining the sintered ceramic block 52, a density difference occurs between a ceramic region in which a plurality of inner electrodes 53 are laminated via ceramic layers and outer ceramic regions, that is, the outermost ceramic layers 52a and 52b. The density difference results in a stress which can produce cracks or delamination in the sintered ceramic block 52.

In a thermal shock test in which multilayer ceramic capacitors are subjected to abrupt temperature changes or in other reliability tests, a crack or delamination occurs in some samples due to the stress caused by the difference in thermal expansion coefficient between the inner electrodes and the ceramic.

Thus, in view of the above problems in the conventional technique, it is an object of the present invention to provide an electronic multilayer ceramic component which is less susceptible to having a crack or delamination and thus has high reliability and high resistance to thermal shock.

SUMMARY OF THE INVENTION

According to an aspect of the present invention, there is provided an electronic multilayer ceramic component comprising: a sintered ceramic block having a first end face, a second end face, upper and lower surfaces connecting said first and second end faces to each other, and a pair of side faces; a plurality of inner electrodes disposed in the sintered ceramic block such that the plurality of inner electrodes overlap in a thickness direction with one another via ceramic layers and such that each inner electrode extends from the first end face toward the second end face but not reaching the second end face or from the second end face toward the first end face but not reaching the first end face; and a first outer electrode and a second outer electrode formed such that the first and second end faces are covered with the first and second outer electrodes, respectively; wherein, when the width of the region in which the plurality of inner electrodes are disposed such that the inner electrodes overlap in the thickness direction with one another via ceramic layers is denoted by EW, the width of a side gap region between ends of the inner electrodes and one of side faces of the sintered ceramic block is denoted by WG, the thickness of a region in which the plurality of inner electrodes are disposed such that the inner electrodes overlap in the thickness direction with one another via ceramic layers is denoted by T, and the thickness of one of the outermost ceramic layers parallel to the plurality of inner electrodes and located outside the region in which the plurality of inner electrodes are disposed such that the inner electrodes overlap in the thickness direction with one another via ceramic layers is denoted by G, the following conditions are satisfied:

$$WG/EW \geq 0.3,$$

and

$$T/G \leq 7.0.$$

In the electronic multilayer ceramic component according to the present invention, the sintered ceramic block preferably has a size equal to or less than 1.6 mm in length, 0.8 mm in width, and 0.8 mm in thickness.

Furthermore, in the electronic multilayer ceramic component according to the present invention, the sintered ceramic block may be made of a dielectric ceramic material so that a multilayer capacitor is formed.

Other features and advantages of the present invention will become apparent from the following description of the invention which refers to the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1A is a cross-sectional view of a multilayer capacitor which is an electronic multilayer ceramic component

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according to an embodiment of the present invention, and FIG. 1B is a cross-sectional view taken along line A—A of FIG. 1A; and

FIG. 2 is a cross-sectional view of a sintered ceramic block of a multilayer capacitor according to a conventional technique.

DETAILED DESCRIPTION OF EMBODIMENTS OF THE INVENTION

The present invention is described in further detail below with reference to specific embodiments in conjunction with the accompanying drawings.

FIG. 1A is a cross-sectional view of a multilayer capacitor which is an electronic multilayer ceramic component according to an embodiment of the present invention. FIG. 1B is a cross-sectional view taken along line A—A of FIG. 1A.

In FIG. 1, a multilayer capacitor 1 includes a sintered ceramic block 2. The sintered ceramic block 2 is formed of a dielectric ceramic material such as barium titanate-based ceramic. A plurality of inner electrodes 3*a*–3*e* are disposed within the sintered ceramic block 2 wherein the inner electrodes 3*a*–3*e* overlap with one another in a thickness direction via ceramic layers. The plurality of inner electrodes 3*a*–3*e* alternately extend from a first end face 2*a* of the sintered ceramic block 2 or a second end face 2*b* toward the opposite end face but do not reach the opposite electrode. That is, each inner electrode extends starting from an end face opposite to an end face from which an inner electrode located at an immediately lower layer extends.

The sintered ceramic block 2 including the inner electrodes 3*a*–3*e* may be produced by multilayer capacitor production method known in the art.

The inner electrodes 3*a*–3*e* may be formed by baking a paste such as a Ag paste, Ag—Pd paste, or Ni paste.

A first outer electrode 4 and a second outer electrode 5 are formed such that the end faces 2*a* and 2*b* of the sintered ceramic block 2 are covered with the first and second outer electrodes 4 and 5, respectively. The outer electrodes 4 and 5 may be formed by means of coating and baking of a conductive paste. Alternatively, the outer electrodes 4 and 5 may be formed by means of evaporation, plating, or other techniques. Still, alternatively, the outer electrodes 4 and 5 may be produced in the form of a multilayer structure by first forming an electrode film by means of coating and baking of a conductive paste and then forming a plated layer thereon.

The multilayer capacitor 1 according to the present embodiment is characterized, as shown in FIG. 1B, in that when the width of the inner electrodes 3*a*–3*e* in the region in which the plurality of inner electrodes 3*a*–3*e* are laminated via ceramic layers is denoted by EW, the width of a side gap region between ends of the inner electrodes 3*a*–3*e* and one of side faces 2*e* and 2*f* of the sintered ceramic block 2 is denoted by WG, the thickness of a region in which the plurality of inner electrodes 3*a*–3*e* are laminated via ceramic layers is denoted by T, and the thickness of one of the outermost ceramic layers parallel to the plurality of inner electrodes and located outside the region in which the plurality of inner electrodes are laminated via ceramic layers is denoted by G, the following conditions are satisfied: $WG/EW \geq 0.3$, and $T/G \leq 7.0$.

In the multilayer capacitor 1 according to the present embodiment, because $WG/EW \geq 0.3$ and $T/G \leq 7.0$, the multilayer capacitor 1 is less susceptible to having a crack or delamination after the baking process for sintering into the ceramic block 2 even when the sintered ceramic block 2 has a very small size such as 1.6 mm in length, 1.6 mm in width, and 0.8 mm in thickness or less. Furthermore, the multilayer capacitor 1 is less susceptible to having a crack or delamination in a thermal shock test. That is, the multilayer capacitor 1 has high reliability. The present embodiment is described in further detail below with reference to specific experimental examples.

EXPERIMENTAL EXAMPLE 1

Sintered ceramic blocks 2 formed of barium titanate-based dielectric ceramic with a length of 1.6 mm, a width of 0.8 mm, and a thickness of 0.8 mm were prepared, wherein inner electrodes 3*a*–3*e* in each sintered ceramic block 2 were formed of Ni. Herein, the number of inner electrode layers was set to 120 to 170, and the distance D between adjacent inner electrodes (FIG. 1B) was set to 3.0 μm. A Cu paste was coated on both end faces of the sintered ceramic block 2 and then baked, thereby forming outer electrodes 4 and 5. In the above process, the ratio WG/EW and the ratio T/G were set to various values as shown in Table 1 thereby obtaining multilayer capacitors 1.

The multilayer capacitors 1 produced in the above-described manner were subjected to (1) a humidity load test (reliability test) and (2) a thermal shock test, and the results were analyzed as described below.

(1) Humidity load test (reliability test) The multilayer capacitors were maintained in an atmosphere of 100% relative humidity at 130° C. After that, the insulation resistance was measured. Those samples having an insulation resistance less than 10^6 Ω were regarded as failed.

(2) Thermal shock test The multilayer capacitors were put into a solder bath maintained at 350° C. without preheating them and dipped therein for 3 sec. After that, the multilayer capacitors were taken out from the solder bath and observed via a microscope to determine whether cracking occurred in the sintered ceramic blocks.

The result is shown in Table 1.

TABLE 1

SAMPLE TYPE	WG/EW	T/G	NUMBER OF FAILED SAMPLES IN HUMIDITY LOAD TEST	NUMBER OF FILES SAMPLES IN THERMAL SHOCK TEST
1	0.10	10.0	5/72	14/50
2	0.15	9.0	0/72	3/50
3	0.30	7.0	0/72	0/50
4	0.50	5.0	0/72	0/50
5	0.70	3.0	0/72	0/50

As can be seen from Table 1, in the multilayer capacitors of type 1 with WG/EW=0.10 and T/G=10.0, a considerably large relative number of samples failed to pass the humidity load test and the thermal shock test.

All multilayer capacitors of type 2 with WG/EW=0.15 and T/G=9.0 passed the humidity load test. However, some of them failed to pass the thermal shock test.

On the other hand, all multilayer capacitors of types 3 to 5, which fall within the scope of the present invention, passed both the humidity load test and the thermal shock test.

EXPERIMENTAL EXAMPLE 2

Multilayer capacitors of types 6–10 with various values of WG/EW and T/G shown in Table 2 were produced in the same manner as in Experimental Example 1 except that the

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outer size of sintered ceramic blocks were set to 1.0 mm in length, 0.5 mm in width, and 0.5 mm in thickness. The obtained multilayer capacitors were evaluated in the same manner as in Experimental Example 1. The result is shown in Table 2.

TABLE 2

SAMPLE TYPE	WG/EW	T/G	NUMBER OF FAILED SAMPLES IN HUMIDITY LOAD TEST	NUMBER OF FILES SAMPLES IN THERMAL SHOCK TEST
6	0.10	10.0	4/72	10/50
7	0.15	9.0	0/72	2/50
8	0.30	7.0	0/72	0/50
9	0.50	5.0	0/72	0/50
10	0.70	3.0	0/72	0/50

As can be seen from Table 2, a considerably large relative number of multilayer capacitors of type 6 with WG/EW=0.10 and T/G=10.0 failed to pass the humidity load test and the thermal shock test. All multilayer capacitors of type 2 with WG/EW=0.15 and T/G=9.0 passed the humidity load test. However, some of them failed to pass the thermal shock test.

On the other hand, all multilayer capacitors of types 8 to 10, which fall within the scope of the present invention, passed both the humidity load test and the thermal shock test.

From the results shown in Tables 1 and 2, it can be seen that multilayer capacitors having high performance in both thermal shock resistance and reliability can be realized for both sizes 1.6 mm×0.8 mm×0.8 mm and 1.0 mm×0.5 mm×0.5 mm, if the ratio WG/EW is set to 0.3 or greater and the ratio T/G is set to 7.0 or smaller according to the present invention.

The reliability and the thermal shock resistance become high with increasing ratio WG/WE, that is, increasing ratio of the side gap width to the width of inner electrodes, and thus there is no upper limit in ratio WG/EW to achieve the objects of the present invention. However, the increase in WG/EW results in an increase in the width of the sintered ceramic block of multilayer capacitor. Thus, in order to meet the requirement for smaller sizes, it is desirable that WG/EW be selected to be equal to or less than 1.1.

The present invention has been described above with reference to multilayer capacitors. The present invention is also applicable to a wide variety of other electronic multilayer ceramic components having a sintered ceramic block in which a plurality of inner electrodes and ceramic layers are laminated via ceramic layers. Some examples of such components are multilayer varistors and multilayer thermistors.

As can be understood from the above description, the present invention has great advantages. That is, in the electronic multilayer ceramic component according to the present invention, the ratio WG/EW is selected to be equal to or greater than 0.3 and the ratio T/G is selected to be equal to or smaller than 7.0, thereby reducing the stress which occurs, when subjected to a thermal shock, due to the difference in thermal expansion coefficient between the inner electrodes and the ceramic, and thus enhancing the thermal shock resistance and reliability even in the case where the sintered ceramic block has a reduced size. Thus, the electronic multilayer component according to the present invention is less susceptible to having a crack or delamination and has excellent reliability.

In the present invention, as described above, because the thermal shock resistance and the reliability are enhanced by setting the ratio WG/EW to a value equal to or greater than 0.3 and the ratio T/G to a value equal or smaller than 7.0, it becomes possible to realize an electronic multilayer ceramic component having higher thermal shock resistance and higher reliability than can be achieved by conventional techniques, even when a sintered ceramic block having a very small size such as 1.6 mm in length, 0.8 mm in width, and 0.8 mm in thickness, or less, is employed.

According to a preferable aspect of the present invention, the above-described sintered ceramic block is made of a dielectric ceramic material, which makes it possible to realize a ceramic capacitor having high thermal shock resistance, high humidity resistance, and high reliability.

Although the present invention has been described in relation to particular embodiments thereof, many other variations and modifications and other uses will become apparent to those skilled in the art. It is preferred, therefore, that the present invention be limited not by the specific disclosure herein, but only by the appended claims.

What is claimed is:

1. An electronic multilayer ceramic component comprising:

a sintered ceramic block having a first end face, a second end face, upper and lower surfaces connecting said first and second end faces to each other, and a pair of side faces;

a plurality of inner electrodes disposed in the sintered ceramic block such that said plurality of inner electrodes overlap, in a thickness direction, with one another via ceramic layers and such that each said inner electrode extends from said first end face toward said second end face but not reaching said second end face or from said second end face toward said first end face but not reaching said first end face; and

a first outer electrode and a second outer electrode formed such that said first and second end faces are covered with said first and second outer electrodes, respectively;

wherein, when the width of the region in which said plurality of inner electrodes are disposed such that said inner electrodes overlap in the thickness direction with one another via ceramic layers is denoted by EW, the width of a side gap region between ends of said inner electrodes and one of side faces of said sintered ceramic block is denoted by WG, the thickness of a region in which said plurality of inner electrodes are disposed such that said inner electrodes overlap in the thickness direction with one another via ceramic layers is denoted by T, and the thickness of one of the outermost ceramic layers parallel to said plurality of inner electrodes and located outside the region in which said plurality of inner electrodes are disposed such that said inner electrodes overlap in the thickness direction with one another via ceramic layers is denoted by G, the following conditions are satisfied:

WG (the width of the side gap region between the ends of the inner electrodes and one of the side faces)/EW≧0.3, and

T/G (the thickness of the one outermost ceramic layer)≦7.0.

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2. An electronic multilayer ceramic component according to claim 1, wherein said sintered ceramic block has a size equal to or less than 1.6 mm in length, 0.8 mm in width, and 0.8 mm in thickness.

3. An electronic multilayer ceramic component according to claim 1 or 2, wherein said sintered ceramic block is made of a dielectric ceramic material and wherein a multilayer capacitor is formed.

4. An electronic multilayer ceramic component according to claim 3, wherein said dielectric ceramic material is a barium-titanic-based ceramic layer.

5. An electronic multilayer ceramic component according to claim 1 or 2, wherein the thickness of each outermost ceramic layer is G.

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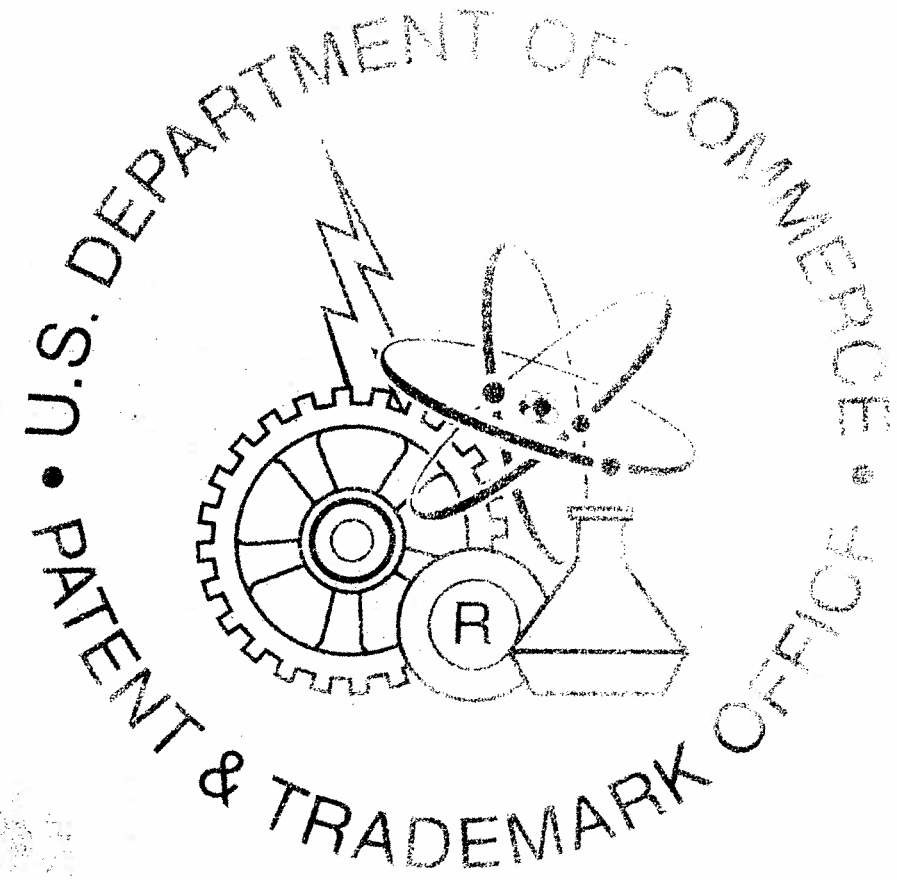

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U.S. PATENT: *6,243,254*
ISSUE DATE: *June 05, 2001*

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EXHIBIT C
42

US006243254B1

(12) **United States Patent**
Wada et al.

(10) **Patent No.: US 6,243,254 B1**
(45) **Date of Patent: Jun. 5, 2001**

(54) **DIELECTRIC CERAMIC COMPOSITION AND LAMINATED CERAMIC CAPACITOR USING THE SAME**

(75) Inventors: **Nobuyuki Wada**, Shiga-ken; **Masamitsu Shibata**, Kyoto; **Takashi Hiramatsu**, Shiga-ken; **Yukio Hamaji**, Otsu, all of (JP)

(73) Assignee: **Murata Manufacturing Co., Ltd.** (JP)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **09/369,988**

(22) Filed: **Aug. 6, 1999**

(30) **Foreign Application Priority Data**

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(51) **Int. Cl.**[7] **H01G 4/06**
(52) **U.S. Cl.** **361/311**; 361/321.2; 361/321.5; 501/134
(58) **Field of Search** 361/321.1, 321.2, 361/321.3, 321.4, 321.5, 322, 311–313; 501/134–139

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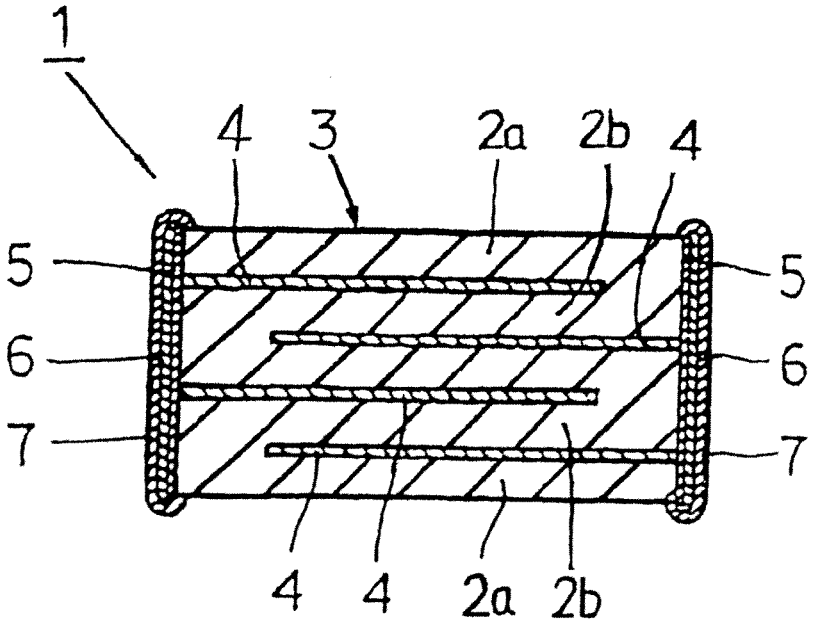
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Primary Examiner—Anthony Dinkins
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(57) **ABSTRACT**

Provided is a highly reliable laminated ceramic capacitor in which decrease of dielectric constant under a high electric field is small and which satisfies the B-grade and X7R grade characteristics, using Ni for the inner electrodes, wherein the dielectric material contains about 0.2 to 5.0 parts by weight of Li_2O—$(Si, Ti)_2$—MO oxides (MO is at least one of the compounds of Al_2O_3 and ZrO_2) or SiO_2—TiO_2—XO oxides (XO is at least one of the compounds of BaO, CaO, SrO, MgO, ZnO and MnO) relative to 100 parts by weight of a principal component represented by $(Ba_{1-x}Ca_xO)_mTiO_2+\alpha Re_2O_3+\beta MgO+\gamma MnO$ (Re_2O_3 represents at least one of Y_2O_3, Gd_2O_3, Tb_2O_3, Dy_2O_3, Ho_2O_3, Er_2O_3 and Yb_2O_3).

20 Claims, 5 Drawing Sheets



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FIG. 1

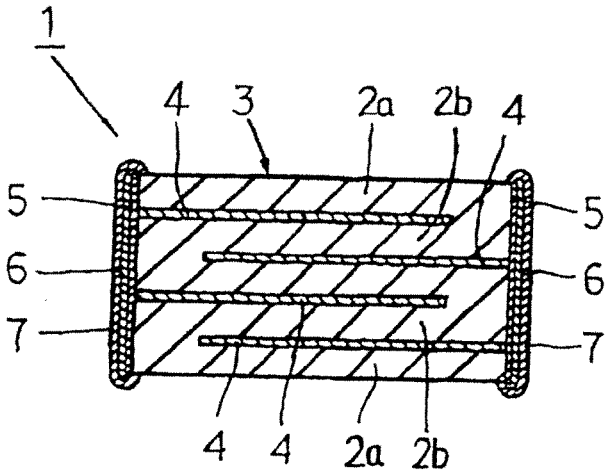


FIG. 2

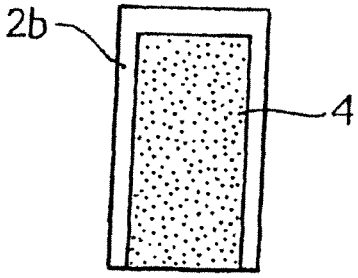
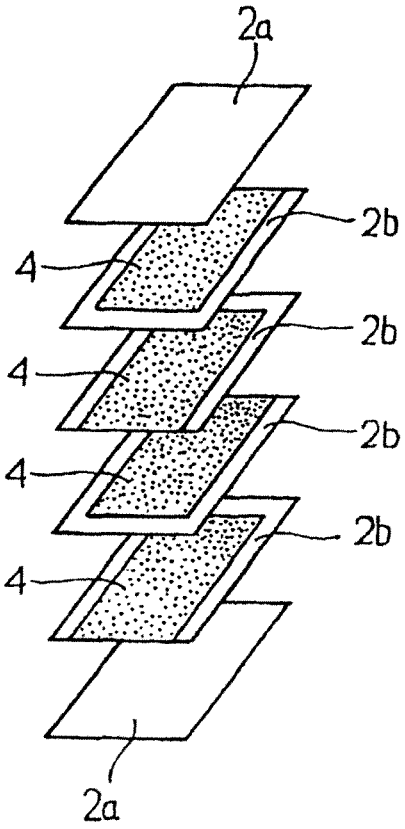


FIG. 3



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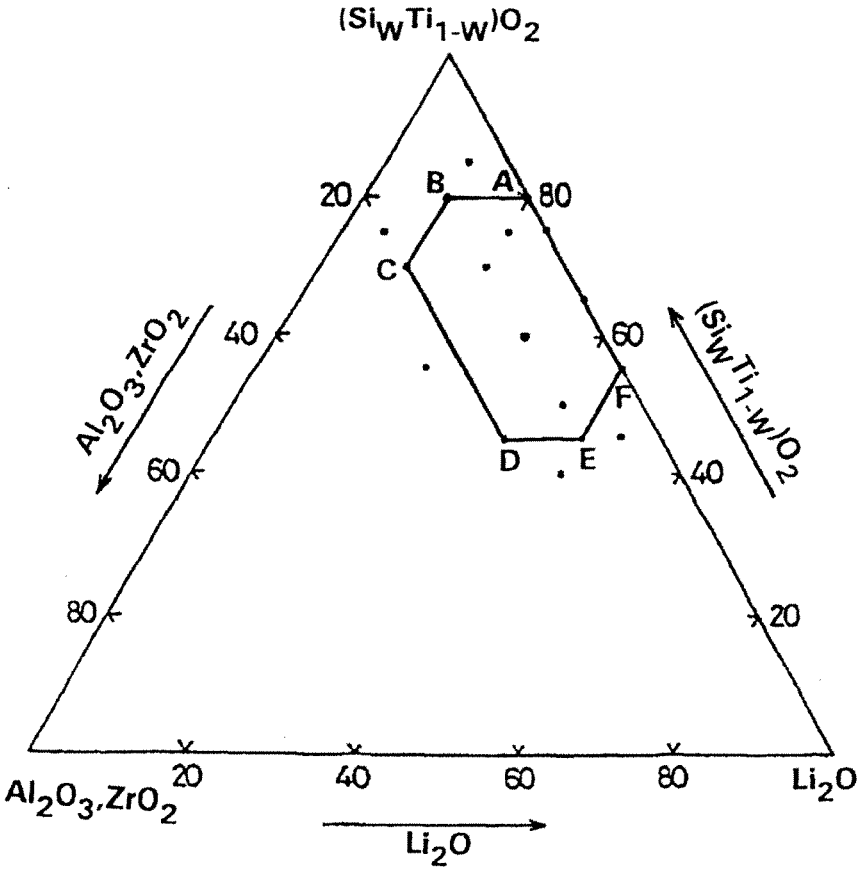


FIG. 4

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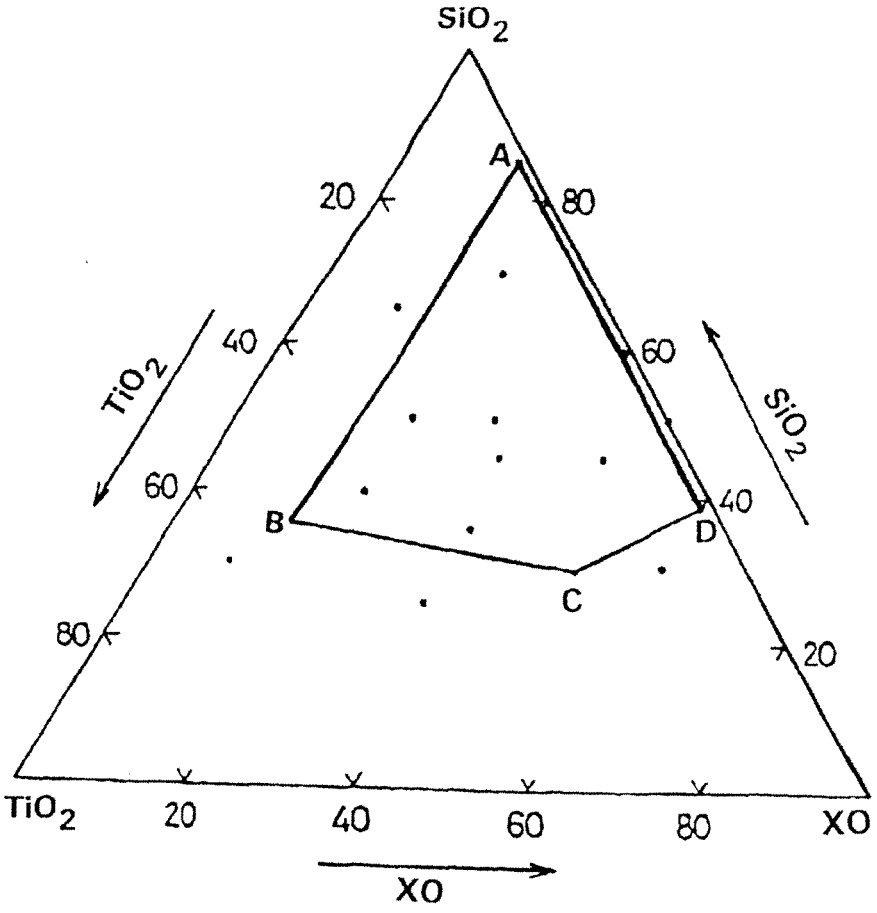


FIG. 5

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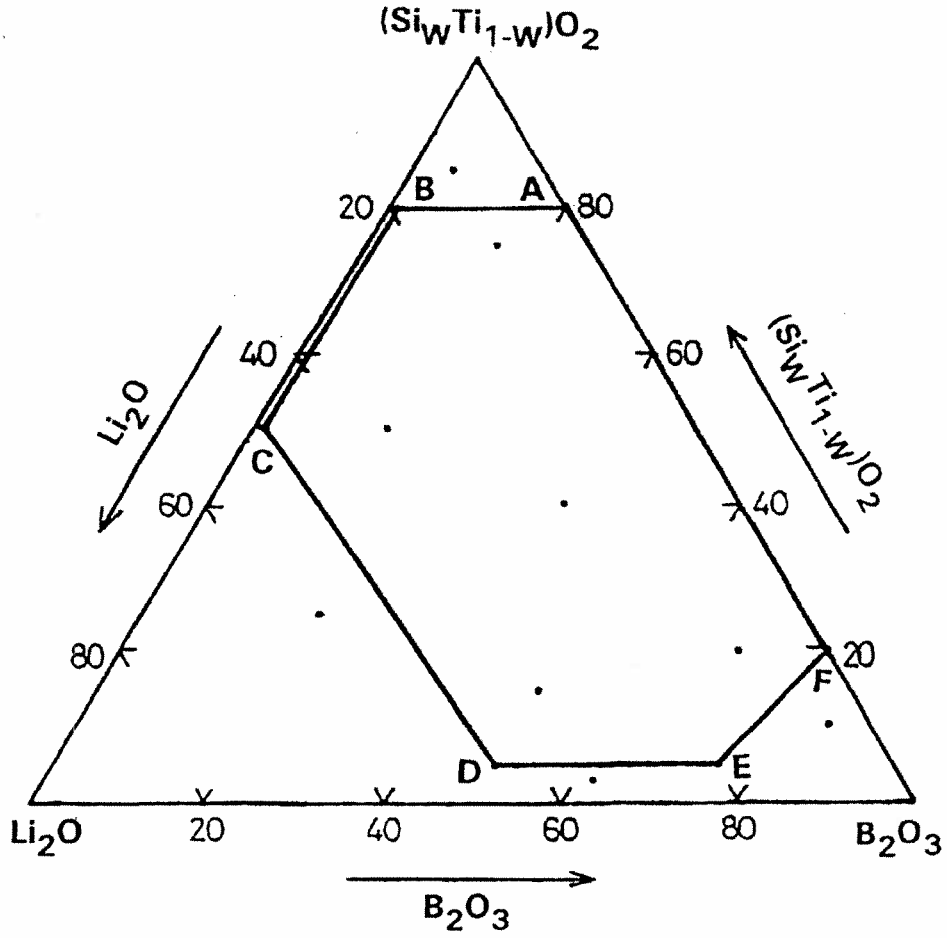


FIG. 6

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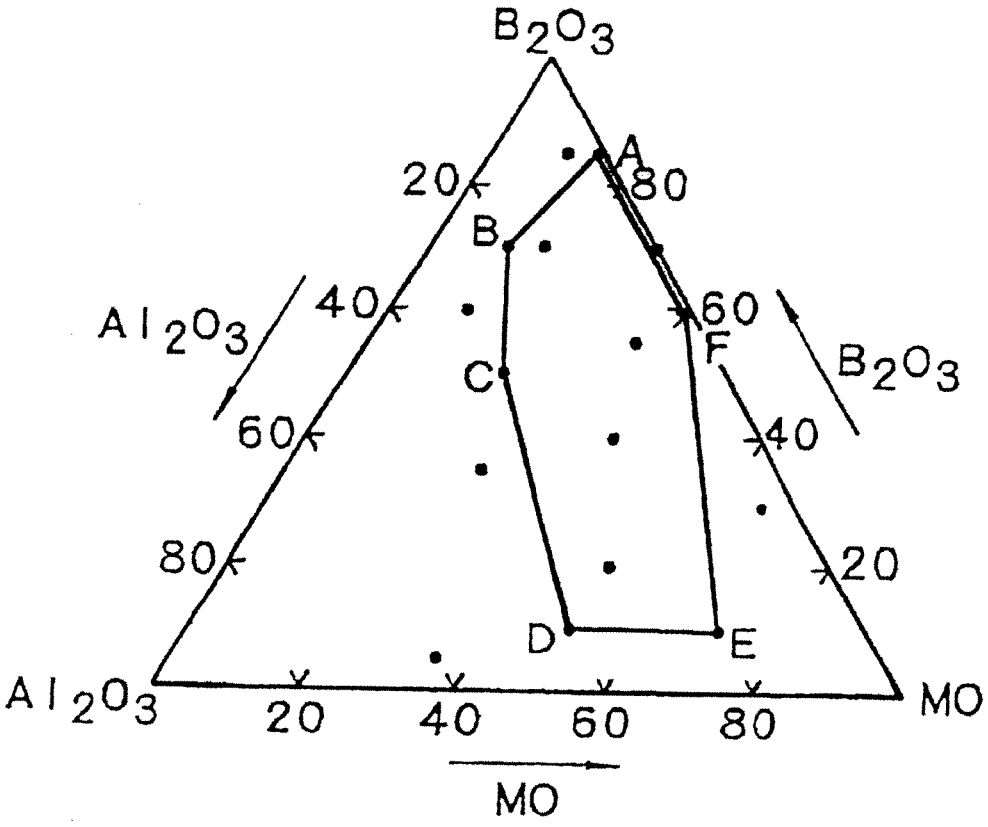


FIG. 7

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DIELECTRIC CERAMIC COMPOSITION AND LAMINATED CERAMIC CAPACITOR USING THE SAME

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to a dielectric ceramic composition and a laminated ceramic capacitor using the same, especially to a ceramic capacitor having inner electrodes made of Ni.

2. Description of the Related Art

Ceramic layers and inner electrode metal layers are alternately stacked in the laminated ceramic capacitor. A cheap base metal such as Ni has been recently used for the inner electrodes in place of expensive noble metals such as Ag and Pd for reducing the production cost. When Ni is used for the electrodes, the capacitor should be fired in a reducing atmosphere where Ni is not oxidized. However, ceramics comprising barium titanate as a principal component may be endowed with semiconductive properties when the ceramics are fired in a reducing atmosphere. Accordingly, as disclosed for example in Japanese Examined Patent Publication No. 57-42588, a dielectric material in which the ratio between the barium site and titanium site in the barium titanate solid solution is adjusted to be larger than the stoichiometric ratio has been developed. This allows the laminated ceramic capacitor using Ni as electrodes to be practically used, thereby expanding its production scale.

Since electronic parts have been rapidly miniaturized with the recent advance of electronics, small size ceramic capacitors with large capacitance as well as temperature stability of electrostatic capacitance are required. The ceramic capacitors having the Ni electrodes are also under the same circumstances.

For complying with the requirements of large capacitance and small size, the dielectric ceramics should be made to be thinner and multi-layered. However, much higher voltage is impressed on the dielectric material when the dielectric ceramic layer is thinned, often causing troubles such as decrease of dielectric constant, increase of temperature dependency of the electrostatic capacitance and deteriorated stability of other characteristics when conventional dielectric materials are used. Especially, when the thickness of the dielectric layer is reduced to 5 μm or less, 10 or less ceramic particles are contained between the inner electrodes, making it difficult to assure a stable quality.

Making the dielectric layer thin is accompanied by other problems. Solder plating layers as external electrodes are usually formed on the baked electrodes of a conductive metal powder in order to comply with automatic packaging of the laminated ceramic capacitor. Therefore, the plating layer is generally formed by electroplating. Oxides containing boron or a glass is added, on the other hand, into some dielectric ceramics as a sintering aid. However, the dielectric ceramic using these additives has so poor resistance against plating that characteristics of the laminated ceramic capacitor may be deteriorated by dipping it into a plating solution. It has been a problem that reliability is markedly decreased in the ceramic capacitor having thin dielectric ceramic layers.

SUMMARY OF THE INVENTION

Accordingly, the object of the present invention is to provide a laminated ceramic capacitor with high reliability and large capacitance especially using Ni for inner electrodes, wherein dielectric constant is not decreased exhibiting a stable electrostatic capacitance even when the dielectric ceramic layers are thinned, and temperature characteristics of the electrostatic capacitance satisfy the B-grade characteristics prescribed in the JIS standard and the X7R-grade characteristics prescribed in the EIA standard.

The present invention also provides a highly reliable laminated ceramic capacitor with large capacitance made of thin dielectric ceramic layers having an excellent plating solution resistance.

In one aspect, the present invention provides a laminated ceramic capacitor provided with a plurality of dielectric ceramic layers, inner electrodes formed between the dielectric ceramic layers and external electrodes being in electrical continuity with the inner electrodes, the dielectric ceramic layer being represented by the following formula:

$$(Ba_{1-x}Ca_xO)_mTiO_2+\alpha Re_2O_3+\beta MgO+\gamma MnO$$

(Re_2O_3 is at least one or more of the compounds selected from Y_2O_3, Gd_2O_3, Tb_2O_3, Dy_2O_3, Ho_2O_3, Er_2O_3 and Yb_2O_3, α,β γ, m and x representing molar ratio in the range of $0.001 \leqq \alpha \leqq 0.10$, $0.001 \leqq \beta \leqq 0.12$, $0.001 < \gamma \leqq 0.12$, $1.000 < m \leqq 1.035$ and $0.005 < x \leqq 0.22$), and containing about 0.2 to 5.0 parts by weight of either a first sub-component or a second sub-component relative to 100 parts by weight of a principal component containing about 0.02% by weight or less of alkali-metal oxides in $(Ba_{1-x}Ca_xO)_mTiO_2$ as a starting material to be used for the dielectric ceramic layer, wherein the first sub-component is a Li_2O—$(Si,Ti)O_2$—MO based oxide (MO is at least one of the compound selected from Al_2O_3 and ZrO_2) and the second sub-component is a SiO_2—TiO_2—XO based oxide (XO is at least one of the compound selected from BaO, CaO, SrO, MgO, ZnO and MnO). The inner electrodes are preferably composed of nickel or a nickel alloy.

The material $(Ba_{1-x}Ca_xO)_mTiO_2$ to be used for the dielectric ceramic layer preferably has a mean particle size of about 0.1 to 0.7 μm.

The first sub-component represented by $xLiO_2$—$y(Si_wTi_{1-w})Q_2$—zMO (x, y and z are represented by molar percentage (mol %) and w is in the range of $0.30 \leqq w \leqq 1.0$) may be within the area surrounded by the straight lines connecting between the succeeding two points represented by A (x=20, y=80, z=0), B (x=10, y=80, z=10), C (x=10, y=70, z=20), D (x=35, y=45, z=20), E (x=45, y=45, z=10) and F (x=45, y=55, z=0) or on the lines in a ternary composition diagram having apexes represented by each component LiO_2, $(Si_wTi_{1-w})O_2$ and MO provided that when the component is on the line A–F, w is in the range of $0.3 \leqq w \leqq 1.0$.

The second sub-component represented by $xSiO_2$—$yTiO_2$—zXO (x, y and z are represented by mol %) may be within the area surrounded by the straight lines connecting between the succeeding two points represented by A (x=85, y=1, z=14), B (x=35, y=51, z=14), C (x=30, y=20, z=50) and D (x=39, y=1, z=60) or on the lines in a ternary composition diagram having apexes represented by each component SiO_2, TiO_2 and XO.

At least one of the compounds Al_2O_3 and ZrO_2 are contained with a combined amount of about 15 parts by weight (ZrO_2 is about 5 parts by weight or less) in the second sub-component relative to 100 parts by weight of the SiO_2—TiO_2—XO based oxide.

The external electrodes are composed of sintered layers of a conductive metal powder or a conductive metal powder supplemented with a glass frit.

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Alternately, the external electrodes are composed of sintered layers of a conductive metal powder or a conductive metal powder supplemented with a glass frit, and plating layers formed thereon.

It is preferable to use the ceramic having the composition to be described hereinafter in order to improve the plating resistance. The dielectric ceramic layer in the laminated ceramic capacitor is represented by the following formula:

$$(Ba_{1-x}Ca_xO)_mTiO_2+\alpha Re_2O_3+\beta MgO+\gamma MnO$$

(Re_2O_3 is at least one or more of the compounds selected from Y_2O_3, Gd_2O_3, Tb_2O_3, Dy_2O_3, Ho_2O_3, Er_2O_3 and Yb_2O_3, α, β γ, m and x representing molar ratio in the range of $0.001 \leqq \alpha \leqq 0.10$, $0.001 \leqq \beta 0.12$, $0.001 < \gamma \leqq 0.12$, $1.000 < m \leqq 1.035$ and $0.005 < x \leqq 0.22$), and contains about 0.2 to 5.0 parts by weight of the compound selected from either a first sub-component, a second sub-component or a third sub-component relative to 100 parts by weight of a principal component containing about 0.02% by weight or less of alkali-metal oxides in $(Ba_{1-x}Ca_x)_mTiO_2$ as a starting material to be used for the dielectric ceramic layers, wherein the first sub-component is a Li_2O—B_2O_3—(Si, Ti)O_2 based oxide, the second sub-component is a Al_2O_3—MO—B_2O_3 based oxide (MO is at least one of the compound selected from BaO, CaO, SrO, MgO, ZnO and MnO) and the third sub-component is SiO_2.

The first sub-component represented by $xLiO_2$—YB_2O_3—$Z(Si_wTi_{1-w})O_2$ (x, y and z are represented by mol % and w is in the range of $0.30 \leqq w \leqq 1.0$) is preferably within the area surrounded by the straight lines connecting between the succeeding two points represented by A (x=0, y=20, z=80), B (x=19, y=1, z=80), C (x=49, y=1, z=50), D (x=45, y=50, z=5), E (x=20, y=75, z=5) and F (x=0, y=80, z=20) or on the lines in a ternary composition diagram having apexes represented by each component LiO_2, B_2O_3 and $(Si_wTi_{1-w})O_2$.

At least one of the compounds Al_2O_3 and ZrO_2 are contained in a combined amount of about 20 parts by weight or less (ZrO_2 is about 10 parts by weight or less) in the first sub-component relative to 100 parts by weight of the Li_2O—B_2O_3—(Si, Ti)O_2 based oxide.

The second sub-component represented by xAl_2O_3—yMO—zB_2O_3 (x, y and z are represented by mol %) is preferably within the area surrounded by the straight lines connecting between the succeeding two points represented by A (x=1, y=14, z=85), B (x=20, y=10, z=70), C (x=30, y=20, z=50), D (x=40, y=50, z=10), E (x=20, y=70, z=10) and F (x=1, y=39, z=60) or on the lines in a ternary composition diagram having apexes represented by each component Al_2O_3, yMO and zB_2O_3.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a cross section showing one example of the laminated ceramic capacitor according to the present invention.

FIG. 2 is a plane view showing the dielectric ceramic layer part having the inner electrodes in the laminated ceramic capacitor shown in FIG. 1.

FIG. 3 is a disassembled perspective view showing the laminated ceramic part in the laminated ceramic capacitor shown in FIG. 1.

FIG. 4 is a ternary composition diagram of the LiO_2—$(Si_wTi_{w-w})O_2$—MO based oxide.

FIG. 5 is a ternary composition diagram of the SiO_2—TiO_2—XO based oxide.

FIG. 6 is a ternary composition diagram of the Li_2O—B_2O_3—$(Si_wTi_{1-w})O_2$ based oxide.

FIG. 7 is a ternary composition diagram of the Al_2O_3—MO—B_2O_3 based oxide.

DESCRIPTION OF THE PREFERRED EMBODIMENT

The laminated ceramic capacitor according to the present invention will now be explained in more detail with reference to the accompanying drawings.

FIG. 1 is a cross section showing one example of the laminated ceramic capacitor according to the present invention, FIG. 2 is a plane view showing the dielectric ceramic layer part having the inner electrodes in the laminated ceramic capacitor shown in FIG. 1 and FIG. 3 is a disassembled perspective view showing the laminated ceramic part in the laminated ceramic capacitor shown in FIG. 1. In the laminated ceramic capacitor **1** according to the present invention as shown in FIG. 1, outer electrodes **5**, and first plating layers **6** and second plating layers **7** if necessary, are formed on both ends of a ceramic laminated body **3** obtained by laminating a plurality of dielectric ceramic layers **2***a* and **2***b* via inner electrodes **4**.

The dielectric ceramic layers **2***a* and **2***b* are composed of a dielectric ceramic composition having as principal components barium calcium titanate $(Ba_{1-x}Ca_x)_mTiO_2$, at least one compound selected from Y_2O_3, Gd_2O_3, Tb_2O_3, Dy_2O_3, Ho_2O_3, Er_2O_3 and Yb_2O_3, MgO and MnO, and containing as sub-components either a Li_2O—(Si, Ti)O_2—MnO based oxide (MO is at least one of the compounds selected from Al_2O_3 and ZrO_2) or a SiO_2—TiO_2—XO based oxide (XO is at least one of the compounds selected from BaO, CaO, SrO, MgO, ZnO and Mno). The composition described above allows a laminated ceramic capacitor with high reliability and excellent insulating strength to be obtained, wherein the ceramic capacitor can be fired without endowing it with semiconductive properties even by firing in a reducing atmosphere, the temperature characteristics of the electrostatic capacitance satisfy the B-grade characteristics prescribed in the JIS standard and the X7R-grade characteristics prescribed in the EIA standard and the ceramic capacitor has a high insulation resistance at room temperature and at high temperatures.

Also, a highly reliable laminated ceramic capacitor, whose dielectric constant is less affected by variation of electric field even when the dielectric ceramic layers are thinned and magnetic field strength is increased, can be obtained by using a barium calcium titanate material with a mean particle size of about 0.1 to 0.7 μm. The dielectric ceramic assumes a core-shell structure in which Re components (Re is at least one or more of the elements selected from Y, Gd, Tb, Dy, Ho, Er and Yb) are distributed in the vicinity of and at grain boundaries by diffusion during firing.

A highly reliable dielectric material can be also obtained by using a barium calcium titanate containing about 0.02% by weight or less of alkali metal oxides such as Na_2O and K_2O.

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The ratio (n) of (barium+calcium)/titanium in the barium calcium titanate material is not specifically limited. However, the ratio (n) in the range from about 0.990 to 1.035 is desirable when stability for producing powder materials is taken into consideration.

Li_2O—(Si, Ti)O_2—MO based oxides contained in the principal components described above serve for firing the dielectric ceramics at a relatively low temperature of 1250° C., improving high temperatures load characteristics. SiO_2—TiO_2—XO based oxides included in the principal components also allow the sintering property to be excellent along with improving the voltage load characteristics at a high temperature and humidity. Further, a higher insulation resistance can be obtained by allowing Al_2O_3 and ZrO_2 to be contained in the SiO_2—TiO_2—XO based oxides.

The inner electrode **4** is composed of base metals such as nickel or a nickel alloy.

The outer electrode **5** is composed of a sintered layer of various conductive metals such as Ag, Pd, Ag—Pd, Cu or a Cu alloy, or a sintered layer prepared by blending the foregoing conductive metal powder with various glass fits such as B_2O_3—Li_2O—SiO_2—BaO based, B_2O_3—SiO_2—BaO based, Li_2O—SiO_2—BaO based or B_2O_3—SiO_2—ZnO based glass frit. It is possible to form a plating layer on this sintered layer. Either a first plating layer **6** comprising Ni, Cu or a Ni—Cu alloy may be merely formed or a second plating layer **7** comprising tin or a solder may be formed on the first plating layer.

The method for producing the laminated ceramic capacitor according to the present invention will be described hereinafter in the order of its production steps with reference to FIGS. **1** to **3**.

Powder materials produced by a solid phase method for allowing oxides and carbonates to react at a high temperature or a powder material produced by a wet synthesis method such as a hydrothermal synthesis method or alkoxide method are prepared as starting materials of the dielectric ceramics. A solution of an alkoxide or an organometallic compound may be used for the additives other than oxides and carbonates.

After weighing the prepared materials in a prescribed composition ratio with mixing, the mixed powder is turned into a slurry by adding an organic binder to obtain a green sheet (the dielectric ceramic layers **2***a* and **2***b*) by molding the slurry into a sheet. The inner electrodes **4** comprising nickel or a nickel alloy are then formed on one face of the green sheet (the dielectric ceramic layers **2***b*). Any method including screen printing, vacuum deposition or plating may be used for forming the inner electrodes **4**.

Then, a required number of the green sheets (the dielectric ceramic layers **2***b*) having the inner electrodes **4** are laminated, which are inserted between the green sheets having no inner electrodes (the dielectric ceramic layers **2***a*) to form a laminated body after pressing. A ceramic laminated body **3** is obtained by firing the laminated body at a given temperature in a reducing atmosphere.

A pair of the outer electrodes **5** are formed on both side ends of the ceramic laminate body **3** so as to be in electrical continuity with the inner electrodes **4**. While the outer electrodes **5** are usually formed by coating the metal powder paste on the ceramic laminated body **3** obtained by firing and baking the paste, the outer electrode may be formed simultaneously with forming the ceramic laminated body **3** by coating the paste prior to firing.

Finally, the first plating layer **6** and the second plating layer **7** are formed, if necessary, on the outer electrodes **5**, thereby completing the laminated ceramic capacitor **1**.

EXAMPLES

Example 1

Starting materials TiO_2, $BaCO_3$ and $CaCO_3$ are at first prepared. After mixing and crushing the materials, the mixture is heated at 1000° C. or more to synthesize nine kinds of barium calcium titanate shown in TABLE 1. The mean particle size was determined by observing the particles of the material under a scanning electron microscope.

TABLE 1

Kind of Barium Calcium Titanate	$(Ba_{1-x}Ca_xO)_nTiO_2$ x	(Ba + Ca)/Ti n	Content of Alkali Metal Oxide Impurities (% by weight)	Mean Particle Size (μm)
A	0.003	1.000	0.003	0.50
B	0.100	1.000	0.010	0.50
C	0.200	0.998	0.012	0.50
D	0.250	0.998	0.015	0.50
E	0.100	1.000	0.062	0.50
F	0.080	1.005	0.003	0.15
G	0.100	1.008	0.020	0.25
H	0.100	1.000	0.010	0.75
I	0.100	1.000	0.010	0.08

Oxides, carbonates and hydroxides of respective components of the first sub-component were weighed so as to be a composition (molar) ratio of $0.25Li_2O$-$0.65(0.30TiO_2$-$0.70SiO_2)$-$0.10Al_2O_3$ and the mixture was crushed to obtain a powder. Likewise, oxides, carbonates and hydroxides of respective components of the second sub-component were weighed so as to be a composition ratio of $0.66Si_2O$-$0.17TiO_2$-0.15BaO-0.02MnO (molar ratio) and the mixture was crushed to obtain a powder. Then, after heating the powders of the first and second sub-components to 1500° C. in different crucibles, respectively, they were quenched and crushed to obtain respective oxide powders with a mean particle size of 1 μm or less.

In the next step, $BaCO_3$ or TiO_2 for adjusting the molar ratio m of (Ba, Ca)/Ti in the barium calcium titanate, and Y_2O_3, Gd_2O_3, Tb_2O_3, Dy_2O_3, Ho_2O_3, Er_2O_3, Yb_2O_3, MgO and MnO with purity of 99% or more were prepared. These powder materials and the foregoing oxide powders for the first and second sub-components were weighed to be the compositions shown in TABLE 2. The amount of addition of the first and second sub-components are given in parts by weight relative to 100 parts by weight of the principal component, i.e., $(Ba_{1-x}Ca_xO)_mTiO_2+\alpha Re_2O_3+\beta MgO+\gamma MnO$. A polyvinyl butylal based binder and an organic solvent such as ethanol were added to the weighed materials and the mixture was wet-milled with a ball-mill to prepare a ceramic slurry. This ceramic slurry was formed into a sheet by a doctor blade method, obtaining a rectangular green sheet with a thickness of 4.5 μm. Then, a conductive paste mainly containing Ni was printed on the ceramic green sheet to form conductive paste layers constituting the inner electrodes.

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TABLE 2

Sample No.	Kind of Barium Calcium Titanate	(Ba1 - xCaxO)m·TiO2 + αMgO + γMnO x	m	α Y2O3	Gd2O3	Tb2O3	Dy2O3	Ho2O3	Er2O3	Yb2O3	β	γ	The First Sub-Component (parts by weight)	The Second Sub-Component (parts by weight)
*1	A	0.003	1.01	0	0	0	0.02	0	0	0	0.02	0.005	1	0
*2	D	0.250	1.01	0	0	0	0.02	0	0	0	0.02	0.005	1	0
*3	B	0.100	1.01	0	0	0	0.0005	0	0	0	0.02	0.005	1	0
*4	B	0.100	1.01	0	0	0	0.11	0	0	0	0.02	0.005	1	0
*5	B	0.100	1.01	0	0	0	0.02	0	0	0	0.0008	0.005	1	0
*6	B	0.100	1.01	0	0	0	0.02	0	0	0	0.13	0.005	1	0
*7	B	0.100	1.01	0	0	0	0.02	0	0	0	0.02	0.0008	1	0
*8	B	0.100	1.01	0	0	0	0.02	0	0	0	0.02	0.13	1	0
*9	B	0.100	0.995	0	0	0	0.02	0	0	0	0.02	0.005	1	0
*10	B	0.100	1	0	0	0	0.02	0	0	0	0.02	0.005	1	0
*11	B	0.100	1.036	0	0	0	0.02	0	0	0	0.02	0.005	1	0
*12	B	0.100	1.01	0	0	0	0.02	0	0	0	0.02	0.005	0	0
*13	B	0.100	1.01	0	0	0	0.02	0	0	0	0.02	0.1	0	0
*14	B	0.100	1.01	0	0	0	0.02	0	0	0	0.02	0.005	5.5	0
*15	B	0.100	1.01	0	0	0	0.02	0	0	0	0.02	0.005	0	5.5
*16	E	0.100	1.01	0	0	0	0.02	0	0	0	0.02	0.005	1	0
17	H	0.100	1.01	0	0	0	0.02	0	0	0	0.02	0.005	1	0
18	I	0.100	1.01	0	0	0	0.02	0	0	0	0.02	0.005	1	0
19	G	0.100	1.025	0.025	0	0	0	0	0	0	0.02	0.005	0	1
20	G	0.100	1.02	0	0.08	0	0	0	0	0	0.05	0.008	4	0
21	G	0.100	1.015	0	0	0.05	0	0	0	0	0.05	0.005	3	0
22	B	0.100	1.01	0	0	0	0	0.02		0	0.02	0.05	2	0
23	B	0.100	1.01	0	0	0	0	0	0.02	0	0.02	0.05	0	1
24	G	0.200	1.005	0	0	0	0	0	0	0.03	0.02	0.05	0	1
25	C	0.200	1.005	0.005	0	0	0.02	0	0	0	0.02	0.005	0	1
26	F	0.080	1.015	0.005	0.015	0	0	0	0	0	0.02	0.005	2	0
27	F	0.080	1.015	0	0	0	0.02	0	0	0	0.02	0.005	0	2

*The samples marked (*) are out of the range of the present invention.

Next, a plurality of ceramic green sheets on which the conductive paste layers had been formed were laminated to obtain a laminated body so that the sides where the conductive paste layers are exposed alternately come to the opposite ends. The laminated body was heated at a temperature of 350° C. in a N_2 atmosphere. After driving out the binder, the laminated body was fired in a reducing atmosphere comprising a H_2—N_2—H_2O gas with an oxygen partial pressure of 10^{-9} to 10^{-12} MPa to obtain a ceramic sintered body.

After firing, an Ag paste containing a B_2O_3—Li_2—SiO_2—BaO based glass frit was coated on both side faces of the ceramic sintered body, which was baked at a temperature of 600° C. in the N_2 atmosphere to form the outer electrodes electrically connected to the inner electrodes.

The laminated ceramic capacitor thus obtained had an overall dimension with a width of 5.0 mm, a length of 5.7 mm and a thickness of 2.4 mm with a thickness of the dielectric ceramic layers inserted between the inner electrodes of 3 μm. The total number of the effective dielectric ceramic layers was five with a confronting electrode area per layer of 16.3×10^{-6} m^2.

Electric characteristics of these laminated ceramic capacitors were then determined. Electrostatic capacitances and dielectric losses (tan δ) were measured per JIS C5102 standard using an automatic bridge type measuring apparatus and dielectric constant was calculated from the electrostatic capacitance obtained. Insulation resistance was also measured using an insulation resistance meter by impressing a direct-current voltage of 10 V for 2 minutes to calculate resistivity (ρ).

DV vias characteristics were also measured. The electrostatic capacitance was determined while impressing a direct-current voltage of 15 V (5 kV/mm) and the rate of change of the electrostatic capacitance (ΔC %) was determined relative to the electrostatic capacitance measured without impressing a direct-current voltage.

The rate of temperature dependent change of the electrostatic capacitance was also measured. The maximum value of the rate of change in the temperature range from −25° C. to 85° C. relative to the capacitance at 20° C. (ΔC/C20) and the maximum value of the rate of change in the temperature range from −55° C. to 125° C. relative to the capacitance at 25° C. (ΔC/C25) were determined with respect to the rate of change of the capacitance.

A high temperature load test was carried out by measuring the time dependent changes of the insulation resistance when a direct-current voltage of 30 V was impressed at 150° C. Lifetime of each sample was defined to be the time when the insulation resistance of each sample had decreased to 10^5 Ω or less, and a mean lifetime was determined using a plurality of the samples.

The dielectric breakdown voltage was measured by impressing DC voltages with a voltage increasing rate of 100 V/sec. The results are summarized in TABLE 3.

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TABLE 3

Sample No.	Burning Temp. (° C.)	Dielectric Constant	Dielectric Loss tan δ (%)	Rate of Change of Capacitance ΔC% DC 5Kv/mm	Rate of Temperature Dependent Change of Capacitance ΔC/C20% −25~+85° C. (%)	ΔC/C25% −55~+125° C. (%)	Dielectric Resistivity Log ρ (Ω.cm)	Dielectric Breakdown Voltage DC (kV/mm)	Mean Lifetime (h)
*1	1300	3360	4.5	−65	−9.7	−15.6	13.2	14	3
*2	1250	1130	9.3	−35	−4.5	−6.5	13.1	15	23
*3	1250	2430	4.6	−55	−1.5	−10.6	13.2	14	2
*4	1250	1220	3.1	−37	−18.1	−23.3	13.5	15	15
*5	1250	2570	3.6	−63	−15.6	−24.7	12.9	12	65
*6	1350	1760	4.4	−45	−7.8	−14.6	13.1	14	2
*7	1250	1950	4.7	−57	−9.6	−15.4	11.8	14	17
*8	1250	1730	3.8	−56	−13.6	−19.7	11.2	14	8
*9	1250	2100	5.6	−60	−12.3	−18.6	11.2	8	–
*10	1250	2060	5.3	−62	−12.2	−17.5	11.6	9	–
*11	1300	1950	4.4	−50	−8.6	−14.4	12.3	9	1
*12	1350	1530	5.1	−45	−8.8	−13.7	11.4	10	–
*13	1350	1470	5.3	−47	−8.9	−14.2	11.5	9	–
*14	1200	1680	3.2	−48	−14.5	−30.6	13.1	14	5
*15	1200	1740	3.4	−42	−13.3	−26.8	13.1	14	3
*16	1250	1750	3.7	−48	−10.5	−15.1	13.1	14	21
17	1250	2370	4.7	−51	−4.7	−6.7	13.1	13	52
18	1150	1040	2.5	−30	−8.4	−14.2	13.5	15	174
19	1175	1410	2.2	−35	−9.6	−14.4	13.2	14	85
20	1150	1260	2.3	−33	−8.8	−13.7	13.2	15	110
21	1175	1260	2.3	−36	−9.2	−14.6	13.2	14	105
22	1200	1900	2.1	−42	−8.6	−13.4	13.2	14	85
23	1250	2010	2.5	−44	−8.5	−13.8	13.2	15	80
24	1250	1430	1.8	−34	−7.8	−11.4	13.1	14	110
25	1250	1450	1.9	−31	−8.2	−11.1	13.2	15	120
26	1175	1260	1.7	−32	−9.5	−14.5	13.2	14	92
27	1175	1340	1.6	−33	−9.2	−13.5	13.2	14	95

*The samples marked by (*) are out of the range of th e present invention.

The cross section of the laminated ceramic capacitor obtained was polished and subjected to chemical etching. It was found from scanning electron microscopic observation of the grain size in the dielectric ceramics that the grain size was almost equal to the particle size of the barium calcium titanate starting material in the samples having the compositions within the range of the present invention.

As are evident from TABLE 1 to TABLE 3, the rate of temperature dependent change of the electrostatic capacitance satisfies the B-grade characteristic standard prescribed in the JIS standard in the temperature range from −25° C. to +85° C., along with satisfying the X7R-grade characteristic standard prescribed in the EIA standard in the temperature range from −55° C. to +125° C., in the laminated ceramic capacitor according to the present invention. In addition, the rate of change of the capacitance when a DC voltage of 5 kV/mm is impressed is as small as within 51%, the change of the electrostatic capacitance being also small when the capacitor is used has thin layers. Moreover, the mean lifetime in the high temperature load test is as long as 52 hours or more, enabling one to fire at a firing temperature of 1250° C. or below.

The reason why the compositions are limited in the present invention will be described hereinafter.

In the composition represented by the following formula:

$$(Ba_{1-x}Ca_xO)_mTiO_2+\alpha Re_2O_3+\beta MgO+\gamma MnO$$

(Re_2O_3 represents at least one of the compounds selected from Y_2O_3, Gd_2O_3, Tb_2O3, Dy_2O_3, Ho_2O_3, Er_2O_3 and Yb_2O_3 and α, β and γ represent molar ratios), a CaO content (x) of about 0.005 or less as in the sample No. 1 is not preferable since the rate of impressed voltage dependent change of the capacitance becomes large and the mean lifetime becomes extremely short. It is also not preferable that the CaO content (x) exceeds about 0.22 as in the sample No. 2 because the dielectric loss is increased. Accordingly, the preferable CaO content (x) is in the range of $0.005<x\leqq 0.22$.

A Re_2O_3 content (α) of less than about 0.001 as in the sample No. 3 is also not preferable because the mean lifetime becomes extremely short. It is also not preferable that the content of Re_2O_3 (α) exceed about 0.10 since the temperature characteristics do not satisfy the B/X7R-grade characteristics while the mean lifetime is shortened. Accordingly, the preferable Re_2O_3 content (α) is in the range of $0.001\leqq\alpha\leqq 0.10$.

A MgO content (β) of less than about 0.001 as in the sample No. 5 is also not preferable because the rate of impressed voltage dependent change of the capacitance becomes large while the temperature characteristics do not satisfy the B/X7R-grade characteristics. It is also not preferable that the amount of addition (β) of MgO exceed about 0.12 as in the sample No. 6 since the sintering temperature becomes high to extremely shorten the mean lifetime. Accordingly, the preferable MgO content (β) is in the range of $0.001\leqq\beta\leqq 0.12$.

A MnO content (γ) of less than about 0.001 as in the sample No. 7 is also not preferable because the capacitance is lowered while the mean lifetime is shortened. It is also not preferable that the MnO content (γ) exceed about 0.12 as in the sample No. 8 since the temperature characteristics do not satisfy the B/X7R-grade characteristics, the resistivity becomes low and the mean lifetime is shortened. Accordingly, the preferable range of the MnO content (γ) is $0.001<\gamma\leqq 0.12$.

It is not preferable that the ratio (m) of (Ba, Ca)/Ti is less than about 1.000 as in the samples No. 9 and No. 10 because

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the temperature characteristics do not satisfy the B/X7R-grade characteristics, thereby lowering the resistivity besides immediately causing short circuit troubles when a voltage is impressed in the high temperature load test. It is also not preferable that the ratio (m) of (Ba, Ca)/Ti exceed about 1.035 as in the sample No. 11 because sintering is insufficient to extremely shorten the mean lifetime. Accordingly, the preferable ratio (m) of (Ba, Ca)/Ti is in the range of $1.000<m\leqq1.035$.

It is not preferable that the contents of the first and second sub-components are zero as in the samples No. 12 and No. 13 because the resistivity is lowered to immediately cause short circuit troubles when a voltage is impressed in the high temperature load test. It is also not preferable that the contents of the first and second sub-components exceed about 5.0 parts by weight as in the sample Nos. 14 and 15 because the second phase based on glass components is increased and the temperature characteristics do not satisfy the B/X7R-grade characteristics and the mean lifetime is extremely shortened. Accordingly, the preferable content of either the first component or the second component is in the range of about 0.2 to 5.0 parts by weight.

The content of the alkali metal oxides contained in barium calcium titanate as impurities is adjusted to about 0.02% by weight or less because, when the content of the alkali metal oxides exceeds about 0.02% by weight as in the sample No. 16, the mean lifetime is shortened.

The sample No. 17 in which the mean particle size of barium calcium titanate exceeds 0.7 μm shows a little poor mean lifetime of 52 hours. The sample No. 18 in which the mean particle size of barium calcium titanate is less than 0.1 μm shows, on the other hand, a little small dielectric constant of 1040. Accordingly, the preferable mean particle size of barium calcium titanate is in the range from about 0.1 to 0.7 μm.

Example 2

A dielectric powder material represented by the following formula was prepared using the barium calcium titanate (B) in TABLE 1:

$(Ba_{0.90}Ca_{0.10}O)_{1.010}TiO_2+0.02Dy_2O_3+0.02MgO+0.01MnO$ (molar ratio)

A laminated ceramic capacitor was produced by the same method as used in Example 1, except that a Li_2O—(Si,Ti)O_2—MO based oxide as the first sub-component having a mean particle size of 1 μm listed in TABLE 4 was added to the mixture above. The size and shape of the laminated ceramic capacitor produced in this example were the same as those in Example 1. The electric characteristic were measured by the same method as used in Example 1. The results are shown in TABLE 5.

TABLE 4

	First Subcomponent					
Sample No.	Amount of addition (parts by weight)	Composition (mol %, except w) Li_2O	(Si_wTi_{1-w})	w	Al_2O_3	ZrO_2
101	1	20	80	0.3	0	0
102	1	10	80	0.6	5	5
103	1	10	70	0.5	20	0
104	2	35	45	1	10	10
105	2	45	45	0.5	10	0
106	2	45	55	0.3	0	0
107	1.5	20	70	0.6	5	5
108	1.5	20	70	0.4	10	0
109	2	30	60	0.7	5	5
110	2	30	60	0.8	10	0
111	2	40	50	0.6	5	5
112	2	40	50	0.9	0	10
113	2	10	85	0.4	5	0
114	2	5	75	0.6	10	10
115	3	20	55	0.5	25	0
116	3	45	40	0.8	0	15
117	3	50	45	0.7	5	0
118	2	25	75	0.9	0	0
119	2	25	75	1	0	0
120	2	35	65	0.9	0	0
121	2	35	65	1	0	0
122	1	20	70	0.2	0	10

TABLE 5

Sample No.	Burning Temp. (° C.)	Dielectric Constant	Dielectric Loss tan δ (%)	Rate of Change of Capacitance ΔC% DC 5Kv/mm	Rate of Temperature Dependent Change of Capacitance ΔC/C20% −25~+85° C. (%)	ΔC/C25% −55~+125° C. (%)	Dielectric Resistivity Log ρ (Ω.cm)	Dielectric Breakdown Voltage DC (kV/mm)	Mean Lifetime (h)
101	1250	1920	2.4	−43	−8.2	−12.8	13.2	14	82
102	1250	1910	2.4	−42	−7.8	−12.6	13.1	15	86
103	1250	1870	2.5	−41	−7.7	−12.3	13.2	14	84
104	1225	1850	2.4	−41	−7.5	−12.5	13.5	15	88
105	1225	1870	2.4	−42	−7.2	−11.7	13.2	14	90
106	1225	1870	2.4	−40	−7.8	−12.0	13.1	14	80
107	1250	1910	2.4	−42	−8.1	−12.1	13.3	14	85
108	1250	1910	2.3	−42	−7.8	−11.8	13.2	14	90
109	1225	1890	2.5	−41	−7.7	−11.7	13.3	14	90
110	1225	1900	2.5	−42	−7.9	−12.1	13.2	14	95
111	1225	1890	2.4	−42	−7.6	−12.1	13.2	15	91
112	1225	1850	2.3	−40	−7.6	−11.8	13.3	14	87

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TABLE 5-continued

Sample No.	Burning Temp. (° C.)	Dielectric Constant	Dielectric Loss tan δ (%)	Rate of Change of Capacitance ΔC% DC 5Kv/mm	Rate of Temperature Dependent Change of Capacitance ΔC/C20% −25~+85° C. (%)	ΔC/C25% −55~+125° C. (%)	Dielectric Resistivity Log ρ (Ω.cm)	Dielectric Breakdown Voltage DC (kV/mm)	Mean Lifetime (h)
113	1300	1620	2.2	−42	−7.9	−12.2	11.5	9	–
114	1300	1460	2.4	−41	−8.0	−12.6	10.8	8	–
115	1300	1330	2.6	−42	−7.8	−12.5	10.6	8	–
116	1300	1420	2.8	−43	−7.8	−12.2	10.8	8	–
117	1300	1360	2.4	−43	−8.6	−12.4	11.2	8	–
118	1250	1920	2.3	−43	−7.8	−11.7	13.2	15	88
119	1300	1450	2.1	−40	−8.2	−11.6	11.1	9	–
120	1250	1900	2.5	−42	−7.6	−11.7	13.2	14	88
121	1300	1350	2.1	−44	−8.5	−12.8	10.2	8	–
122	1350	1420	2.1	−44	−8.2	−11.5	10.2	8	–

–: Measurement is Impossible

As are evident from Table 4 and Table 5, the sample Nos. 101 to 112, 118 and 120, in which Li_2O—$(Si_wTi_{1-w})O_2$—Mo based oxides with compositions within the area surrounded by the straight lines connecting between the succeeding two points represented by A (x=20, y=80, z=0), B (x=10, y=80, z=10), C (x=10, y=70, z=20), D (x=35, y=45, z=20), E (x=45, y=45, z=10) and F (x=45, y=55, z=0) (and where w is in the range of $0.3 \leqq w < 1.0$ when the composition is on the line A–F) or on the lines in a ternary composition diagram having apexes represented by each component LiO_2, $(Si_wTi_{1-w})O_2$ and MO (x, y and z are represented by mol % and w is in the range of $0.3 \leqq w \leqq 1.0$ when the component is on the line A-F,) are added, has a dielectric constant of as large as 1850, the rate of temperature dependent changes of the electrostatic capacitance satisfy the B-grade characteristic standard prescribed in the JIS standard in the temperature range from −25° C. to +85° C., and satisfy the X7R-grade characteristic standard prescribed in the EIA standard in the temperature range from −55° C. to +125° C. In addition, the rate of change of the capacitance when a DC voltage of 5 kV/mm is impressed is as small as within 43%, the change of the electrostatic capacitance being small when used as thin layers. The mean lifetime under the high temperature load test is as long as 80 hours or more, enabling a firing temperature of 1250° C.

When the compositions of the Li_2O—$(Si, Ti)O_2$—Mo based oxides are out of the range of the present invention as in the sample Nos. 113 to 117, 119, 121 and 122, on the contrary, sintering is insufficient to immediately cause short circuit troubles in the high temperature load test.

Example 3

A dielectric powder material represented by the following formula was prepared using barium calcium titanate in TABLE 1-B:

$$(Ba_{0.90}Ca_{0.10}O)_{1.010} \cdot TiO_2 + 0.02Gd_2O_3 + 0.05MgO + 0.010MnO$$
(molar ratio)

Laminated ceramic capacitors were produced by the same method as used in Example 1, except that SiO_2—TiO_2—XO based oxides as the second sub-components (including those supplemented with Al_2O_3 and ZrO_2) as shown in TABLE 6 with a mean particle size of 1 μm or less produced by heating at 1200 to 1500° C. were added to the powder material above. The size and shape of the laminated ceramic capacitors produced are the same as in Example 1. Electric characteristics were measured by the same method as used in Example 1. The results are shown in TABLE 7.

TABLE 6

Sample No.	Second Sub-Component: Amount of Addition (parts by weight)	Composition (mol %): SiO_2	TiO_2	XO: BaO	CaO	SrO	MgO	ZnO	MnO	Total	Additive Parts by Weight: Al_2O_3	ZrO_2
201	1	85	2	1	0	0	0	4	9	14	0	0
202	1	35	51	0	10	0	0	0	4	14	0	0
203	1	30	20	0	30	0	15	4	1	50	0	0
204	1	39	1	20	20	2	0	13	5	60	0	0
205	1	70	10	5	5	0	0	10	0	20	0	0
206	1	45	10	0	0	0	0	15	30	45	0	0
207	1	50	20	10	10	3	7	0	0	30	0	0
208	1	50	30	0	16	0	0	0	4	20	0	0
209	1	35	30	25	10	0	0	0	0	35	0	0
210	1	40	40	10	0	0	0	5	5	20	0	0
211	1	45	22	3	30	0	0	0	0	33	15	0
212	1	45	22	3	30	0	0	0	0	33	10	5
213	1	65	25	5	5	0	0	0	0	10	0	0

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TABLE 6-continued

Sample No.	Second Sub-Component: Amount of Addition (parts by weight)	Composition (mol %): SiO_2	TiO_2	XO: BaO	CaO	SrO	MgO	ZnO	MnO	Total	Additive Parts by Weight: Al_2O_3	ZrO_2
214	1	25	40	15	0	10	0	5	5	35	0	0
215	1	30	10	30	25	0	0	5	0	60	0	0
216	1	50	0	35	15	0	0	0	0	50	0	0
217	1	45	22	30	0	0	3	0	0	33	25	0
218	1	45	22	30	0	3	0	0	0	33	0	15
219	1	30	60	10	0	0	0	0	0	10	0	0

TABLE 7

Sample No.	Burning Temp. (° C.)	Dielectric Constant	Dielectric Loss tan δ (%)	Rate of Change of Capacitance: ΔC% DC 5Kv/mm	Rate of Temperature Dependent Change of Capacitance: ΔC/C20% −25~+85° C. (%)	ΔC/C25% −55~+125° C. (%)	Dielectric: Resistivity Log ρ (Ω.cm)	Breakdown Voltage DC (kV/mm)	Mean Lifetime (h)
201	1250	1940	2.4	−41	−7.7	−11.2	13.2	14	92
202	1250	1910	2.3	−42	−7.5	−11.2	13.2	15	96
203	1250	1950	2.4	−42	−8.1	−11.6	13.3	14	88
204	1250	1920	2.3	−44	−7.8	−11.5	13.2	15	85
205	1250	1930	2.3	−41	−8.1	−11.5	13.2	14	91
206	1250	1890	2.2	−40	−8.0	−12.1	13.4	14	95
207	1250	1910	2.3	−43	−8.1	−11.7	13.3	14	88
208	1250	1900	2.3	−42	−8.3	−11.8	13.3	14	92
209	1250	1930	2.3	−43	−8.1	−11.9	13.3	14	88
210	1250	1920	2.3	−43	−8.1	−12.5	13.3	14	85
211	1250	1880	2.2	−41	−7.5	−11.1	13.5	15	96
212	1250	1920	2.3	−42	−8.3	−11.8	13.6	14	92
213	1300	1620	3.1	−42	−7.2	−12.1	11.2	8	—
214	1300	1530	2.9	−42	−7.3	−11.8	11.1	8	—
215	1300	1460	2.7	−40	−7.2	−12.5	11.4	9	—
216	1300	1470	2.7	−40	−7.8	−12.9	11.3	9	—
217	1300	1430	2.9	−38	−7.1	−11.7	11.5	8	—
218	1300	1510	2.8	−41	−6.6	−11.2	11.4	8	—
219	1300	1480	3.1	−40	−7.1	−12.2	11.2	8	—

As are evident from Table 6 and Table 7, the sample Nos. 201 to 210 in which SiO_2—TiO_2—XO based oxides with compositions within the area surrounded by the straight lines connecting between the succeeding two points represented by A (x=85, y=1, z=14), B (x=35, y=51, z=14), C (x=30, y=20, z=50) and D (x=39, y=1, z=60) or on the lines in a ternary composition diagram having apexes represented by each component SiO_2, TiO_2 and XO (x, y and z are represented by mol %) are added, has a dielectric constant of as large as 1890 or more, the rate of temperature dependent changes of the electrostatic capacitance satisfy the B-grade characteristic standard prescribed in the JIS standard in the temperature range from −25° C. to +85° C., and satisfy the X7R-grade characteristic standard prescribed in the EIA standard in the temperature range from −55° C. to +125° C. In addition, the rate of change of the capacitance when a DC voltage of 5 kV/mm is impressed is as small as within 44%, the change of the electrostatic capacitance being small when used as thin layers. The mean lifetime under the high temperature load test is as long as 85 hours or more, enabling a firing temperature of 1250° C.

When the compositions of the SiO_2—TiO_2—XO based oxides are out of the range of the present invention as in the sample Nos. 213 to 216 and 219, on the contrary, sintering is insufficient, immediately causing short circuit troubles when a voltage is impressed in the high temperature load test.

While the resistivity can be enhanced by allowing Al_2O_3 and ZrO_2 in the SiO_2—TiO_2—Xo based oxides as in the sample Nos. 211 and 212, sintering becomes insufficient when the amount of addition of Al_2O_3 exceeds about 15 parts by weight or the amount of addition of ZrO_2 exceeds about 5 parts by weight as in the sample Nos. 217 and 218, immediately causing short circuit troubles when a voltage is impressed in the high temperature load test.

When the dielectric ceramic particles of the samples having the compositions within the range of the present invention obtained in the Examples 1 to 3 were analyzed with a transmission electron microscope, core-shell structures in which the Re components (Re denotes Y, Gd, Tb, Dy, Ho, Er and Yb) are diffused in the vicinity of and at the grain boundary were confirmed.

As is evident from the foregoing descriptions, the dielectric ceramic layers in the laminated ceramic capacitor according to the present invention are composed of a dielectric ceramic composition that is not reduced even when they

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are fired in a reducing atmosphere. Therefore, base metals such as nickel and a nickel alloy can be used as electrode materials, along with making it possible to reduce the production cost of the laminated ceramic capacitor because the material is able to be fired at a relatively low temperature of 1250° C.

Reduction of the dielectric constant, or the electrostatic capacitance, is small even when a high electric field is impressed on the thin layer of the dielectric ceramic layer in the laminated ceramic capacitor using the dielectric ceramic composition, ensuring high reliability enough for obtaining a small size and thin layered laminated ceramic capacitor having large capacitance.

The dielectric ceramic layers 2*a* and 2*b* may be composed of a dielectric ceramic composition containing the principal components comprising barium calcium titanate $(Ba_{1-x}Ca_xO)_mTiO_2$, at least one or more of the oxides selected from Y_2O_3, Gd_2O_3, Tb_2O_3, Dy_2O_3, Ho_2O_3, Er_2O_3 and Yb_2O_3, MgO and MnO; and a sub-component selected from Li_2O—B_2O_3—(Si, Ti)O_2 based oxides, Al_2O_3—MO—B_2O_3 based oxides (MO is at least one oxide selected from BaO, CaO, SrO, MgO, ZnO and MnO) and SiO_2. The composition described above allows the ceramic composition to be fired in a reducing atmosphere without endowing it with semiconductive properties. Consequently, a highly reliable laminated ceramic capacitor with high insulation resistance at room temperature and at high temperatures and having excellent insulation strength can be obtained while the temperature characteristics of the electrostatic capacitance satisfying the B-grade characteristics prescribed in the JIS standard and X7R-grade characteristics prescribed in the EIA standard.

A highly reliable ceramic capacitor, in which the electric field dependent change of dielectric constant is small even when thin ceramic layers are placed in a high field intensity, can be obtained by using a barium calcium titanate material with a mean particle size of about 0.1 to 0.7 μm. The dielectric ceramic has a core-shell structure in which Re components (Re is one or more of the elements selected from Y, Gd, Tb, Dy, Ho, Er and Yb) are distributed in the vicinity and at the grain boundaries due to diffusion during firing.

A highly reliable dielectric material is also obtainable by using a barium calcium titanate material containing about 0.02% by weight or less of alkali metal oxides such as Na_2O and K_2O.

Although the ratio (n) of (barium+calcium)/titanium in the barium calcium titanate material is not especially limited, the ratio (n) in the range from about 0.990 to 1.035 is desirable in order to diminish particle size distribution in the synthesize powder when stability for producing the powder material is taken into consideration.

The Li_2O—B_2O_3—(Si,Ti)O_2 based oxides contained in the principal component allows the ceramic to be sintered at a relatively low temperature of 1250° C. with no fear of deterioration of its characteristics due to plating. A much higher insulation resistance is obtained by allowing Al_2O_3 and ZrO_2 to be contained in the Li_2O—B_2O_3—(Si, Ti)O_2 based oxides. The Al_2O_3—MO—B_2O_3 based oxides contained in the principal component allows the ceramic to be easily sintered with no fear of deterioration of its characteristics due to plating. Further, SiO_2 contained in the principal component also allows the ceramic to be easily sintered with no fear of deterioration of its characteristics due to plating.

The inner electrodes are composed of a base metal such as nickel and a nickel alloy.

The outer electrodes are composed of a sintered layer comprising various conductive metals such as Ag, Pd, Ag—Pd, Cu and a Cu alloy, or a sintered layer produced by blending the conductive metal powder with B_2O_3—LiO_2—SiO_2—BaO based, B_2O_3—SiO_2—BaO based, LiO_2—SiO_2—BaO based or B_2O_3—SiO_2-ZnO based glass frits. Plating layers can be formed on this sintered layer. The plating layer may be merely composed of the first plating layer 6 comprising Ni, Cu or a Ni—Cu alloy, or a second plating layer 7 with a solder or tin may be formed thereon.

The foregoing method for producing the laminated ceramic capacitor can be also used when the materials described above are used.

Example 4

TiO_2, $BaCO_3$ and $CaCO_3$ as starting materials were firstly prepared and mixed with crushing. The mixed powder was heated at 1000° C. or more to synthesize nine kinds of barium calcium titanate shown in TABLE 1. Mean particle sizes were determined by observing the material under a scanning electron microscope.

Oxides, carbonates and hydroxides were weighed to be in the composition ratio of $0.25Li_2O$-$0.10B_2O_3$-$0.07TiO_2$-$0.58SiO_2$ (molar ratio) of the first sub-component, and a powder was obtained by crushing with mixing. Likewise, oxides, carbonates and hydroxides were weighed to be in the composition ratio of $0.25Al_2O_3$-0.17BaO-0.03MnO-$0.55B_2O_3$ (molar ratio) of the second sub-component, and a powder was obtained by crushing with mixing. The powders of these first and second sub-components were independently placed in crucibles to heat at 1400° C. Respective oxide powders with a mean particle size of 1 μm or less were obtained by quenching followed by crushing.

$BaCO_3$ or TiO_2, and Y_2O_3, Gd_2O_3, Tb_2O_3, Dy_2O_3, Ho_2O_3, Er_2O_3, Yb_2O_3, MgO and MnO with purity of 99% or more were prepared for adjusting the molar ratio (*m*) of (Ba, Ca)/Ti in barium calcium titanate. These powder materials, and the oxide powders as the first and second sub-components were weighed to be the compositions shown in TABLE 8. The first and second sub-components were added in parts by weight relative to 100 parts by weight of the principal component $(Ba_{1-x}Ca_xO)_mTiO_2+\alpha Re_2O_3+\beta MgO+\gamma MnO$. A polybutyral based binder and an organic solvent such as ethanol were added into the weighed mixture, which was wet-milled to prepare a ceramic slurry. This ceramic slurry was formed into a sheet by a doctor blade method, obtaining a rectangular green sheet with a thickness of 4.5 μm. A conductive paste mainly composed of Ni was printed on this green sheet to form conductive paste layers constituting the inner electrodes.

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TABLE 8

Sample No.	Kind of Barium Calcium Titanate	$(Ba_{1-x}Ca_x O)_m TiO_2$ + αRe_2O_3 + βMgO + γMnO x	m	α Y_2O_3	Gd_2O_3	Tb_2O_3	Dy_2O_3	Ho_2O_3	Er_2O_3	Yb_2O_3	β	γ	First Sub-Component (parts by weight)	Second Sub-Component (parts by weight)
1001*	A	0.003	1.01	0	0	0	0.02	0	0	0	0.02	0.005	1	0
1002*	D	0.250	1.01	0	0	0	0.02	0	0	0	0.02	0.005	1	0
1003*	B	0.100	1.01	0	0	0	0.0005	0	0	0	0.02	0.005	1	0
1004*	B	0.100	1.01	0	0	0	0.01	0	0	0	0.02	0.005	1	0
1005*	B	0.100	1.01	0	0	0	0.02	0	0	0	0.008	0.005	1	0
1006*	B	0.100	1.01	0	0	0	0.02	0	0	0	0.13	0.005	1	0
1007*	B	0.100	1.01	0	0	0	0.02	0	0	0	0.02	0.0008	1	0
1008*	B	0.100	1.01	0	0	0	0.02	0	0	0	0.02	0.13	1	0
1009*	B	0.100	0.995	0	0	0	0.02	0	0	0	0.02	0.005	1	0
1010*	B	0.100	1	0	0	0	0.02	0	0	0	0.02	0.005	1	0
1011*	B	0.100	1.036	0	0	0	0.02	0	0	0	0.02	0.005	1	0
1012*	B	0.100	1.01	0	0	0	0.02	0	0	0	0.02	0.005	0	0
1013*	B	0.100	1.01	0	0	0	0.02	0	0	0	0.02	0.1	0	0
1014*	B	0.100	1.01	0	0	0	0.02	0	0	0	0.02	0.005	5.5	0
1015*	B	0.100	1.01	0	0	0	0.02	0	0	0	0.02	0.005	0	5.5
1016*	E	0.100	1.01	0	0	0	0.02	0	0	0	0.02	0.005	1	0
1017	H	0.100	1.01	0	0	0	0.02	0	0	0	0.02	0.005	1	0
1018	I	0.100	1.01	0	0	0	0.02	0	0	0	0.02	0.005	1	0
1019	G	0.100	1.025	0.025	0	0	0	0	0	0	0.02	0.005	0	1
1020	G	0.100	1.02	0	0.08	0	0	0	0	0	0.05	0.008	4	0
1021	G	0.100	1.015	0	0	0.05	0	0	0	0	0.05	0.005	3	0
1022	B	0.100	1.01	0	0	0	0	0.02	0	0	0.02	0.05	2	0
1023	B	0.100	1.01	0	0	0	0	0	0.02	0	0.02	0.05	0	1
1024	C	0.200	1.005	0	0	0	0	0	0	0.03	0.02	0.05	0	1
1025	C	0.200	1.005	0.005	0	0	0.02	0	0	0	0.02	0.005	0	1
1026	F	0.080	1.015	0.005	0.015	0	0	0	0	0	0.02	0.005	2	0
1027	F	0.080	1.015	0	0	0	0.02	0	0	0	0.02	0.005	0	2

*The Samples marked by (*) are out of the range of the present invention.

Next, a plurality of ceramic green sheets on which the conductive paste layers had been formed were laminated to obtain a laminated body so that the sides where the conductive paste layers are alternately exposed come to the opposite ends. The laminated body was heated at a temperature of 350° C. in a N_2 atmosphere. After driving out the binder, the laminated body was fired in a reducing atmosphere comprising a H_2—N_2—H_2O gas with an oxygen partial pressure of 10^{-9} to 10^{-12} MPa to obtain a ceramic sintered body.

After firing, an Ag paste containing a B_2O_3—Li_2O—SiO_2—BaO based glass frit was coated on both side faces of the ceramic sintered body, which was baked at a temperature of 600° C. in the N_2 atmosphere to form the couter electrodes electrically connected to the inner electrodes.

A plating solution comprising nickel sulfate, nickel chloride and boric acid was prepared, and nickel plating layers were formed on the silver outer electrodes by a barrel plating method. Then, a solder plating solution comprising an AS (alkano-sulfonic acid) bath was prepared and a solder plating was applied on the nickel plating layer by the barrel plating method, obtaining a laminated ceramic capacitor in which the outer electrodes were covered with plating layers.

The laminated ceramic capacitor obtained as described above had an overall dimension with a width of 5.0 mm, a length of 5.7 mm and a thickness of 2.4 mm, the thickness of the effective dielectric ceramic layer inserted between the inner electrodes being 3 μm. The total number of the effective dielectric ceramic layers was five with an area of the confronting electrode per layer of 16.3×10^{-6} m^2.

The electric characteristics of these laminated ceramic capacitors were then determined. The methods for measuring the electrostatic capacitance, dielectric loss (tan δ), insulation resistance, DC bias characteristics and temperature dependency (rate of change) of the electrostatic capacitance, the content of the high temperature load test, and the method for measuring dielectric breakdown voltage were the same as hitherto described. The results are listed in TABLE 9.

TABLE 9

Sample No.	Burning Temp. (° C.)	Dielectric Constant	Dielectric Loss tan δ (%)	Rate of Change of Capacitance ΔC% DC 5Kv/mm	Rate of Temperature Dependent Change of Capacitance ΔC/C20% −25~+85° C. (%)	ΔC/C25% −55~+125° C. (%)	Dielectric Resistivity Log ρ (Ω.cm)	Dielectric Breakdown Voltage DC (kV/mm)	Mean Lifetime (h)
*1001	1300	3310	3.8	−66	−9.5	−15.6	13.1	14	3
*1002	1250	1090	9.5	−33	−4.3	−6.1	13.1	15	26
*1003	1250	2540	5.1	−57	−3.3	−9.7	13.2	14	1

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TABLE 9-continued

Sample No.	Burning Temp. (° C.)	Dielectric Constant	Dielectric Loss tan δ (%)	Rate of Change of Capacitance ΔC% DC 5Kv/mm	Rate of Temperature Dependent Change of Capacitance ΔC/C20% −25~+85° C. (%)	ΔC/C25% −55~+125° C. (%)	Dielectric Resistivity Log ρ (Ω.cm)	Dielectric Breakdown Voltage DC (kV/mm)	Mean Lifetime (h)
*1004	1250	1200	3.6	−41	−18.4	−23.4	13.3	15	21
*1005	1250	2470	3.3	−59	−14.8	−22.9	12.6	14	74
*1006	1350	1570	3.7	−41	−6.7	−14.2	13.1	14	3
*1007	1250	1890	2.8	−44	−9.4	−14.8	11.7	13	3
*1008	1250	1830	2.7	−41	9.5	−14.7	12.1	14	5
*1009	1250	2070	3.9	−55	−12.4	−19.6	11.4	9	–
*1010	1250	2050	4.7	−58	−12.7	−18.4	11.5	9	–
*1011	1300	1950	4.4	−51	−9.3	−14.7	12.2	10	1
*1012	1350	1610	5.3	−47	−9.2	−14.1	11.5	11	–
*1013	1350	1630	5.2	−48	−9.3	−14.5	11.7	12	1
*1014	1200	1570	3.5	−47	−13.8	−29.5	13.2	14	7
*1015	1200	1680	3.3	−45	−13.5	−27.7	13.1	14	5
*1016	1250	1750	3.7	−45	−10.8	−15.4	13.1	14	18
1017	1250	2470	3.4	−52	−5.1	−7.7	13.2	14	54
1018	1150	1050	2.3	−31	−7.7	−14.3	13.4	14	162
1019	1175	1450	2.4	−33	−9.7	−14.7	13.2	14	108
1020	1150	1260	2.3	−31	−9.4	−14.3	13.3	15	111
1021	1175	1310	2.5	−32	−9.5	−14.8	13.3	14	107
1022	1200	1920	2.5	−41	−8.5	−12.8	13.2	14	83
1023	1250	1990	2.4	−43	−8.5	−12.5	13.3	14	81
1024	1250	1430	2.5	−37	−7.1	−10.2	13.1	14	110
1025	1250	1450	2.5	−35	−6.8	−10.8	13.2	14	120
1026	1175	1160	2.4	−33	−9.7	−14.3	13.2	14	91
1027	1175	1270	2.1	−32	−9.8	−14.7	13.2	14	94

*The Samples marked by (*) are out of the range of the present invention.

The cross section of the laminated ceramic capacitor was polished and subjected to chemical etching to observe the grain diameter of the dielectric ceramic under a scanning electron microscope. It was found that the grain diameter was almost equal to the particles size of the barium calcium titanate material in the samples having the compositions within the range of the present invention.

As is evident from TABLE 8 and TABLE 9, the rate of temperature dependent changes of the electrostatic capacitance in the laminated ceramic capacitor according to the present invention satisfies the B-grade characteristic standard prescribed in the JIS standard in the temperature range from −25° C. to +85° C. and the X7R grade characteristic standard prescribed in the EIA standard in the temperature range from −55° C. to +125° C. Moreover, the rate of change of the capacitance under an impressed DC voltage of 5 kV/mm is as small as 52%, indicating that the change of the electrostatic capacitance is also small when thin layers are used in the capacitor. The mean lifetime in the high temperature load test is as long as 45 hours, enabling one to fire at a temperature of 1250° C or less.

The reasons why the compositions are limited will be described hereinafter.

In the system comprising the principal component;

$$(Ba_{1-x}Ca_xO)_mTiO_2+\alpha Re_2O_3+\beta MgO+\gamma MnO$$

(Re_2O_3 is at least one or more of the compounds selected from Y_2O_3, Gd_2O_3, Tb_2O_3, Dy_2O_3, Ho_2O_3, Er_2O_3 and Yb_2O_3; α, β and γ representing molar ratios), the first and the second sub-components, the content (x) of CaO of about 0.05 or less as in the sample No. 1001 is not preferable since the rate of impressed voltage dependent change of the capacitance is large and the mean lifetime is extremely shortened. A content (x) of CaO exceeding about 0.22 as in the sample No. 1002 is not preferable, on the other hand, since the dielectric loss is increased. Accordingly, the preferable CaO constant (x) is in the range of $0.005<x\leqq0.22$.

It is not preferable that the Re_2O_3 content (α) is less than about 0.001 as in the sample No. 1003 since the mean lifetime is extremely shortened. A Re_2O_3 content (α) of exceeding about 0.10 as in the sample No. 1004 is also not preferable, on the other hand, since the temperature characteristics do not satisfy the B/X7R grade characteristics and the mean lifetime is shortened. Accordingly, the preferable Re_2O_3 content (α) is in the range of $0.001\leqq\alpha\leqq0.10$.

It is not preferable that the MgO content (β) is less than about 0.001 as in the sample No. 1005 since the temperature characteristics do not satisfy the B/X7R grade characteristics. A MgO content (β) of exceeding about 0.12 as in the sample No. 1006 is also not preferable, on the other hand, since the sintering temperature becomes so high that the mean lifetime is extremely shortened. Accordingly, the preferable MgO content (β) is in the range of $0.001\leqq\beta\leqq0.12$.

It is not preferable that the MnO content (γ) is about 0.001 or less as in the sample No. 1007 since the resistivity is lowered and the mean lifetime is extremely shortened. A MnO content (γ) of exceeding about 0.12 as in the sample No. 1008 is also not preferable, on the other hand, since the mean lifetime is extremely shortened. Accordingly, the preferable MnO content (γ) is in the range of $0.001<\gamma\leqq0.12$.

It is not preferable that the ratio (m) of (Ba, ca)/Ti is about 1.000 or less as in the sample Nos. 1009 and 1010 since the temperature characteristics do not satisfy the B/X7R grade characteristics and the resistivity becomes low and short circuit troubles are immediately caused when a voltage is impressed in the high temperature load test. It is also not

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preferable, on the other hand, that the ratio (m) of (Ba, ca)/Ti exceeds about 1.035 as in the sample No. 1011 because sintering becomes insufficient to extremely shorten the mean lifetime. Accordingly, the preferable ratio (m) of (Ba, ca)/Ti is in the range of $1.000<m\leqq1.035$.

It is not preferable that the content of the first and second sub-component is zero as in the sample Nos. 1012 and 1013 since the resistivity becomes low along with immediately causing circuit troubles when a voltage is impressed in the high temperature load test. It is also not preferable, on the other hand, that the content of the first and second sub-components exceed about 5.0 parts by weight as in the sample Nos. 1014 and 1015 because an increased amount of the secondary phase is formed and the temperature characteristics do not satisfy the B/X7R grade characteristics, extremely shortening the mean lifetime. Accordingly, the content of either the first sub-component or the second sub-component is preferably in the range from 0.2 to 5.0.

The content of alkali metal oxides that are contained in barium calcium titanate as impurities is adjusted to about 0.02% by weight or less because, as in the sample No. 1016, the mean lifetime is shortened when the content of the alkali metal oxides exceeds about 0.02% by weight.

The sample No. 1017 in which the mean particle size of barium calcium titanate exceeds 0.7 μm shows a little poor mean lifetime of 52 hours. The sample No. 1018 in which the mean particle size of barium calcium titanate is less than 0.1 μm shows, on the other hand, a little smaller dielectric constant of 1050. Accordingly, the preferable mean particle size of barium calcium titanate is in the range from about 0.1 to 0.7 μm.

Example 5

Starting materials TiO_2, $BaCO_3$ and $CaCO_3$ were firstly prepared and mixed with crushing as in Example 4. The mixed powder was heated at 1000° C. or more to synthesize nine kinds of barium calcium titanate shown in TABLE 1. Mean particle sizes were determined by observing the material under a scanning electron microscope. SiO_2 was also prepared as a third sub-component.

$BaCO_3$ or TiO_2 for adjusting the molar ratio (m) of (Ba, Ca)/Ti, and Y_2O_3, Gd_2O_3, Tb_2O_3, Dy_2O_3, Ho_2O_3, Er_2O_3, Yb_2O_3, MgO and MnO with purity of 99% or more were prepared. These powder materials and the SiO_2 powder as the third sun-component were weighed to be the compositions shown in TABLE 10. The amount of addition of SiO_2 is expressed in parts by weight relative to 100 parts by weight of the principal component $(Ba_{1-x}Ca_xO)_mTiO_2+\alpha Re_2O_3+\beta MgO+\gamma Mno$.

TABLE 10

$(Ba_{1-x}Ca_xO)_mTiO_2 + \alpha Re_2O_3 + \beta MgO + \gamma MnO$

Sample No.	Kind of Barium Calcium Titanate	x	m	α							β	γ	Third SubComponent SiO_2 (parts by weight)
				Y_2O_3	Gd_2O_3	Tb_2O_3	Dy_2O_3	Ho_2O_3	Er_2O_3	Yb_2O_3			
*1101	A	0.003	1.01	0	0	0	0.02	0	0	0	0.02	0.005	1
*1102	D	0.250	1.01	0	0	0	0.02	0	0	0	0.02	0.005	1
*1103	B	0.100	1.01	0	0	0	0.0005	0	0	0	0.02	0.005	1
*1104	B	0.100	1.01	0	0	0	0.11	0	0	0	0.02	0.005	1
*1105	B	0.100	1.01	0	0	0	0.02	0	0	0	0.0008	0.005	1
*1106	B	0.100	1.01	0	0	0	0.02	0	0	0	0.13	0.005	1
*1107	B	0.100	1.01	0	0	0	0.02	0	0	0	0.02	0.0008	1
*1108	B	0.100	1.01	0	0	0	0.02	0	0	0	0.02	0.13	1
*1109	B	0.100	0.995	0	0	0	0.02	0	0	0	0.02	0.005	1
*1110	B	0.100	1	0	0	0	0.02	0	0	0	0.02	0.005	1
*1111	B	0.100	1.036	0	0	0	0.02	0	0	0	0.02	0.005	1
*1112	B	0.100	1.01	0	0	0	0.02	0	0	0	0.02	0.005	0
*1113	B	0.100	1.01	0	0	0	0.02	0	0	0	0.02	0.1	0
*1114	B	0.100	1.01	0	0	0	0.02	0	0	0	0.02	0.005	5.5
*1115	E	0.100	1.01	0	0	0	0.02	0	0	0	0.02	0.005	1
1116	H	0.100	1.01	0	0	0	0.02	0	0	0	0.02	0.005	1
1117	I	0.100	1.01	0	0	0	0.02	0	0	0	0.02	0.005	1
1118	G	0.100	1.025	0.025	0	0	0	0	0	0	0.02	0.005	1
1119	G	0.100	1.02	0	0.08	0	0	0	0	0	0.05	0.008	4
1120	G	0.100	1.015	0	0	0.05	0	0	0	0	0.05	0.005	3
1121	B	0.100	1.01	0	0	0	0	0.02	0	0	0.02	0.05	2
1122	B	0.100	1.01	0	0	0	0	0	0.02	0	0.02	0.05	1
1123	C	0.200	1.005	0	0	0	0	0	0	0.03	0.02	0.05	1
1124	C	0.200	1.005	0.005	0	0	0.02	0	0	0	0.02	0.005	1
1125	F	0.080	1.015	0.005	0.015	0	0	0	0	0	0.02	0.005	1
1126	F	0.080	1.015	0	0	0	0.02	0	0	0	0.02	0.005	0.5

*The samples marked by (*) are out of the range of the present invention.

Laminated ceramic capacitors were then produced by the same method as in Example 4. The size and shape of the laminated ceramic capacitors produced were the same as those in Example 4. The electric characteristics were measured by the same method as used in Example 1, the results of which are shown in TABLE 11.

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TABLE 11

Sample No.	Burning Temperature (° C.)	Dielectric Constant	Dielectric Loss tan δ (%)	Rate of Change of Capacitance ΔC% DC 5Kv/mm	Rate of Temperature Dependent Change of Capacitance ΔC/C20% −25~+85° C. (%)	ΔC/C25% −55~+125° C. (%)	Resistivity Log ρ (Ω.cm)	Dielectric Breakdown Voltage DC (kV/mm)	Mean Lifetime (h)
*1101	1300	1340	3.0	−68	−9.8	−15.4	13.1	15	4
*1102	1250	1110	9.4	−33	−4.5	−6.7	13.2	14	21
*1103	1250	2410	2.1	−57	−1.7	−10.6	13.3	14	1
*1104	1250	1250	2.9	−57	−18.2	−13.5	13.5	15	11
*1105	1250	2610	2.5	−65	−15.5	−25.1	11.5	11	13
*1106	1350	1820	2.7	−48	−7.9	−15.1	13.1	15	1
*1107	1250	1910	2.2	−56	−9.2	−15.3	11.2	14	14
*1108	1250	1700	2.4	−54	−14.1	−20.1	11.4	14	7
*1109	1250	2050	4.5	−59	−12.3	−19.2	11.2	9	—
*1110	1250	1980	2.8	−63	−12.5	−17.2	11.7	8	—
*1111	1300	2070	3.1	−52	−9.0	−14.1	12.4	8	2
*1112	1350	1530	3.5	−44	−8.7	−13.5	11.1	11	–
*1113	1350	1510	3.9	−47	−8.7	14.0	11.3	8	–
*1114	1200	1720	2.8	−49	−15.2	−29.8	13.2	14	4
*1115	1250	1710	2.2	−59	−15.1	−16.5	13.1	14	10
1116	1250	2900	1.7	−52	−4.8	−6.5	13.2	13	62
1117	1150	1130	2.1	−31	−10.2	−14.9	13.3	15	190
1118	1175	1400	2.1	−34	−9.4	−14.2	13.4	15	89
1119	1150	1270	2.4	−34	−8.7	−14.1	13.2	14	109
1120	1175	1270	2.3	−35	−9.3	−14.3	13.1	14	100
1121	1200	1910	2.0	−43	−8.8	−13.5	13	15	84
1122	1250	2030	2.1	−41	−7.9	−13.2	13.3	14	92
1123	1250	1410	2.3	−35	−8.1	−11.8	13.1	14	115
1124	1250	1420	2.4	−30	−7.9	−11.0	13	14	132
1125	1175	1270	2.1	−33	−9.8	−14.3	13.2	15	89
1126	1175	1310	2.0	−31	−9.2	−13.7	13.2	15	98

* The samples marked by (*) are out of the range of the present invention.

The grain size of the polished cross section of the laminated ceramic capacitor obtained was determined under a scanning electron microscope after chemical etching, finding that the grain size was almost equal to the particle size of the barium calcium titanate as a starting material in the samples having the compositions within the range of the present invention.

As is evident from TABLE 10 and TABLE 11, the rate of temperature dependent change of the laminated ceramic capacitor according to the present invention satisfies the B-grade characteristic standard prescribed in the JIS standard in the temperature range from −15° C. to +85° C. and the X7R-grade characteristic standard prescribed in the EIA standard in the temperature range from −55° C. to +125° C. Moreover, the rate of change of the capacitance under an impressed DC voltage of 5 kV/mm is as small as 52%, indicating that the change of the electrostatic capacitance is also small when the capacitor is used as a thin layer. The mean lifetime in the high temperature load test is as long as 62 hours, enabling one to fire at a temperature of 1250° C. or less.

The reason why the compositions according to the present invention are limited in the present invention will be described hereinafter.

In the system comprising the principal component

$$(Ba_{1-x}Ca_xO)_mTiO_2+\alpha Re_2O_3+\beta MgO+\gamma MnO$$

(Re_2O_3 represents at least one of the compounds selected from Y_2O_3, Gd_2O_3, Tb_2O_3, Dy_2O_3, Ho_2O_3, Er_2O_3 and Yb_2O_3 and α, β and γ represent molar ratios) and the third sub-component, a content (x) of CaO of about 0.005 or less as in the sample No. 1101 is not preferable since the rate of impressed voltage dependent change of the capacitance becomes large besides the mean lifetime becomes extremely short. It is also not preferable that the content (x) of CaO exceeds about 0.22 as in the sample No. 1102 because the dielectric loss is increased. Accordingly, the preferable CaO content (x) is in the range of $0.005<x\leqq 0.22$.

A Re_2O_3 content (α) of less than about 0.001 as in the sample No. 1103 is also not preferable because the mean lifetime becomes extremely short. It is also not preferable that the content of Re_2O_3 (α) exceeds about 0.10 as in the sample No. 1104 since the temperature characteristics do not satisfy the B/X7R-grade characteristics while the mean lifetime is shortened. Accordingly, the preferable Re_2O_3 content (α) is in the range of $0.001\leqq\alpha\leqq 0.10$.

A MgO content (β) of less than about 0.001 as in the sample No. 1105 is also not preferable because the rate of impressed voltage dependent change of the capacitance becomes large, the temperature characteristics do not satisfy the B/X7R-grade characteristics and the resistivity is lowered, shortening the mean lifetime. It is also not preferable, on the other hand, that the amount of addition (β) of MgO exceeds about 0.12 as in the sample No. 1106 since the sintering temperature becomes high to extremely shorten the mean lifetime. Accordingly, the preferable MgO content (β) is in the range of $0.001\leqq\beta\leqq 0.12$.

A MnO content (γ) of less than about 0.001 as in the sample No. 1107 is also not preferable because the resistivity is low while the mean lifetime is shortened. It is also not preferable, on the other hand, that the MnO content (γ) exceeds about 0.12 as in the sample No. 1108 since the temperature characteristics do not satisfy the B/X7R-grade characteristics, the resistivity becomes low and the mean lifetime is shortened. Accordingly, the preferable range of the MnO content (γ) is $0.001\leqq\gamma\leqq 0.12$.

It is not preferable that the ratio (m) of (Ca, Ca)/Ti is less than about 1.000 as in the sample Nos. 1109 and No. 1110

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because the temperature characteristics do not satisfy the B/X7R-grade characteristics and the resistivity is lowered, immediately causing short circuit troubles when a voltage is impressed in the high temperature load test. It is also not preferable, on the other hand, that the ratio (m) of (Ca, Ca)/Ti exceed about 1.035 as in the sample No. 1111 because sintering is insufficient to extremely shorten the mean lifetime. Accordingly, the preferable ratio (m) of (Ca, Ca)/Ti is in the range of $1.000<m\leqq1.035$.

It is not preferable that the contents of the first and second sub-components are zero as in the samples No. 1112 and No. 1113 because the resistivity is lowered to immediately cause short circuit troubles when a voltage is impressed in the high temperature load test. It is also not preferable, on the other hand, that the contents of the first and second sub-components exceed about 5.0 parts by weight as in the sample No. 1114 because the second phase based on glass components is increased besides the temperature characteristics do not satisfy the B/X7R-grade characteristics and the mean lifetime is extremely shortened. Accordingly, the preferable content of either the first component or the second component is in the range from about 0.2 to 5.0 parts by weight.

The content of the alkali metal oxides contained in barium calcium titanate as impurities is adjusted to about 0.02% by weight or less because when the content of the alkali metal oxides exceeds about 0.02% by weight as in the sample No. 1115, the mean lifetime is shortened.

The sample No. 1116 in which the mean particle size of barium calcium titanate exceeds about 0.7 μm shows a little poor mean lifetime of 52 hours. The sample No. 1117 in which the mean particle size of barium calcium titanate is less than about 0.1 μm shows, on the other hand, a little smaller dielectric constant of 1130. Accordingly, the preferable mean particle size of barium calcium titanate is in the range from 0.1 to 0.7 μm.

Example 6

A starting material having the following composition was prepared as a dielectric powder using barium calcium titanate (B) as shown in TABLE 12:

$(Ba_{0.90}Ca_{0.10}O)_{1.010}\cdot TiO_2+0.02Dy_2O_3+0.02MgO+0.01MnO$ (molar ratio)

Laminated ceramic capacitors were produced by the same method as used in Example 1, except that the Li_2O—B_2O_3—(Si, Ti)O_2 based oxide (including those supplemented with Al_2O_3 and ZrO_2) as the first sub-component with a mean particle size of 1 μm or less produced by heating at 1200 to 1500° C. was added to the powder material. The size and shape of the laminated ceramic capacitor produced are the same as that produced in Example 4. The electric characteristics were measured by the same method as in Example 4, the results of which are shown in TABLE 13.

TABLE 12

	First Subcomponent						
Sample No.	Amount of addition (parts by weight)	Composition (mol %, except w) Li_2O	B_2O_3	(Si_wTi_{1-w})	w	Additive Parts by Weight Al_2O_3	ZrO_2
1201	1	0	20	80	0.7	0	0
1202	1	19	1	80	0.7	0	0
1203	1	49	1	50	0.8	0	0
1204	2	45	50	5	0.5	0	0
1205	2	20	75	5	0.4	0	0
1206	2	0	80	20	0.4	0	0
1207	1.5	35	15	50	0.5	0	0
1208	1.5	35	50	15	0.9	0	0
1209	2	20	40	40	0.3	0	0
1210	2	10	15	75	0.7	0	0
1211	2	10	70	20	0.4	5	2
1212	2	35	15	50	0.7	15	5
1213	2	35	15	50	0.7	20	0
1214	2	35	15	50	0.7	0	10
1215	3	10	5	85	0.5	0	0
1216	3	55	20	25	0.7	0	0
1217	3	35	62	3	0.7	0	0
1218	2	5	85	10	0.7	0	0
1219	2	10	15	75	0.1	0	0
1220	2	35	50	15	1	0	0
1221	2	35	50	15	0.7	30	0
1222	1	35	50	15	0.7	0	20

TABLE 13

Sample No.	Burning Temperature (° C.)	Dielectric Constant	Dielectric Loss tan δ (%)	Rate of Change of Capacitance ΔC% DC 5Kv/mm	Rate of Temperature Dependent Change of Capacitance ΔC/C20% −25~+85° C. (%)	ΔC/C25% −55~+125° C. (%)	Resistivity Log ρ (Ω.cm)	Dielectric Breakdown Voltage DC (kV/mm)	Mean Lifetime (h)
1201	1250	1880	2.4	−42	−7.8	−12.5	13.0	13	81
1202	1250	1870	2.4	−43	−7.6	−12.4	13.1	13	88
1203	1250	1850	2.3	−42	−7.8	−12.4	13.1	13	83
1204	1225	1830	2.3	−41	−7.7	−12.1	13.1	13	85
1205	1225	1860	2.5	−41	−7.1	−12.1	13.0	13	84
1206	1225	1840	2.4	−40	−8.1	−12.5	13.1	13	80
1207	1250	1880	2.4	−43	−8.0	−11.8	13.0	13	86
1208	1250	1900	2.5	−45	−8.3	−12.7	13.0	12	88
1209	1225	1850	2.4	−44	−7.7	−12.3	13.1	13	83
1210	1225	1870	2.4	−45	−7.9	−12.5	13.0	13	83
1211	1225	1880	2.4	−44	−8.0	−12.6	13.3	14	91

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TABLE 13-continued

Sample No.	Burning Temperature (° C.)	Dielectric Constant	Dielectric Loss tan δ (%)	Rate of Change of Capacitance ΔC% DC 5Kv/mm	Rate of Temperature Dependent Change of Capacitance ΔC/C20% −25–+85° C. (%)	ΔC/C25% −55–+125° C. (%)	Resistivity Log ρ (Ωcm)	Dielectric Breakdown Voltage DC (kV/mm)	Mean Lifetime (h)
1212	1225	1860	2.3	−44	−8.5	−12.5	13.3	14	97
1213	1225	1810	2.2	−43	−8.2	−12.4	13.4	14	95
1214	1225	1780	2.2	−43	−7.5	−12.1	13.3	14	92
1215	1350	1650	4.3	−42	−7.2	−11.7	11.1	12	2
1216	1350	1770	4.1	−42	−7.4	−11.8	11.4	10	7
1217	1300	1580	3.5	−41	−7.3	−11.3	11.6	11	26
1218	1300	1870	3.4	−44	−7.8	−11.8	11.8	11	18
1219	1350	1830	4.7	−44	−7.7	−12.1	11.1	11	4
1220	1300	1910	3.9	−45	−8.1	−12.7	12.4	12	22
1221	1350	1880	4.7	−44	−7.9	−12.6	10.8	12	1
1222	1350	1920	5.6	−45	−8.3	−13.4	10.7	12	2

As is evident from TABLE 12 and TABLE 13, the sample Nos. 1201 to 1210, in which Li_2O—B_2O_3—$(Si_wTi_{1-w})O_2$ based oxides with compositions within the area surrounded by the straight lines connecting between the succeeding two points represented by A (x=0, y=20, z=80), B (x=19, y=1, z=80), C (x=49, y=1, z=50), D (x=45, y=50, z=5), E (x=20, y=75, z=5) and F (x=0, y=80, z=20) or on the lines in a ternary composition diagram having apexes represented by each component Li_2O, B_2O_3 and $Si_wTi_{1-w})O_2$ (x, y and z are represented by mol %) are added, has a dielectric constant of as large as 1830 or more, the rate of temperature dependent changes of the electrostatic capacitance satisfy the B-grade characteristic standard prescribed in the JIS standard in the temperature range from −25° C. to +85° C., and satisfy the X7R-grade characteristic standard prescribed in the EIA standard in the temperature range from −55° C. to +125° C. In addition, the rate of change of the capacitance when a DC voltage of 5 kV/mm is impressed is as small as within 45%, the change of the electrostatic capacitance being small when used as thin layers. The mean lifetime under the high temperature load test is as long as 80 hours or more, enabling a firing temperature of 1250° C.

When the content of the Li_2O—B_2O_3—(Si, Ti)O_2 based oxide is out of the range of the present invention as in the sample Nos. 1215 and 1220, on the contrary, sintering is insufficient or electric characteristics are deteriorated due to plating after firing, shortening the mean lifetime in the high temperature load test.

While the resistivity can be enhanced by allowing Al_2O_3 and ZrO_2 to be contained in the Li_2O—B_2O_3—(Si, Ti)O_2 based oxide as in the sample Nos. 1211 and 1214, sintering becomes insufficient to shorten the mean lifetime in the high temperature load test as in the sample Nos. 1221 and 1222 when the amount of addition of Al_2O_3 exceeds 20 parts by weight or the amount of addition of ZrO_2 exceeds 10 parts by weight.

Example 7

A starting material having the following composition was prepared as a dielectric powder using barium calcium titanate (B) as shown in TABLE 14:

$$(Ba_{0.90}Ca_{0.10}O)_{1.010}\cdot TiO_2+0.02Gd_2O_3+0.05MgO+0.010MnO$$
(molar ratio)

Laminated ceramic capacitors were produced by the same method as used in Example 1, except that the Al_2O_3—MO—B_2O_3 based oxide as the second sub-component with a mean particle size of 1 μm or less produced by heating at 1200 to 1500° C. as shown in TABLE 14 was added to the powder material. The size and shape of the laminated ceramic capacitor produced are the same as that produced in Example 4. The electric characteristics were measured by the same method as in Example 4, the results of which are shown in TABLE 15.

TABLE 14

Sample No.	Amount of Addition	The Second Sub-Component Composition (mol %) Al_2O_3	MO BaO	CaO	SrO	MgO	ZnO	MnO	Total	B_2O_3
1301	1	1	5	5	0	0	0	4	14	85
1302	1	20	8	0	0	0	2	0	10	70
1303	1	30	6	10	2	2	0	0	20	50
1304	1	40	0	30	0	0	5	15	50	10
1305	1	20	0	30	0	0	10	30	70	10
1306	1	1	0	5	5	24	5	0	39	60
1307	1	15	10	0	0	0	3	2	15	70
1308	1	10	10	15	0	5	0	5	35	55
1309	1	20	0	30	5	0	3	2	40	40
1310	1	30	5	35	5	0	5	0	80	20

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TABLE 14-continued

Sample No.	Amount of Addition	The Second Sub-Component: Composition (mol %)								
		Al_2O_3	MO: BaO	CaO	SrO	MgO	ZnO	MnO	Total	B_2O_3
1311	1	5	10	0	0	0	0	0	10	85
1312	1	30	5	5	0	0	0	0	10	60
1313	1	40	20	0	0	0	3	2	25	35
1314	1	60	30	0	0	0	3	2	35	5
1315	1	5	15	35	10	0	3	2	65	30
1316	1	0	15	15	0	0	0	0	30	70

TABLE 15

Sample No.	Burning Temperature (° C.)	Dielectric Constant	Dielectric Loss tan δ (%)	Rate of Change of Capacitance ΔC% DC 5Kv/mm	Rate of Temperature Dependent Change of Capacitance ΔC/C20% -25~+85° C. (%)	ΔC/C25% -55~+125° C. (%)	Resistivity Log ρ (Ω.cm)	Dielectric Breakdown Voltage DC (kV/mm)	Mean Lifetime (h)
1301	1250	1860	2.4	-43	-7.2	-10.9	13.2	13	87
1302	1250	1870	2.4	-43	-7.3	-11.1	13.1	13	87
1303	1250	1900	2.5	-45	-8.1	-12.2	13.2	13	84
1304	1250	1880	2.4	-45	-7.8	-12.2	13.2	13	88
1305	1250	1890	2.4	-43	-8.0	-12.3	13.2	13	92
1306	1250	1850	2.3	-43	-7.9	-12.1	13.2	14	88
1307	1250	1870	2.5	-44	-7.5	-11.9	13.2	13	90
1308	1250	1880	2.5	-45	-7.9	-12.2	13.3	13	88
1309	1250	1790	2.3	-43	-7.3	-11.8	13.2	14	92
1310	1250	1830	2.3	-42	-8.0	-12.1	13.2	13	87
1311	1350	1780	3.7	-41	-7.8	-11.8	11.5	11	3
1312	1350	1560	4.5	-41	-7.1	-11.4	10.9	10	2
1313	1350	1630	5.1	-43	-7.8	-11.7	11.1	10	1
1314	1350	1810	3.5	-48	-8.4	-12.1	11.2	11	2
1315	1350	1650	5.7	-44	-7.7	-11.9	11.1	11	4
1316	1250	1820	4.8	-47	-8.1	-12.5	11.4	12	5

As is evident from TABLE 14 and TABLE 15, the sample Nos. 1301 to 1310, in which Al_2O_3—MO—B_2O_3 based oxides with compositions within the area surrounded by the straight lines connecting between the succeeding two points represented by A (x=1, y=14, z=85), B (x=20, y=10, z=70), C (x=30, y=20, z=50), D (x=40, y=50, z=10), E (x=20, y=70, z=10) and F (x=1, y=39, z=60) or on the lines in a ternary composition diagram having apexes represented by each component Al_2O_3, MO and B_2O_3 are added, have a dielectric constant of as large as 1790 or more, the rate of temperature dependent changes of the electrostatic capacitance satisfy the B-grade characteristic standard prescribed in the JIS standard in the temperature range from −25° C. to +85° C., and satisfy the X7R-grade characteristic standard prescribed in the EIA standard in the temperature range from −55° C. to +125° C. In addition, the rate of change of the capacitance when a DC voltage of 5 kV/mm is impressed is as small as within 45%, the change of the electrostatic capacitance being small when used as thin layers. The mean lifetime under the high temperature load test is as long as 84 hours or more, enabling a firing temperature of 1250° C.

When the content of the Al_2O_3—MO—B_2O_3 based oxide is out of the range of the present invention as in the sample Nos. 1311 to 1316, on the contrary, sintering is insufficient or electric characteristics are deteriorated due to plating after firing, shortening the mean lifetime in the high temperature load test.

From the results obtained by analyzing the in the dielectric ceramic particles under a transmission electron microscope with respect to the samples having the compositions within the range of the present invention obtained in Examples 4 to 7, it was confirmed that all the samples have core-shell structures in which the Re components (Re represents Y, Gd, Tb, Dy, Ho, Er and Yb) are diffused in the vicinity of or at the grain boundaries.

Accordingly, the present invention provides a highly reliable and plating solution resistive ceramic capacitor using Ni or a Ni alloy for the inner electrodes.

What is claimed is:

1. A dielectric ceramic comprising

$$(Ba_{1-x}Ca_xO)_mTiO_2+\alpha Re_2O_3+\beta MgO+\gamma MnO$$

in which Re is at least one member selected from the group consisting of Y, Gd, Tb, Dy, Ho, Er and Yb; α, β γ, m and x are molar ratios; $0.001 \leqq \alpha \leqq 0.10$; $0.001 \leqq \beta \leqq 0.12$; $0.001 < \gamma \leqq 0.12$; $1.000 < m \leqq 1.035$; and $0.005 < x \leqq 0.22$, and

about 0.2 to 5.0 parts by weight of either a first sub-component or a second sub-component or a third sub-component relative to 100 parts by weight of $(Ba_{1-x}Ca_xO)_mTiO_2$, wherein

the $(Ba_{1-x}Ca_xO)_mTiO_2$ contains about 0.02% by weight or less of alkali metal oxides,

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the first sub-component is a Li_2O—$(Si,Ti)O_2$—MO oxide in which M is at least one of Al and Zr,

the second sub-component is a SiO_2—TiO_2—XO oxide in which X is at least one selected from the group consisting of Ba, Ca, Sr, Mg, Zn and Mn, and the third sub-component is SiO_2.

2. A dielectric ceramic according to claim 1, wherein the $(Ba_{1-x}Ca_xO)_mTiO_2$ has a mean particle size of about 0.1 to 0.7 μm.

3. A dielectric ceramic according to claim 1, wherein the first sub-component is present and comprises $xLiO_2$—$y(Si_wTi_{1-w})O_2$—zMO, x, y and z are molar percentages and $30 \leqq w \leqq 1.0$, and is within the area surrounded by straight lines connecting between succeeding two points represented by A (x=20, y=80, z=0), B (x=10, y=80, z=10), C (x=10, y=70, z=20), D (x=35, y=45, z=20), E (x=45, y=45, z=10) and F (x=45, y=55, z=0) or on said lines in a ternary composition diagram having apexes represented by the components LiO_2, $(Si_wTi_{1-w})O_2$ and MO, provided that when the first sub-component is on the line A–F, $0.3 \leqq w < 1.0$.

4. A dielectric ceramic according to claim 3, wherein comprising at least one of Al_2O_3 and ZrO_2 in a combined amount of about 20 parts by weight or less and in which the ZrO_2 is 10 parts by weight or less relative to 100 parts by weight of the Li_2O—$(Si,Ti)O_2$—MO oxide.

5. A dielectric ceramic according to claim 3, wherein said points are A (x=0, y=20, z=80), B (x=19, y=1, z=80), C (x=49, y=1, z=50), D (x=45, y=50, z=5), E (x=20, y=75, z=5) and F (x=0, y=80, z=20) and wherein the $(Ba_{1-x}Ca_xO)_m$ TiO_2 has a mean particle size of about 0.1 to 0.7 μm.

6. A dielectric ceramic according to claim 1, wherein the second sub-component is present and comprises $xSiO_2$—$yTiO_2$—zXO, x, y and z are molar percentages, and is within the area surrounded by straight lines connecting between succeeding two points represented by A (x=85, y=1, z=14), B (x=35, y=51, z=14), C (x=30, y=20, z=50) and D (x=39, y=1, z=60) or on said lines in a ternary composition diagram having apexes represented by the components SiO_2, TiO_2 and XO.

7. A dielectric ceramic according to claim 6, comprising at least one of Al_2O_3 and ZrO_2 in a combined amount of about 15 parts by weight or less and the ZrO_2 is 5 parts by weight or less relative to 100 parts by weight of the SiO_2—TiO_2—XO oxide.

8. A dielectric ceramic according to claim 6, wherein said points are A (x=1, y=14, z=85), B (x=20, y=10, z=70), C (x=30, y=20, z=50), D (x=40, y=50, z=10), E (x=20, y=70, z=10) and F (x=1, y=39, z=60) and wherein the $(Ba_{1-x}Ca_xO)_m$ TiO_2 has a mean particle size of about 0.1 to 0.7 μm.

9. A dielectric ceramic according to claim 1 in which the third sub-component is present.

10. A dielectric ceramic according to claim 2, wherein the molar ratio of (Ba+Ca)/Ti is about 0.99 to 1.035.

11. A laminated ceramic capacitor having:

a plurality of dielectric layers containing the dielectric ceramic according to claim 1;

a plurality of inner dielectric layers comprising Ni or a Ni alloy and existing among a plurality of said dielectric layers; and

external electrodes in electrical continuity to a plurality of said inner dielectric layers and being on the surface of said ceramic capacitor.

12. A laminated ceramic capacitor according to claim 11, wherein said external electrodes comprise a sintered layer of conductive metal powder or conductive metal powder and glass frit.

13. A laminated ceramic capacitor having:

a plurality of dielectric layers containing the dielectric ceramic according to claim 2;

a plurality of inner dielectric layers comprising Ni or a Ni alloy and existing among a plurality of said dielectric layers; and

external electrodes in electrical continuity to a plurality of said inner dielectric layers and being on the surface of said ceramic capacitor.

14. A laminated ceramic capacitor according to claim 13, wherein said external electrodes comprise a sintered layer of conductive metal powder or conductive metal powder and glass frit.

15. A laminated ceramic capacitor having:

a plurality of dielectric layers containing the dielectric ceramic according to claim 3;

a plurality of inner dielectric layers comprising Ni or a Ni alloy and existing among a plurality of said dielectric layers; and

external electrodes in electrical continuity to a plurality of said inner dielectric layers and being on the surface of said ceramic capacitor.

16. A laminated ceramic capacitor according to claim 15, wherein said external electrodes comprise a sintered layer of conductive metal powder or conductive metal powder and glass frit.

17. A laminated ceramic capacitor having:

a plurality of dielectric layers containing the dielectric ceramic according to claim 6;

a plurality of inner dielectric layers comprising Ni or a Ni alloy and existing among a plurality of said dielectric layers; and

external electrodes in electrical continuity to a plurality of said inner dielectric layers and being on the surface of said ceramic capacitor.

18. A laminated ceramic capacitor according to claim 17, wherein said external electrodes comprise a sintered layer of conductive metal powder or conductive metal powder and glass frit.

19. A laminated ceramic capacitor having:

a plurality of dielectric layers containing the dielectric ceramic according to claim 9;

a plurality of inner dielectric layers comprising Ni or a Ni alloy and existing among a plurality of said dielectric layers; and

external electrodes in electrical continuity to a plurality of said inner dielectric layers and being on the surface of said ceramic capacitor.

20. A laminated ceramic capacitor according to claim 19, wherein said external electrodes comprise a sintered layer of conductive metal powder or conductive metal powder and glass frit.

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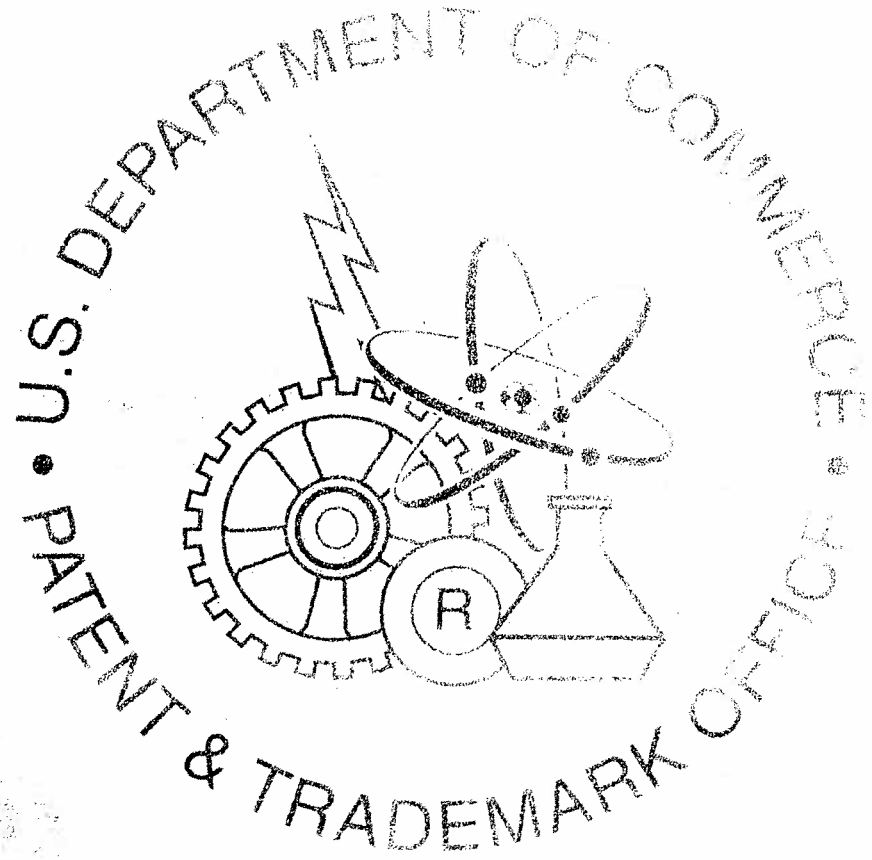

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Ueno et al.

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[54] **LAMINATED CERAMIC ELECTRONIC PARTS**

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[52] **U.S. Cl.** **361/306.3**; 361/311; 361/321.2; 361/321.5

[58] **Field of Search** 361/301.1, 303, 361/305, 306.3, 311–313, 321.1–321.5, 320; 501/134–138; 29/25–42; 338/20, 21

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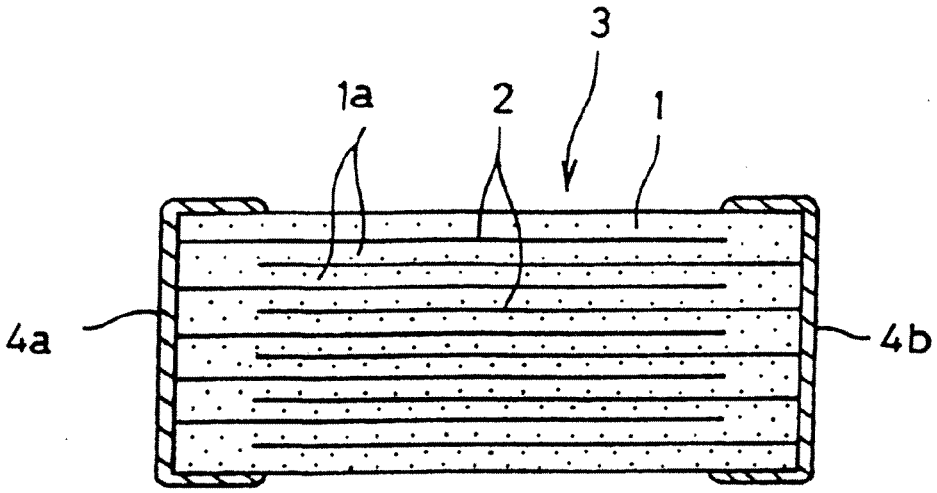
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[57] **ABSTRACT**

There is provided a highly reliable laminated ceramic electronic part in which delamination or crack can be suppressed from occurring during a sintering process even if a number of lamination of internal electrodes is increased and a thickness of the ceramic layer is reduced and which excels in thermal shock resistance. The laminated ceramic electronic part is constructed so as to satisfy the following requirements of that a thickness of the ceramic layer is 10 μm or less; a number of lamination of the internal electrodes is 200 or more; a ratio of a thickness of the internal electrode to the thickness of the ceramic layer (thickness of internal electrode/thickness of ceramic layer) is 0.10 to 0.40; and a ratio of a volume of the internal electrode to a volume of the ceramic element (volume of internal electrodes/volume of ceramic element) is 0.10 to 0.30.

3 Claims, 1 Drawing Sheet



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FIG. 1

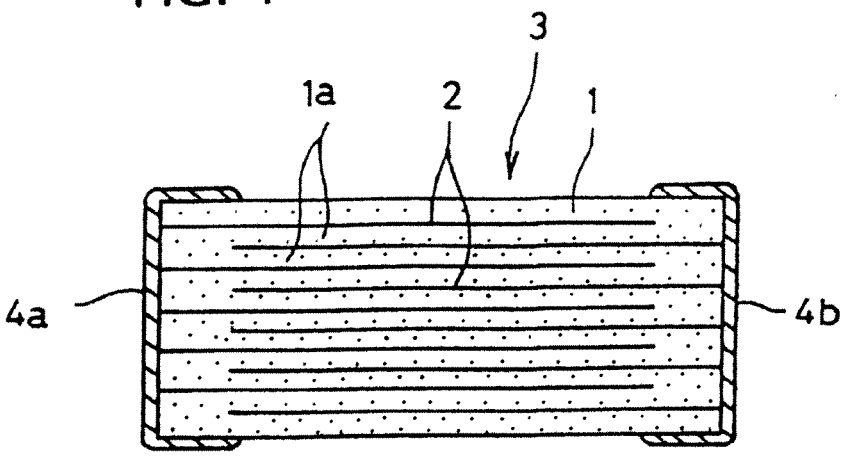
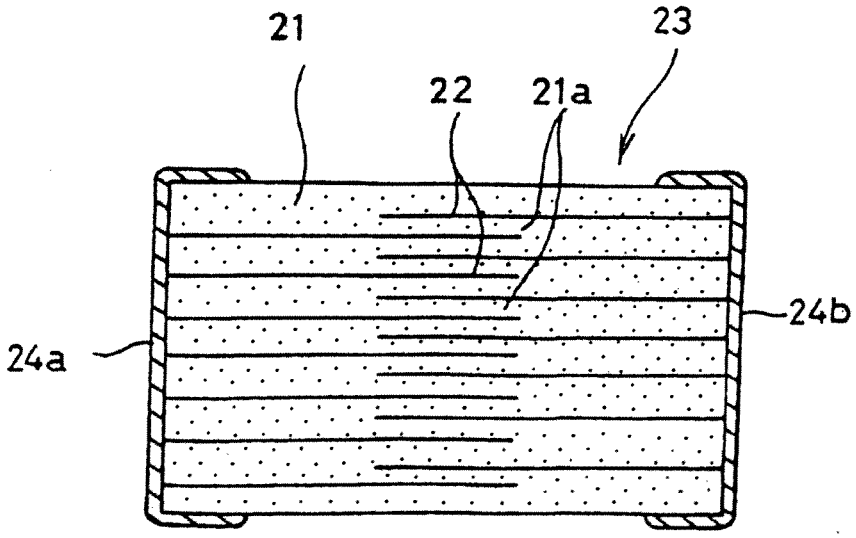


FIG. 2 PRIOR ART



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LAMINATED CERAMIC ELECTRONIC PARTS

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to laminated ceramic electronic parts and more specifically to laminated ceramic electronic parts such as a laminated ceramic capacitor and a laminated varistor having a structure in which a plurality of internal electrodes are disposed so as to overlap each other via ceramic layers within a ceramic element composing the electronic part.

2. Description of Related Art

A typical laminated ceramic electronic part in the form of a surface mounted laminated ceramic capacitor is shown in FIG. 2. Capacitor **23** is constructed by disposing a pair of external terminals **24***a* and **24***b*, which are in electrical contact with a plurality of internal electrodes **22**, at opposite ends of a ceramic dielectric block **21**. The dielectric block **21** is formed of a lamination of thin ceramic layers **21***a* having the internal electrodes **22** disposed therebetween. This laminated structure makes it possible to obtain a large capacitance even though the overall size of the capacitor **22** is small.

Due to improvements in the ability to decrease the thickness of the ceramic layers **21***a*, it has become possible to both reduce the thickness of the ceramic layers **21***a* and increase the total number of internal electrodes **21***a* while at the same time decreasing the overall size of the capacitor **23** (or other laminated ceramic electronic part). Laminated ceramic parts having over 100 laminated ceramic layers, each as thin as 5 μm, have become commercially available.

While the reduction in the size of the laminated layers has improved the characteristics of the final product (reduced size and capacitance), it has created manufacturing problems. As a result of the thinning of the ceramic layers, there is little difference between the thickness of the ceramic layers and the thickness of the internal electrodes and the ratio of the combined thickness of the internal electrodes to the total thickness of the electronic part can exceed 3.0. Because the internal electrodes have become a larger percentage of the overall electronic part, they have a much greater effect on the sintering characteristics of the product.

This has the disadvantageous effect of increasing the incidence of delamination and cracking during the sintering process, thus increasing the occurrence of defective parts and degrading the reliability of the parts. Additionally, the laminated ceramic electronic part is likely to form cracks when it receives thermal shocks.

SUMMARY OF THE INVENTION

Accordingly, it is an object of the present invention to solve the above-mentioned problems by providing highly reliable laminated ceramic electronic parts in which delamination or cracking can be suppressed during the sintering process and which excels in thermal shock resistance even if the number of internal electrodes is increased and the thickness of the individual ceramic layer (located between the internal electrodes) is reduced.

In order to achieve the above-mentioned object, the present invention includes a ceramic electronic part having a structure in which a plurality of internal electrodes are disposed so as to overlap each other via respective ceramic layers and the internal electrodes are led to terminals on the opposite sides of the ceramic element and in which each layer satisfies the following requirements:

(a) the thickness of each respective ceramic layer is 10 μm or less;

(b) the number of internal electrodes is 200 or more;

(c) the ratio of the thickness of the internal electrodes to the thickness of the ceramic layers (thickness of internal electrode/thickness of ceramic layer) is between 0.10 and 0.40; and

(d) the ratio (volume of internal electrode/volume of ceramic element) of the total volume of the internal electrodes to the volume of the ceramic element (i.e., the combined volume of internal electrodes and the ceramic material) is between 0.10 and 0.30.

By satisfying the foregoing requirements, it becomes possible to suppress delamination and cracking from occurring during the sintering process, to improve thermal shock resistance and to provide a highly reliable laminated ceramic electronic part even when the number of laminated internal electrodes is increased and the thickness of the ceramic layer is reduced.

That is, it becomes possible to reduce the influence of the sintering characteristic of the material of the internal electrode during the sintering process and to prevent delamination and cracking from occurring during the sintering process by controlling the ratio of the thickness of the internal electrode to the thickness of the ceramic layer (thickness of internal electrode/thickness of ceramic layer). It also becomes possible to enhance the strength of the laminated ceramic electronic part against thermal stress and to provide the highly reliable laminated ceramic electronic part by controlling the ratio (volume of internal electrodes/volume of ceramic element) of the total volume of the internal electrodes to the total volume of the ceramic element (i.e., the total volume of internal electrodes and the ceramic material).

The specific nature of the invention, as well as other objects, uses and advantages thereof, will clearly appear from the following description and the from the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWING(S)

FIG. 1 is a section view showing a structure of a laminated ceramic electronic part (laminated ceramic capacitor) according to one embodiment of the present invention; and

FIG. 2 is a section view showing a structure of a prior art laminated ceramic electronic part (laminated ceramic capacitor).

DESCRIPTION OF PREFERRED EMBODIMENT

One preferred embodiment of the present invention will be described below in detail. FIG. 1 is a section view showing a structure of a laminated ceramic electronic part (laminated ceramic capacitor in the present embodiment) according to the embodiment of the invention.

As shown in FIG. 1, the laminated ceramic capacitor is constructed by disposing external electrodes **4***a* and **4***b*, which are in electrical contact with a plurality of internal electrodes **2**, at opposite ends of a ceramic element (e.g., a capacitor) **3**. The internal electrodes **2** are disposed so as to face each other via ceramic layers **1***a* within a ceramic body **1** and a respective end of each internal electrode **2** is coupled to external electrode **4***a* or **4***b*.

Several sample capacitors were formed and their characteristics tested to determine the effect of the present invention. A summary of the results of these tests are set forth in Table 1 below.

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As shown in the first column of Table 1, green sheets having a thickness after sintering of either 9.8 μm, 6.2 μm or 4.3 μm, were used. For example, green sheets having a thickness of 9.8 μm were used for the first sample 1. After the green sheets were formed, conductive paste for forming the internal electrode was printed on one surface of the green sheets. The thickness of each internal electrode for the respective sample is indicated in Table 1. Then, after laminating and compressing them such that a number of lamination of the electrodes turns out to be 200, 200 laminations were compressed together and cut into a predetermined size (length L=3.2 mm, width W=1.6 mm) to obtain laminates (non-sintered ceramic element).

After heat treating the ceramic element under predetermined conditions to degrease and sinter it, conductive paste for forming the external electrode was applied to opposite ends of the sintered ceramic element. Final, the ceramic element with the conductive paste applied to its ends was sintered to form the external electrodes and the laminated ceramic capacitor as shown in FIG. 1 was produced.

The characteristics of each of the sample laminated ceramic capacitors were tested to determine the value of electrostatic capacity, the value of insulation resistance, the incidence of delamination, the incidence of cracking on the surface of the ceramic element during sintering and the incidence of cracking (incidence of thermal shock crack) when a thermal shock (_T=350° C.) is applied to the samples. Table 1 shows the results of these tests.

Electrostatic Capacity, Insulation Resistance: n=100

Incidence of Delamination and Cracking: n=500

Incidence of Cracking due to Thermal Shock: n=500

As shown in Table 1, it has been confirmed that while (1) the value of electrostatic capacity is small in Sample No. 1 whose ratio of the thickness of the internal electrode is below that of the scope of the invention (0.10 to 0.40), (2) the value of insulation resistance is small in Sample No. 11 whose ratio of the thickness of the internal electrode exceeds that of the scope of the invention, and (3) the incidences of delamination, cracking and cracking due to thermal shock are high in Sample Nos. 5, 10, 15 and 16 whose ratio of the volume of the internal electrode exceeds that of the scope of the invention (0.10 to 0.30), the samples within the scope of the invention which satisfy the requirements of that the ratio of the thickness of the internal electrode to that of the ceramic layer (thickness of internal electrode/thickness of ceramic layer) is between 0.10 and 0.40 and the ratio of the volume of the internal electrode to the volume of the ceramic element (volume of internal electrode/volume of ceramic element) is between 0.10 and 0.30 can obtain characteristics which are practically no problem with respect to the values of electrostatic capacity and of insulation resistance, cause no delamination nor cracking during the sintering process and cause no cracking due to thermal shock.

It is noted that while the present embodiment has been explained by exemplifying a laminated ceramic capacitor, the present invention is applicable not only to laminated ceramic capacitors but also to various laminated ceramic electronic parts such as a laminated varistor having the structure in which a plurality of internal electrodes are disposed so as to overlap each other via ceramic layers within the ceramic element.

The present invention is not limited to the embodiment described above also in other points. That is, it is possible to add various applications and modifications thereto within the scope of the invention with respect to the thickness of the ceramic layer, the number of lamination of the internal electrodes, the rate of the thickness of the internal electrode to that of the ceramic layer, the rate of the volume of the internal electrode to that of the ceramic element and the like.

In accordance with the present invention is it possible to suppress delamination and cracking from occurring during the sintering process even when the number of internal

TABLE 1

	Thickness of Ceramic Layer (μm)	Thickness of Internal Electrode (μm)	Ratio of Thickness of Internal Electrode (—)	Ratio of Volume of Internal Electrode (—)	Value of Electrostatic Capacity (μF)	Value of Insulation Resistance log IR	Incidence of Delamination (%)	Incidence of Cracking (%)	Incidence of Thermal Shock Cracking (%)
*1	9.8	0.68	0.06	0.075	1.81	12.01	0.00	0.00	0.00
2	9.8	0.99	0.10	0.100	2.25	12.00	0.00	0.00	0.00
3	9.8	1.13	0.15	0.112	2.37	11.98	0.00	0.00	0.00
4	9.8	1.97	0.20	0.186	2.43	11.87	0.00	0.00	0.00
*5	9.8	2.50	0.26	0.307	2.23	11.98	0.33	1.35	2.13
*6	6.2	0.58	0.09	0.095	2.78	11.53	0.00	0.00	0.00
7	6.2	0.87	0.14	0.135	3.54	11.25	0.00	0.00	0.00
8	6.2	1.15	0.19	0.172	3.42	11.15	0.00	0.00	0.00
9	6.2	1.87	0.31	0.257	3.15	11.01	0.00	0.01	0.00
*10	6.2	2.40	0.38	0.310	3.07	11.07	0.53	0.97	0.54
*11	4.3	0.41	0.95	0.103	3.98	10.10	0.00	0.00	0.00
12	4.3	0.71	0.16	0.170	4.54	10.93	0.00	0.00	0.00
13	4.3	0.97	0.23	0.200	4.95	11.25	0.00	0.00	0.00
14	4.3	1.23	0.29	0.210	5.01	10.98	0.00	0.00	0.00
*15	4.3	1.65	0.41	0.310	4.99	10.33	0.13	0.52	1.58
*16	4.3	2.40	0.56	0.390	4.83	10.54	0.97	1.35	3.51

It is noted that in Table 1, those samples marked with * fall outside the scope of the present invention (comparative examples) and the other samples fall within the scope of the invention.

The "Ratio of Thickness of Internal Electrode" is the ratio of the individual thickness of the internal electrode to each individual thickness of each ceramic layer (thickness of internal electrode/thickness of ceramic layer) and the "Ratio of Volume of Internal Electrode" is the ratio of the volume of the internal electrodes to the total volume of the ceramic element (i.e., the total volume of the internal electrodes and the ceramic layer)

Further, the number of samples (n) evaluated to determine the various characteristics shown were as follows in Table 1.

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electrodes is increased and the thickness of the ceramic layer is reduced and to provide the highly reliable laminated ceramic electronic part which excels in its thermal shock resistance.

While the preferred embodiment has been described, variations thereto will occur to those skilled in the art within the scope of the present inventive concept which is delineated by the following claim.

What is claimed is:

1. A laminated ceramic electronic part having a plurality of ceramic layers with internal electrodes located therebetween, said internal electrodes overlapping each other via respective ceramic layers, said internal electrodes and said ceramic layers defining a ceramic element, said internal electrodes being electrically coupled to respective terminals on respective opposite sides of said ceramic element; said laminated ceramic electronic part satisfying the following requirements:

(a) the thickness of each said ceramic layer is 10 μm or less;

(b) the number of said internal electrodes is 200 or more;

(c) the ratio of the thickness of each said internal electrode to the thickness of each said ceramic layer is 0.10 to 0.40; and

(d) the ratio of the combined volume of said internal electrodes to the total volume of said ceramic element is 0.10 to 0.30.

2. A laminated ceramic electronic part, comprising:

(a) a ceramic element including:

(1) a plurality of overlapping internal electrodes;

(2) a plurality of internal ceramic layers located between respective pairs of said overlapping internal electrodes;

(3) upper and lower ceramic layers located above and below the uppermost and lowermost ones of said overlapping internal electrodes, respectively;

(b) a pair of external electrodes formed on at least one outer surface of said ceramic element, each of said overlapping internal electrodes being electrically coupled to a respective external electrode;

(c) said ceramic element satisfying the requirements:

(1) the thickness of each said internal ceramic layer is 10 μm or less;

(2) the number of said internal electrodes is 200 or more;

(3) the ratio of the thickness of each said internal electrode to the thickness of each said internal ceramic layer is 0.10 to 0.40; and

(4) the ratio of the combined volume of said internal electrodes to the combined volume of said ceramic element is 0.10 to 0.30.

3. A laminated ceramic electronic part, comprising:

(a) a ceramic element including:

(1) a plurality of overlapping internal electrodes;

(2) a plurality of internal ceramic layers located between respective pairs of said overlapping internal electrodes;

(3) upper and lower ceramic layers located above and below the uppermost and lowermost ones of said overlapping internal electrodes, respectively;

(b) a pair of external electrodes formed on at least one outer surface of said ceramic element, each of said overlapping internal electrodes being electrically coupled to a respective external electrode;

(c) said ceramic element satisfying the requirements:

(1) the thickness of each said internal ceramic layer is 10 μm or less;

(2) the number of said internal electrodes is 200 or more;

(3) the ratio of the average thickness of each said internal electrode to the average thickness of each said internal ceramic layer is 0.10 to 0.40; and

(4) the ratio of the combined volume of said internal electrodes to the combined volume of said ceramic element is 0.10 to 0.30.

* * * * *

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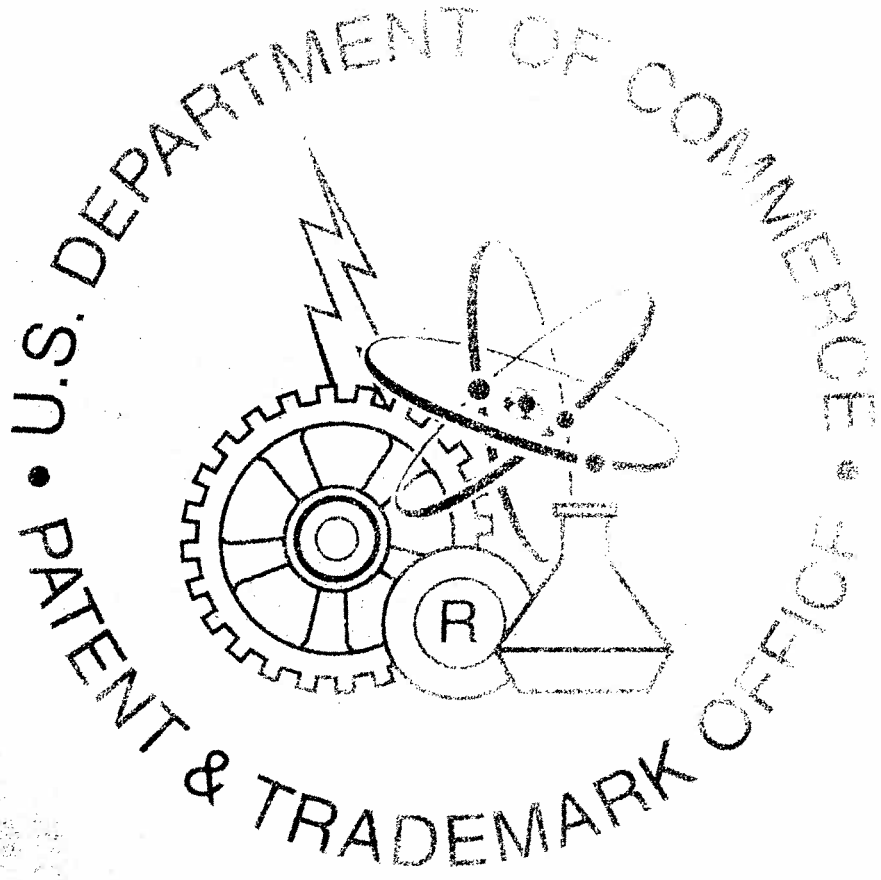


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